奈米金氧半場效電晶體之通道熱能區背向散射實驗

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摘要

在奈米場效電晶體中，熱能區通道背向散射理論現在已經被廣泛的應用。這個理論的論點在於接近源極端平衡的熱能區範圍。然而熱能區範圍寬度的角色還沒有完全地被探討。 在這個研究中，我們將從通道閘極長度為 68 奈米的場效電晶體中以一系列實驗去萃取通道背向散射係數，其可以分為兩個部分包括近平衡的背向散射平均自由路徑及熱能區寬度。由萃取的熱能區寬度可以轉換為在不同的閘極與汲極電壓下接近源極端的通道導電能帶的分佈圖。而通道背向散射理論則完全取決於導電能帶的趨勢變化。因此在這篇論文中，我們直接把熱能區寬度做成模型提供深入的物理探討且發現其具備了下列幾種特性: (1) 在線性操作區中，熱能區寬度與閘電壓有比較弱的關係; (2) 在飽和區之中，熱能區寬度則與汲極電壓以及入射電荷(表達為閘極推動電壓的函數)有關; 以及(3) 熱能區寬度與熱電壓的冪次方成正比的關係，而此冪次方則與溫度、閘極電壓以及汲極電壓無關。此簡潔模型亦有用於電流電壓特性的重現。

Nanoscale MOSFETs Channel k_BT Layer Backscattering Experiment

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Abstract

Currently a widely recognized channel backscattering theory finds potential applications in the areas of nanoscale FETs. The theory prevails over the channel quasi-equilibrium k_BT layer, a critical zone near the thermal reservoir source. However, the role of the k_BT layer width, as well as its promising potentials, has not been fully explored yet. In this study, a series of experiments are conducted to decouple the channel backscattering coefficients in a 68-nm gate length bulk n-channel MOSFET into two distinct components: the quasi-equilibrium mean free path for backscattering and the width of the k_BT layer. The k_BT layer widths obtained from various temperatures are transformed into near-source channel conduction-band profiles for different gate voltages and different drain voltages. The strictly confirmed conduction-band profiles are of value in the areas of channel backscattering. They straightforwardly furnish guidelines not reported before, leading to a new compact model for the k_BT layer width l: (i) l is a weak function of gate voltage in linear region; (ii) in saturation region l follows the amount of injected carriers while the drain voltage tends to shift the l versus gate voltage curve; and (iii) $l \propto (k_BT/q)^d$ with the power exponent d ($\approx$ 0.5) independent of temperature, gate voltage, and drain voltage. Experimental I-V characteristics are also reproduced as well.

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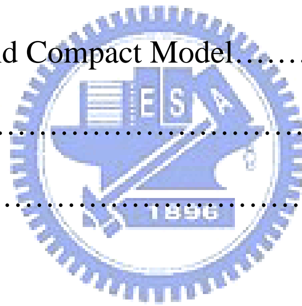

Figure Captions

Fig.1 (a) Schematic illustration of channel backscattering theory in terms of cross section, and the conduction-band profile. F^{+}, the incident flux from the source, is located at the peak of the source-channel barrier. F^{-} is the incident flux from the drain. (b) A flux model in the saturation condition.

Fig.2 A schematic flowchart for the procedure of extracting r_c and separating ℓ.

Fig.3 Square symbol is measured C-V data at temperature of 298K. The dash line is from Schrödinger-Poisson simulation and the solid line is from the Berkeley's C-V simulation.

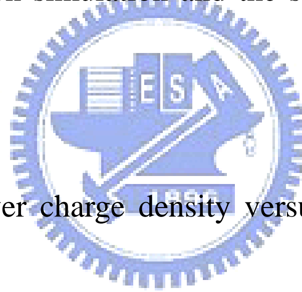

Fig.4 Simulated inversion-layer charge density versus gate voltage under T=298K, 263K, and 233K.

Fig.5 Simulated thermal injection velocity density versus gate voltage under T=298K, 263K, and 233K.

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Fig.13 Measured quasi-equilibrium electron mobility versus effective field.

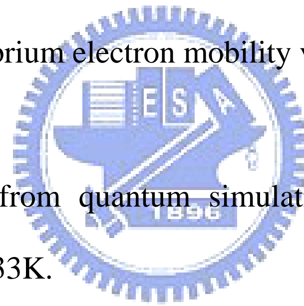

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Fig.17 Extracted gate length versus L_{mask}.

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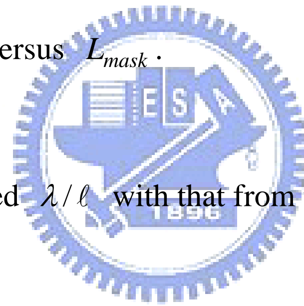

Fig.24 Comparison of extracted λ / ℓ with that from temperature method.

Fig.25 Comparison of extracted r_c with that from temperature method.

Fig. 26 Extracted ϑ versus gate voltage with different drain voltage.

Fig. 27 Transformed channel conduction-band profiles for (a) $V_D = 1.0$ V, (b) $V_D = 0.5$ V, and (c) $V_D = 0.1$ V.

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