Chapter 1 Introduction

Complementary MOS (CMOS) devices continue to shrink into the nanometer area. Owing to physical limitations gradually encountered, the conventional carrier transport, i.e., the drift-diffusion model, essentially fails in the nanoscale MOSFETs. Therefore, they require some innovations to circumvent the hurdles due to the fundamental physics that constrain the conventional MOSFETs [1]. In this thesis, we will research the channel backscattering theory which can adequately describe carrier transport in the nanoscale MOSFETs. The theory has gained increasing attention due to the ability to provide a new perspective about carrier transport in nanoscale MOSFETs [2], [3].

The channel backscattering theory describes a wave-like transport of carriers through the channel from the source to drain. According to the theory, the whole channel in saturation condition can be separated into two distinct regions as schematically demonstrated in Fig. 1(b): $0 < x < l$ and $l < x < L_{eff}$. Here l denotes the critical distance from the source the thermally injected carriers travel over a k_BT (k_B is the Boltzmann's constant and T is the temperature) layer; and L_{eff} is the channel length. Within the k_BT layer, multiple backscattering processes occur[2], [3]. In the channel, scattering event occurs due to the presence of impurity atoms, lattice vibrations of the atoms (which are called the acoustic and optical phonons), and surface roughness. A certain fraction r_C of the incident flux F is effectively reflected and returns to the source [1]. The total charge in the inversion layer near the source, which comprises the injected and reflected components, is controlled by MOS electrostatics. The transmitted flux $(1–r_C)F$ out of the k_BT layer undergoes no net reflections to the k_BT layer due to significant potential gradient in the remainder of the channel. Consequently, the drain current per unit channel width can be expressed as

[2], [3]

$$I_D = Q_{inv} \upsilon_{inj} \frac{(1 - r_C)}{(1 + r_C)} \quad (1)$$

where Q_{inv} is the inversion-layer charge density per unit area and υ_{inj} is the thermal injection velocity. Obviously, r_C is a key coefficient of channel backscattering since once characterized in a nanoscale MOSFET, it readily determines how close to the ballistic limit the device can be operated.

Experimentally, r_C can be extracted by current-voltage (I-V) fitting [4]-[6] or by a temperature dependent method [7]. Owing to multiple backscatterings in the k_BT layer, both the quasi-equilibrium mean-free-path λ and the width of the k_BT layer are functionally coupled through a single r_C [2]:

$$r_C = \frac{1}{1 + \lambda / l} \quad (2)$$

In the recent work [8], l and λ were decoupled from the experimental r_c at the fixed drain voltage and the values of l obtained from different temperatures were transformed into near-source channel conduction-band profiles.

In this thesis, we present a quite comprehensive study of applying the backscattering coefficient decoupling/transformation process in [8] to a certain nanoscale MOSFET, with emphasis on (i) corroborating evidence to the validity of the decoupling/transformation process in a self-consistent nanometer; and (ii) the effect of changing drain voltage on the band bending in the k_BT layer. Indeed, the experimentally determined conduction-band profiles are of value in the areas of channel backscattering. They straightforwardly furnish guidelines not reported before, leading to a compact model for the layer of interest. This model, explicitly expressing k_BT layer width as a function of gate voltage, drain voltage, and temperature, enables I-V (current versus voltage) reproduction.

Chapter 2 Backscattering Theory and Quantum Simulator

In this chapter, the origin of the backscattering based drain current expression is explained using the scattering matrix. In the saturation region of operation, the complicated expression can substantially reduce to a simple one. Then, we will employ the existing quantum mechanical simulator to deal with the sub-band energy levels relevant to the underlying physics.

Section 2.1 Backscattering Theory

From Fig. 1(a), we can see two conduction-bands E_{c1} and E_{c2}: E_{c1} is in the equilibrium condition (V_D=0 V) and E_{c2} refers to the non-equilibrium case with the drain voltage applied. In this figure, F^+ is the injection flux from source to drain and F^- is the flux injected from drain to source. T is the transmission coefficient for the flux from source to drain and the transmission coefficient, T', is in the opposite direction [9].

When the conduction-band is in equilibrium condition, E_{c1}, the scattering matrix is symmetrical, so $T=T'=T_o$. Therefore, the scattering matrix can be written by [9]

$$S=\begin{bmatrix} T & 1-T' \\ 1-T & T' \end{bmatrix}=\begin{bmatrix} T & 1-T \\ 1-T & T \end{bmatrix}=\begin{bmatrix} T_o & 1-T_o \\ 1-T_o & T_o \end{bmatrix} \quad (3)$$

In the case of applying a drain voltage, the symmetry mentioned above no longer exists: the transmission coefficient T' will be smaller depending exponentially on the barrier encountered. We can represent T' by $Te^{-qV_D/KT}$ in the ballistic conditions. The transmission coefficient T may be larger than T_o due to DIBL. So the scattering matrix can be represented by [9]

$$S=\begin{bmatrix} T & 1-Te^{-qV_D/KT} \\ 1-T & Te^{-qV_D/KT} \end{bmatrix} \quad (4)$$

Therefore, the drain current can be described as

$$I_{DS} = W[J^+(0) - J^-(0)] = W[TJ^+(0) - J^-(L)T^-] = qW(F^+T - F^-Te^{-qV_D/KT})$$

$$= qW[F^+(1-R) - F^-(1-R)e^{-qV_D/KT}] \quad (5)$$

Note that $J^-(0) = qF^-(0) = q[F^-T^- + (1-T)F^+] = J^-(L)T^- + (1-T)J^+(0)$. Here R is backscattering coefficient which is defined by $R = 1-T$.

For device operated in **linear region**, $V_D << KT/q$, we have $F^+ \approx F^-$ and $R \approx R_o$. Therefore, the drain current can be expressed by

$$I_D = qW[F^+(1-R_o) - F^-(1-R_o)e^{-qV_D/KT}]$$

$$\approx qW[F^+(1-R_o) - F^-(1-R_o)(1-\frac{qV_D}{KT})] = qWF^+(1-R_o)\frac{qV_D}{KT} \quad (6)$$

At the beginning of the channel, the product of the total carrier density times the thermal injection velocity is

$$n(0)v_{inj}(0) = F^+ - [-(1-R)F^- - RF^+] = (1+R)F^+ + (1-R)F^- = 2F^+. \quad (7)$$

This leads to $F^+ = \frac{v_{inj}}{2}\frac{C_{eff}}{q}(V_G - V_{th})$. We can obtain the drain current formula in the **linear region** :

$$I_{Dlin} = Wv_{inj}C_{eff}(V_G - V_{th})(1-R_o)\frac{V_D}{2KT/q} \quad (8)$$

As for **saturation region** of operation, $V_D >> \frac{KT}{q}$, (5) can reduce to :

$$I_{DS} = qW[F^+(1-R) - F^-(1-R)e^{-qV_D/KT}] \approx qWF^+(1-r_c) \quad (9)$$

Here we have made R= r_c, the channel backscattering coefficient.

Again at the beginning of the channel, we have

$$n(0)v_{inj}(0) = F^+ - [-F^+r_c] = F^+(1+r_c) \quad (10)$$

This readily leads to $F^+ = \frac{n(0)v_{inj}}{1+r_c} = \frac{C_{eff}(V_G - V_{th})v_{inj}/q}{1+r_c}$.

Therefore, we can write the drain current in the **saturation region** as

$$I_{Dsat} = WC_{eff}(V_G - V_{th})v_{inj}\frac{1-r_c}{1+r_c} \quad (11)$$

In real devices, the terminal drain current involves the drain / source series resistances, R_D and R_S, and DIBL (Drain-Induced-Barrier-Lowering). Thus the expression (11) is augmented into

$$I_{Dsat} = WC_{eff}[(V_G - I_D R_S) - (V_{tho} - DIBL \times (V_D - I_D R_S - I_D R_D))]v_{inj}\frac{1-r_c}{1+r_c} \quad (12)$$

where $V_G - I_D R_S$ and $V_D - I_D R_S - I_D R_D$ represent the intrinsic gate voltage and intrinsic drain voltage, respectively.

Section 2.2 Quantum Simulation

In (12), the parameters C_{eff} and v_{inj} could not be directly assessed from the experimental data. They must be calculated with the sub-band energy levels and Fermi level through quantum mechanical simulation.

As the MOSEFT dimension scales down, the quantum effect is more and more important. We employ a 1-D quantum mechanical simulator developed by Prof. Lundstrom and Prof. Datta's the group at Purdue University [10]. This program solves the following equations simultaneously:

$$\frac{\partial^2 V}{\partial z^2} = \frac{\rho}{\varepsilon} \quad \text{(Poisson's Equation)} \quad (13)$$

$$-\frac{\hbar}{2m_z}\frac{\partial^2}{\partial z^2}\psi + V\psi = E\psi \quad \text{(Schrödinger Equation)} \quad (14)$$

With process parameters and the operating temperature as input, the simulator can quantify the sub-band energy levels and Fermi level, which in turn yield electron population in the underlying two-dimensional electron gas (2DEG) inversion layer. Again with the same sub-band levels and Fermi level as input, the effective thermal injection velocity at the top of the source-channel junction barrier can be readily

calculated as [7]

$$v_{inj} = \frac{\sum n_s^i v_{inj}^i}{\sum n_s^i} \tag{15}$$

where n_s^i is the charge density associated with sub-band i in a certain direction and v_{inj}^i is the corresponding thermal injection velocity [7], [11]

$$n_s^i = \gamma \frac{m_{di}}{\pi\hbar^2} \frac{k_B T}{2} \ln[1+\exp(\frac{E_f - E_i}{k_B T})] \tag{16}$$

$$v_{inj}^i = \sqrt{\frac{2k_B T m_{ci}}{\pi m_{di}^2}} \frac{\Im_{1/2}(\frac{E_f - E_i}{k_B T})}{\ln[1+\exp(\frac{E_f - E_i}{k_B T})]} \tag{17}$$

Here, γ is the valley degeneracy, m_{ci} is the conductivity effective mass for subband i, m_{di} is the density-of-states effective mass for subband i, E_i is the energy level of subband i, E_f is the Fermi level, and $\Im_{1/2}$ is the Fermi-Dirac integral of order one-half. For two-fold valleys, $m_{ci} = m_t$ and $m_{di} = m_t$, and for four-fold valleys, $m_{ci} = 2m_t m_l /(m_l + m_t)$ and $m_{di} = (m_t m_l)^{1/2}$. Here the longitudinal mass m_l = 0.916 m_o and the transverse mass $m_t = 0.19 m_o$.

Chapter 3 Extraction and Separation Method

In this experiment, we explore the bulk n-channel MOSFETs, which were fabricated using state-of-the-art process with mask gate width W=10 μm and mask gate length L_{mask} ranging from 10 μm to 0.075 μm. In this study, the main extraction procedure is demonstrated on L_{mask} = 0.09 μm. We adopt HP4156B and a thermal chuck/cooling system with the measurement conditions: V_G = 0~1.2V; V_D = 0.025, 0.1, 0.5, and 1.0V; and the operating temperature = 298K, 263K, and 233K.

Fig. 2 shows the flowchart of the procedure of extracting r_c and l. The round-corner frames indicate experimental data needed; the indented-corner frames represent extracted / simulated parameter values; and the connection lines illustrate the relationship between frames arranged in such a way to assess and decouple backscattering coefficients.

Section 3.1 C-V Fitting

We used ICS software to control HP4284 while measuring C-V characteristics. The C-V measurement was performed on a 50μm×50μm test key. The measured C-V is displayed in Fig. 3.

Section 3.1-1 Process Parameters

The measured C-V curve is compared with that calculated by the quantum simulator with gate oxide thickness T_{ox}, poly doping concentration N_{poly} and channel doping concentration N_{sub} as input. T_{ox}, N_{poly} and N_{sub} each can be adjusted to affect the C-V curve, but only a distinct set of T_{ox}, N_{poly} and N_{sub} can be found with a perfect C-V match. As shown in Fig. 3, T_{ox}, N_{poly} and N_{sub} are simultaneously obtained by C-V fitting. Here, two different C-V comparisons were done: one from

Schrödinger-Poisson solving [10] and the other from Berkeley's C-V simulation. They can both create desirable results, besides at high voltage biases where leakage current occurred in the real experiment. C-V fitting eventually led to T_{ox} = 1.65nm, N_{poly} = $9\times10^{19}cm^{-3}$ and N_{sub} = $8\times10^{17}cm^{-3}$.

Section 3.1-2 Quasi-Equilibrium Device Parameters

With known T_{ox}, N_{poly} and N_{sub} as input, the Schrödinger-Poisson solver was carried out to calculate inversion layer charge Q_{inv}, the thermal injection velocity v_{inj}, and the effective gate capacitance C_{eff}. Fig. 4 shows the calculated inversion charges, Q_{inv}, versus gate voltage for T=298K, 263K, and 233K. The thermal injection velocity, v_{inj}, is displayed in Fig. 5 versus gate voltage with temperature used as the parameter. From these results, some important properties can be drawn. First, at low gate voltage, or at the non-degenerate limit, the thermal injection velocity considerably increases with temperature, regardless of gate voltage. Second, at high gate voltage, or near degenerate limit, the thermal injection velocity increases with gate voltage whereas the rate of increase declines with increasing temperature. The same dependencies are mentioned elsewhere [7]. According to MOS electrostatics, Q_{inv} can be expressed as

$$Q_{inv} = qn_s = C_{eff}(V_G - V_{tho}) \tag{18}$$

The effective oxide capacitive C_{eff} is defined by [12]

$$C_{eff} = \frac{C_I C_Q}{C_I + C_Q} \tag{19}$$

where C_I is the gate dielectric capacitance and C_Q is the semiconductor (or quantum) capacitance related to the quantum mechanical confinement, polysilicon depletion,

finite density-of-states, etc. From the slope of the Q_{inv} versus V_{GS}, as shown in Fig. 6, we obtain C_{eff} =1.366×10^{-6}, 1.371×10^{-6}, and 1.375×10^{-6} F/cm^2 for temperatures of 298, 263, and 233K, respectively.

Section 3.2 Drain Current against Gate Voltage

The drain current versus gate voltage, $I_D - V_G$, is measured under temperatures = 298K, 263K, and 233K for different drain voltages of 0.025V, 0.1V, 0.5, and 1.0V. The results are shown in Fig. 7 for L_{mask} =90nm.

Section 3. 2. 1 Threshold Voltage

The threshold voltage is a key parameter in MOSFET design and modeling. There are many definitions and extraction methods for the threshold voltage. In this work, we employ maximum trans-conductance method in the linear region to assess quasi-equilibrium threshold voltage and the constant subthreshold current method in the saturation region to extract the DIBL [13].

Section 3. 2. 1. 1 Quasi-Equilibrium Threshold Voltage Extraction

The maximum-g_m method is used in the linear region with low V_{DS} of 25mV. In this method, a tangent line is established at the drain current with the maximum trans-conductance, as shown in Fig. 8. However, this method depends strongly on the S/D series resistances [13]. Through linear extrapolation to zero, the quasi-equilibrium threshold voltage V_{tho} was obtained. Fig. 9 shows the extracted V_{tho} versus L_{mask}. For L_{mask} of 90nm, V_{tho} = 0.3282, 0.345, and 0.360V for temperatures of 298, 263, and 233K, respectively.

Section 3. 2. 1. 2 DIBL Extraction

With channel length scaling down, it is gradually important to consider short-channel effects such as V_{th} roll-off and Drain Induced Barrier-Lowering (DIBL). We use constant subthreshold current method to determine threshold voltage operating in the saturation region (high V_{DS}). The critical constant current is defined as the drain current when the gate voltage is the threshold voltage from the maximum-gm method in the linear region [13], as shown in Fig. 10.

Drain-induced-barrier-lowering (DIBL) is defined as the gate voltage shift (ΔV_{GS}) at the constant drain current due to a change in the drain voltage (ΔV_{DS}). From Fig. 11, threshold voltage reduction due to increasing V_{DS} is mainly due to the DIBL effect. Fig. 12 shows threshold voltage versus L_{mask} for drain voltage of 1 V. It can be seen that DIBL effect is insignificant for the long-channel device. With the channel shortening, DIBL effect imposes increasing influence on the threshold voltage.

Section 3. 2. 2 Near-Equilibrium Mobility

We measure the long channel device (L_{mask} =10um) operated at the low drain voltage (V_{DS} =0.025 V) to extract near-thermal-equilibrium mobility. We can establish the mobility relationship from the traditional formula in the linear region. Because V_{DS} is very small, we can write drain current as:

$$I_D = \mu \cdot C_{eff} \cdot \frac{W}{L}[(V_{Go} - V_{th})V_D - \frac{1}{2}V_D^2] \approx \mu \cdot C_{eff} \cdot \frac{W}{L}(V_G - I_D R_S - V_{tho})V_D \qquad (20)$$

Differentiating (20) with respect to the drain voltage, we can get

$$\frac{dI_D}{dV_D} = \mu \cdot C_{eff} \cdot \frac{W}{L} \cdot (V_G - I_D R_S - V_{tho}) \qquad (21)$$

Then, the near-thermal-equilibrium mobility is

$$\mu = \frac{dI_D}{dV_D} \cdot \frac{L}{C_{eff} \cdot W \cdot (V_G - I_D R_S - V_{tho})} \tag{22}$$

The measured near-thermal-equilibrium mobility is plotted in Fig.13 versus effective vertical field for different temperatures. The effective field is defined by the following equation [14]

$$E_{eff} = (\frac{q}{\varepsilon_{si}})(N_{dpl} + \eta\ N_s) \tag{23}$$

where N_{dpl} is the depletion doping concentration and N_s is the inversion layer carrier concentration. According to abrupt junction approximation the N_{dpl} can read:

$$N_{dpl} = (4\varepsilon_{si}\phi_B N_{sub} / q)^{1/2}$$

$$\phi_B = \frac{k_B T}{q} \ln(N_{sub} / n_i) \tag{24}$$

where ϕ_B is the difference between E_{Fi} and E_F (p-type) and N_{sub} is the substrate impurity concentration. In (23), η is a key parameter in determining E_{eff}. On the (100) surface η is taken to be $\frac{1}{2}$ for the electron mobility and $\frac{1}{3}$ for the hole mobility [14].

From our study, the mobility can be divided into three distinct regions: Coulomb scattering, phonon scattering, and surface scattering. The Coulomb scattering (ionized impurity in the depletion and charges in the oxide) dominates at the low field and low temperature region. The surface roughness scattering has a strong dependence on the field, because the strong field can confine carriers close to the interface where the scattering practically occurs. The phonon scattering is well recognized to have strong temperature dependence [14], [15].

From Fig. 14, we can elucidate why mobility increases as the temperature decreases. Because the occupancy of 2-fold valleys gradually increases as the temperature drops down. Since the 2-fold valleys have the lower transverse effective

mass parallel to the interface or channel than 4-fold valleys. Therefore, the mobility increases with decreasing temperature.

Section 3. 2. 3 Mean-Free-Path for Backscattering

The mean-free-path, λ , is a controlling factor that determines device performance, especially in the nano-scale MOSFETs. In the backscattering theory, we use the wave concept to describe the carrier transport in the channel. While a carrier crosses a unit length, the possibility of collision can be represented by $1/\lambda$. Therefore, as the channel length becomes smaller than mean-free-path, there is less possibility to run into the scattering. From this aspect, the mean-free-path can influence the backscattering coefficient r_c.The mean-free-path λ is related with μ and v_{inj} by [2]

$$\lambda = \frac{2k_B T}{q}\frac{\mu}{v_{inj}} \tag{25}$$

Therefore, we can extract mean-free-path for backscattering from the previous results. The calculated mean-free-path versus gate voltage is plotted in Fig. 15.

Section 3.3 Gate Current against Gate Voltage

$I_G - V_G$ curves are measured for different L_{mask} , ranging from 10μm to 0.075μm. They are shown in Fig. 16. With such $I_G - V_G$ data, the corresponding gate length L_{gate} may be obtained through the ratio technique.

Section 3.3.1 Effective Length

For a well-fabricated wafer, the L_{mask} versus L_{eff} can be plot ted in terms of a linear relationship. L_{mask} is the design length on the polysilicon mask and L_{eff}

depends upon the lithography and etching process. There are a number of process variations affecting L_{eff}. Thus L_{eff} may be either larger or smaller than L_{mask}. For the same L_{mask} design, L_{eff} may vary across the wafer. By keeping the same gate current per unit area, we can extract L_{eff} via

$$\frac{I_G{}^o}{L_{eff}^o W^o} = \frac{I_G{}^i}{L_{eff}^i W^i} \Rightarrow L_{eff}^i = L_{eff}^o \frac{W^o}{W^i} \frac{I_G^i}{I_G^o} \tag{26}$$

In Equation (26), the superscript "i" represents the short-channel device and the superscript "o" represents the long-channel device. Taking $I_G - V_G$ data of L_{mask} =10μm to compare with those from short channel devices, the L_{eff} in the latter can be determined. Fig. 17 shows the resultant L_{mask} and corresponding L_{eff}.

Section 3.3.2 Source / Drain Series Resistance Extraction

As depicted in Fig. 18 (a), there exists the parasitic series resistance R_{SD} between the external terminal and the active region. The effect of the source / drain series resistance must be examined using the equivalent circuit in Fig. 18 (b). In our work, we assume the source series resistance R_S to be equal to the drain series resistance R_D. R_S and R_D each connect intrinsic MOSFET to the external terminals where a drain to source bias $V_{DS}^{'}$ is applied. Therefore, the intrinsic gate voltage and intrinsic drain voltage can be written by $V_{GO} = V_G^{'} - I_D R_S$ and $V_{DSO} = V_{DS}^{'} - I_D R_{SD}$, respectively.

The externally measured total resistance can be written as [16]

$$R_{tot} \equiv \frac{V_{DS}^{'}}{I_D} = R_{SD} + R_{ch} \tag{27}$$

where $V_{DS}^{'}$ and I_D correspond to the linear region or low-drain bias and R_{ch} is the channel resistance as defined by [16]

$$R_{ch} \equiv \frac{V_{DSO}}{I_{DS}} = \frac{L_{mask} - \Delta L}{\mu_{eff} C_{ox} W (V_G - V_{th})} = \frac{L_{eff}}{\mu_{eff} C_{ox} W (V_G - V_{th})} \tag{28}$$

where ΔL is the channel length variation and V_{th} is associated with the intrinsic devices. Then, by substituting (28) into (27) for different L_{mask} and with the same W, the parameters R_{SD}, ΔL, and C_{ox} can be obtained within the process variation. During the procedure, μ_{eff} does not change with channel length. The linear threshold voltage V_{th} depends on channel length because of short channel effects. From above statements, the total resistance can be represented by [16]

$$R_{tot}(V_G) = R_{SD} + L_{eff} f(V_G - V_{th}) \tag{29}$$

In order to solve R_{SD}, L_{eff} and V_{th} simultaneity, differentiating (29), with respect to V_G while keeping R_{SD} independent or a weak function of V_G, leads to

$$S(V_G) \equiv \frac{dR_{tot}}{dV_G} = L_{eff} \frac{df(V_G - V_{th})}{dV_G} \tag{30}$$

In well defined shift-and-ratio extraction method, two kinds of devices are included: one long channel device and the other short channel device. The ratio between the two channels is [16]

$$r(\delta, V_G) \equiv \frac{S^o(V_G)}{S^i(V_G - \delta)} \tag{31}$$

where the superscript "i" represents the short-channel device and the superscript "o" represents the long-channel device. When the amount δ is equal to the threshold voltage difference between the two devices, $(V_{th}^o - V_{th}^i)$, the ratio r becomes nearly independent of V_G. Once the correct shift is found, it is a straightforward way to

solve L_{eff}^{i} from the ratio r. The channel length can be solved from the averaged ratio [16]

$$< r >_{\delta_{\min}} = \frac{L_{eff}^{o}}{L_{eff}^{i}} \approx \frac{L_{mask}}{L_{eff}^{i}} \tag{32}$$

As for R_{SD}, it can be calculated from (29) or equivalently the formulation [16]:

$$R_{SD} = \frac{< r >_{\delta_{\min}} R_{tot}^{i}(V_G - \delta_{\min}) - R_{tot}^{o}(V_G)}{< r >_{\delta_{\min}} - 1} \tag{33}$$

Taking L_{mask} =1.2 μm as a typical long channel case, the resulting R_{SD} and effective channel lengths are shown in Fig. 19 versus L_{mask}. A straight line through the data points in Fig.19 reveals that the channel length variations are fairly constant for all undertaken devices. The R_{SD} can also be regarded constant. The average value of R_{SD} =150 $\Omega - \mu m$ was then determined, leading to $R_S (= R_D) \approx 75\,\Omega - \mu m$.

Section 3.4 Results

According to the drain current formula (12), we can see that all the required parameters have been extracted. Thus, the backscattering coefficient r_c can be extracted by I-V fitting. The results are given in Fig. 20 (a) against gate voltage for V_D = 1V with temperature used as the parameter. Fig. 20 (b) and (c) are the case of V_D = 0.5V and 0.1V, respectively. From Fig. 20, it can be seen that (1) r_c decreases with increasing gate voltage and then, critically, tends to saturate for $V_G \geq 0.8$V; (2) at V_D=0.1V, r_c is nearly constant; (3) r_c increases with decreasing drain voltage; and (4) r_c decreases with decreasing temperature. From these results, we can argue that the temperature primarily controls the thermal vibrations in the silicon lattice, which cause the phonon scattering. Therefore, lowering the device temperature can reduce the phonon scattering and the backscattering coefficient [1].

Because the magnitude of the mean-free-path and the backscattering coefficients have been known, the corresponding k_BT-layer width can readily be obtained by the following formula:

$$r_c = \frac{l}{\lambda + l} \tag{34}$$

The results for different drain voltages are shown in Fig. 21 versus gate voltage for three temperatures. From Fig. 21 (a) and (b), it can be seen that the k_BT-layer width narrows with increasing gate voltage. In Fig. 21 (c), it can be observed that k_BT-layer width is not quite sensitive to gate voltage. As far as temperature relationship is concerned, k_BT-layer width decreases as decreasing temperature. A change in temperature produces a broad spreading in k_BT-layer widths, especially at low gate voltages.

Chapter 4 Temperature Coefficient Method

Section 4.1 Power-Law Relationship

In the above chapters, we can see that there are many parameters having some relations with the temperature. This means that another method can be developed to calculate backscattering coefficient, r_c. To do so, we replace separate r_c with λ and ℓ:

$$I_{Dsat} = WC_{eff}(V_G - I_D R_S - V_{th})v_{inj}\frac{1-r_c}{1+r_c} = WC_{eff}(V_G - I_D R_S - V_{th})v_{inj}\frac{\lambda/\ell}{2+\lambda/\ell} \quad (35)$$

To accommodate Eq. (35), the following power-law relationships are established:

$$\begin{aligned} &v_{inj} \propto T^a && \frac{dV_{th}}{dT} = \eta \\ &\mu \propto T^b && \\ &l = DT^d && C_{eff} \propto T^{\beta} \\ &\lambda = \frac{2k_B T \cdot \mu}{q \cdot v_{inj}} = CT^{b+1-a} && I_D \propto T^{\alpha} \end{aligned} \quad (36)$$

From the above relationships, we obtain

$$\frac{\lambda/\ell}{2+\lambda/\ell} = \frac{CT^{b+1-a}}{2DT^d + CT^{b+1-a}} \quad (37)$$

Differentiating (37) with respect to temperature leads to

$$\frac{d(\frac{\lambda}{2l+\lambda})}{dT} = \frac{d(\frac{CT^{b+1-a}}{2DT^d + CT^{b+1-a}})}{dT} = \frac{(b+1-a-d)DT^d\,2CT^{b-a}}{(2DT^d + CT^{b+1-a})^2} \quad (38)$$

Again differentiating (35) with respect to temperature produces

$$\begin{aligned} \frac{dI_D}{dT} = \ \mathrm{W}\,[& v_{inj}\frac{\lambda}{2l+\lambda}\frac{dC_{eff}}{dT}(V_G - I_D R_S - V_{th}) + v_{inj}\frac{\lambda}{2l+\lambda}C_{eff}(-\frac{dI_D}{dT}R_S - \frac{dV_{th}}{dT}) \\ & + \frac{\lambda}{2l+\lambda}C_{eff}(V_G - I_D R_S - V_{th})\frac{dv_{inj}}{dT} + C_{eff}(V_G - I_D R_S - V_{th})v_{inj}\frac{d(\frac{\lambda}{2l+\lambda})}{dT}\,] \end{aligned} \quad (39)$$

Further dividing (39) by drain current, one obtains

$$\frac{dI_D}{dT}\times\frac{1}{I_D}=\frac{dC_{eff}}{dT}\times\frac{1}{C_{eff}}+\frac{dv_{inj}}{dT}\times\frac{1}{v_{inj}}+\left(-\frac{dI_D}{dT}R_S-\frac{dV_{th}}{dT}\right)\times\frac{1}{V_G-I_DR_S-V_{th}}+$$

$$\frac{d\left(\frac{\lambda}{2l+\lambda}\right)}{dT}\times\frac{2l+\lambda}{\lambda} \qquad (40)$$

Finally substituting (38) into (40), we get

$$\frac{dI_D}{dT}\times\frac{1}{I_D}=\frac{\alpha}{T}=\frac{\beta}{T}+\frac{1}{V_G-I_DR_S-V_{th}}\left(-\frac{dI_D}{dT}R_S-\eta\right)+\frac{1}{T}\left(a+\frac{2(b+1-a-d)}{2+\lambda/l}\right)$$

As a result of mathematical manipulation, an analytic form is created:

$$\frac{\lambda}{l}=\frac{-2(b+1-a-d)}{a-\alpha+\beta-\frac{T\left(\eta+\frac{dI_d}{dT}Rs\right)}{V_G-I_DR_s-V_{th}}}-2 \qquad (41)$$

Section 4.2 Temperature Coefficients Extraction

According to Eq. (41), there are six temperature coefficients: a, b, d, β, η and α, which can be individually assessed by thermal injection velocity v_{inj} in Fig. 5, the mobility μ in Fig. 13, the k_BT layer width l in Fig. 21, the effective gate capacitance C_{eff} in Fig. 6, the threshold voltage V_{th} in Fig. 9 and 12, and the drain current in Fig. 7, respectively. They are addressed in the following.

Section 4. 2. 1 Thermal Injection Velocity, Mobility, and k_BT Layer Width

The extracted temperature-dependent power coefficients a, b, and d at different drain voltages are shown in Fig. 22 against gate voltage. We can see that the v_{inj} component, a, decreases as the gate voltage increases and the l component, d, maintains “a” nearly constant value of around 0.5 regardless of drain voltage. The mobility component, b, decreases and tends to saturate with increasing gate voltage.

Section 4.2.2 Gate Capacitance

From the above treatments, C_{eff} =1.3663×10^{-6}, 1.3709×10^{-6}, 1.3749×10^{-6} F/cm^2 for temperatures of 298, 263, and 233K, respectively. This leads to the power coefficient of the effective capacitance, β =-2.515×10^{-2}.

Section 4.2.3 Threshold Voltage

From the above definition, the threshold voltage is written as

$$V_{th} = V_{tho} - \Delta V_{th} = V_{tho} - DIBL \times V_D \tag{42}$$

To simplify the V_{th} relationship with temperature, we combine V_{tho} with DIBL using a linear relation to find the temperature coefficient; That is,

$$\eta = \frac{dV_{th}}{dT} \tag{43}$$

Fig. 23 shows the resultant η versus L_{mask} for different drain voltages. In the case of L_{mask} =90nm, η = -0.49mV/K as from the near-equilibrium threshold voltage for three temperatures. It is also found that η slightly decreases with increasing drain voltage and increasing L_{mask}.

Section 4 Corroborating Evidence

According to (41), λ / l was calculated as given in Fig. 24 against gate voltage for three different drain voltages. Also plotted together in Fig.24 is that from the extraction/decoupling procedure. Again, good agreement was simultaneously achieved for three different drain voltages. This is also the case for r_c as shown in Fig.25. Therefore, the work can reasonably confirm not only the validity of the extraction and separation method but also the channel backscattering theory itself.

Chapter 5 Near-Source Conduction-Band Profiles

In the framework of channel backscattering theory, near-source conduction-band profiles can determine the performance of the device. The injected carriers encounter possibility of the backscattering in the k_BT-layer region. Out of this region the carriers will still run into the scattering, but they do not have enough energy to return into the source. Therefore, it is very important to create the near-source conduction -band profiles. The source-channel junction barrier heights are modulated by the gate voltage as well as drain voltage. Therefore, the k_BT-layer width is influenced by the gate voltage, the drain voltage, and the operating temperature. In this chapter, we will examine the k_BT-layer width in more details.

Section 5.1 Created Conduction-Band Profiles

Within the framework of the channel backscattering theory, the channel conduction-band is bent down by a thermal energy k_BT while traversing from the injection point (i.e., the top of the source-channel barrier) to the end of the layer. According to this definition, the temperature dependent k_BT-layer widths in Fig. 21 were transformed into near-source channel conduction-band profiles. The power exponent "d" associated with the k_BT-layer width, which can be taken as a measure of the degree of the band bending, appears to remain constant (≈ 0.5 in average), regardless of drain voltage. Hence, we can write $l = \vartheta\ (k_BT/q)^{0.5}$ with ϑ as a fitting parameter. Surprisingly, this expression is comparable with that deduced from approximate solving of Poisson's equation [17]. Fig. 26 shows corresponding extracted ϑ versus gate voltage for different temperatures, revealing that ϑ is indeed independent of temperature. Therefore, we can reasonably plot the near near-source conduction-band profile, along the channel as shown in Fig. 27. The

potential gradient increases in magnitude with increasing distance from the source, as expected. At drain voltage of 1.0V and 0.5V, we can see that the conduction-band profile depends strongly upon as gate voltage. However, at lower drain voltage of 0.1V, the conduction-band profile is a weak function of gate voltage.

Section 5.2 Guidelines and Compact Model

Indeed, the strictly confirmed near-source conduction-band profiles in Fig. 8 are of value in the areas of channel backscattering. They straightforwardly furnish several guidelines. Firstly, the channel potential profiles are a weak function of gate voltage for V_D = 0.1 V as compared with higher drain voltages. This is expected since in the linear region (i.e., V_D = 0.1 V), the channel inversion layer electrically connects source and drain together and as a result, the whole channel undergoes the potential modulation by gate voltage. Secondly, for V_D = 0.5 and 1 V, the channel potential profiles are a strong function of gate voltage while drain voltage is to produce a shift in the l versus V_G curve. Such dependencies are due to the presence of the off-equilibrium region near the drain. In other words, only part of the channel near the source experiences the potential modulation by gate voltage; and an increase in drain voltage causes an increase in the width of the off-equilibrium region. Thirdly, there is a power law relationship between the layer width and thermal energy with the power exponent (≈ 0.5) independent of temperature, gate voltage, and drain voltage.

Based on above guidelines, a compact model can be established for the layer of interest in the saturation case:

$$l = 34 \times \left(\frac{k_B T}{q}\right)^{0.5} V_D^{-0.27} \left(V_G - V_{tho} + DIBL \times V_D\right)^{-0.6} \quad \text{(nm)} \tag{44}$$

This model adequately reproduces the experimental drain current at V_D = 0.5 and 1 V against gate voltage for three temperatures, as shown in Fig. 28 (a), (b), and (c). It is

noteworthy that l follows the amount of injected carriers, which is related to the term ($V_G - V_{tho} + DIBL \times V_D$), rather than the single V_G. The reasons are that the latter produced a poor fitting. As for the V_D = 0.1 V, we made ϑ=160nm/V$^{0.5}$ that can lead to good reproduction for three different temperatures as shown in Fig. 28 (a), (b), and (c).

Chapter 6 Conclusion

Near-source channel conduction-band profiles have been systematically produced through the decoupling of the channel backscattering coefficients in a nanoscale MOSFET. The validity of the decoupling/transformation process has been corroborated in a self-consistent manner. The strictly confirmed conduction-band profiles are of value in the areas of channel backscattering. The details of the experimental band bending have also straightforwardly provided new guidelines leading to a compact model for the layer of interest. This new model has exhibited the ability to reproduce above-threshold drain currents for different drain voltages, different gate voltages, and different temperatures.

References:

[1] Mayank Gupta, “Ballistic MOSFETs, the Ultra Scaled Transistors”, *IEEE Potentials,* Volume 21, Issue 5, Dec 2002-Jan 2003 Page(s):13 – 16.

[2] M. S. Lundstrom, “Elementary scattering theory of the Si MOSFET,” *IEEE Electron Device Letters*, vol. 18, pp. 361-363, July 1997.

[3] D.K. Ferry, R. Akis, D. Vasileska, “Quantum effects in MOSFETs: use of an effective potential in 3D Monte Carlo simulation of ultra-short channel devices,” *IEDM Tech. Digest*, pp. 287 -290, 2000.

[4] M. S. Lundstrom and Z. Ren, “Essential physics of carrier transport in nanoscale MOSFETs,” *IEEE Trans. Electron Devices*, vol. 49, pp. 133-141, Jan. 2002.

[5] M.-J. Chen, H.-T. Huang, K.-C. Huang, P.-N. Chen, C.-S. Chang, and C. H. Diaz, “Temperature dependent channel backscattering coefficients in nanoscale MOSFETs,” in *IEDM Tech. Dig.*, Dec. 2002, pp. 39-42.

[6] G. Timp, J. Bude, K. K. Bourdelle, J. Garno, A. Ghetti, H. Gossmann, M. Green, G. Forsyth, Y. Kim, R. Kleiman, F. Klemens, A. Kornblit, C. Lochstampfor, W. Mansfield, S. Moccio, T. Sorsch, D. M. Tennant, W. Timp, and R. Tung, “The ballistic nano-transistor,” in *IEDM Tech. Dig.*, Dec. 1999, pp. 55-58.

[7] F. Assad, Z. Ren, D. Vasileska, S. Datta, and M. S. Lundstrom, “On the performance limits for Si MOSFET’s: a theoretical study,” *IEEE Trans. Electron*

Devices, vol. 47, pp. 232-240, Jan. 2000.

[8] M.-J. Chen, H.-T. Huang, Y.-C. Chou, R.-T. Chen, Y.-T. Tseng, P.-N. Chen, and C. H. Diaz, "Separation of channel backscattering coefficients in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, pp. 1409-1415, Sept. 2004.

[9] Mark Lundstrom, *Fundamentals of Carrier Transport, second edition*, School of Electrical and Computer Engineering Purdue University, West Lafayette, Indiana, USA: Cambridge University Press, 2000.

[10] http://www.nanohub.purdue.edu

[11] K.Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.,* Vol.76, pp.4879-4890.Oct. 1994.

[12] Jing Wang, and M. S. Lundstrom, "Ballistic transport in high electron mobility transistor," *IEEE Trans. Electron Devices*, vol. 50, pp. 1404-1609, Sept. 2003.

[13] X. Zhou, K.Y. Lim, and D. Lim, "A simple and unambiguous definition of threshold voltage and its implications in deep-submicron MOS device modeling," *IEEE Trans. Electron Devices*, vol. 46, pp. 807-809, Sept. 1999.

[14] Shin–ichi Takagi, Akira Toriumi, Masao Iwase, and Hiroyuki Tango, "On the universality of inversion layer mobility in Si MOSFETs: Part I－effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, pp. 2357-2368, Sept. 1994.

[15] Shin–ichi Takagi, Judy L. Hoyt, Jeffrey J. Welser, and James F. Gibbons, " Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field effect transistors," *J. Appl. Phys.,* Vol.80, pp.1567-1577, Aug. 1996.

[16] Yuan Taur, "MOSFET Channel Length: Extraction and Interpretation," *IEEE Trans. Electron Devices*, vol. 47, pp.160-169, Jan. 2000.

[17] A. Rahman and M. S. Lundstrom, "A compact scattering model for the nanoscale double-gate MOSFET," *IEEE Trans. Electron Devices,* vol. 49, pp. 481-489, March 2002.