A 40 mW 3 Gb/s Self-Compensated Differential Transimpedance Amplifier With Enlarged Input Capacitance Tolerance in 0.18 μm CMOS Technology

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***Abstract*—By combining an appropriate differential-sensing scheme with the bootstrapping technique, this paper presents a self-compensated design topology which is shown to be effective at reducing the loading effects due to the photodiode and the ESD protection circuit at the differential inputs. The built-in offset creation technique is introduced to overcome voltage headroom limitation. Furthermore, the negative impedance compensation is employed to enhance the gain-bandwidth product. The IC is shown to be tolerant of ESD protection circuit with 0.5 pF equivalent capacitance at the differential inputs. While connected to an InGaAs PIN photodiode exhibiting 0.8 pF equivalent capacitance, the implemented IC has achieved a differential transimpedance gain of 3.5 kΩ and a -3 dB bandwidth of 1.72 GHz. At a data rate of 3 Gb/s, the measured dynamic range is from -20 dBm to $+0$ dBm at a bit-error rate of 10^{-12} with a $2^{31}-1$ pseudorandom test pattern. The negative impedance compensation is shown to achieve enhancement factors of 4.5 dB and 520%, respectively, for transimpedance gain and -3 dB bandwidth. The IC totally consumes 40 mW from a 1.8 V supply.**

***Index Terms*—Negative impedance compensation, optical receiver, transimpedance amplifier.**

I. Introduction

FOR optical communications, the optical receiver front-end plays an important role in determining the dynamic range of the whole network. A typical optical receiver front-end consists of a photodiode (PD), a transimpedance amplifier (TIA) and a limiting amplifier (LA). Nowadays, most commercial products have been connected to off-chip PDs fabricated in III-V compound semiconductor technology to achieve high bandwidth and high sensitivity simultaneously. To guarantee acceptable production yield, appropriate on-chip ESD protection circuit must be included in the TIA design. Inevitably, both the PD and the ESD protection circuit may contribute significant input capacitances to the TIA. For multi-gigabit applications, generally the PD equivalent capacitance lies between 0.5 pF and 1 pF. Typically, the equivalent capacitance of the ESD protection circuit lies in sub-pF range. It has been shown that the resulting input capacitance may significantly degrade both the bandwidth and the sensitivity in conventional designs [1]. To make a high-gain TIA more tolerant of large input capacitance, the multi-stage design topology has been widely employed in the past decade [2], [3]. It is capable of achieving low equivalent input resistance without sacrificing transimpedance gain and noise performance. However, it may suffer from large power consumption and poor phase margin. Considering the low input resistance requirement, apparently the common-base and common-gate amplifier may become other attractive candidates. Furthermore, by incorporating the transconductance boosting technique, the regulated-cascode design topology has become one other main stream especially suitable for high-speed applications [4]–[6]. However, its major drawback is the resulting poor noise performance. To further extend the operating data rate of a TIA, various inductive peaking techniques have been developed in the past years [7], [8]. Recently, the negative-impedance compensation (NIC) has been successfully employed to implement low-power low-noise TIA [9] and LA [10]. The NIC has been shown to be capable of improving gain and bandwidth simultaneously. Compared to the inductive peaking, the NIC is not only more flexible but also cost-effective. In summary, all of the design techniques described above focus on the TIA design without any appropriate treatment of the input loading capacitances. Apparently, once the input capacitance can be reduced, the following TIA design becomes significantly simplified. Employing a positive feedback loop for the voltage control of the PD, the bootstrapping technique, as proposed in our previous work [11], has been shown to be capable of reducing the effective input capacitance due to the PD. As a result, a TIA with both high transimpedance gain and wide dynamic range can be easily achieved. Furthermore, by combining an appropriate differential-sensing scheme with the bootstrapping technique, we have successfully demonstrated a self-compensated TIA (SC-TIA) with enlarged input capacitance tolerance [12]. Recently, several fully-differential CMOS TIAs have been demonstrated for multi-gigabit applications in literatures [13], [14]. However, these designs lack the capability to provide dc signal path as well as a suitable PD reverse bias voltage. In this paper, we will discuss the fundamentals of the SC-TIA and the NIC. Then we will propose a wide dynamic range CMOS SC-TIA design employing the NIC for achieving greatest enhancements in both transimpedance gain and bandwidth.

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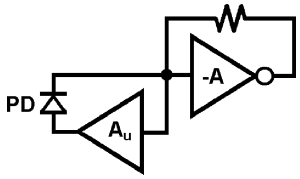

Fig. 1. Schematic of TIA employing bootstrapping technique.

II. Fundamentals of SC Design Topology

In a conventional single-ended TIA, one terminal of the PD is connected to the TIA input and the other terminal is connected to a constant bias voltage. Therefore the PD behaves like a loading capacitance at the TIA input. The bootstrapping technique, as shown in Fig. 1, introduces an additional positive feedback loop for appropriate voltage control of the PD. Therefore, the voltage at the PD anode will automatically track the voltage at the PD cathode to reduce the photocurrent-induced transient voltage across the PD. As a result, the effective input capacitance due to the PD with a equivalent capacitance C_D is given by

$$C_{\text{in}} = C_D \cdot (1 - A_u). \tag{1}$$

To achieve a better capacitance suppression ratio, a unity-gain voltage buffer with low output impedance is required. However $A_u < 1$ is required for stability in this design. On the other hand, if both the photocurrents coming from the anode and the cathode of the PD can be used for signal detection simultaneously, then a differential-sensing design with doubled transimpedance gain can be obtained. The differential-sensing scheme potentially provides improved signal-to-noise ratio and power supply rejection. Apparently the simplest implementation of the unity-gain voltage buffer is a source follower. As we can see, the source buffer can also serve as a unity-gain current buffer to transfer the photocurrent coming from the PD anode to its drain terminal so as to enable the desired differential-sensing capability. The proposed SC design topology is shown in Fig. 2, where C_1 and C_2 denote the grounded input capacitances due to the bondpads and the ESD protection circuits, R_{in} denotes the equivalent input resistance of the following TIA. Both the current sources I_1 and I_2 are required to bias M_1 properly. Assume that the channel length modulation effect, the body effect, and all the other parasitic capacitances are negligible. We have

$$\frac{V_1}{I_{\text{in}}} = R_{\text{in}} \frac{1 + \frac{s}{z_1}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{2}$$

$$\frac{V_2}{I_{\text{in}}} = -R_{\text{in}} \frac{1 + \frac{s}{z_2}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{3}$$

where

$$\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right) = 1 + s\left[R_{\text{in}}C_2 + \frac{C_D + C_1}{g_{m1}}\right] + s^2 \frac{R_{\text{in}}(C_D C_1 + C_D C_2 + C_1 C_2)}{g_{m1}} \tag{4}$$

$$z_1 = \frac{1}{R_{\text{in}}(C_1 + C_2)} \text{ and } z_2 = \frac{g_{m1}}{C_1}. \tag{5}$$

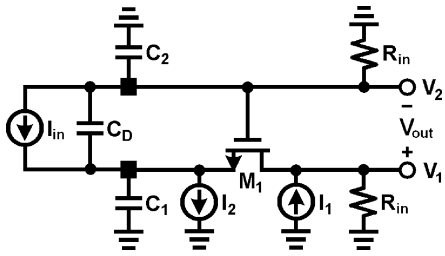

Fig. 2. Schematic of the SC design topology.

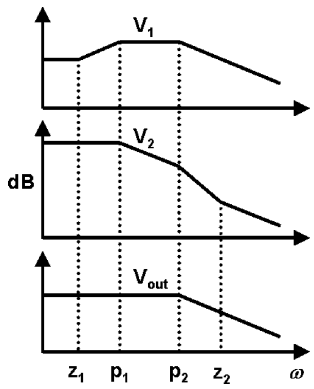

Fig. 3. Photo responses of the SC design topology.

Assuming $g_{m1}R_{\text{in}} \gg 1$ and $p_1 \ll p_2$, the two pole frequencies can be approximated as

$$p_1 = \frac{1}{R_{\text{in}}C_2} \text{ and } p_2 = \frac{g_{m1}}{C_D + C_1 + \frac{C_D C_1}{C_2}}. \tag{6}$$

It is apparent that $z_1 < p_1 < p_2 < z_2$. Therefore the differential photoresponse is given by

$$\frac{V_{\text{out}}}{I_{\text{in}}} = \frac{V_1 - V_2}{I_{\text{in}}} = R_{\text{in}} \frac{2 + s\left(\frac{1}{z_1} + \frac{1}{z_2}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \approx 2R_{\text{in}} \frac{1 + \frac{s}{(2z_1)}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)}. \tag{7}$$

Considering a typical case $C_1 = C_2 = C$, from (5) and (6) we have $p_1 = 2z_1$. As a result, perfect pole-zero cancellation occurs in (7). It follows that the -3 dB bandwidth of the differential photo response is limited by the second pole which is given by

$$p_2 = \frac{g_{m1}}{(2C_D + C)}. \tag{8}$$

Fig. 3 shows the corresponding Bode magnitude plots of the photo responses derived above. In summary, the grounded input capacitances C_1 and C_2 cause a bandwidth reduction in the photo response V_2 and a high-frequency peaking in the photo response V_1. If C_1 and C_2 are approximately equal, then these two effects can ideally cancel each other to minimize the resulting bandwidth degradation. Therefore, the differential photo response becomes less sensitive to the grounded input capacitances. If the bootstrapping transistor M_1 is excluded in Fig. 2,

then it becomes a symmetric differential-sensing scheme. The resulting pole frequency can be derived as

$$p_{SDS} = \frac{1}{[R_{\rm in}(2C_D + C)]}. \tag{9}$$

From (8) and (9), it shows that the SC design topology achieves a bandwidth enhancement factor of $(g_{m1}R_{\rm in})$. Moreover, as we can see in Fig. 2, the SC design topology can automatically provide a reverse bias voltage of $V_{\rm GS}$ to the PD so as to guarantee an acceptable operating bandwidth.

The price paid in the SC design topology is the extra noise introduced by the bootstrapping transistor and the required bias current sources. Assuming that the noise currents in these three components follow the direction of the bias current, the equivalent input noise currents of the following TIA are derived as

$$I_{n,V1} = \frac{V_{n,V1}}{R_{\rm in}} = I_{n,I1} - \frac{\frac{s}{p_2}}{1+\frac{s}{p_2}} I_{n,M1} - \frac{1}{1+\frac{s}{p_2}} I_{n,I2} \tag{10}$$

$$I_{n,V2} = \frac{V_{n,V2}}{R_{\rm in}} = \alpha \frac{\frac{s}{p_2}}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} (I_{n,M1} - I_{n,I2}) \tag{11}$$

where $\alpha = C_D/(2C_D + C) < 0.5$. The differential noise current is given by

$$I_{n,eq} = I_{n,V1} - I_{n,V2} = I_{n,I1} - I_{n,M1} + \frac{1 + s\left(\frac{1}{p_1} - \frac{\alpha}{p_2}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} (I_{n,M1} - I_{n,I2}). \tag{12}$$

It follows $I_{n,eq} \approx I_{n,V1}$ because $p_2 \gg \alpha p_1$. That is, the noise current $I_{n,V2}$ is negligible compared to $I_{n,V1}$. Computing the mean-square values, we have

$$\overline{I_{n,eq}^2} \approx 4kT\gamma \left[g_{m,I1} + \frac{g_{m,M1}\frac{\omega^2}{p_2^2}}{1+\frac{\omega^2}{p_2^2}} + \frac{g_{m,I2}}{1+\frac{\omega^2}{p_2^2}} \right] \tag{13}$$

where ω is the angular frequency and γ is the noise factor of the MOSFET. At low frequencies the noise performance is dominated by the noise components introduced by I_1 and I_2 [1]. The noise component introduced by M_1 increases with increasing frequency. To reduce the noise current, long-channel transistors can be used to provide I_1 and I_2 owing to the decrease in γ. Furthermore, for a given bias current, the overdrive voltages of the transistors must be maximized to improve the noise performance. As we can see, the obtained noise performance is similar to that obtained in the common-gate amplifier. The major advantage of the SC design topology is the improved SNR by a factor of 6 dB due to its differential-sensing capability.

III. Fundamentals of NIC

Fig. 4 shows the small-signal model for a TIA employing the NIC, where the Norton equivalent is used to model the inverting amplifier and the employed negative impedance is denoted by $-\mathrm{Z}_C$. The closed-loop transimpedance gain can be derived as

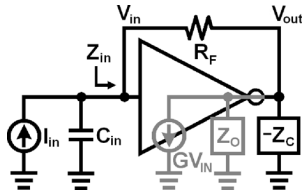

Fig. 4. Schematic of TIA employing NIC.

$$\frac{V_{\rm out}}{I_{\rm in}} = \frac{V_{\rm in}}{I_{\rm in}} \cdot \frac{V_{\rm out}}{V_{\rm in}} = \left(\frac{1}{\frac{1}{Z_{\rm in}} + sC_{\rm in}} \right) A_V \tag{14}$$

where

$$A_V = \frac{V_{\rm out}}{V_{\rm in}} = -\frac{G - \frac{1}{R_F}}{\frac{1}{R_F} + \frac{1}{Z_o} - \frac{1}{Z_C}} \tag{15}$$

$$Z_{\rm in} = \frac{R_F}{1 - A_V}. \tag{16}$$

Typically we have $G \gg 1/R_F$. From (15), the NIC is shown to effectively cancel the loading effects caused by Z_o and R_F. To maximize the enhancement, the NIC must provide both resistive and capacitive compensations. As we can see from (15), the negative resistance and the negative capacitance can enhance the dc gain and the bandwidth of the closed-loop voltage gain, A_V, respectively. From (16), hence the equivalent input impedance $\mathrm{Z}_{\rm in}$ can be significantly reduced. For a large $C_{\rm in}$, generally the input pole dominates the frequency response of the transimpedance gain. Once $\mathrm{Z}_{\rm in}$ can be reduced, the input pole can be moved to a higher frequency. For high-gain applications, it is apparent that Z_o is the major object to be compensated. Therefore, if the output impedance Z_o can be kept as high as possible, then not only the implementation of the required NIC becomes easier but also the noise introduced by the NIC can be minimized.

IV. Chip Implementation

Fig. 5 shows the complete circuit diagram of the SC-TIA IC. The IC is implemented in a 0.18 μm CMOS technology. To reduce waveform distortion and improve overload characteristic, it is necessary to incorporate automatic offset cancellation (AOC) circuit. In this design, the AOC is provided by a dual-loop feedback circuit comprising two error amplifiers and two controllable current sources realized by M_2 and M_3. The working principle of the AOC is to maintain constant dc currents passing through both feedback resistors while receiving the photocurrent. An on-chip grounded capacitor of several pF is connected to the output of each error amplifier to introduce a lower cut-off frequency of about 50 kHz. A simple RC network, comprising R_C and C_C, is used to provide both the ac coupling path required for capacitance suppression and the dc control of the PD reverse bias voltage. In this design, the supply voltage is 1.8 V and the reverse bias voltage for the PD is 1.2 V. If the input dc currents of the core differential TIA, T_1, are kept close to zero, then the voltage headroom available for the output of T_1 is about a half of the rest voltage headroom, that is, 0.3 V. Apparently, it may cause difficulty in achieving high open-loop

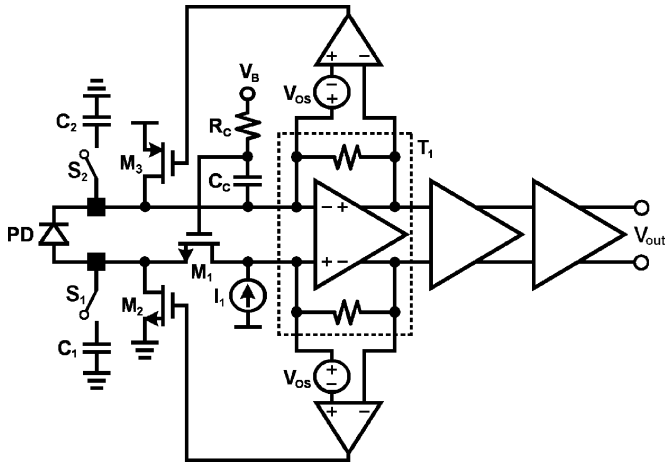

Fig. 5. Schematic of the SC-TIA IC.

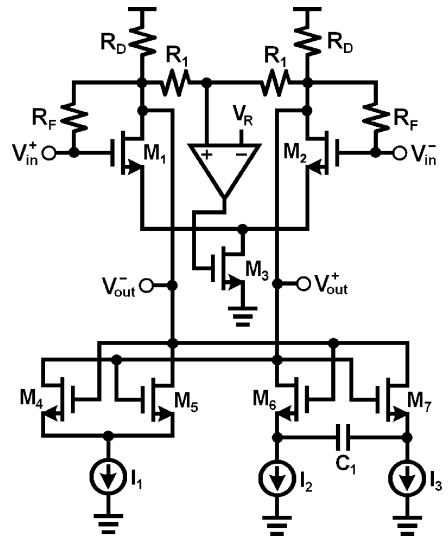

Fig. 6. Schematic of the core differential TIA.

gain. To overcome this problem, the two error amplifiers used for achieving AOC are designed with a built-in offset voltage, $V_{\rm OS}$, of approximately 0.3 V. Thus the available voltage headroom is doubled. Following the core circuit, a wideband gain stage and an output buffer capable of driving 50 Ω loads are included. The capacitors C_1 and C_2 are used to simulate the equivalent capacitances of the ESD protection circuits. In this design $C_1 = C_2 = 0.5$ pF is used. By controlling the switches $\rm S_1$ and $\rm S_2$, the effects of the parasitic capacitances on the receive performance can be evaluated directly.

Fig. 6 shows the circuit diagram of the core differential TIA, $\rm T_1$. A simple single-stage design is used to serve as the main amplifier due to its excellent noise performance and stability. The major drawback is the poor open-loop gain. In general, active loads can be employed instead of resistors to achieve significant gain boosting. However it inevitably results in degraded dynamic range due to the poor linearity of the active loads. In this design, both the built-in offset creation and the NIC are used instead to improve the gain-bandwidth product. The former technique results in doubled voltage headroom and hence the open-loop gain can be increased by using a larger resistance

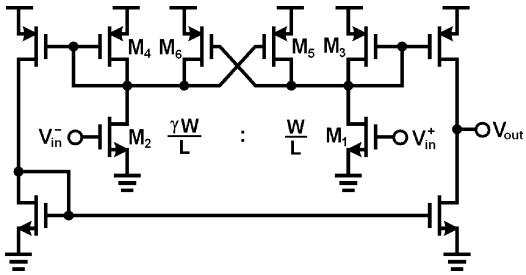

Fig. 7. Schematic of the error amplifier with built-in offset.

for R_D. The negative resistance is generated by $\rm M_4$, $\rm M_5$ and I_1. The negative capacitance is generated by $\rm M_6$, $\rm M_7$ and C_1. Both compensation strengths can be adjusted by I_1 and C_1, separately. Moreover, an additional feedback circuit, consisting of the resistor string using two R_1 resistors, an error amplifier and $\rm M_3$, is included to properly control the output common-mode voltage so as to guarantee a stable operating condition.

To evaluate the effect of the NIC on the overall performance, the tail currents I_1, I_2 and I_3 can be fully turned off if required. The AOC along with the common-mode control loop in $\rm T_1$ keeps the input and output common-mode voltages of $\rm T_1$ constant all the time. When the NIC is turned off, the common-mode control loop increases the bias current of $\rm M_1$ and $\rm M_2$. The increasing $\rm g_{m1}$ increases the loop gain, hence increasing both the transimpedance gain and the bandwidth simultaneously. Basically, the evaluation of the NIC is based on identical power consumption in $\rm T_1$. If $\rm g_{m1}$ remains constant in the evaluation, then a wider performance gap is to be expected.

To simplify the noise analysis for $\rm T_1$, a fully-symmetric circuit is assumed and the input capacitances are neglected. Assuming $g_{m6}/2C_1 \gg p_2$, for $\omega \leq p_2$ the equivalent differential noise current at each output can be approximated as

$$\overline{V_{n,out}^2} = \frac{2R_o^2}{(g_{m1}R_o+1)^2}\left(\overline{I_{n,M1}^2}+\overline{I_{n,M4}^2} + \overline{I_{n,I2}^2}+\overline{I_{n,RD}^2}+g_{m1}^2R_F^2\overline{I_{n,RF}^2}\right) \quad (17)$$

where $R_o = 1/(g_{m1} - g_{m4} + 1/R_D)$. Assuming $g_{m1}R_o \gg 1$, the corresponding input referred noise current in the differential-sensing scheme is derived as

$$\overline{I_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{(2R_F)^2} = \frac{2kT\gamma}{g_{m1}R_F^2}\left[1+\frac{g_{m4}+g_{m,I2}}{g_{m1}}\right] + \frac{2kT}{g_{m1}^2R_F^2R_D}+\frac{2kT}{R_F}. \quad (18)$$

By using the built-in offset creation technique, R_D is almost doubled. As a result, the required $\rm g_{m4}$ becomes smaller and hence the resulting noise degradation is reduced. In general, the SNR of a differential TIA is 3 dB worse than its single-ended counterpart. However, the differential-sensing capability can provide a 6 dB SNR improvement. Therefore, a differential TIA with differential-sensing capability can potentially achieve a 3 dB SNR improvement according to (18).

Fig. 7 shows the circuit diagram of the error amplifier used for the AOC. It is basically a two-stage amplifier employing the negative resistance compensation for gain boosting. The 0.3 V

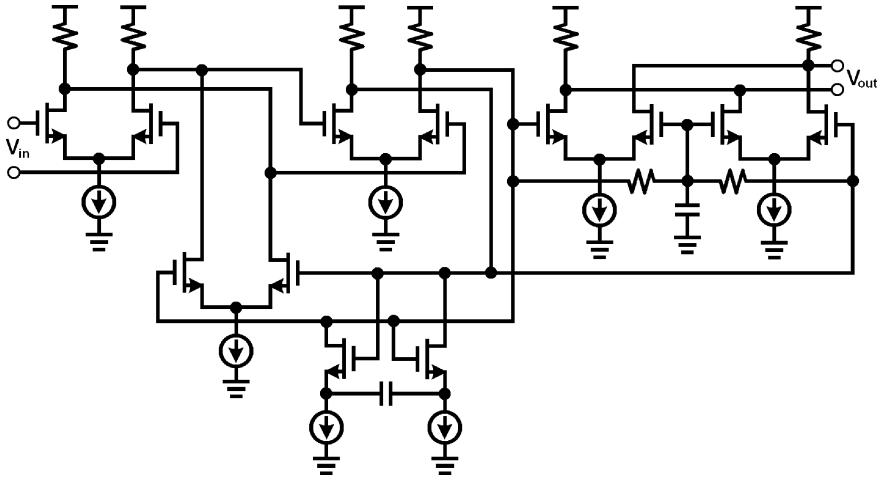

Fig. 8. Schematic of the gain stage and the output buffer.

built-in offset is created by introducing large geometric mismatch between the differential input transistors according to the relation given by

$$V_{\rm OS} = (\sqrt{\gamma} - 1)\,(V_{\rm GS2} - V_t) \tag{19}$$

where γ denotes the width ratio between the input transistors, V_t denotes the threshold voltage for NMOS devices. From (19), apparently the overdrive voltage must be maximized to minimize the undesired variation in $V_{\rm OS}$ due to the variation in V_t, hence the tail current source of the input differential pair is excluded as we can see in Fig. 7. In addition, the negative resistance created by the cross-coupled pair consisting of $\rm M_5$ and $\rm M_6$ is used to improve the voltage gain. The resulting voltage gain is inversely proportional to the difference in transconductance between $\rm M_3$ and $\rm M_5$, hence it can be easy to achieve great enhancement by keeping the $\rm W/L$ ratio of $\rm M_5$ slightly smaller than that of $\rm M_3$. For the error amplifier design used for the output common-mode voltage control in Fig. 6, a matched differential pair with a tail current source is used as the input stage to minimize the offset.

For the design of the gain stage following the core differential TIA, the active feedback technique [15], [16] combined with negative capacitance compensation is used to not only achieve wideband performance but also reduce the large loading capacitance due to the output buffer. On the other hand, a wideband f_t-doubler is used for the output buffer design. Fig. 8 shows the corresponding circuit diagram.

Fig. 9 shows the die micrograph of the TIA IC. The IC occupies a chip area of 560×400 μm^2 and the active area excluding the decoupling capacitors is about 100×100 μm^2. The IC totally consumes 40 mW from a 1.8 V supply. The SC-TIA core only uses 8 mW, including 3 mW for the NIC. The rest of the circuits consume 32 mW.

V. Experimental Results

Due to the special circuit arrangement, electrical test is not appropriate for performance evaluation of the TIA IC. For optical test at wavelength of 1310 nm, the TIA IC is connected to a commercial InGaAs PIN PD in a chip-on-board assembly.

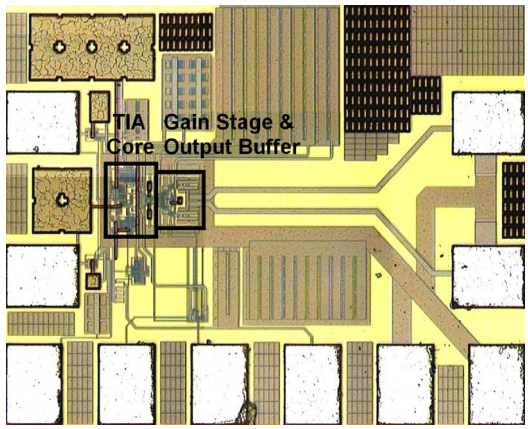

Fig. 9. Die micrograph.

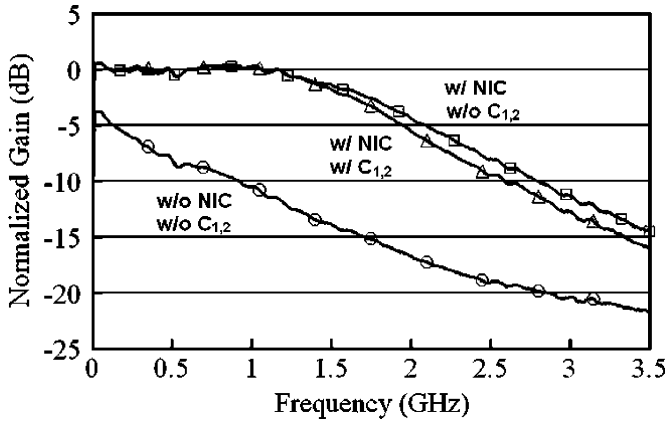

Fig. 10. Measured frequency responses.

The active area of the PD is 70 μm in diameter. The PD responsivity is 0.9 A/W and the corresponding equivalent capacitance is around 0.8 pF at a 1.2 V reverse bias. Fig. 10 shows the measured optical frequency responses. As the NIC is disabled, the measured -3 dB bandwidth is about 350 MHz whether C_1 and C_2 are connected or not. While enabling the NIC, the measured -3 dB bandwidth is slightly degraded from 1.82 GHz to 1.72 GHz as C_1 and C_2 are connected. The NIC is shown to

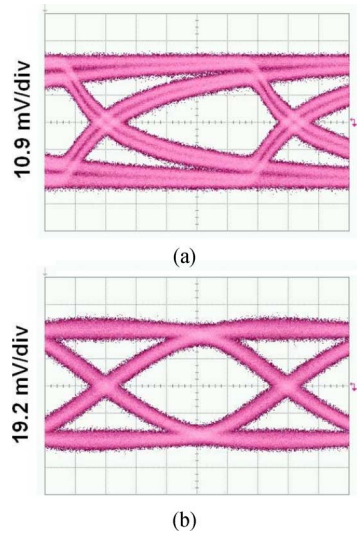

Fig. 11. Measured eye diagrams: (a) without NIC at 1 Gb/s,and (b) with NIC at 3 Gb/s.

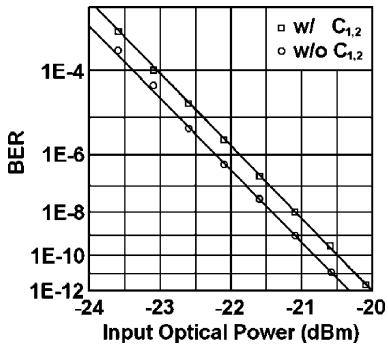

Fig. 12. Measured BER versus input optical power at 3 Gb/s.

achieve enhancement factors of 4.5 dB and 520% respectively for transimpedance gain and bandwidth. For eye diagram measurement, a $2^{31}-1$ pseudo-random bit sequence is used and the extinction ratio of the optical transmitter is 10 dB. Fig. 11 shows the measured eye diagrams at an input optical power of -15 dBm. Without the NIC, the IC cannot properly operate at 1 Gb/s. With the NIC, the IC can support applications at data rate up to 3 Gb/s. The loading effects of C_1 and C_2 on the measured eye diagrams are almost negligible. Apparently the measured time-domain results are in great agreement with the measured frequency responses. For the bit-error rate (BER) measurement, the output signal of the optical receiver is amplified by a commercial 10 Gb/s limiting amplifier before it is sent into the BER tester. Fig. 12 shows the measured BER versus input optical power at 3 Gb/s. At a BER of 10^{-12}, the sensitivity is slightly degraded from -20.3 dBm to -20 dBm as C_1 and C_2 are connected. To evaluate the overload characteristic at 3 Gb/s, the IC is tested at an input optical power of $+0$ dBm and the measured eye diagram is shown in Fig. 13. The observed jitter is 75 $\mathrm{ps_{PP}}$. In summary, the IC has achieved a dynamic range of greater than -20 dBm to $+0$ dBm without incorporating any gain control. The measured differential transimpedance gain is

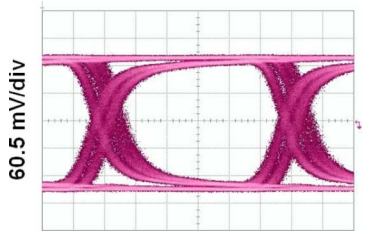

Fig. 13. Measured 3 Gb/s eye diagram at input optical power of $+0$ dBm.

TABLE I
PERFORMANCE COMPARISON

	[4]	[5]	[12]	This Work
Process	0.6μm CMOS	0.35μm CMOS	0.35μm SiGe BiCMOS	0.18μm CMOS
Design	RGC-TIA	RGC-TIA	SC-TIA	SC-TIA+NIC
Supply Voltage	5V	3V	3V	1.8V
PD Capacitance	1pF	0.3pF	0.7pF	0.8pF
Data Rate	1.25Gb/s	2.5Gb/s	2.5Gb/s	3Gb/s
Bandwidth	860MHz (Electrical)	2.2GHz (Electrical)	1.46GHz	1.82GHz
Gain	800Ω	530Ω	15kΩ	3.5kΩ
Sensitivity	$5\mu A_{PP}$ BER=10^{-12} (Electrical)	$16\mu A_{PP}$ BER=10^{-12} (Electrical)	-24.5dBm BER=10^{-12}	-20.3dBm BER=10^{-12}
Overload	N/A	N/A	-3dBm	+0dBm
Dynamic Range	N/A	N/A	21.5dB	20.3dB
Power Consumption	85mW	22.5mW	21mW	40mW

3.5 kΩ without any stability problem. The measured maximum differential output swing is 570 $\mathrm{mV_{PP}}$.

Table I summarizes the performance of our SC-TIA along with previous publications. Apparently, the SC-TIA can achieve high gain, wide dynamic range and low power consumption simultaneously. Combining with the NIC, the SC-TIA is suitable for low-voltage applications.

VI. CONCLUSION

The SC-TIA has been shown to provide improved SNR owing to the differential-sensing capability. The SC-TIA IC is shown to be tolerant of ESD protection circuit with 0.5 pF equivalent capacitance at the differential inputs. The observed sensitivity degradation is 0.3 dB due to the additional 0.5 pF input capacitances. The built-in offset creation technique not only doubles the voltage headroom available for the core TIA but also improves the overload characteristic. By using the NIC, the obtained enhancement factors for transimpedance gain and bandwidth are 4.5 dB and 520%, respectively. Without incorporating any gain control, the IC has achieved a dynamic range of greater than 20 dB.

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