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碩士論文

複晶矽薄膜電晶體之製程與可靠度之研究

Study on the Process and Reliability of Poly-Si Thin-Film Transistors

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摘　　要

在本論文中，首先，我們提出在摻氟矽玻璃(FSG)上製造的複晶矽薄膜電晶體。實驗結果顯示元件的電特性和均勻度可藉由摻雜適量的氟原子達到明顯的改善。與傳統複晶矽薄膜電晶體相較之下，製造在摻氟矽玻璃上的複晶矽薄膜電晶體具有較高的導通電流及場效遷移率，並使得漏電流降低。這是因為氟原子能修補複晶矽與絕緣層介面處及位於通道中複晶矽晶格邊界的缺陷。再者，由於氟與矽原子可形成較強的鍵結，經過熱載子應力(hot carrier stress)測試後，發現摻入氟原子的複晶矽薄膜電晶體具有較好的可靠度。

接著，我們進行有關多重通道(multi-channel)複晶矽薄膜電晶體的研究。藉由增加通道的數目來提高閘極的控制能力，可以改善元件的電特性；包括提高導通電流，降低臨界電壓(threshold voltage)及次臨限擺幅(subthreshold swing)。然而，元件的可靠度卻會因此而變差。我們推測是由於在多重通道的結構中，靠近汲極端的電場強度會增加，而導致更嚴重的碰撞游離(impact ionization)所造成。

最後，我們探討有關複晶矽薄膜電晶體生命週期(lifetime)的問題。發現到最糟的熱載子應力測試條件是在閘極電壓大約等於臨界電壓的情形下，而非傳統上

閘極電壓等於二分之一汲極電壓。此外，亦發現到在高的汲極電壓(drain voltage)應力測試條件下，導通電流隨時間的劣化具有相同的斜率，生命週期的分佈亦呈線性關係，因為在此情形下元件的傷害主要是由碰撞游離(impact ionization)所造成。然而，在低的汲極電壓(drain voltage)測試條件下會有不同的現象發生。這是因為此時必須考慮寄生雙極性接面電晶體效應(parasitic bipolar junction transistor action)。

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ABSTRACT

In this thesis, first, a process-compatible scheme for fabricating poly-Si TFTs on an FSG buffer layer was proposed and demonstrated. Experimental results reveal that remarkably improved device performance and uniformity can be achieved with appropriate fluorine concentration. The poly-Si TFT fabricated on FSG layers has a higher on-current, a lower leakage current, and a higher field-effect mobility compared with the conventional poly-Si TFT. The fluorine atoms can passivate the Si/SiO_2 interface states and grain boundary trap states in the poly-Si. Furthermore, the incorporation of fluorine also increases the reliability of poly-Si TFTs against hot carrier stressing, which is attributed to due to the formation of the rather strong Si-F bonds.

Then, Multi-channel poly-Si TFTs were studied. The device's electrical characteristic such as on-current, threshold voltage, and subthreshold swing were improved with increasing the channel stripes due to the enhancement of gate control capability. However, the device's reliability was deteriorated. We concluded that

electric field strength near the drain side was enlarged in multi-channel structure, causing severer impact ionization.

Finally, we studied the lifetime issue of poly-Si TFTs. It was found that the worst-case of stress conditions is under $V_G \approx V_{th}$, not $V_G = 1/2\ V_D$. Moreover, it is revealed that under high V_D of stress conditions, the I_{on} degradation has the same slope with stress time and the lifetime distribution has a linear relationship due to impact ionization dominating. However, under low V_D, it shows a different phenomenon. We concluded that the parasitic BJT should be considered in these stress conditions.

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Chapter 1

Introduction

1.1 Overview of Poly-Si Thin-Film Transistors

In 1966, the first polycrystalline silicon thin film transistors (Poly-Si TFTs) were fabricated by C. H. Fa *et al.* [1]. So far, numerous research reports have been proposed to study the conduction mechanism, fabrication processes and device structures of the poly-Si TFTs in order to enhance the device performance. However, the research in poly-Si TFTs fabrication with temperature below 600°C was not commenced until 1980s. In the past twenty years, low-temperature polysilicon (LTPS) TFTs have been widely investigated in industrial applications, such as active-matrix liquid-crystal displays (AMLCDs) [2-4], high density static random access memories (SRAMs) [5], electrical erasable programming read only memories (EEPROM) [6][7] and candidate for 3-D ICs' applications [8], etc. Within those applications, the application of active-matrix liquid-crystal displays (AMLCDs) is the major driving force to promote the developments of poly-Si TFT technology.

It is known that hydrogenated amorphous silicon (α-Si:H) TFTs were used for the pixel switching device at the first generation of AMLCDs. The advantages of α-Si:H TFTs are their compatibility with low processing temperature on large-area glass substrates and high off-stated impedance which result in a low leakage current. However, its low electron field effect mobility typically below 1 $cm^2V^{-1}sec^{-1}$ has limited the development for AMLCDs technology. So, poly-Si TFTs have attracted much attention, because the field effect mobility in poly-Si is significantly higher than

that in α-Si, thus higher driving current can be achieved in poly-Si [9]. The higher driving current allows small-dimensioned TFTs to be used as the pixel switching elements, thus promoting the aperture ratio and the panel brightness, and therefore improving the performance of display.

The conduction mechanism and the performance of poly-Si TFTs are strongly related to grain boundaries and intragranular defects. For example, the defects in grain boundary would trap carriers and generate a potential barrier which degrades the on-stated current of poly-Si TFTs. Moreover, the grain boundaries also provide the path of leakage current. In order to obtain desirable electrical characteristics of poly-Si TFTs, several methods have been proposed to improve the device performance by enlarging the grain size of poly-Si films [10] and reducing the trap states in grain boundaries. It has been reported that the α-Si films can be crystallized by several techniques, such as SPC (solid-phase crystallization) [11], ELA (excimer laser annealing) [12][13] and MILC (metal-induced lateral crystallization) [14] to obtain a large grain size of poly-Si to raise the field effect mobility. Additionally, there were other methods such as plasma treatments to passivate the defects in the channel or narrowing the channel width to reduce the trap state density. We will make a discussion in next section.

1.2 Motivation

1.2.1 Passivation of Trap States

The electrical characteristics of poly-Si TFT is mainly influenced by the defects in the grain boundaries and within the grain [15]. Trap states resulted from those defects within the channel lead to poor device performance, such as low field effect mobility, large leakage current [16], bad subthreshold slope and high threshold

voltage. It is necessary to recover the trap states in the poly-Si channel to enhance the device performance. For this purpose, hydrogenation has been suggested to be an effective method [17-19]. The atomic hydrogen can recover interface states between poly-Si and SiO_2 and passivate defects in the grain boundaries to improve the device characteristics. Furthermore, other different treatments have been demonstrated to further enhance the device performance, for instance, H_2/N_2 mixture plasma [20], nitrogen implantation with H_2 plasma [21], pre-oxidation NH_3 annealing with H_2 plasma [22], NH_3 plasma [23], O_2 plasma [24][25], and H_2/O_2 plasma [25]. The atomic nitrogen and oxygen also have passivation effect by themselves and moreover the hydrogen passivation effects are greatly enhanced with their incorporation, leading to the observed great improvement in the device performance. Nevertheless, poly-Si TFTs with hydrogenation treatment have a troublesome problem in the performance degradation for the devices under electrical stress. It have been reported that the reliability of hydrogen-passivated TFTs was considerably poor because weak Si-H bonds or Si-Si bonds might be broken to cause the creation of trap states in the poly-Si channel [26].

In order to passivate the trap states within the poly-Si channel and enhance both the device performance and reliability, recently, fluorination technique has been brought out. This is because the Si-F bonds existed in the poly-Si channel and SiO_2/poly-Si interface are rather strong than Si-H bonds. In many research reports, incorporating fluorine atoms into poly-Si channel by ion implantation technique was widely used [27-30]. However, this method is not suitable for large-area electronics, and a subsequent high temperature process, required to activate implanted fluorine atoms and recover the damage created by implantation, is not compatible with the AMLCD process application. In addition, another method that using fluorine-doped silicon oxide (SiO_xF_y) as a diffusion source of fluorine atoms was revealed by C. H.

Kim *et al* [31][32], but that caused the process more complicated due to an extra etching step.

From all of above, a simple, effective, and process compatible method is needed to be found. Therefore, we proposed a novel scheme for fabricating poly-Si TFTs on an FSG buffer layer. The poly-Si TFTs fabricated on FSG layers have a larger on-current, a lower leakage current, and a higher field-effect mobility compared with the conventional poly-Si TFTs. Furthermore, the incorporation of fluorine also increased the reliability of poly-Si TFTs against hot carrier stress, which is attributed to the formation of Si-F bonds.

1.2.2 Multiple Channel

It has been demonstrated that there are a large number of grain boundary trap states in the poly-Si channel, and then localized potential barriers are produced to affect the transportation of carriers from grain to grain [33-35]. Therefore, it is believed that the existence of grain boundaries within the poly-Si channel region of TFTs has a direct influence on the electrical characteristics of devices [36][37]. Then, many groups have tried to reduce the grain boundary trap states for improving the electrical characteristics of poly-Si TFTs.

It has been proposed that poly-Si TFTs with narrow channel width exhibits better performance such as lower threshold voltage [38] and smaller subthreshold swing [39]. This phenomenon is concluded to be caused by reducing the grain boundary trap states. In addition, the gate electrode layer across the channel may induce side-channels in both sides of the channel region and these side-channels will increase the effective channel width. Especially, when channel width was scaled down, the side-channel effect might be more distinct. On the other hand, it has been revealed

that average carrier concentration in the channel region of the poly-Si gate electrode corner increase due to the electrostatic focusing from the top gate and both side gates of the stripes [40]. It is believed that the gate control capability can be significantly improved due to the narrow channel width. Accordingly, poly-Si TFTs with narrow and multiple channels were proposed to enhance the electrical characteristics [40-43]. However, to date, there is no complete reliability analysis of poly-Si TFTs with multiple channels.

So, we focused on the investigation of the factors mainly affecting the performance of the multiple channel poly-Si TFTs. The side-channel effects and trap state density reduction were studied comprehensively. Moreover, the reliability issue of poly-Si TFTs with multiple channels was also disclosed.

1.2.3 Lifetime

Generally, high voltage stress was used to test the reliability of the device, and to extract its lifetime. Then, we analyzed the degradation mechanism of the device to realize what happened during the stress. It has been reported that the worst-case hot carrier degradation for conventional MOSFETs is under V_G=1/2 V_D [44], and the device's degradation depends on the trap states generation, which are proportional to the I_{sub} [45]. This means that drain-avalanche-hot-carrier (DAHC) injection causes the severest damage on the device's characteristics. Therefore, DAHC-induced substrate current I_{sub} was used to monitor the device degradation and predict the device lifetime.

However, it is known that the worst-case hot carrier degradation for SOI MOSFETs is under $V_G \approx V_{th}$ [46]. After hot-carrier stress, the degradation mechanism of the device was significantly different at both low and high drain bias [47][48].

They concluded that the parasitic bipolar transistors (PBT) might be the dominate factor to enhance the stressed current and also the device degradation rate. So, the lifetime of MOSFETs is unsuitable for SOI MOSFETs.

As we know, poly-Si TFTs is similar to SOI MOSFETs. Both of their body is floating. Moreover, the reliability issues of poly-Si TFTs haven't been well-studied yet, especially in the lifetime prediction. Therefore, in this thesis, we want to investigate the lifetime prediction of poly-Si TFTs, and the degradation mechanism at different drain bias under hot carrier stress.

1.3 Organization of the Thesis

In the following sections, we will show our research efforts.

In Chapter 2, the electrical characteristics and fabrication processes of low temperature poly-Si TFTs on an FSG buffer layer will be proposed. Experimental results reveal that the reliability and uniformity of our devices have remarkable improvements in comparison with conventional TFTs. In addition, we will discuss the degradation phenomenon on electrical characteristics and reliability caused by the incorporation of too many fluorine atoms.

In Chapter 3, the fabrication processes and electrical characteristics of n-channel ploy-Si TFTs with different stripes of channel will be proposed. Experimental results reveal that poly-Si TFTs with multiple channels have better performance than the conventional TFTs. Then, we will make a complete discussion about the reliability issue of poly-Si TFTs with multiple channels.

In Chapter 4, the reliability issue of poly-Si TFTs will be investigated by applying different drain bias. It is found that I_{on} degradation under both high and low drain bias of stress conditions has different phenomenon. Then, we will analyze the

degradation mechanism under hot carrier stress with low drain bias.

At the end of this thesis, we will make a conclusion in Chapter 5.

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Chapter 2

Characteristics of Low Temperature Poly-Si TFTs on FSG Buffer Layer

2.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention owing to the possibility of realizing the integration of driving circuits and pixel switching elements on a single glass substrate, and the potential to accomplish the System-on-Panel (SOP) [1]. High-performance and high-reliability poly-Si TFTs are required to achieve this goal. Excimer laser annealing (ELA) has been utilized in enlarging the grain size of the poly-Si to reduce trap states, leading to an excellent device performance [2][3]. However, the random distribution of grain boundaries in poly-Si films still causes a large leakage current and poor device uniformity. Hydrogenation process has been utilized to terminate the grain boundary trap states [4]. Unfortunately, hydrogenated poly-Si TFTs suffer from an instability issue due to weak Si-H bonds breaking [5]. On the other hand, a low-temperature PECVD-oxide buffer layer is conventionally adopted to block the contaminations from the inexpensive glass or flexible plastic substrate. Nevertheless, the mismatch between the thermal expansion coefficient of the poly-Si and that of the oxide causes considerable mechanical tensile stress at the interface during ELA, leading to the degradation in device performance [6-9]. All these drawbacks limit the applications of poly-Si TFTs.

Recently, fluorine atoms have been proposed to passivate trap states in the

poly-Si [10-15]. This is because that the rather strong Si-F bonds exist in the poly-Si channel and SiO_2/poly-Si interface, and thus reduce the trap-state density in the poly-Si channel region. In addition, the composition of Si-F bonds is more stable than Si-H bonds and Si-O bonds, and improves the device reliability obviously. However, ion implantation is not appropriate for extremely large-sized glass substrate in current productions. High temperature process that was required to activate implanted fluorine atoms and recover the damage created by implantation is not compatible with the AMLCD process application. In addition, another method that deposited fluorine-doped silicon oxide (SiO_xF_y) on the channel as a diffusion source of fluorine atoms was revealed by C. H. Kim *et al*, but that caused the process more complicated due to an extra etching step.

Therefore, a new method must be found to introduce fluorine atoms into poly-Si films. Fluorinated silicate oxide (FSG) has been known easy to integrate using plasma-enhanced chemical vapor deposition (PECVD) systems. The out-diffused fluorine atoms form FSG can terminate trap states and also release the strain bonds at the interface [16]. This work proposes a novel process-compatible fluorination technique using a FSG film as the buffer layer. Poly-Si TFTs fabricated on FSG buffer layers exhibit high device performance, uniformity and reliability.

2.2 Experimental

Figure 2-1 schematically depicts the process flow of the proposed poly-Si TFT. First, 500-nm-thick thermal oxide was grown on the Si wafers by furnace system to substitute for the glass substrate and all the experimental devices in this study were fabricated on thermally-oxidized Si wafers. Then, a 40-nm-thick FSG buffer layer was deposited using a PECVD system at 350°C with SiH_4, CF_4 and N_2O as process gases.

In order to determine the effect of fluorine content in FSG layers, varying CF_4 flow rates of 10, 20, and 40 sccm, with a SiH_4 flow rate of 90 sccm and a N_2O rate of 5 sccm, were used to grow various FSG buffer layers, denoted by FSG1, FSG2 and FSG3, respectively. Table 2-1 lists the conditions of precursors to grow FSG buffer layers. The fluorine contents in FSG1, FSG2 and FSG3 were calculated from the SIMS profiles of the as-deposited FSG layers (as shown in Fig. 2-2) and were about 2%, 4%, and 7%, respectively.

Then, 100-nm-thick amorphous silicon layers were deposited on the FSG buffer layers in a low-pressure chemical vapor deposition (LPCVD) system with silane (SiH_4) gas source at 550°C. The deposition pressure was 100mTorr and the SiH_4 flow rate was 40sccm. Next, a semi-Gaussian-shaped KrF excimer laser with wavelength of 248nm was performed for the phase transformation from amorphous to polycrystalline silicon at the laser energy density of 420mJ/cm^2 with substrate heating of 400°C under the chamber pressure of 10^{-3}Torr. The average grain size of the poly-Si is approximately 300nm.

Individual active regions were then patterned and defined. After a clean process, a 100-nm-thick TEOS oxide was deposited with TEOS and O_2 gas source by PECVD at 350°C for gate insulator. A 200-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD. Then, gate electrode was patterned and the regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15}ions/cm^{-2} and 40keV, respectively. The dopant activation was performed by excimer laser annealing with laser energy density of 220mJ/cm^2, followed by a deposition of 400nm-thick passivation oxide in a PECVD system at 350°C and the definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited by thermal evaporation and patterned for metal pads. For comparison, the control samples were fabricated on a 40-nm-thick conventional PECVD-oxide buffer

layer.

2.3 Method of Device Parameter Extraction

In this thesis, we use Ellipsometer to measure the thickness of poly-Si, amorphous-Si and TEOS oxide films in the fabrication procedure. All the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision Semiconductor Parameter Analyzer.

Many methods have been proposed to extract the characteristic parameters of poly-Si TFTs. In this section, those methods are described.

2.3.1 Determination of Threshold Voltage

Threshold voltage (V_{th}) is an important parameter required for the channel length-width and series resistance measurements. However, V_{th} is not uniquely defined. Various definitions have been proposed and the reason can be found in I_D-V_{GS} curves. One of the most common techniques is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of 50~100mV to ensure operation in the linear region [17]. The drain current is not zero when V_{GS} below threshold voltage and approaches zero asymptotically. Hence the I_{DS} versus V_{GS} curve can be extrapolated to I_D=0, and the V_{th} is determined from the extrapolated intercept of gate voltage (V_{GSi}) by

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \quad \text{---------- (Eq. 2.1)}$$

Equation (2.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain current when threshold voltage measurements are made. The I_{DS}-V_{GS} curve deviates from a straight line at gate voltage below V_{th} due to subthreshold current and above V_{th} due to series resistance

and mobility degradation effects. It is common practice to find the point of maximum slope of the I_{DS}-V_{GS} curve and fit a straight line to extrapolate to I_D=0 by means of finding the point of maximum of transconductance (Gm).

In this thesis, we use a simpler method to determinate the V_{th} called constant drain current method. The voltage at a specified threshold drain current is taken as the V_{th}. This method is adopted in the most studied papers of poly-Si TFTs. It can be given a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the threshold current is specified at (W/L)×10nA for V_{DS}=0.1V and (W/L)×100nA for V_{DS}=5V, where W and L are channel width and channel length, respectively.

2.3.2 Determination of Subthreshold-Swing

Subthreshold swing (S.S.) is a typical parameter to describe the control ability of gate toward channel, which reflects the turn on/off speed of a device. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude.

The S.S. should be independent of drain voltage and gate voltage. However, in reality, the S.S. increases with drain voltage due to channel shortening effect such as charge sharing, avalanche multiplication and punchthrough effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as the serial resistance and interface states.

In this thesis, the S.S. is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.3.3 Determination of Field Effect Mobility

Usually, field effect mobility (μ_{eff}) is determined from the maximum value of transconductance (Gm) at low drain bias. The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, so that the first order of I-V relation in the bulk Si MOSFETs can be applied to poly-Si TFTs. The drain current in linear region ($V_{DS} < V_{GS} - V_{th}$) can be approximated as the following equation:

$$I_{DS} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^{2} \right] \quad \text{---------- (Eq. 2.2)}$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. Thus, the transconductance is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{eff} C_{ox} \left(\frac{W}{L} \right) V_{DS} \quad \text{---------- (Eq. 2.3)}$$

Therefore, the field-effect mobility is

$$\mu_{eff} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)} \Big|_{V_{DS} \to 0} \quad \text{---------- (Eq.2.4)}$$

2.3.4 Determination of ON/OFF Current Ratio

On/off current ratio is one of the most important parameters of poly-Si TFTs since a high-performance device exhibits not only a large on-current but also a small off-current (leakage current). The leakage current mechanism in poly-Si TFTs is not like that in MOSFET. In MOSFET, the channel is composed of single crystalline Si and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel region. However, in poly-Si TFTs, the channel is composed of poly-Si. A large amount of trap state densities in grain structure attribute a lot of defect states in energy band gap to enhance the tunneling effect. Therefore, the leakage current is much larger in poly-Si TFTs than in MOSFET. When

the voltage drops between gate voltage and drain voltage increases, the band gap width decreases and the tunneling effect becomes much more severe. Normally we can find this effect in typical poly-Si TFTs' I_{DS}-V_{GS} characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decreases/increases for n/p-channel TFTs.

There are a lot of ways to specify the on and off-current. In this chapter, take n-channel poly-Si TFTs for examples, the on-current is defined as the drain current when gate voltage at the maximum value and drain voltage is 5V. The off-current is specified as the minimum current when drain voltage equals to 5V.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum \quad Current \quad of \quad I_{DS} - V_{GS} \quad Plot \quad at \quad V_{DS} = 5V}{Minimum \quad Current \quad of \quad I_{DS} - V_{GS} \quad Plot \quad at \quad V_{DS} = 5V} \quad \text{-------- (Eq. 2.5)}$$

2.3.5 Extraction of Grain Boundary Trap State Density

The Trap State Density (N_t), which can be determined by the theory established by Levinson *et al.* [18], which is based on Seto's theory [19].

For poly-Si TFTs, the drain current I_{DS} can be given as following:

$$I_{DS} = \mu_{FE} C_{ox} \left(\frac{W}{L} \right) V_{DS} V_{GS} \exp\left(\frac{-q^3 N_t^{\,2} L_c}{8\varepsilon_{Si} kTC_{ox} V_{GS}} \right) \quad \text{---------- (Eq. 2.6)}$$

Where,

μ_{eff}	field-effect mobility of carriers
q	electron charge
k	Boltzmann's constant
ε_{Si}	dielectric constant of silicon
T	temperature
N_t	trap-state density per unit area
L_c	channel thickness

This expression, first developed by Levinson *et al.*, is a standard MOSFET's equation with an activated mobility, which depends on the grain-boundary barrier

height. Levinson *et al.* assumed that the channel thickness was constant and equal to the thickness of the poly-Si film (t). This simplifying assumption is permissible only for very thin film (t<10nm). The trap-state density can be obtained by extracting a straight line on the plot of $ln(I_{DS}/V_{GS})$ versus $1/V_{GS}$ at low drain voltage and high gate voltage.

Proano *et al.* [20] thought that a barrier approximation is to calculate the gate induced carrier channel thickness by solving Poisson's equation for an undoped material and to define the channel thickness (L_c) as a thickness in which 80% of the total charges were induced by the gate. Doing so, one obtains

$$L_c = \frac{8kTt_{ox}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}}}}{q(V_{GS}-V_{fb})} \quad \text{---------- (Eq. 2.7)}$$

which varies inversely with $(V_{GS}-V_{fb})$. This predicts, by substituting Eq.2.7 into Eq.2.6, that $ln[I_{DS}/(V_{GS}-V_{fb})]$ versus $1/(V_{GS}-V_{fb})^2$. We use the gate voltage at which minimum leakage current occurs as flat-band voltage (V_{fb}). Effective trap-state density (N_t) can be determined from the square root of the slope.

2.4 Results and Discussion

2.4.1 Characteristics of Poly-Si TFTs on FSG layer

Figure 2-3 shows the transfer characteristics (I_{DS}-V_{GS}) of the conventional and the proposed poly-Si TFTs with different FSG buffer layers. The measurements was performed at drain voltage of V_{DS}=5V. The measured and extracted parameters from the devices are listed in Table 2-2. The threshold voltage, subthreshold swing, on-current (V_{GS}=25V), and off-current (V_{GS}=-10V) were measured at V_{DS}=5V.

In the Fig. 2-3, we can see that the poly-Si TFTs fabricated on the FSG buffer

layers exhibit better on-state and off-state characteristics than those of the control sample. Notably, under a large negative gate bias, the leakage currents of the TFTs on FSG layers (3.08×10^{-9}A, 3.32×10^{-10}A, and 9.95×10^{-10}A for FSG1, FSG2, and FSG3, respectively) are over one order of magnitude lower than that on the conventional oxide buffer layer (1.14×10^{-7}A). This is attributed to the facts that the reduced the traps by the incorporation of fluorine in the poly-Si films during ELA [13] and the released tensile stress at the poly-Si/buffer-oxide-layer interface [16]. Moreover, the threshold voltage and subthreshold swing of the poly-Si TFTs on FSG layers (4.77V & 1.422V/dec., 4.82V & 1.44V/dec., and 4.95V & 1.45V/dec. for FSG1, FSG2, and FSG3, respectively) were found to be superior to those of the control sample (5.07V & 1.55V/dec.).

It has been revealed that the threshold voltage and subthreshold swing are more sensitive to the density of deep trap states near midgap associated with the dangling bonds [4]. For this reason, it is inferred that the dangling bonds within the poly-Si channel and SiO_2/poly-Si interface were effectively passivated by fluorine atoms. Figure 2-4 shows the field-effect mobility of the conventional and the proposed poly-Si TFTs. They were found to be 63.9cm^2/V.s, 69.1cm^2/V.s, 65.4cm^2/V.s, and 43cm^2/V.s for control, FSG1, FSG2, and FSG3, respectively. As can be seen, except FSG3, the field-effect mobility was improved by the incorporation of fluorine atoms within the poly-Si channel. It was demonstrated that the field-effect mobility is significantly influenced by the tail states near the band edge caused by the strain bonds in poly-Si and SiO_2/Si interface [4]. Therefore, we believe that fluorine atoms introduced into poly-Si channel can not only passivate the dangling bonds, but also release the strain bonds within the poly-Si channel and SiO_2/poly-Si interface. However, for the degradation phenomenon in FSG3, we will explain later.

The evidence of the fluorine incorporation can be firmly demonstrated with the

SIMS profiles of fluorine, as shown in Fig. 2-5. It was clearly observed that considerable fluorine atoms were introduced and confined in the poly-Si for the FSG samples and, in particular, two fluorine peaks were located at the top and bottom interfaces. Therefore, we believe that the grain boundary trap states, both the top and bottom interface states were terminated by fluorine atoms. Moreover, in order to verify the effect of fluorine passivation, the effective trap state density (N_t) was calculated. Figure 2-6 shows the plot of $ln(I_{DS}/V_{GS})$ versus $1/V_{GS}$ at low drain voltage and high gate voltage for all samples. The effective trap state density caculated form the slopes for the control, FSG1, FSG2, FSG3 were $5.64\times10^{12}cm^{-2}$, $3.91\times10^{12}cm^{-2}$, $3.97\times10^{12}cm^{-2}$, and $4.01\times10^{12}cm^{-2}$, respectively. These figures strongly hint that the fluorine can effectively passivate the present trap states in poly-Si channel region.

However, the FSG3 shows a detrimental effect on the performance of the resulting TFT. This is attributed to the moisture absorption. According to previous report, the moisture absorption increased with increasing fluorine content in the FSG layers [21]. The absorbed moisture would easily form OH or react with fluorine to form HF, which in turn deteriorate the devices and result in the degraded performance and reliability [22].

2.4.2 Uniformity and Reliability of Poly-Si TFTs on FSG layer

Figure 2-7 displays the statistical distributions of the field-effect mobility (μ_{eff}), the leakage current (I_{off}), and the threshold voltage (V_{th}) of the conventional and the proposed poly-Si TFTs with different FSG buffer layer deposition conditions. The vertical bars in the figure indicate the minimum and maximum values of the devices characteristics and the squares present the average values. The average values of the μ_{eff} for the control, FSG1, FSG2 and FSG3 samples were $57.7cm^2/V.s$, $66.7cm^2/V.s$,

63.9cm^2/V.s, and 45.2cm^2/V.s with standard deviations of 4.05, 2.98, 3.09 and 4.15, respectively. This tendency indicates that with moderate fluorine content in FSG layers the average values and the deviations of μ_{eff} can be greatly improved. Also, the average values of the I_{off} for the control, FSG1, FSG2, and FSG3 samples were 6.8×10^{-8}A, 7.8×10^{-9}A, 1.3×10^{-9}A, and 1.8×10^{-9}A with standard deviations of 8.14×10^{-8}, 2.46×10^{-9}, 6.55×10^{-10} and 1.93×10^{-9}, respectively. The average of the V_{th} for the control, FSG1, FSG2, and FSG3 samples were 5.50V, 5.2V, 4.89V, and 4.88V with standard deviations of 0.21, 0.037, 0.22 and 0.13, respectively. These results imply that fabricating poly-Si TFTs on FSG buffer layers with moderate fluorine concentration can improve the device performance as well as the uniformity of its characteristics. The uniformity of the poly-Si TFTs is strongly affected by the random distribution of grain boundaries. Therefore, using fluorine to terminate those trap states within poly-Si channel can effectively alleviate the influence of grain boundaries.

Then, we would discuss the reliability issue of the conventional and the proposed poly-Si TFTs with different FSG buffer layer deposition conditions. The hot-carrier stress was performed at $V_{D,stress}$=20V, $V_{G,stress}$=10V, and source electrode grounded for 1000sec to investigate the device reliability. Figure 2-8 plots the variations of on-state current (I_{on}), threshold voltage (V_{th}), and field-effect mobility (μ_{eff}) over stress time. The variations of I_{on}, V_{th}, and μ_{eff} were defined as $(I_{on,stressed}-I_{on,initial})/I_{on,initial}\times100\%$, $(V_{th,stressed}-V_{th,initial})/V_{th,initial}\times100\%$, and $(\mu_{eff,stressed}-\mu_{eff,initial})/\mu_{eff,initial}\times100\%$, respectively, where $I_{on,stressed}$, $V_{th,stressed}$, $\mu_{eff,stressed}$, $I_{on,initial}$, $V_{th,initial}$, and $\mu_{eff,initial}$ represent the measured values before and after electrical stress.

Notably, the control shows relatively large variations in I_{on}, V_{th}, and μ_{eff} after 1000sec stress, whereas the FSG2 has slight change in I_{on} and V_{th} and stays almost unchanged in μ_{eff}. These results imply that poly-Si TFTs fabricated on the FSG layer

greatly reduced the device degradation under hot carrier stress, which is due to the formation of the rather strong Si-F bonds. Since the calculated percentages of fluorine content in the FSG layers are 2%, 4% and 7% for FSG1, FSG2, and FSG3, respectively, we deduce based on the above experimental results that the trap states can be effectively passivated when the fluorine content in the FSG is above 2%; while the absorbed moisture in the FSG as the content of fluorine is above 4% starts to induce visible corrosion of the poly-Si structures after competing with the trap states termination. Definitely, the corrosion becomes more severe as the content of fluorine reached 7%. As a result, the optimized condition of fluorine content of FSG is probably within 2% to 4%.

2.5 Summary

A process-compatible scheme for fabricating poly-Si TFTs on an FSG buffer layer is proposed. Significant improvements in the device performance and uniformity were successfully demonstrated with fluorine incorporation in the poly-Si layer. This is attributed to the reduction of the trap state density in poly-Si and SiO_2 interface. Additionally, the incorporation of fluorine atoms also promotes the hot-carrier immunity due to the formation of the strong Si-F bonds. Fabricating poly-Si TFTs on FSG buffer layers with appropriate fluorine content improves not only the electrical performance and uniformity but also the reliability.

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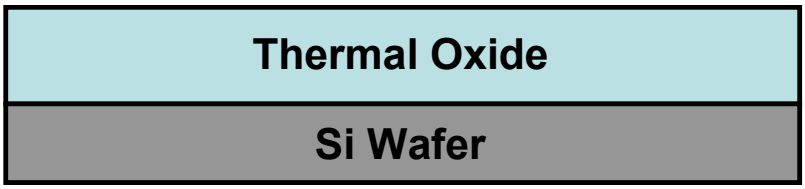
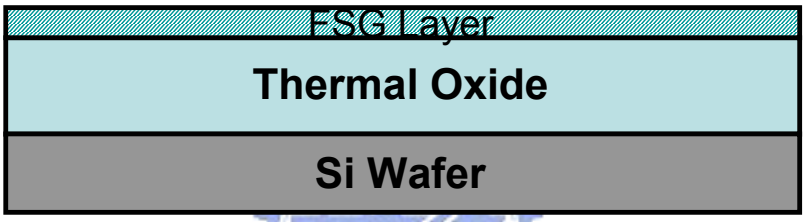
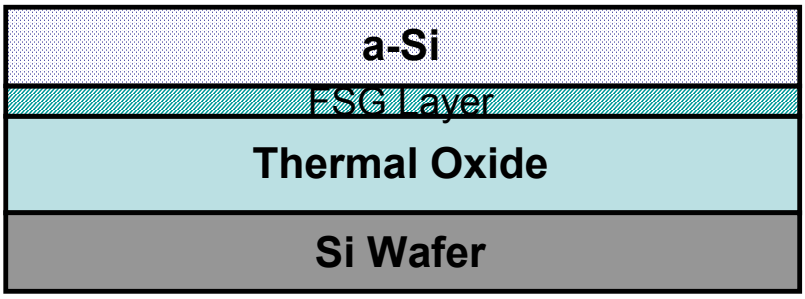


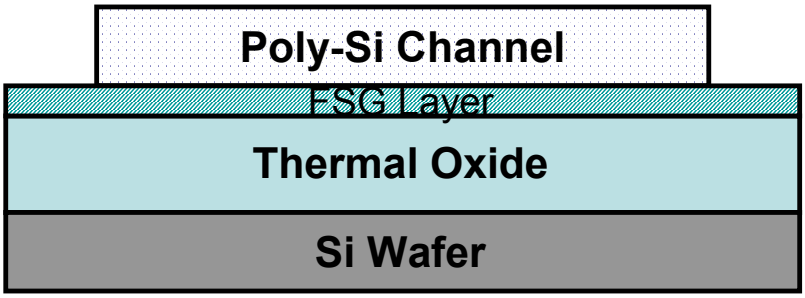
(a) Thermal oxidation grown by furnace.



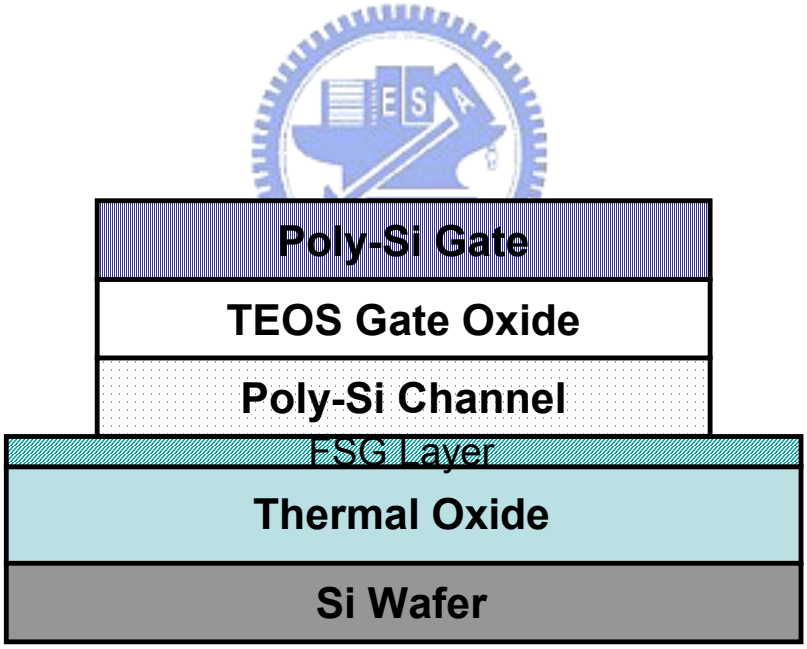
(b) FSG layer deposited by PECVD.



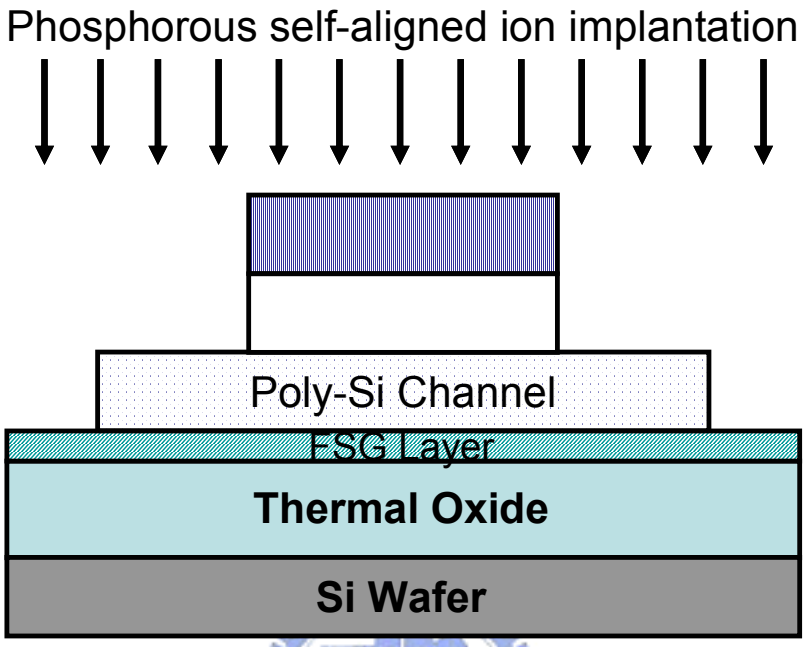
(c) Amorphous Si (a-Si) deposited by LPCVD.



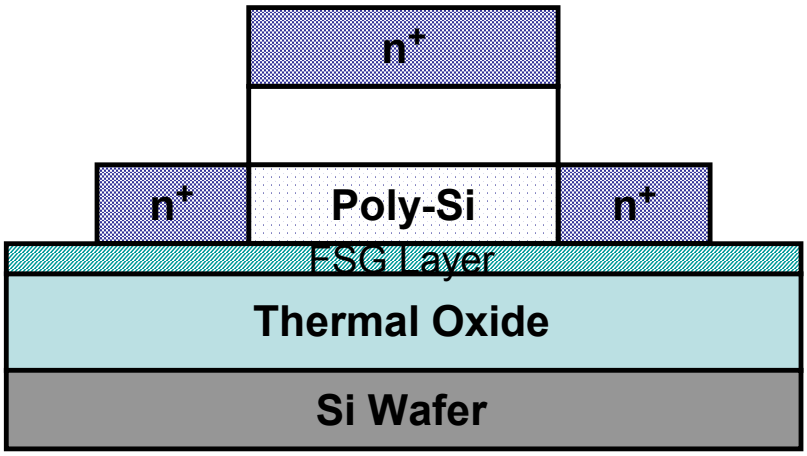
(d) Recrystallization of a-Si film into poly-Si channel by ELA, active region defined.



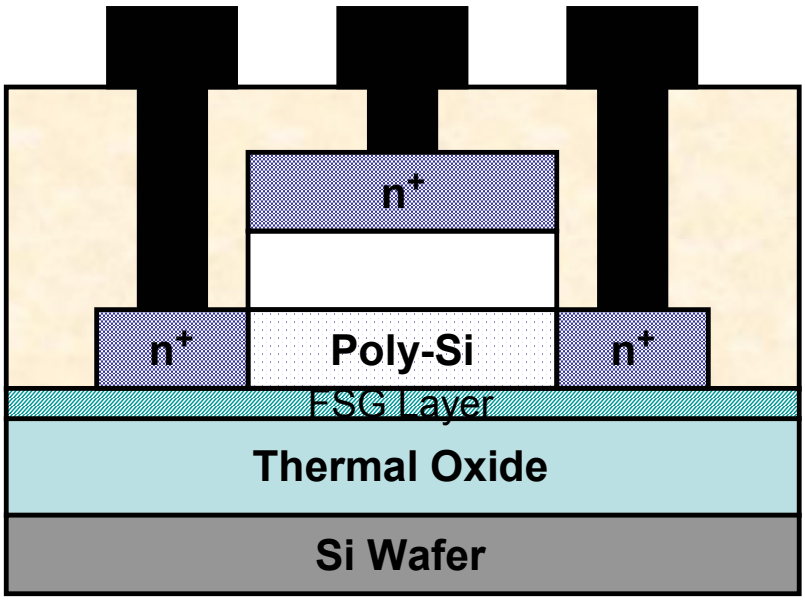
(e) Deposition of TEOS gate oxide by PECVD and poly-Si gate by LPCVD.



(f) The gate electrode defined and self-align phosphorous ion implantation.



(g) Dopant activation by excimer laser annealing.



(h) Deposition of passivation oxide, contact holes opened and metal pads formation.

Fig. 2-1 Process flow of the proposed poly-Si TFTs on a FSG buffer layer.

Table 2-1 Summary of different deposition conditions of FSG buffer layer.

Gas / Sample	CF_4	N_2O	SiH_4
Control	0	90	5
FSG1	10	90	5
FSG2	20	90	5
FSG3	40	90	5

Unit：sccm

Table 2-2 Summary of device parameters of the conventional and the proposed poly-Si TFTs (W/L = 40 μm/10 μm) with different FSG layer deposition conditions.

	Control	FSG1	FSG2	FSG3
V_{th}(V)	5.07	4.77	4.82	4.96
S.S(V/dec.)	1.55	1.422	1.44	1.45
μ_{eff} (cm^2/V.s)	63.9	69.1	65.4	43
I_{on} @ V_G = 25V(A)	4.33×10^{-4}	7.01×10^{-4}	6.39×10^{-4}	5.11×10^{-4}
I_{off} @ V_G = -10V(A)	1.14×10^{-7}	3.08×10^{-9}	3.32×10^{-10}	9.95×10^{-10}
ON/OFF Ratio	3.80×10^{3}	2.28×10^{5}	1.92×10^{6}	5.14×10^{5}
N_t(cm^{-2})	5.64×10^{12}	3.91×10^{12}	3.97×10^{12}	4.01×10^{12}

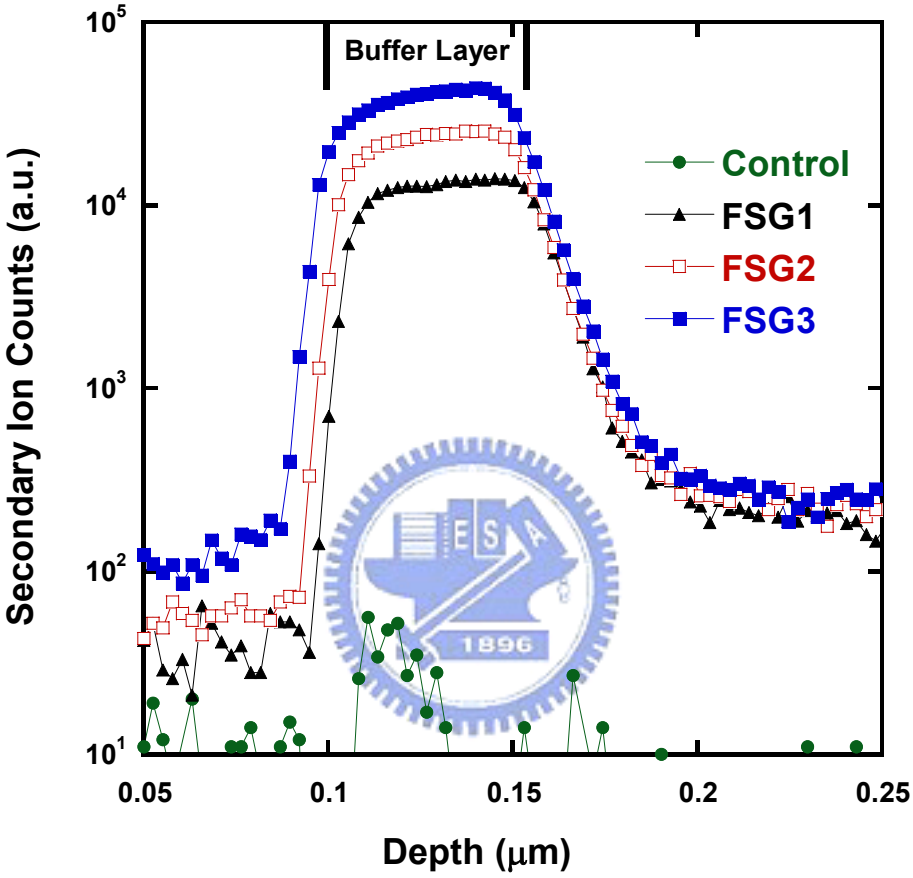


Fig. 2-2 SIMS profiles of the FSG layer as-deposited samples with different FSG layer deposition conditions.

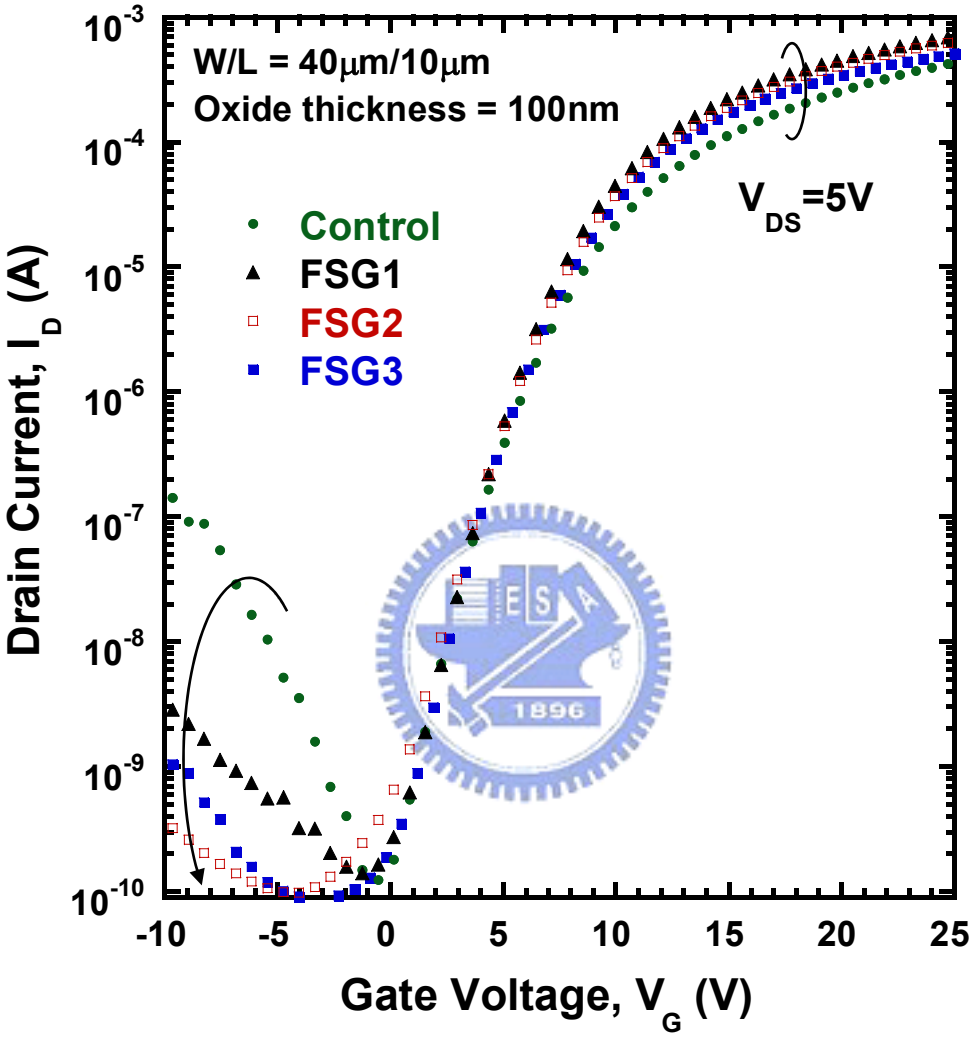


Fig. 2-3 Transfer characteristics of the conventional and the proposed poly-Si TFTs with different FSG layer deposition conditions.

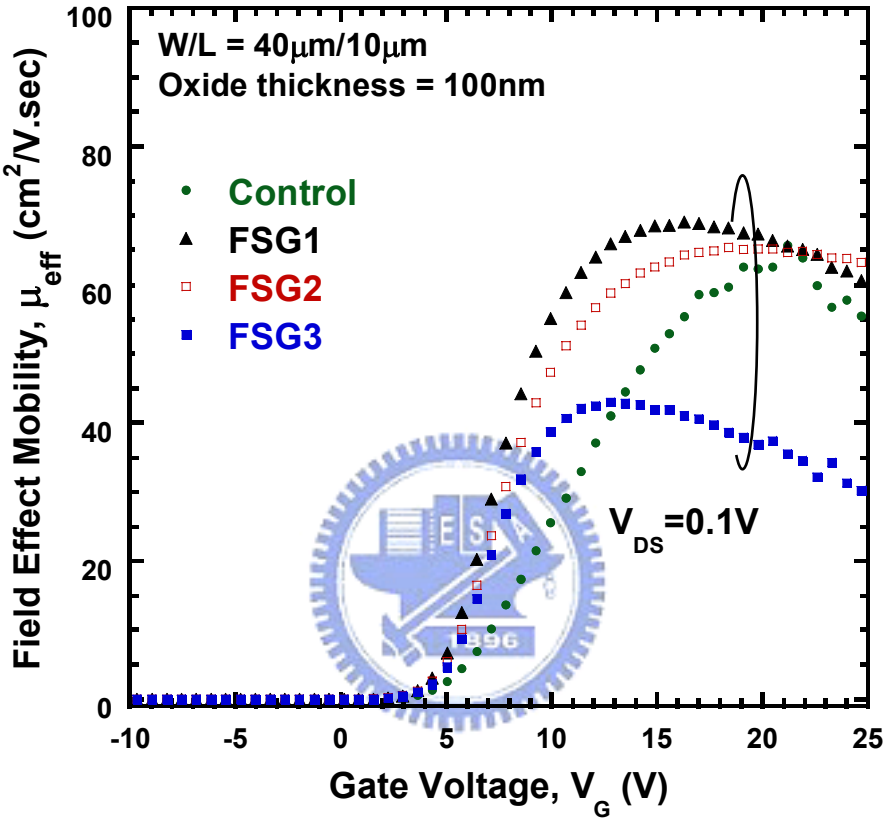


Fig. 2-4 Field effect mobility of the conventional and the proposed poly-Si TFTs with different FSG layer deposition conditions.

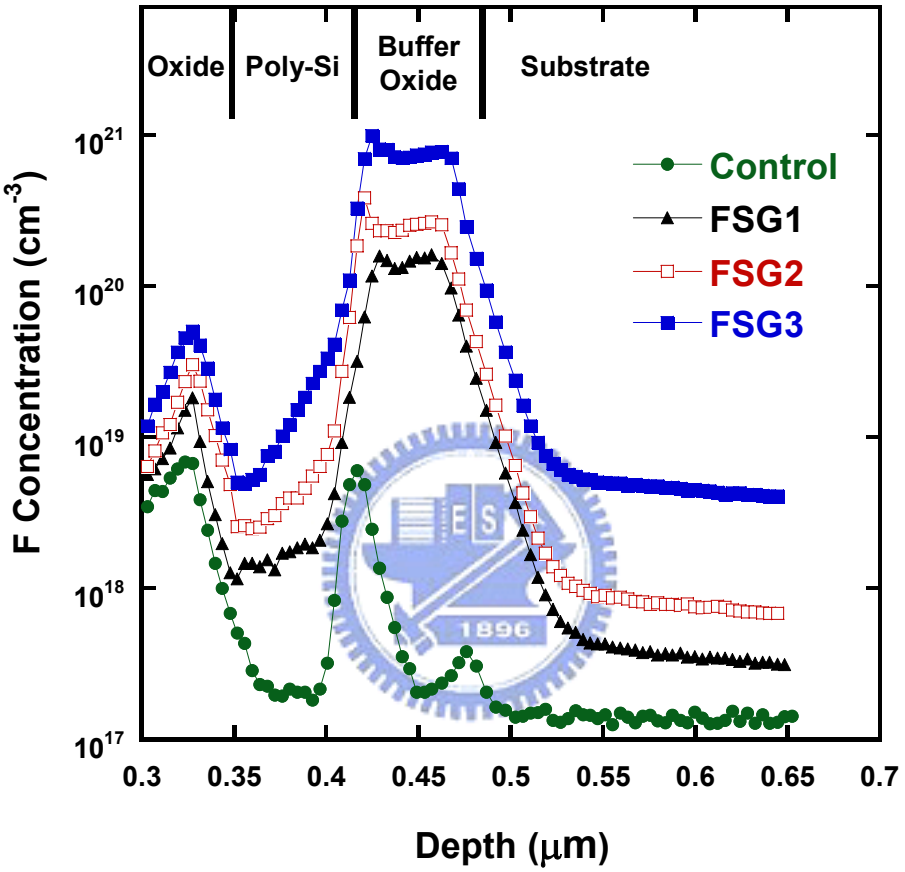


Fig. 2-5 SIMS profiles of the conventional and the proposed poly-Si TFTs with different FSG layer deposition conditions.

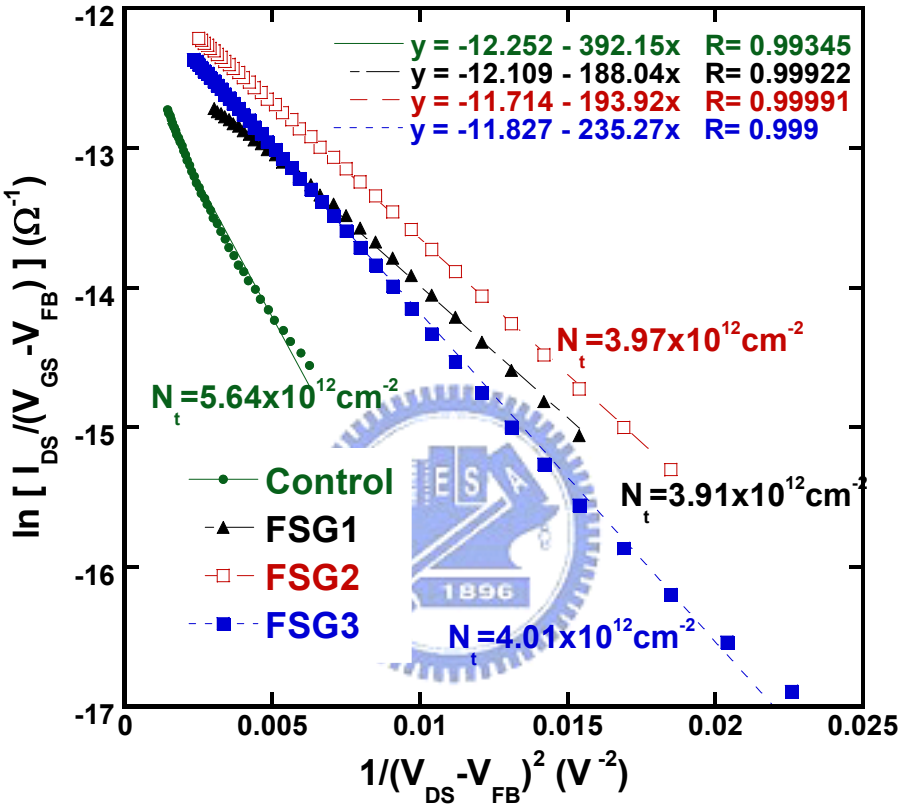
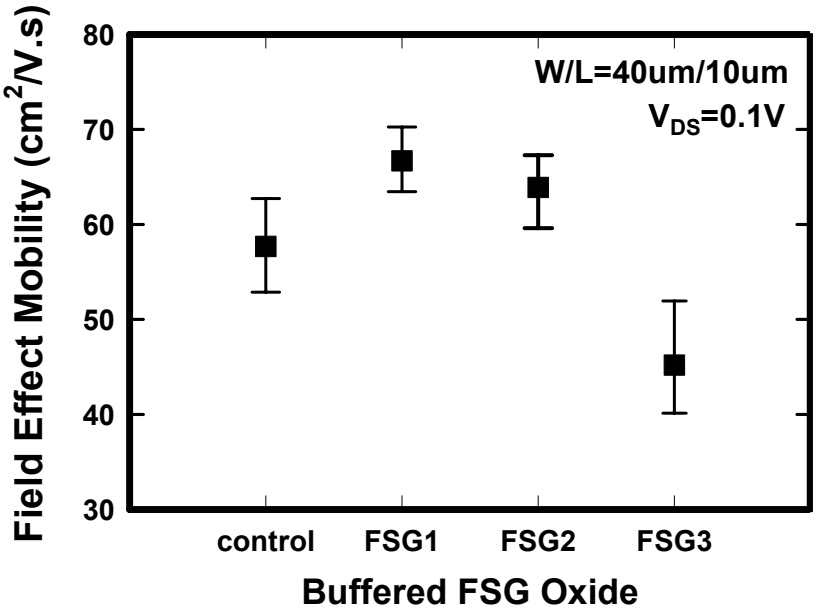
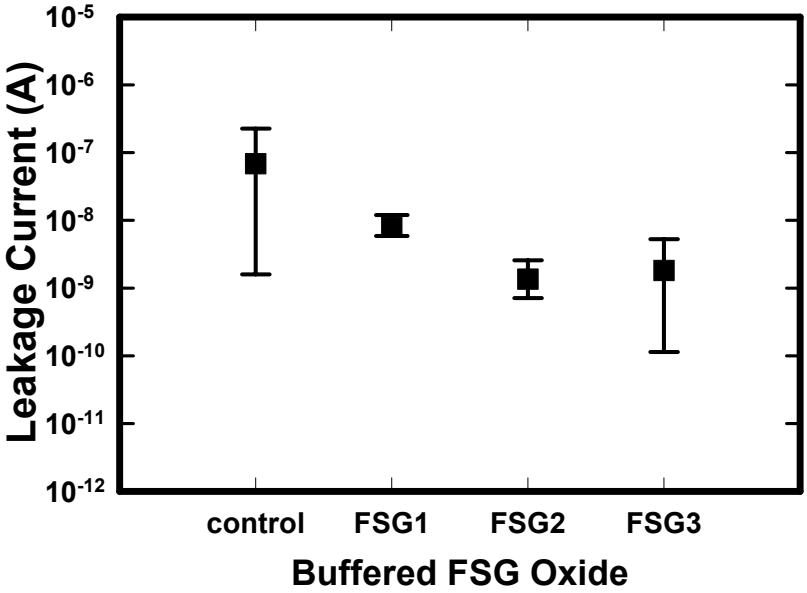


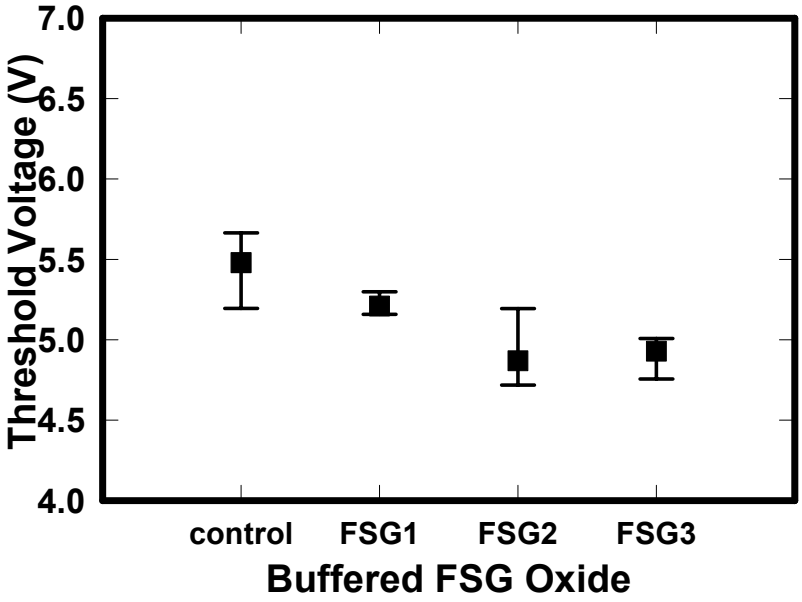
Fig. 2-6 Trap state density extraction of the conventional and the proposed poly-Si TFTs with different FSG layer deposition conditions.



(a) Field effect mobility distribution

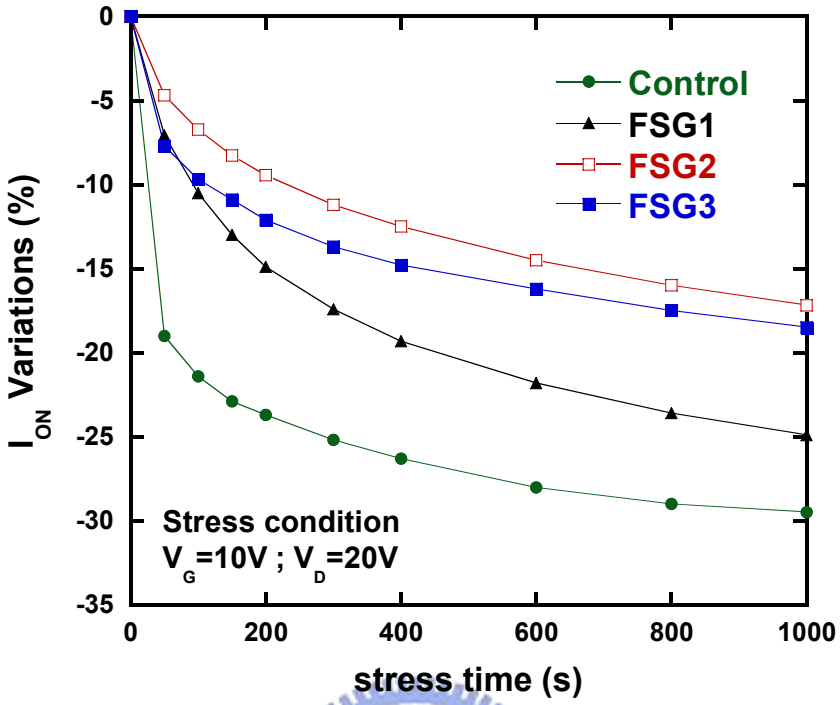


(b) Leakage current distribution

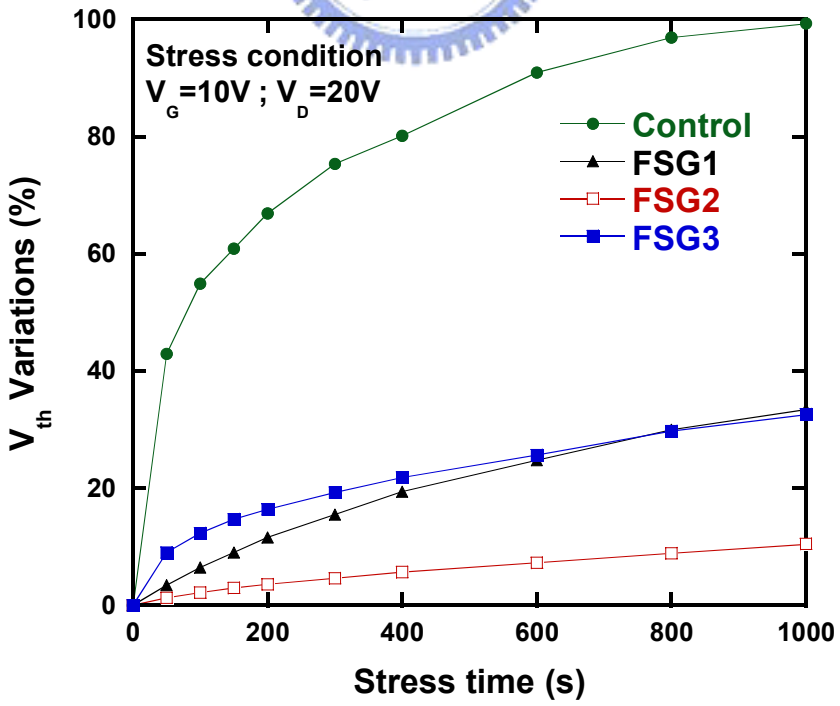


(c) Threshold voltage distribution

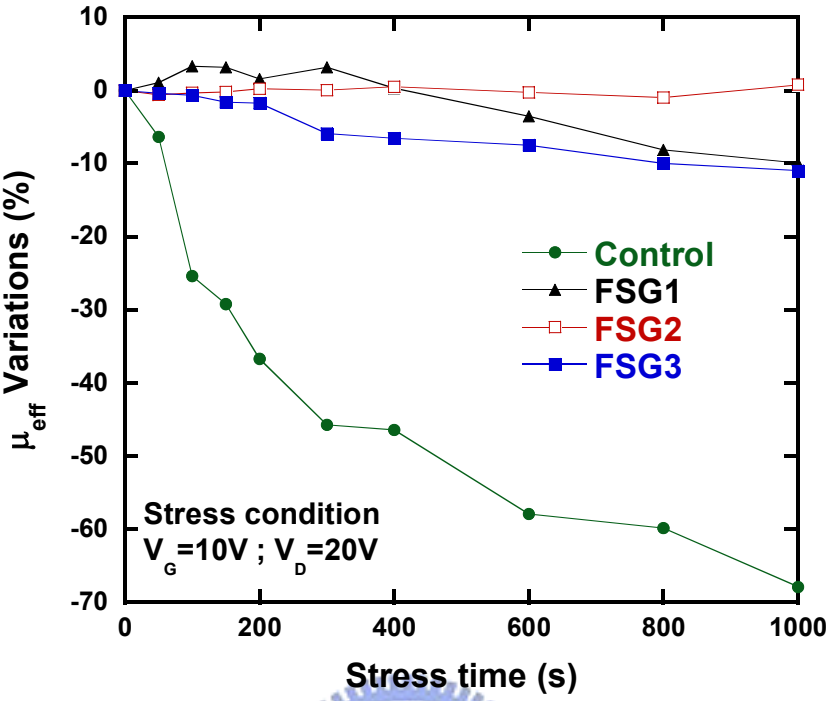
Fig. 2-7 Distribution of (a) filed-effect mobility and (b) leakage current of the poly-Si TFTs on different buffer layers. The vertical bars indicate the minimum and maximum values of the devices characteristics and the squares are the average values.



(a) On-current degradation with stress time



(b) Threshold voltage degradation with stress time



(c) Field effect mobility degradation with stress time

Fig. 2-8 (a) on-current, (b) threshold voltage, and (c) field effect mobility degradation as a function of stress time under hot-carrier stress.

Chapter 3

Electrical Characteristics and Reliability of Multi-channel Poly-Si TFTs

3.1 Introduction

It is known that the existence of grain boundaries within the poly-Si channel region has great influence on the electrical characteristics of poly-Si TFTs [1][2]. In some previous research reports, it has been demonstrated that there are a large number of grain boundary trap states in the poly-Si channel, and localized potential barriers are produced for the transportation of carriers from grain to grain [3-5].

Many suggestions have been proposed and revealed that poly-Si TFTs with narrow channel width have better performance such as lower threshold voltage [6], smaller subthreshold swing [7], and effective kink effect suppression [8][9] due to the reduction of grain boundary trap states. It has been concluded that the grain boundary trap states existed in the channel near the pattern edge is much lower than elsewhere [6]. As the channel width is scaled down, the effect of the poly-Si pattern edge become dominant. Additionally, it has also been reported that kink effect can be enhanced with the existence of grain boundary trap states [8][9]. The larger grain boundary trap state causes the severer impact ionization, and results in pronounced kink effect.

Moreover, the gate electrode across the channel may induce side-channels in both sides of the channel region and these side-channels will increase the effective channel width. Especially, when channel width scaled down, the side-channel effect

might be more distinct. The average carrier concentration in the channel region of the poly-Si gate electrode corner is increased by the electrostatic focusing from the top gate and both side gates of the stripes [10]. It is believed that the gate control capability was improved obviously in narrow width devices. Accordingly, poly-Si TFTs with narrow and multiple channels have been proposed to enhance the electrical characteristics [10-13]. However, there is no complete reliability analysis in the poly-Si TFTs with narrow and multiple channels.

In this chapter, we demonstrate that the fabrication process and electrical characteristics of n-channel ploy-Si TFTs with different narrow channel stripes. We can see that poly-Si TFTs with multiple channels have better performance than that of the conventional TFTs. Finally, we make a complete discussion about the reliability issue of poly-Si TFTs with multiple channels.

3.2 Experimental

Figure 3-1 shows the process flow of the proposed poly-Si TFTs. First, 500-nm-thick thermal oxide was grown on the Si wafer by using a furnace system. All the experimental devices in this study were fabricated on thermally oxidized Si wafers. Then, 100-nm-thick amorphous silicon layers were deposited on the thermal oxide layer using a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Then, amorphous silicon films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24 hours in an N_2 ambient to form poly-Si films. Poly-Si films were patterned into active regions by transformer couple plasma (TCP) etching system using mixture gases of Cl_2 and HBr.

After RCA cleaning procedure, a 100-nm-thick TEOS oxide was deposited by LPCVD with TEOS and O_2 gases at 695°C to form the gate insulator. A 200-nm-thick

poly-Si was deposited to serve as the gate electrode by LPCVD at 595°C. Then, the poly-Si film was patterned and etched by TCP etching system to form the gate electrode and the gate oxide on source/drain was removed using dilute HF solution. The regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15}ions/cm^{-2} and 40keV, respectively. The dopant activation was performed by rapid thermal annealing (RTA) system at 700°C for 20sec, followed by a deposition of 400nm-thick passivation oxide using PECVD system at 350°C and the definition of contact holes. Finally, a 500-nm-thick Al was deposited by sputter and patterned for metal pads, and devices were passivated by NH_3 plasma treatment for 2 hours at 300°C.

Figure 3-2 presents the cross-section of the conventional and multi-channel poly-Si TFTs, which is parallel to the direction of the source and drain electrode. Figure 3-3 depicts the cross-section perpendicular to the direction of the source and drain electrode. In next section, we will discuss the transfer characteristics of the conventional and proposed TFTs with single, 8, 20, and 40 stripes of the same total channel width, as shown in Fig. 3-4. The detailed data of these structures were summarized in Table 3-1. Moreover, we will also discuss the reliability issue of the conventional and proposed TFTs with different stripes of channel.

3.3 Results and Discussion

3.3.1 Characteristics of Poly-Si TFTs with Multiple Channels

Figure 3-5 shows the transfer characteristics (I_{DS}-V_{GS}) for the conventional and proposed TFTs with different stripes of channel. Table 3-2 summarizes the measured and extracted parameters from the devices. The threshold voltage, subthreshold swing, on-state current (V_{GS}=20V) and the off-state current (V_{GS}=-5V) were measured at

V_{DS}=1V. As can be seen, the electrical characteristics of the poly-Si TFTs with multiple channels are significantly improved. The threshold voltage and subthreshold swing decreased with the stripes of channel.

It has been reported that the grain boundary trap state density in the channel regions near the pattern edge is much lower than elsewhere in the poly-Si channel [6][7]. In order to verify if the trap state density reduced or not, the effective trap state density (N_t) was calculated. Figure 3-7 shows the effective trap state density of the poly-Si TFTs with various stripes of channel. The effective trap state density for S1, M8, M20, and M40 are $5.80\times10^{12}cm^{-2}$, $5.71\times10^{12}cm^{-2}$, $5.40\times10^{12}cm^{-2}$, and $5.06\times10^{12}cm^{-2}$, respectively. Actually, the N_t is calculated from transfer characteristics. Therefore, we deduce that the improved N_t, threshold voltage, and subthreshold swing were owing to the improvement in the gate control capability in the TFT with various stripes. This is because the better gate control capability causes the lower potential barrier locating at the grain boundary.

Moreover, as in Fig. 3-5 and Fig. 3-6, the on-state current and field effect mobility are also improved as the stripes of poly-Si channel increase. Generally, the increase of effective channel width due to additional sidewall may result in the enhancement of on-stated current. However, from Fig. 3-8, we can see that the increase ratios of the on-state current for M8, M20, and M40 are 7.45%, 24.9%, and 36.3%, respectively, and they are much larger than the increase ratio of the effective channel width. Therefore, it can be concluded that the channel sidewall effect was not the dominant factor to improve the electrical characteristics of multiple channel poly-Si TFTs. The improvements on the on-stated current and field effect mobility were contributed to the increasing average carrier concentration due to the enhancement of gate control capability [10], because the electrostatic focusing from the top gate and both side gates of the stripes caused the average carrier concentration

in the channel region of the poly-Si gate electrode corner to increase.

Figure 3-9 shows the output characteristics of the conventional and proposed poly-Si TFTs with different stripes of channel under $V_G - V_{th}$=0.5; 2; 3.5V. It can be seen that the kink effect was suppressed with the increase of the stripes of poly-Si channels. The better gate control ability, the larger depletion region existed in the channel, and therefore the fewer holes accumulated within the channel region. So, it can be concluded that the kink effect suppression was attributed to the improvement of gate control capability.

Figure 3-10 presents the on-state current, field effect mobility, and threshold voltage as a function of different gate length with the number of channel stripes. We can see that the threshold voltage, field effect mobility, and on-state current were improved with increasing the number of channel stripes. This result can be found in every channel length. However, it can also be seen that the field effect mobility decreased with the increase of channel length. We attribute this phenomenon to the increase of series resistance.

3.3.2 Reliability of Poly-Si TFTs with Multiple Channels

Finally, the reliability issue of the conventional and the proposed poly-Si TFTs with single, 2, 4, 10, and 20 stripes of the same total channel width were discussed. The hot-carrier stress test was performed at $V_{D,stress}$=15V, $V_{G,stress}$=10V, and source electrode grounded for 200sec to investigate the device reliability. Figure 3-11 shows the variations of the on-state current (I_{on}) and threshold voltage (V_{th}) over hot carrier stress time. The variations of I_{on} and V_{th}, were defined as $(I_{on,stressed} - I_{on,initial})/I_{on,initial} \times 100\%$ and $(V_{th,stressed} - V_{th,initial})/V_{th,initial} \times 100\%$, respectively, where $I_{on,stressed}$, $V_{th,stressed}$, $I_{on,initial}$, and $V_{th,initial}$, represent the measured values before and after

electrical stress. Generally, less grain boundary trap state density will cause slighter impact ionization under hot carrier stress, and hence the reliability of device will be improved. However, in Fig. 3-11, we can see that the degradation rate of the on-state current and threshold voltage deteriorated with the increase of the stripes of poly-Si channel. Therefore, we will make a discussion about this phenomenon.

Figure 3-12 presents the trap state density in the poly-Si channel before and after 4sec, 10sec, and 100sec hot carrier stress with the stress conditions of V_{DS}=15V, V_{GS}=10V and source electrode grounded. Figure 3-13 shows the increasing ratio of trap state density within the channel after 4sec, 10sec, and 100sec electrical stress. It was significantly demonstrated that the trap state density after hot carrier stress increased with poly-Si channel stripes increasing. To explain this phenomenon, we used MEDICI to simulate the electric field distribution in the channel region of device with dual-gate and single-gate, as shown in Fig. 3-15 and Fig. 3-16, respectively. Figure 3-14 shows the schematic plot of dual-gate and single-gate structures for simulations. To simplify the simulation, in this model, we only considered the influence of the number of gate strips, and not considered that of the grain boundary. We can see that the electric field strength at the drain side of the dual-gate poly-Si TFTs is larger than that of the single-gate poly-Si TFTs under the same bias conditions (V_{DS}=15V, V_{GS}=10V). Of course, this phenomenon will be more significant in the tri-gate poly-Si TFTs. Besides electric field strength near the drain, corner effect and sidewall roughness will also enhance the device's degradation rate. Therefore, it is concluded that the electric field at the drain side was enlarged with the increase of the stripes of poly-Si channel under hot carrier stress to cause severer impact ionization and hence to generate more trap states.

3.4 Summary

The effects of the numbers of the channel strips in multi-channel TFTs on the performance and reliability have been investigated. As the stripes increased, the electrical characteristics of devices were improved significantly due to the enhancement of gate control capability. However, a severer reliability was found which can be attributed to the enlargement of electric field at drain side. Therefore, for the fabrication of high reliable devices and yield improvement of multi-channel TFTs, the channel structures must be carefully designed.

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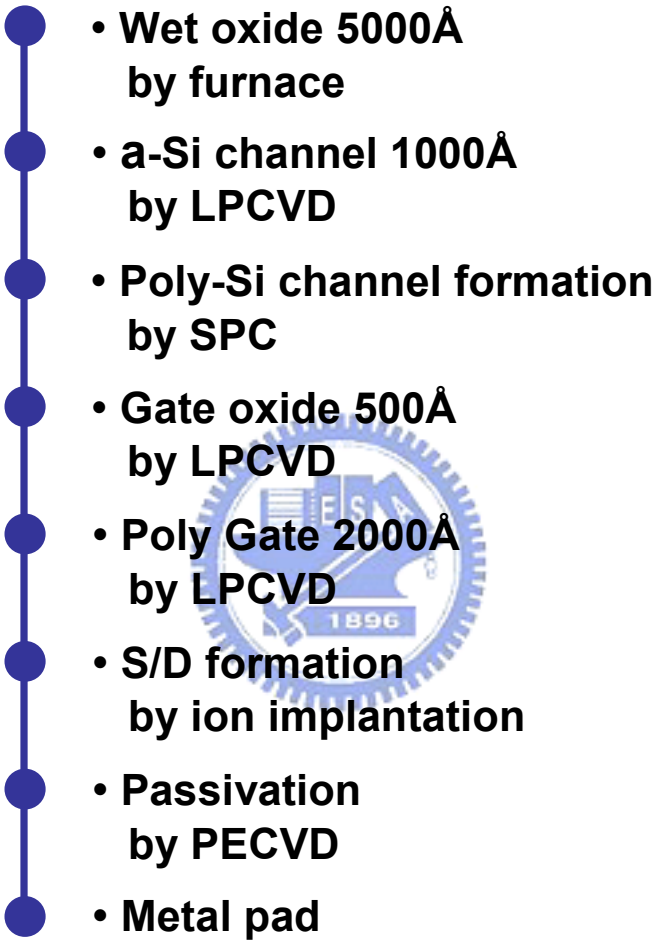


Fig. 3-1 Process flow of the conventional and multi-channel poly-Si TFTs.

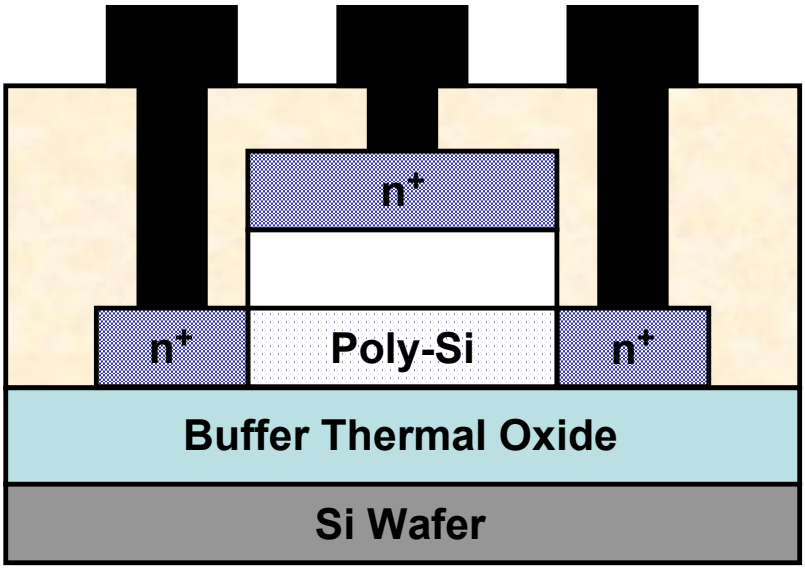


Fig. 3-2 Cross-section of the conventional and multi-channel poly-Si TFTs is parallel to the direction of the source and drain electrode.

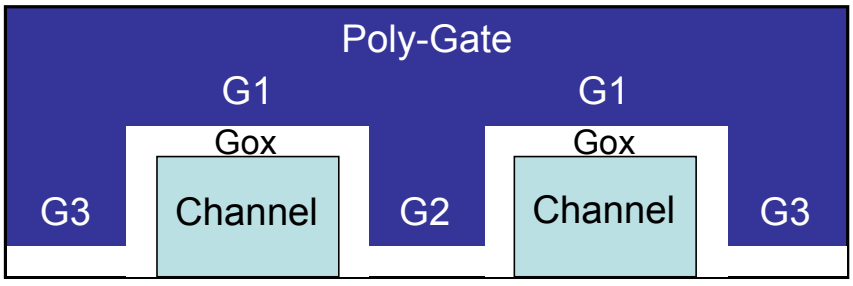
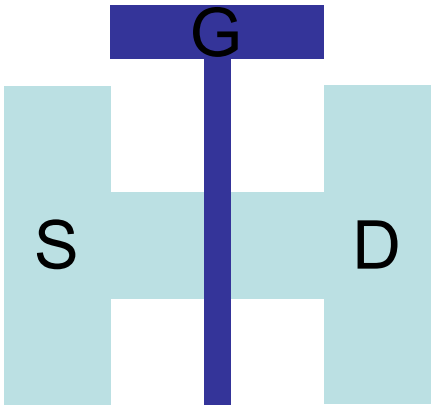
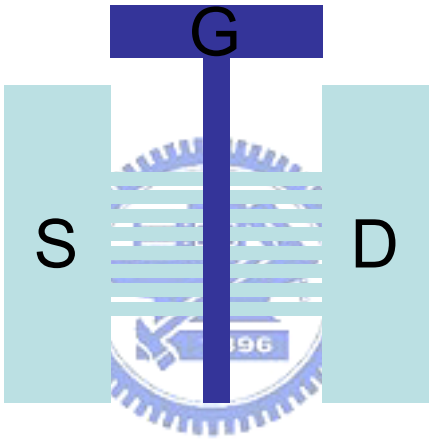


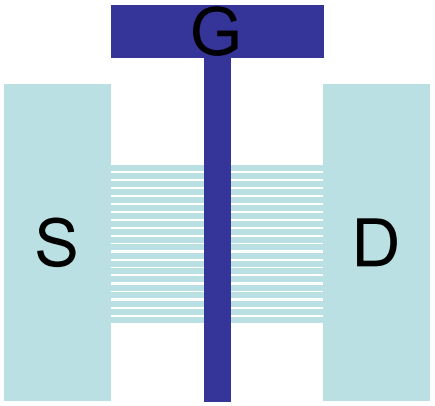
Fig. 3-3 Cross-section of the conventional and multi-channel poly-Si TFTs is perpendicular to the direction of the source and drain electrode.



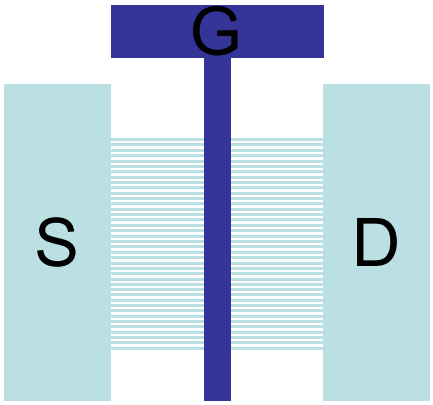
(a) Conventional TFT with single channel (S1)



(c) Multi-channel TFT with 8 stripes (M8)



(d) Multi-channel with 20 stripes (M20)



(e) Multi-channel with 40 stripes (M40)

Fig. 3-4 Top view of the conventional and multi-channel poly-Si TFTs in (a), (b), (c), and (d). (The effective channel width W_{eff} = 40 μm ; channel length L = 2 μm.)

Table 3-1 Summary of the dimensions of S1, M4, M8, M20, and M40 TFTs. All devices have the same active channel thickness 100nm, gate TEOS-oxide thickness 50nm, and total channel width 40 μm.

	S1	M8	M20	M40
Gate length (μm)	2	2	2	2
Channel number	1	8	20	40
Each channel width (μm)	40	5	2	1

Table 3-2 Summary of device parameters of the conventional and the proposed multi-channel poly-Si TFTs (W/L = 40 μm/2 μm) with different stripes of channel.

	S1	M8	M20	M40
V_{th}(V)	9.65	9.33	8.97	8.67
S.S(V/dec.)	1.257	1.230	0.987	0.923
μ_{eff} (cm^2/V.s)	25.3	26.1	28.5	29.6
I_{on} @ V_G = 20V(A)	2.76×10^{-4}	2.96×10^{-4}	3.44×10^{-4}	3.76×10^{-4}
I_{off} @ V_G = -5V(A)	1.56×10^{-11}	1.56×10^{-11}	1.51×10^{-11}	1.43×10^{-11}
ON/OFF Ratio	1.79×10^{7}	1.91×10^{7}	2.37×10^{7}	2.89×10^{7}
N_t(cm^{-2})	5.80×10^{12}	5.71×10^{12}	5.40×10^{12}	5.06×10^{12}

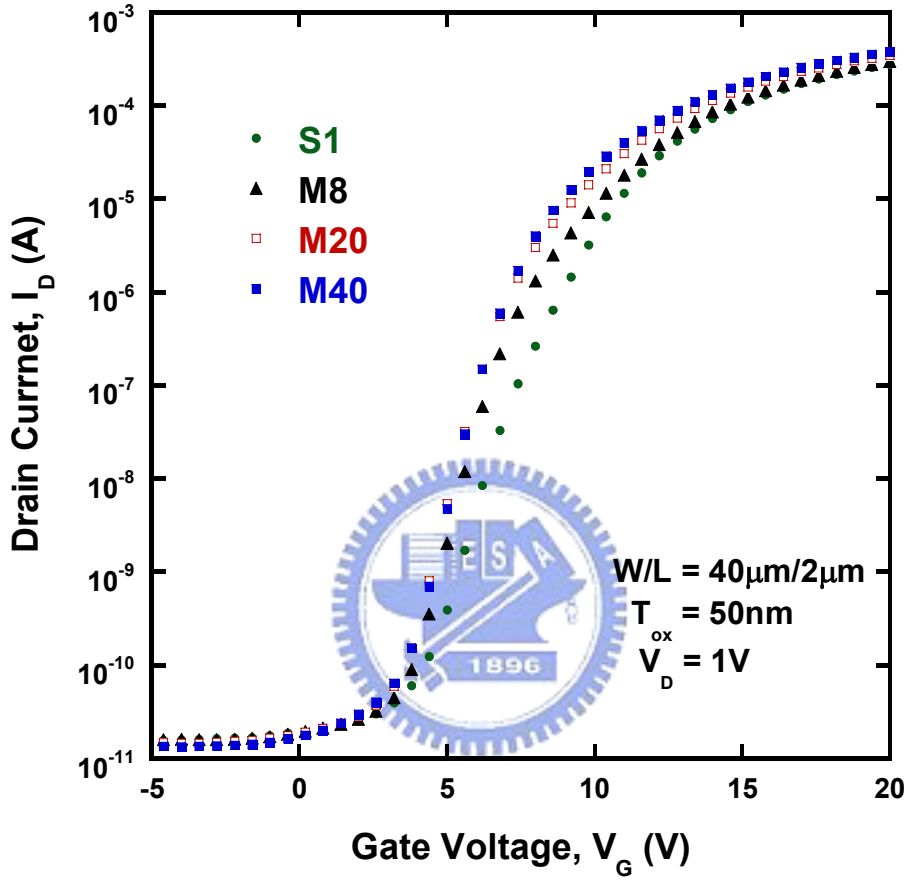


Fig. 3-5 Transfer characteristics of the conventional and the proposed multi-channel poly-Si TFTs with different stripes of channel.

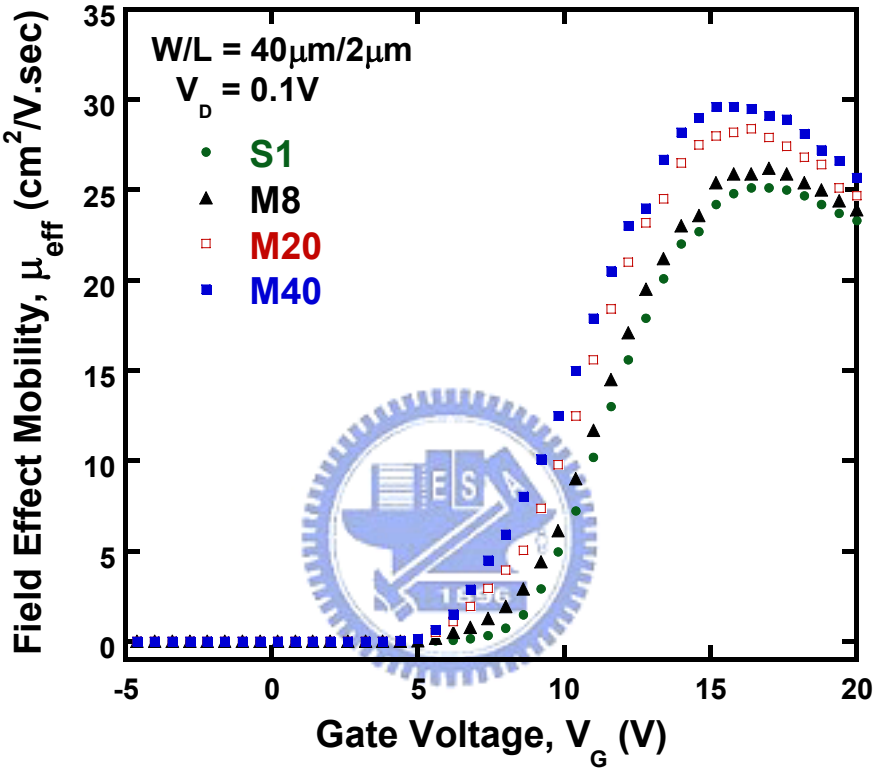


Fig. 3-6 Field effect mobility of the conventional and the proposed multi-channel poly-Si TFTs with different stripes of channel.

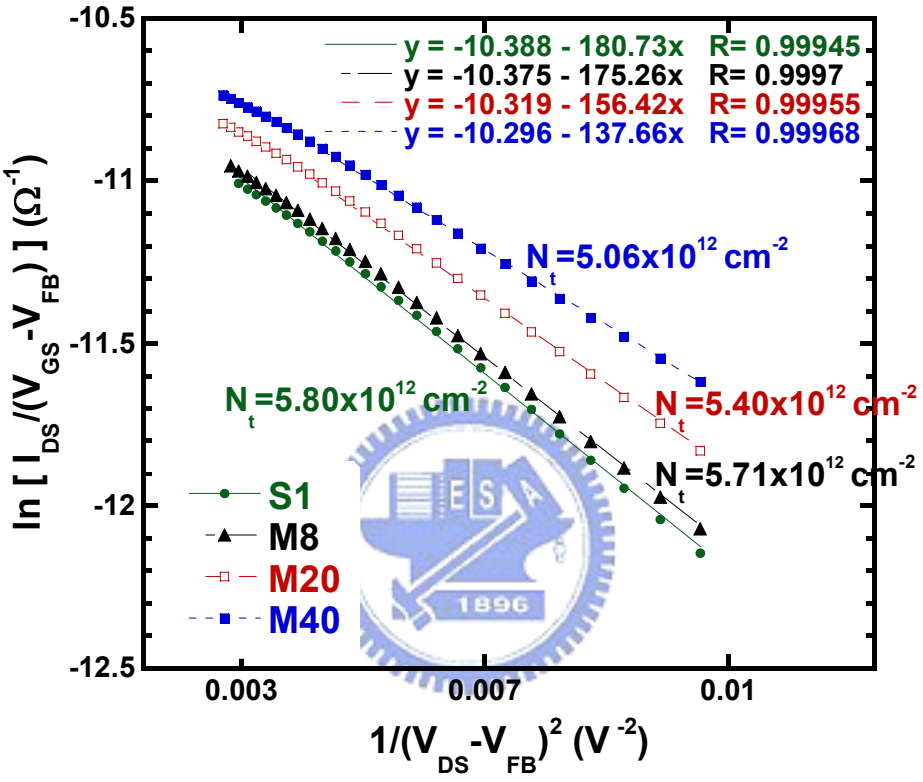


Fig. 3-7 Trap state density extraction of the conventional and the proposed multi-channel poly-Si TFTs with different stripes of channel.

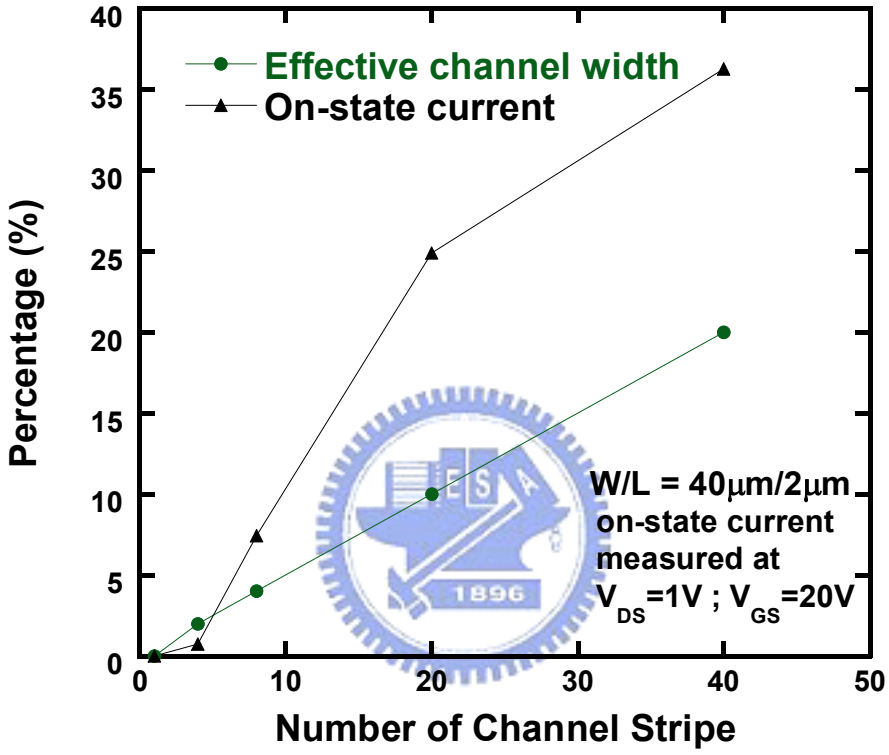


Fig. 3-8 Increasing ratio of the effective channel width and the on-state current as a function of number of channel stripes.

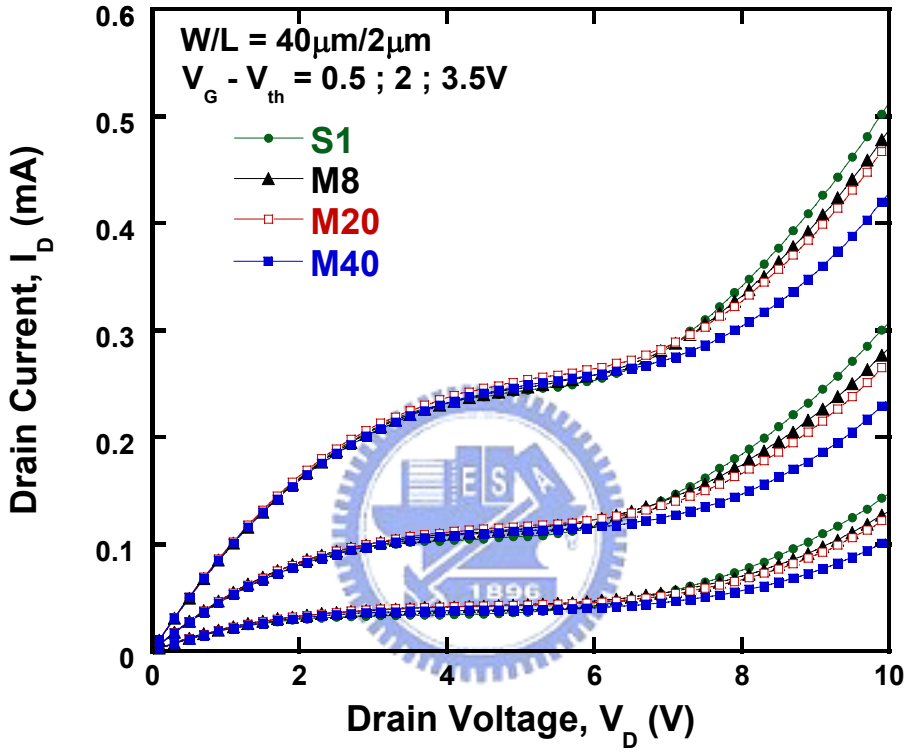
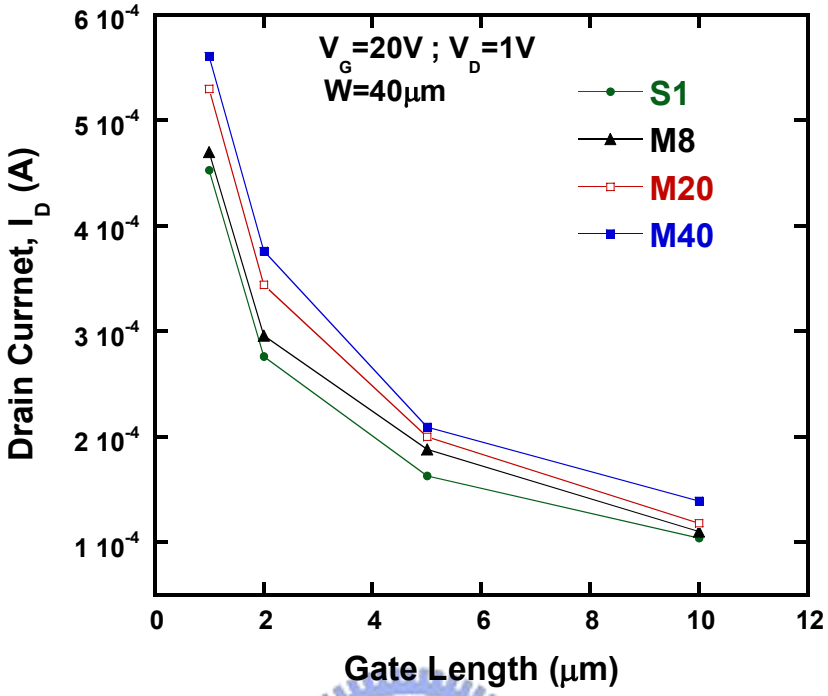
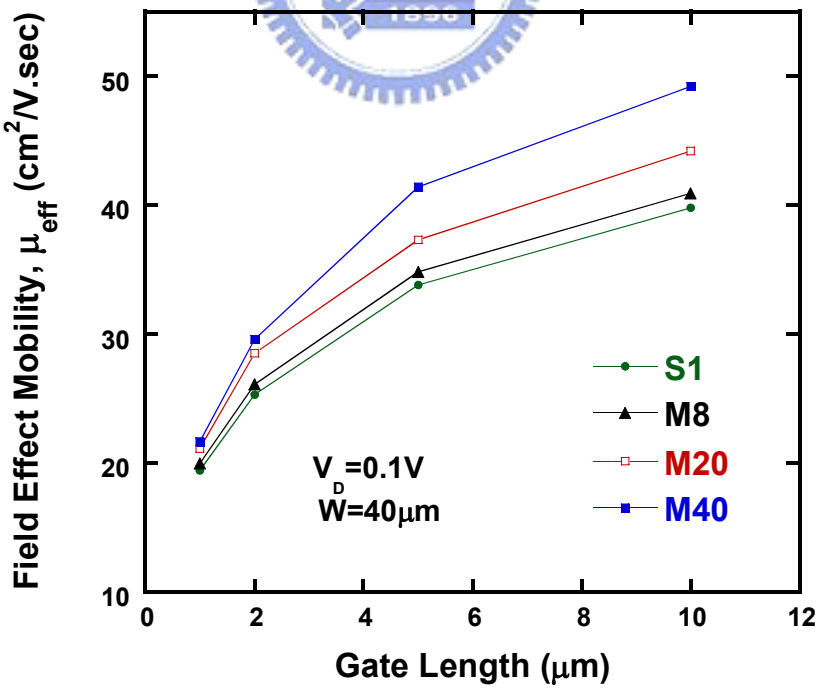


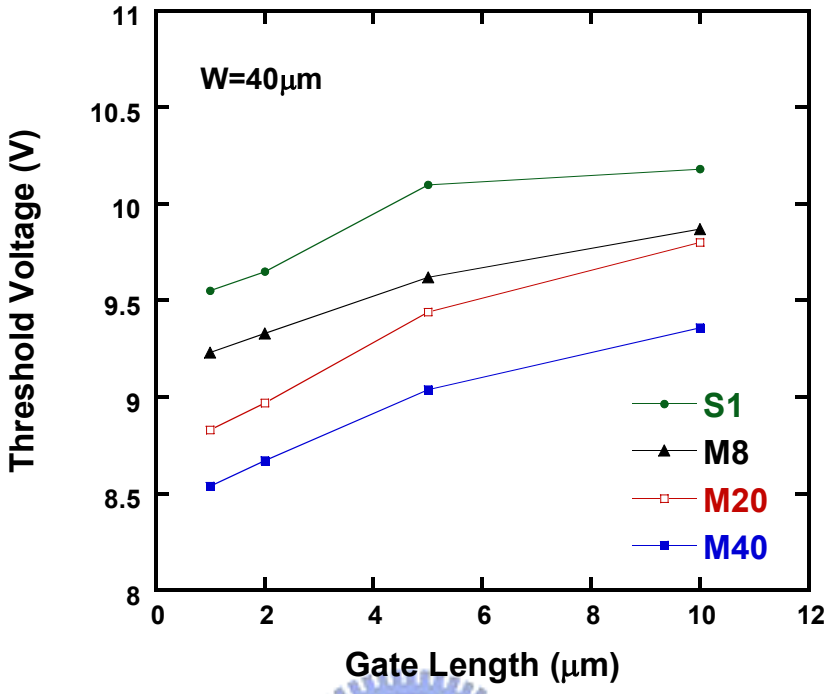
Fig. 3-9 Output characteristics of the conventional and the proposed poly-Si TFTs with different stripes of channel. ($V_G - V_{th}$ = 0.5; 2; 3.5V)



(a) On-state current

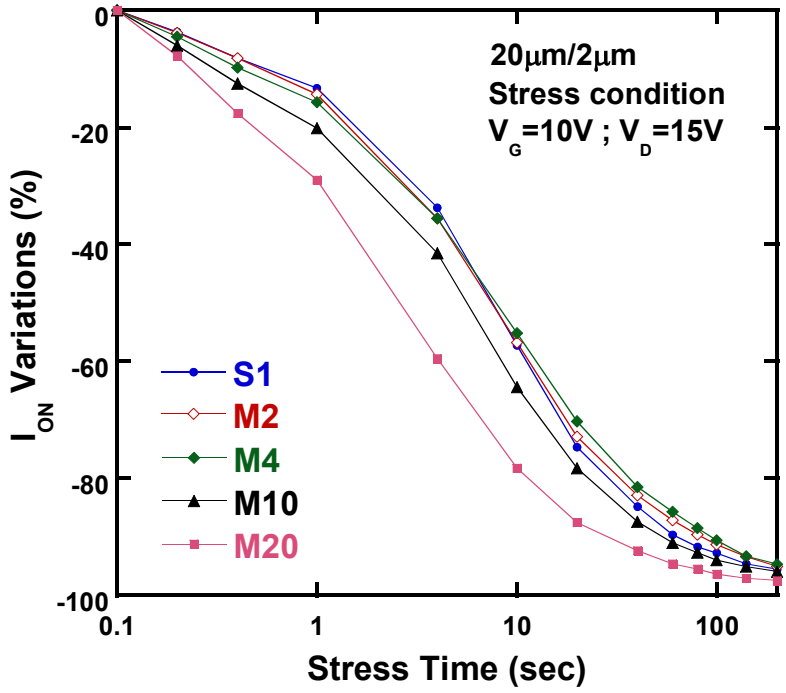


(b) Field effect mobility

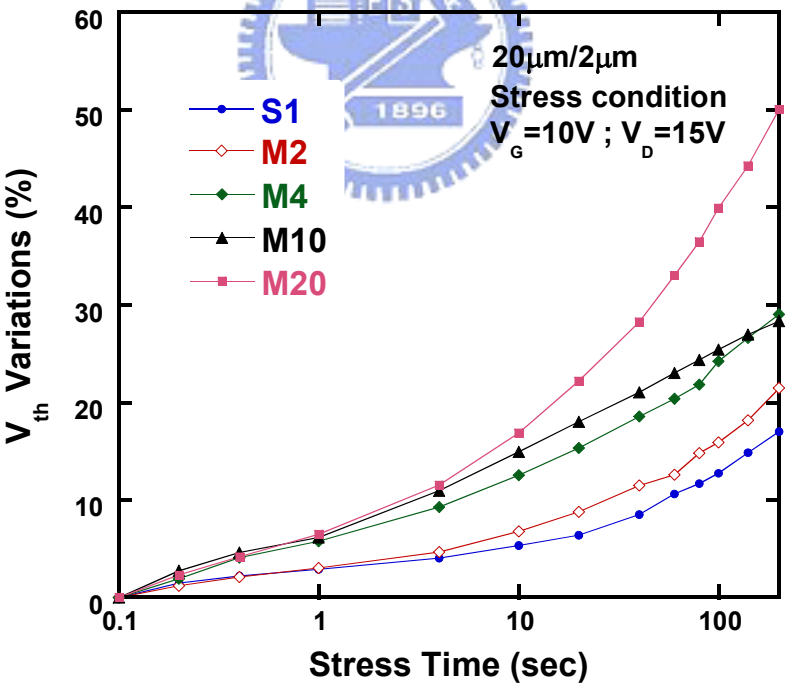


(c) Threshold voltage

Fig. 3-10 (a) on-state current, (b) field effect mobility, and (c) threshold voltage as a function of different gate length with the number of channel stripes.



(a) On-state current degradation with stress time



(b) Threshold voltage degradation with stress time

Fig. 3-11 (a) on-current, and (b) threshold voltage degradation as a function of stress time under hot-carrier stress.

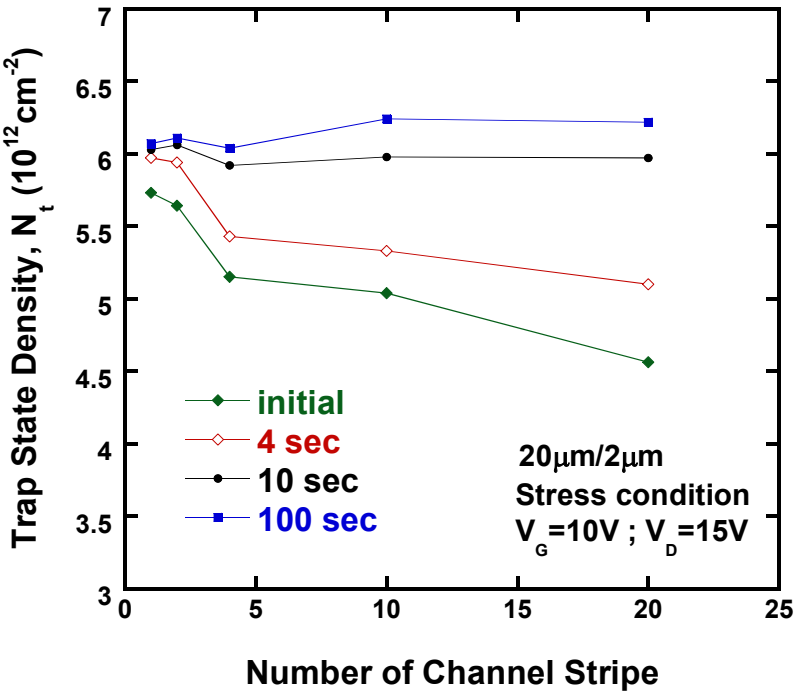


Fig.3-12 Trap state density (N_t), before and after 4sec, 10sec, and 100sec stress with different number of channel stripes.

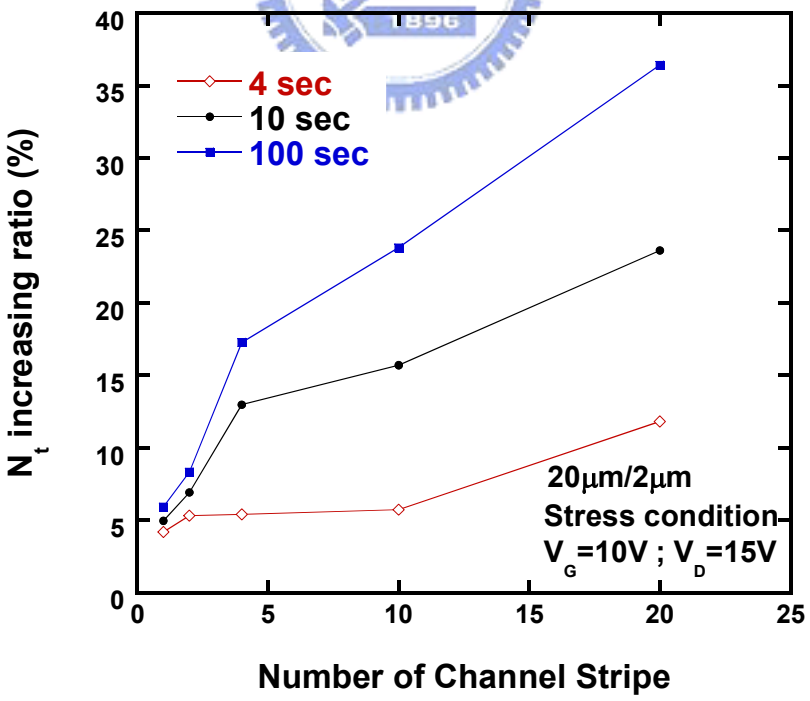


Fig. 3-13 Increasing ratio of trap state density after 4sec, 10sec, and 100sec stress with different number of channel stripes.

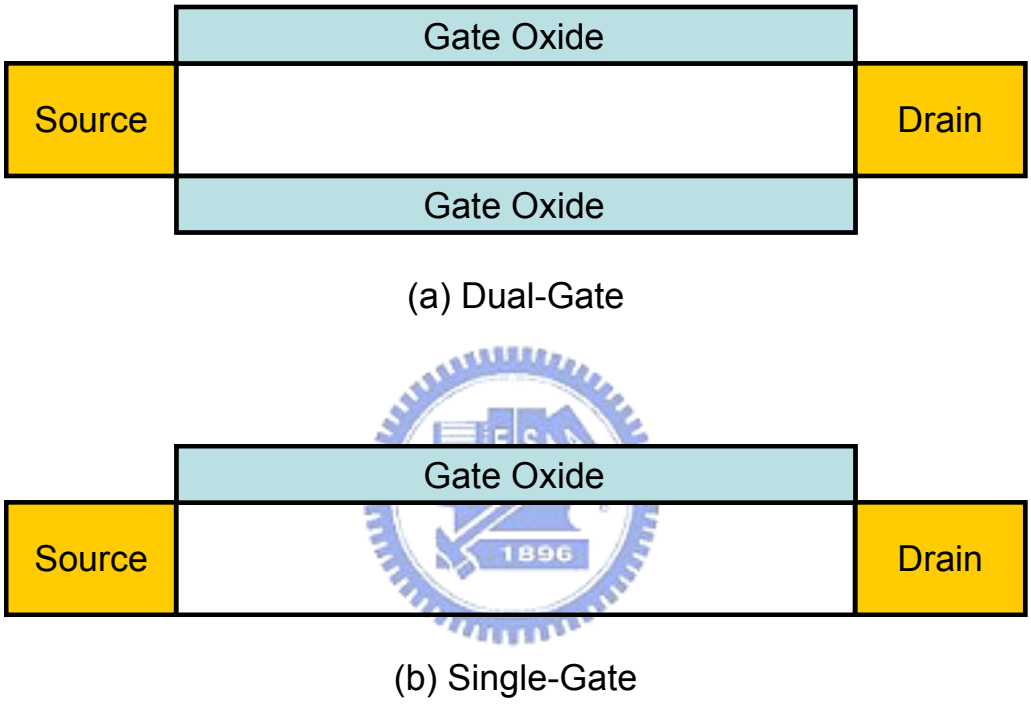


Fig. 3-14 Schematic plot of structures for simulation.

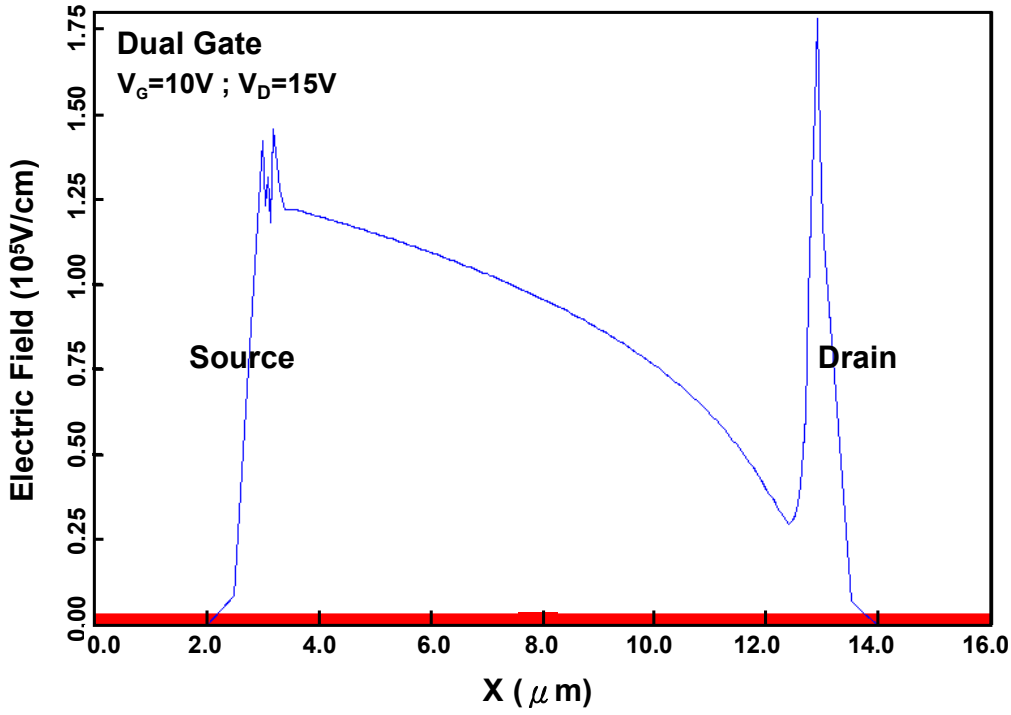


Fig.3-15 Electric field distribution in the poly-Si channel of dual-gate TFTs.

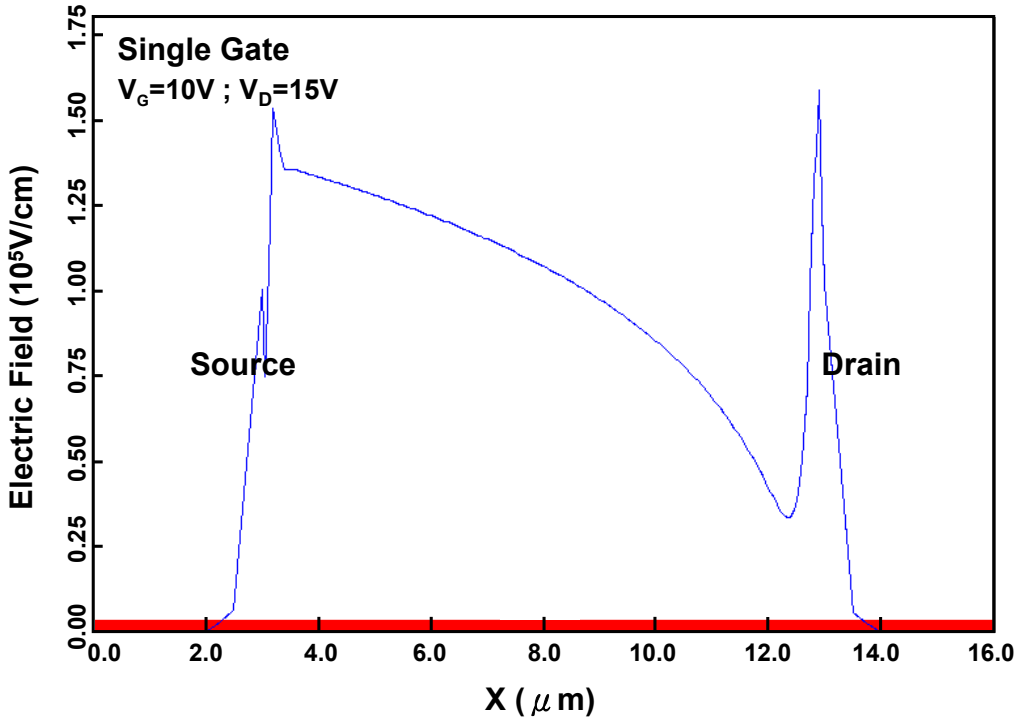


Fig. 3-16 Electric field distribution in the poly-Si channel of single-gate TFTs.

Chapter 4

The Lifetime of Poly-Si Thin-Film Transistors

4.1 Introduction

Lifetime is a convenient characteristic to monitor the device's reliability. It is often used for the comparison of hot carrier immunity of different structures and technologies of devices. For this purpose, we usually apply high voltage to extract device's lifetime. As we know, poly-Si TFTs have been widely used in many applications. However, to date, the lifetime prediction of poly-Si TFTs hasn't been well-studied.

For MOSFETs, drain-avalanche-hot-carrier (DAHC) injection, based on impact ionization near the drain, causes the severest damage on the device's characteristics. The device's degradation depends on the trap states generation, which is also proportional to the substrate current (I_{sub}) [1]. Therefore, DAHC-induced I_{sub} is used to monitor the device degradation and to predict the device lifetime. Under the severest DAHC stress, the empirical model for the lifetime prediction has been reported. It is found that threshold voltage shift (ΔV_{th}), Gm degradation ($\Delta Gm/Gm_0$), or On-current degradation ($\Delta I_{on}/I_{on0}$), can be expressed as [2][3]

$$\Delta V_{th}\left(\Delta Gm/Gm_0, or \Delta I_{on}/I_{on0}\right) = A \times t^n \quad \text{---------- (Eq. 4.1)}$$

The slope *n*, in the log-log plot depends on the hot-carrier injection conditions. This tendency is valid for conventional MOSFETs.

However, for poly-Si TFTs, besides impact ionization, parasitic bipolar transistor (PBT) can also enhance the drain current to accelerate the device

degradation [4]. Due to the lack of body terminal in poly-Si TFT, holes generated during impact ionization will be recombined with electron as they flow to the channel, or they will accumulate in the substrate near the source. The injection of holes into the body will lowers the potential barriers between the source and the channel. When the voltage drop across the body-source junction is large enough, the parasitic bipolar transistors (PBT) will be turned on. The action of PBT will enhance the on-current and then increase the device degradation rate [5]. Therefore, PBT should be considered as predicting the lifetime of poly-Si TFTs. In this section, we used the conventional empirical extrapolating method of MOSFETs to predict the lifetime of poly-Si TFTs. However, there was apparent disagreement observed in low drain stress voltages (V_{DS}). This is believed to be due to the action of PBT.

4.2 Experimental

Figure 4-1 and 4-2 show the process flow and cross-sectional view of the investigated poly-Si TFT. First, 500-nm-thick thermal oxide was grown on the Si wafers by furnace system to substitute for the glass substrate. Then, 100-nm-thick amorphous silicon layers were deposited on the thermal-oxidized layer in a low-pressure chemical vapor deposition (LPCVD) system by pyrolysis of silane (SiH_4) gas source at 550°C. Next, a semi-Gaussian-shaped KrF excimer laser with wavelength of 248nm was performed for the phase transformation from amorphous to polycrystalline silicon at the laser energy density of 480mJ/cm^2 with substrate heating of 400°C under the chamber pressure of 10^{-3}Torr. Individual active regions were then patterned and defined. After an RCA cleaning procedure, a 100nm-thick TEOS oxide was deposited with TEOS and O_2 gas source by PECVD at 350°C for the gate insulator. A 200-nm-thick poly-Si was deposited to serve as the gate electrode by

LPCVD. Then, gate electrode was patterned and the regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15}ions/cm^{-2} and 40keV. The dopant activation was performed by excimer laser annealing with laser energy density of 220mJ/cm^2, followed by a deposition of 400-nm-thick passivation oxide in a PECVD system at 350°C and the definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited by thermal evaporation and patterned for metal pads. The transfer characteristics of the poly-Si TFT is shown in Fig. 4-3.

4.3 Results and Discussion

Impact ionization near the drain is a main mechanism to cause substantial trap states at the interface for MOSFETs under a hot carrier stress. From the empirical model, the I_{on} degradation can be expressed as

$$\Delta I_{on}/I_{on0} = A\times t^{n} \quad \text{---------- (Eq. 4.2)}$$

The magnitude of degradation, A, which has physical meaning as the number of excess carrier generated by impact ionization, has been known to have the V_{DS} dependency:

$$A \propto \exp(-a/V_{DS}) \quad \text{---------- (Eq. 4.3)}$$

where a is a constant. On the other hand, the peak substrate current (I_{sub}) and the increase of trap states, which are also proportional to the number of electron-hole pairs generated by impact ionization, can be also expressed in the same dependency [6][7].

$$N_{it} \propto I_{sub} \propto \alpha \propto \exp(-c/E) \propto \exp(-c/V_{DS}) \propto A^{c/a} \quad \text{---------- (Eq. 4.4)}$$

where α is the impact ionization factor, c is a constant, and E is the local electric

field near the drain. Using (Eq. 4.2), (Eq. 4.3), and (Eq. 4.4), the lifetime (τ) of the MOSFET under a certain criterion can be expressed as:

$$\tau \propto \exp(b/V_{DS}) \quad \text{---------- (Eq. 4.5)}$$

where b is also a constant. Therefore, we will use this conventional empirical model to investigate the lifetime of poly-Si TFTs.

First, we define the worst case of hot carrier stress of poly-Si TFTs. It has been demonstrated that the worst-case hot carrier degradation for MOSFET is known to be under V_G=1/2 V_D [8]. However, due to the PBT action, the worst-case degradation for SOI-MOSFETs is $V_G \approx V_{th}$ [9]. As we know, poly-Si TFTs is similar to SOI MOSFETs; both of their body is floating. Therefore, we deduced that the worst-case degradation for poly-Si TFTs is also under $V_G \approx V_{th}$. Figure 4-4 shows the comparison of the I_D degradation under stress conditions of V_G=1/2 V_D and $V_G \approx V_{th}$ with V_{DS}=20V and 18V. It is obviously shown that the $V_G \approx V_{th}$ conditions cause severest damage of poly-Si TFTs. Therefore, the degradation of poly-Si under stress conditions of $V_G \approx V_{th}$, with V_{DS}=10~20V and source grounded for 1000sec were investigated. Figure 4-5 shows the I_{on} variations as a function of stress time with various V_{DS}. As can be seen, the slope *n*, in log-log plot depends on the V_{DS} strongly. Obviously, two sets of slopes can be observed. The slopes for high V_{DS} are almost equal to 0.5, which indicates that recombination-induced trap states dominate the device degradation [10]. However, the slopes for low V_{DS} stress conditions are higher than that of high V_{DS} stress conditions. A similar tendency has been found in SOI MOSFETs [11][12]. However, the mechanism responsible for this phenomenon has not been well-studied before.

Figure 4-6 presents the lifetime (τ) as function of the reciprocal V_{DS}. The lifetime is defined as the time taken for 10% I_{on} degradation at V_D=1V. We found that the experimental results agree with the empirical model only for high V_{DS} stress

conditions. This indicates that impact ionization model only dominate the device degradation under high V_{DS} stress conditions. Current and electric field near the drain is known to be the most important two factors of impact ionization. When V_{DS} increases, the two factors were then enhanced. Therefore, under high V_{DS} the empirical model is valid for not only MOSFETs but also poly-Si TFTs.

However, there is a deviation under low V_{DS} stress conditions. Moreover, the relationship between the magnitude of device degradation A and reciprocal V_{DS} is show in Fig. 4-7. The agreement between the model and experimental results only can be found under high V_{DS}. Therefore, this proves that the impact ionization model is unsuitable for the low V_{DS} stress conditions.

Comparing the device structures between MOSFETs and poly-Si TFTs, the floating body is the main difference between them. For MOSFETs, the I_{sub} generated by impact ionization in MOSFETs flowed to the body terminals. However, for poly-Si TFTs, the I_{sub} will flow through the substrate toward the source to be recombined or accumulate in the substrate, and turn on the PBT. Moreover, under low V_{DS} stress condition, the current and high electric field near the drain side is not high enough. Therefore, the impact ionization is not the first order effect for the current multiplication. Therefore, we deduce that PBT action plays the main roles on the current enhancement to damage the device characteristics at low V_{DS}. That is why the magnitude of device degradation (A) and lifetime (τ) do not agree with the empirical impact ionization model under low V_{DS} stress conditions.

So, when predicting the lifetime of poly-Si TFTs, the PBT phenomenon must be considered. Figure 4-8 shows the current generation in the poly-Si TFTs with a floating body. In this figure, the intrinsic drain current (I_D) induces a hole current (I_{sub}) due to impact ionization near the drain side, and the I_{sub}, which flows to the source induces a bipolar electron current (I_e), can be expressed as:

$$I_{sub} = (M-1)I_D \quad \text{---------- (Eq. 4.6)}$$

The bipolar electron current (I_e) can be expressed as:

$$I_e = (\beta+1)I_{sub} = (\beta+1)(M-1)I_D \quad \text{---------- (Eq. 4.7)}$$

where β is the bipolar current gain, and M is the impact-ionization multiplication factor, which can be expressed as:

$$(M-1) = \int \alpha dy \quad \text{---------- (Eq. 4.8)}$$

Then, I_e which injects into the channel will enlarge I_D, and enhance impact ionization near the drain to generate higher I_{sub}.

$$I'_D = I_D + I_e = [1+(\beta+1)(M-1)]I_D \quad \text{---------- (Eq. 4.9)}$$

$$I'_{sub} = [(M-1)+(\beta+1)(M-1)^2]I_D \quad \text{---------- (Eq. 4.10)}$$

Therefore, using (Eq. 4.6), (Eq. 4.7), (Eq. 4.9), and (Eq. 4.10), a general form of I_{sub} is derived and expressed as

$$I_{sub} = (M-1)\left\{\frac{\left[(\beta+1)^n(M-1)^n - 1\right]}{\left[(\beta+1)(M-1) - 1\right]}\right\} I_D \approx (\beta+1)^{n-1}(M-1)^n I_D \quad \text{-------- (Eq. 4.11)}$$

Where n is a positive integer. From (Eq. 4.4) and (Eq. 4.5), it is demonstrated that τ is proportional to the reciprocal I_{sub}. So, it can be expresses as:

$$\tau \propto 1/(\beta+1)^{A_0}(M-1)^{B_0} \quad \text{---------- (Eq. 4.12)}$$

where A0 and B0 are constant. As can be seen, this form shows the lifetime prediction including both impact ionization and PBT effects.

Moreover, it has been proposed by using simulation method that the β varies with V_{DS} [4]. The β decreases dramatically with increasing V_{DS} [4]. This can be explained by the high current injection [4][13]. Therefore, under high V_D stress condition, (M-1) is large and β is small, which can be neglected. Then, $\tau \propto$

$1/(M-1)^{B_0}$, which means that the impact ionization dominates. However, under low V_D stress condition, β is large, whereas (M-1) is small. In this condition, the PBT action must be considered. That is why the lifetime prediction as shown in Fig. 4-6 did not agree with the conventional empirical model. Although further investigation is still needed, from this section, we can understand the lifetime prediction model more in poly-Si TFTs.

4.4 Summary

Lifetime of poly-Si TFTs has been investigated. It is found that lifetime extraction of poly-Si TFTs is not the same with that of MOSFETs. The worst-case of stress conditions is under $V_G \approx V_{th}$ not $V_G=1/2\ V_D$. Moreover, I_{on} degradation under both high and low V_D of stress conditions has different phenomena. This is because impact ionization dominated under high V_D. However, under low V_D, the degradation mechanism is complicated; not only impact ionization but also parasitic BJT phenomenon must be considered.

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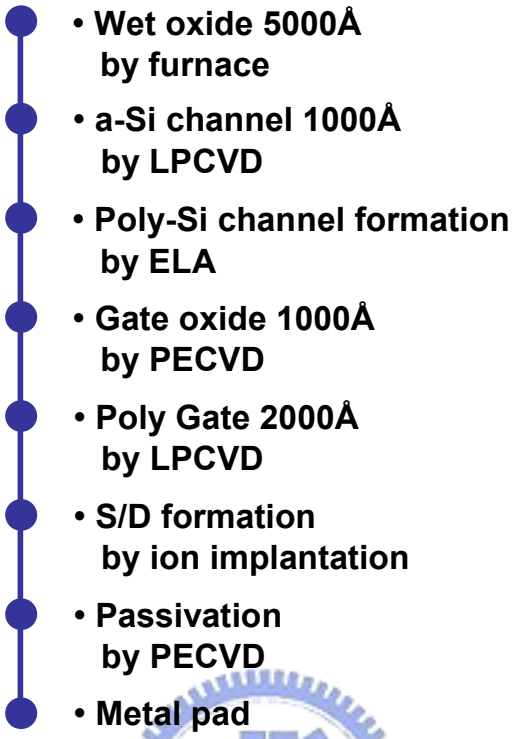

Fig. 4-1 Process flow of the conventional poly-Si TFTs.

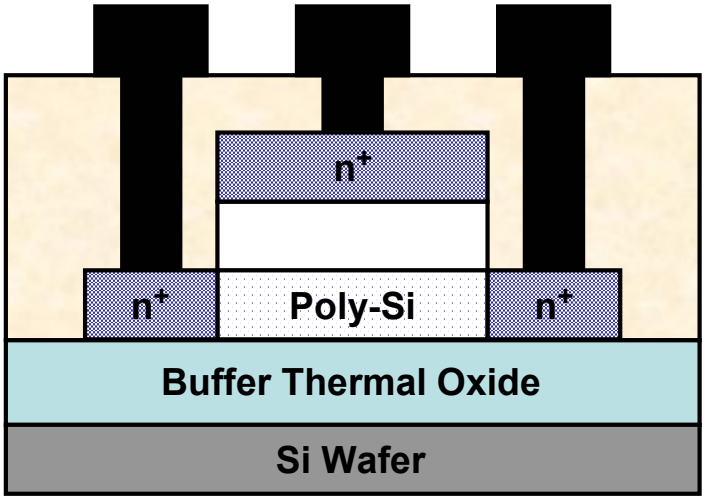

Fig. 4-2 Cross-section of the conventional poly-Si TFTs.

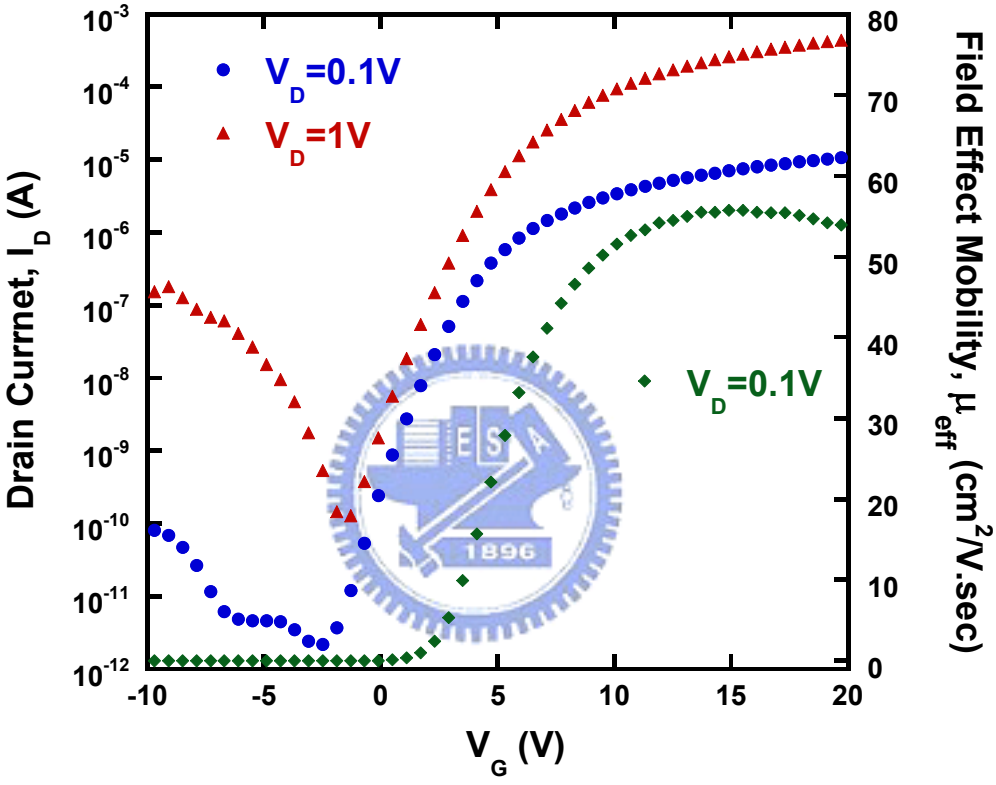

Fig. 4-3 Transfer characteristics of the conventional poly-Si TFTs.

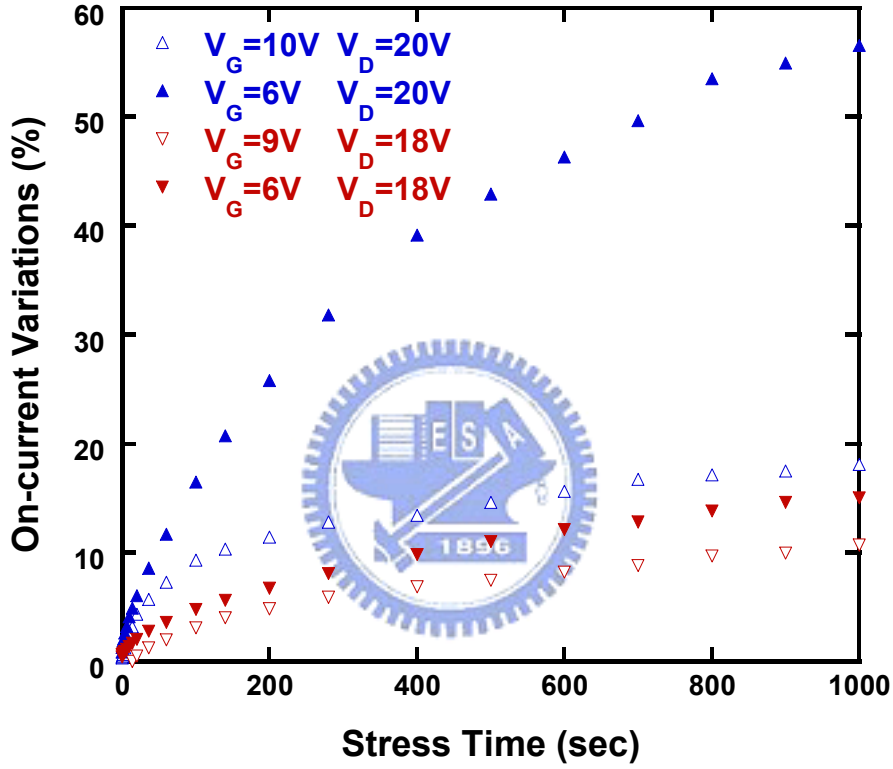

Fig. 4-4 On-current variations under stress conditions of V_G=1/2 V_D and V_G=V_{th} under V_{DS}=20V and 18V.

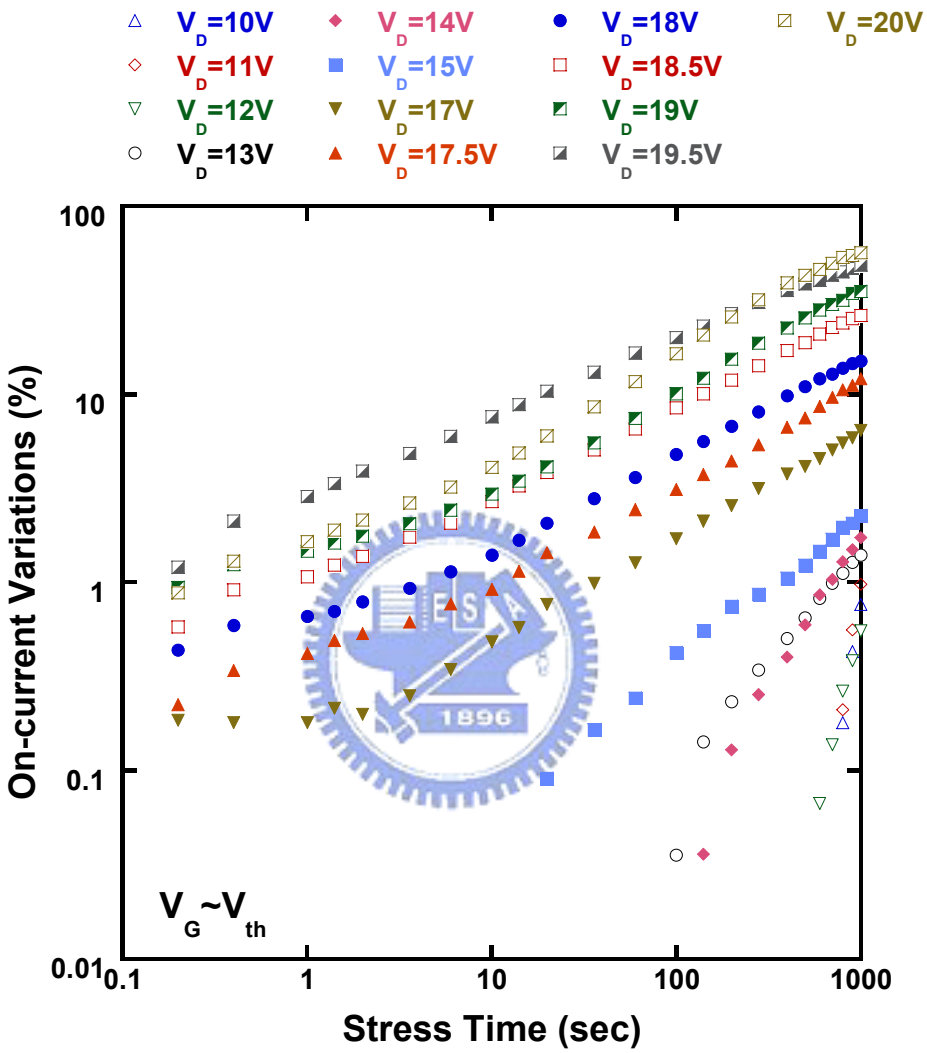

Fig. 4-5 On-current variations as a function of stress time with stress drain voltage (V_{DS}) as a parameter.

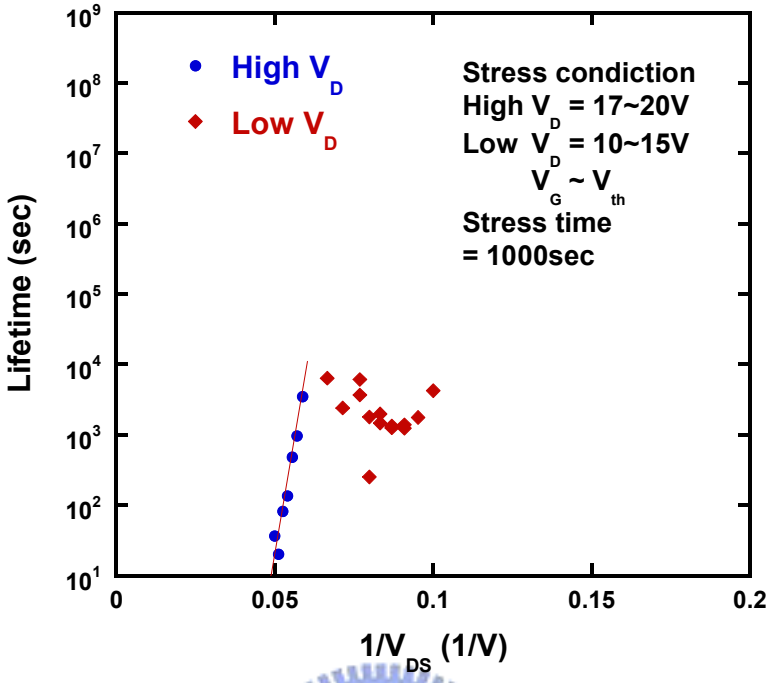

Fig. 4-6 Lifetime as function of the reciprocal drain voltage stress for poly-Si TFTs stressed at $V_{GS} \approx V_{th}$ with V_{DS} from 10 to 20V.

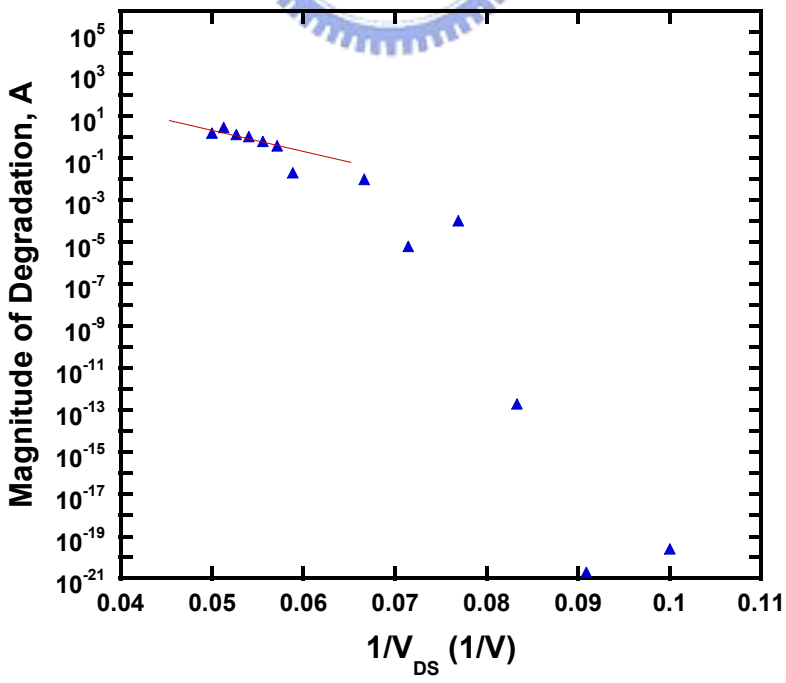

Fig. 4-7 Magnitude of device degradation (A) as a function of drain voltage V_{DS}.

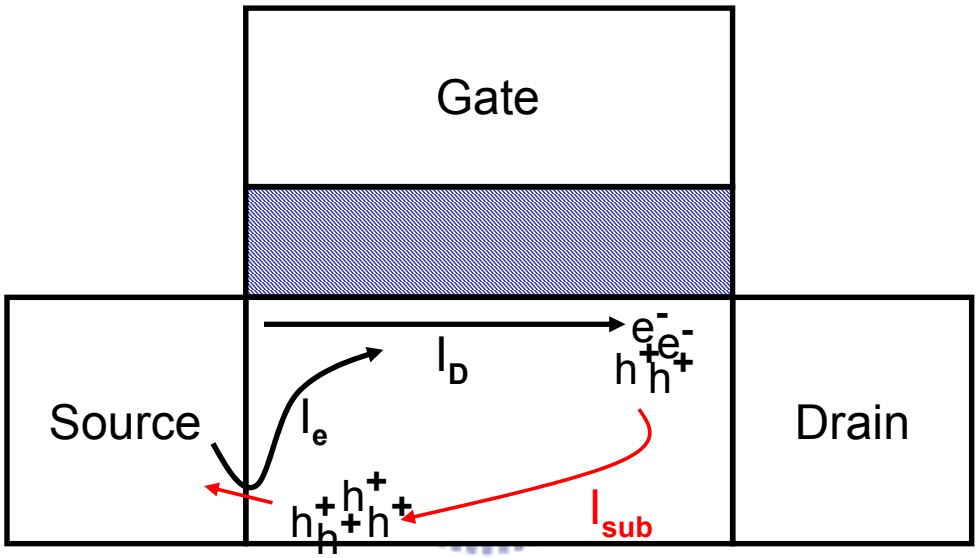

Fig. 4-8 Schematical plot of the occurrence of impact ionization and bipolar multiplication in the poly-Si TFT.

Chapter 5

Conclusions

In this thesis, first, a simple and process-compatible method to fabricate poly-Si TFTs on the FSG buffer layer is proposed. The performance and uniformity of the devices were significantly improved by fluorine incorporation in the poly-Si layer. This is attributed to the reduction of the trap state density in the poly-Si channel and Si/SiO_2 interface. Additionally, the incorporation of fluorine atoms also promotes the hot-carrier immunity due to the formation of the rather stronger Si-F bonds. However, excess fluorine atoms will make the FSG layer unstable, and react with moisture to form HF, which in turn deteriorate the devices and result in the degraded performance and reliability. So, it is concluded that fabricating poly-Si TFTs on FSG buffer layers with appropriate fluorine content (2%~4%) improves not only the electrical performance and uniformity but also the reliability.

Then, the effects of the numbers of the channel strips in multi-channel TFTs on the performance and reliability are investigated. The electrical characteristics of devices were improved significantly with increasing channel stripes due to the enhancement of gate control capability. However, a severer reliability was found, because the enlargement of electric field at drain side caused the severer impact ionization. Therefore, for the fabrication of high reliable devices and yield improvement of multi-channel TFTs, well-designed structures must be considered to lower the electric field strength at drain side, such as lightly-doped drain (LDD).

Finally, lifetime of poly-Si TFTs has been investigated. It was found that the

worst-case of stress conditions for poly-Si TFTs is under $V_G \approx V_{th}$, not under V_G=1/2 V_D. In addition, the I_{on} degradation phenomenon has much difference under both high and low V_D of stress conditions. Under high V_D of stress conditions, the I_{on} degradation mechanism of poly-Si TFTs is the same with that of MOSFETs, which impact ionization dominates. However, under low V_D of stress conditions, not only impact ionization but also parasitic bipolar transistors (PBT) must be considered. Therefore, bipolar current gain (β) and impact-ionization multiplication factor (M) are used to find the new relationship between lifetime prediction and I_{on} degradation mechanism. Nevertheless, the relationship between β and V_D is not clearly defined. So, it is rather difficult to predict the lifetime of poly-Si TFTs under low VD of stress conditions.

簡歷

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