

# 氮化矽記憶體元件資料保存及耐久性之探討

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## 摘要

氮化矽記憶體(SONOS memory) 將是未來非揮發性記憶體元件的主流，它相較於快閃記憶體(Flash)，有著較簡單的結構、簡單的製程，而且可以比傳統浮閘結構快閃記憶體有更佳的微縮能力(scalability)。對於 SONOS 來說，耐久性(endurance)及保存性(retention)是最主要的二項可靠性課題。



在本論文中，我們將探討各種不同上氧化層(blocking oxide)及穿隧氧化層(tunnel oxide) SONOS 結構的資料保存以及元件耐久特性。經由實驗，可以了解直接穿隧的漏電流有一部份是經由上氧化層，而非一般所假設全部經由薄的穿隧氧化層。首先，我們量化注入電荷及電荷流失的量。結果顯示，我們發現到較薄上氧化層 SONOS 元件所流失的電荷較多，尤其是當上氧化層厚度降到  $40 \text{ \AA}$  以下，而這也證明了電荷從上氧化層端所流失。我們也提出一種區分三種漏電流機制的方法，結果發現到直接穿隧(DT)在短時間主導電荷流失，但是長時間( $>10000\text{s}$ )情況下，電荷流失成分以熱放射(thermionic emission)為多，且在 P/E cycle 之後，因為氧化層劣化造成的缺陷促進穿隧(trap assisted tunneling)將逐漸顯著，對較厚的氧化層而言，此漏電將更加嚴重。

接著，我們更深入探討 cycling 效應對於 SONOS 記憶體元件的 ONO 層個別的影響。

由實驗結果更得知，較厚的下氧化層的耐久性的劣化主要原因是下氧化層的劣化，至於薄的下氧化層耐久性之劣化的主因卻是上氧化層的劣化。除此之外，我們得知在整個 cycling 過程中，初期因為氮化矽層的缺陷增加導致操作效率提高，在操作多次後操作效率將因上氧化層的劣化而降低。因此，薄的上氧化層有較佳的耐久性，較小的操作電壓等優點，但是有電荷流失，操作區間(operation window)較小等缺點。尤其是在元件不斷的縮小化的時候，這些結果可以幫助我們更了解電荷流失的情形及其主導的物理機制。




# The Investigation of Data Retention and Endurance in a Nitride Storage Flash Memory

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## Abstract



SONOS (Silicon Oxide Nitride Oxide Silicon) will become the main stream of nonvolatile memory products because of its simplicity in structure and scalable by comparing with conventional floating gate cells. For the scaling of SONOS memory, the endurance and retention are the two major reliability issues.

In this thesis, data retention for various top (blocking) and bottom oxide (tunnel oxide) SONOS cells has been investigated. The direct tunneling through either tunnel or blocking oxide can also be identified experimentally. Results show that the cell with thinner blocking oxide has more charge loss under various baking temperatures, especially when the blocking oxide is thinner than 40 Å. A leakage current separation technique has been developed to distinguish the two leakage components via thermionic and direct tunneling. The direct tunneling dominates the short-term leakage while the long-term leakage is dominated by thermionic emission. After P/E cycling, the trap assisted tunneling will be more important because of the degradation of oxide, and it is more serious for thicker oxide.

Then, we will further study the influence of the cycling effect on the ONO layer of the SONOS memory device. It was found that for thicker tunneling oxide, the degradation of the endurance is originated from the degraded tunneling oxide and the degradation of the endurance comes from the blocking oxide for thinner tunneling oxide device. In addition, we also know that during the whole cycling process, the programming efficiency will be enhanced since the traps generated in nitride increase initially, and then decrease after long term cycles as the blocking oxide degraded. Thick blocking oxide cell has larger operation window and less charge loss, but needs larger gate voltage during program and erase and has poorer endurance. Finally, this will help us to understand the dominant leakage and degradation mechanism of endurance during the scaling of SONOS cells.



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## Table Caption

**Table 2.1** The split conditions of samples used in this work, in which devices have three different blocking oxide thickness and two different tunnel oxide thicknesses.





## Figure Captions

- Fig. 1.1** (a) The MNOS device with a relative thick nitride(>150Å) and high program/erase bias,  
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**Fig. 4.3** The subthreshold characteristic of two cells with different tunneling oxide thickness. There is no difference before and after cycling for thinner tunneling oxide.

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**Fig. 4.11** Endurance of cells with various blocking oxide thickness. This shows good operation window for  $10^4$  PE-cycles and poorer endurance for thicker blocking oxide cell.

**Fig. 4.12** (a) Measured charge pumping current after  $10^5$  PE cycles for samples 4, 5, and 6. (b) Gate-pulse representation in a CP measurement.

**Fig. 4.13** The band diagram of SONOS cell during negative gate bias when the electrons are trapped in the blocking oxide.

**Fig. 4.14** (a) The programming characteristic of sample no. 4 for the different cycle numbers. (b) The enhancement and degradation of the programming efficiency is shown in this figure.

## List of Symbols

$\Delta V_{th}$	The threshold voltage shift (V).
$E_{ox}$	The electric field across the tunnel oxide (MV/cm).
$f$	The occupation ratio of traps in nitride
$n_t$	The trapped electron density ( $1/\text{cm}^3$ )
$N_t$	The trap density ( $1/\text{cm}^3 \cdot \text{eV}$ )
$P_N$	Tunneling probability through the nitride
$P_{ox}$	Tunneling probability through the oxide
$\phi_1$	The barrier height for electron between silicon and oxide (eV)
$\phi_2$	The barrier height for electron between nitride and oxide (eV)
$\phi_s$	The surface potential (V)
$\phi_t$	The trap energy level (eV)
$q$	Magnitude of the electron charge ( $1.6 \times 10^{-19} \text{C}$ )
$t$	The time (s)
$T$	The temperature ( $^{\circ}\text{K}$ )
$T_{eff}$	The effective thickness of the ONO structure ( $\text{\AA}$ ).
$\tau$	The time constant (s)
$\tau_0$	The reciprocal of the “attempt-to-escape” frequency ( $\sim 10^{13} \text{s}$ )
$V_{fb}$	The flat-band voltage (V).
$V_{fb0}$	The initial flat-band voltage (V).
$V_{th}$	The threshold voltage (V).
$V_{th0}$	The initial threshold voltage (V).