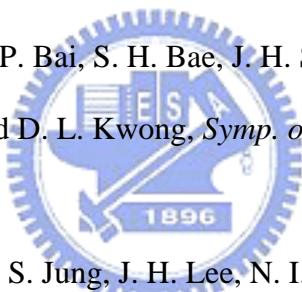


# References

- [1] G.E. Moore, "Progress in digital integrated circuit," IEDM Tech. Dig., p. 11(1975).
- [2] "International Technology Roadmap for Semiconductors (ITRS): 1999," Austin: Semiconductor Industry Association, p.123 (1999).
- [3] M. Schulz, Nature (London) 399 (1999) 729-730.
- [4] D. A. Muller, G. D. Wilk, Appl. Phys. Lett. 79 (2001) 4195-4197
- [5] H. Fukuda, S. Namioka, M. Miura, Y. Ishikawa, M. Yoshino, S. Nomura, Jpn. J. Appl. Phys. 38 (1999) 6034.
- 
- [6] J.-Y. Zhang, I.W. Boyd, Appl. Surf. Sci. 186 (2002) 40-44
- [7] W.-J. Qi, R. Nieh, B.H. Lee, L. Kang, Y. Jeon, J.C. Lee, Phys. Lett. 77( 2000) 3269.
- [8] L. Kang, B.H. Lee, W.-J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, J.C. Lee, IEEE Electron Device Lett. 21 (2000).
- [9] D. Wilk, R.M. Wallace and J.M. Anthony, *J. Appl. Phys.* **89**, 5243 (2001)
- [10] W.-J. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee,

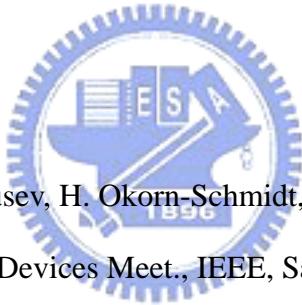
- and J. C. Lee , *Tech. Dig. Int. Electron Devices Meet.*, 145 (1999).
- [11] C.-H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, *Tech. Dig. Int. Electron Devices Meet.*, 27 (2000).
- [12] B. C. Hendrix, A. S. Borovik, C. Xu, J. F. Roeder, T. H. Baum, M. J. Bevan, M.R. Visokay, J. J. Chambers, A. L. Rotondaro, H. Bu, and L. Colombo, *Appl. Phys. Lett.* **80**, 2362 (2002).
- [13] Y. Harada, M. Niwa, S. Lee, and D. L. Kwong, *Symp. on VLSI Tech.*, 26 (2002).
- [14] C. H. Lee, J. J. Lee, W. P. Bai, S. H. Bae, J. H. Sim, X. Lei, R. D. Clark, Y. Harada, M. Niwa, and D. L. Kwong, *Symp. on VLSI Tech.*, 82 (2002).
- 
- [15] J. H. Lee, Y. S. Kim, H. S. Jung, J. H. Lee, N. I. Lee, H. K. Kang, J.H. Ku, H. S. Kang, Y. K. Kim, K. H. Cho, and K. P. Suh, *Symp. on VLSI Tech.*, 84 (2002).
- [16] Q. Lu, H. Takeuchi, X. Meng, T. J. King, C. Hu, K. Onishi, H. J. Cho, and J. C. Lee, *Symp. on VLSI Tech.*, 86 (2002).
- [17] A. L. P. Rotondaro, M. R. Visokay, J. J. Chambers, A. Shanware, R. Khamankar, H. Bu, R. T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M. J. Bevan, T. Grider, J. McPherson, and L. Colombo, *Symp. on VLSI Tech.*, 148 (2002).

[18] R. Nieh, S. Krishnan, H. J. Cho, C. S. Kang, S. Gopalan, K. Onishi, R. Choi, and J. C. Lee, *Symp. on VLSI Tech.*, 186 (2002).

[19] P. J. Chen, E. Cartier, R. J. Carter, T. Kauerauf, C. Zhao, J. Petry, V. Cosnier, Z. Xu, A. Kerber, W. Tsai, E. Young, S. Kubicek, M. Caymax, W. Vandervorst, S. De Gendt, M. Heyns, M. Copel, W. F. A. Besling, P. Bajolet, and J. Maes, *Symp. on VLSI Tech.*, 192 (2002).

[20] I.W. Boyd, J.-Y. Zhang, Nucl. Instrum, Method Phys. Res. B 121 (1997) 349.

[21] A. Kawamoto, J. Jameson, K. Cho, R. Dutton, challenges for atomic scale modeling in alternative gate stack engineering, IEEE Trans. El. Dev 47 (2000) 1787.

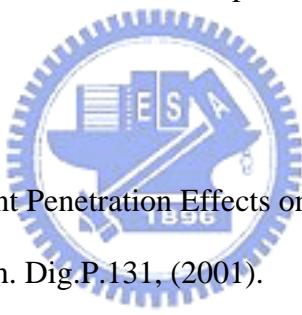


[22] D.A. Buchanan, E.P. Gusev, H. Okorn-Schmidt, K. Rim, M.A. Gribelyuk et al., Tech. Dig. Int. Electron Devices Meet., IEEE, San Francisco (2000) p. 223.

[23] E.P. Gusev, E. Cartier, D.A. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt et al., Microelectron. Eng. 59 (2001) 341.

[24] D. Martin Knotter, "Application and properties of sub-monomolecular layers of silicon dioxide deposited under mild conditions.", Applied Surface Science 99 (1996) p.99-110.

[25] S. Ichimura, A. Kurokawa, K. Nakamura, H. Itoh, H. Nonaka, K. Koike, "Ultrathin SiO<sub>2</sub> film growth on Si by highly concentrated ozone.", Thin Solid Films 377-378 (2000) 518-524.

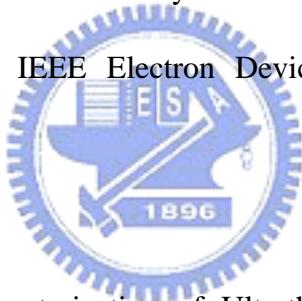
- [26] A. Kurokawa, S. Ichimura,"High purity ozone oxidation on hydrogen passivated silicon surface.", Applied Surface Science 100/101 (1996) 436-439.
- [27] T.J.Malone, D.E. Aspnes, H.Arwin, and T.W. Sigmon, Appl. Phys. Lett., vol. 44, p.517, (1984).
- [28] Yi Wei, Robert M. Wallace, and Alan C. Seabaugh, Appl. Phys. Lett., vol. 69, p.1270, (1996).
- [29] R. Choi, et al., " High-Quality Ultra-thin HfO<sub>2</sub> Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation ", Symp. VLSI Tech.,p.15, (2001).
- 
- [30] K. Onishi et al., " Dopant Penetration Effects on Polysilicon Gate HfO<sub>2</sub> MOSFET's ",VLSI Tech. Dig.P.131, (2001).
- [31] H.-J. Cho, D-G. Park, et al., " Characteristics of TaOxNy Gate Dielectric with Improved Thermal Stability", Jpn. J. Appl. Phys. Vol. 40, p. 2814, (2001).
- [32] H.-J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan, and J. C. Lee et al, " Novel Nitrogen Profile Engineering for Improved TaN/HfO<sub>2</sub>/Si MOSFET Performance "IEDM Tech., p.459, (2001)
- [33] A.L.P. Rotondaro et al., " Advanced CMOS Transistors with a Novel HfSiON

Gate Dielectric "VLSI Tech., p.148, (2002).

- [34] M. Koyama1, K.Suguro, M. Yoshiki, Y.Kamimuta, M. Koike, M.Ohse, C.Hongo and A. Nishiyama1 et al., "Thermally Stable Ultra-Thin Nitrogen incorporated ZrO<sub>2</sub> Gate Dielectric Prepared by Low Temperature Oxidation of ZrN ", Tech Digest of IEDM, p.459, (2001).

- [35] R. Choi, et al., " High-Quality Ultra-thin HfO<sub>2</sub> Gate Dielectric MOSFETs with TaN Electrode and Nitridation Surface Preparation ", Symp. VLSI Tech., p.15, (2001).

- [36] Tung Ming Pan, "Robust ultrathin oxynitride dielectrics by NH<sub>3</sub> nitridation and N<sub>2</sub>O RTA treatment" IEEE Electron Device Letters, VOL. 21, NO. 8, AUGUST (2000).



- [37] Tung Ming Pan "Characterization of Ultrathin Oxynitride (18–21 Å) Gate Dielectrics by NH<sub>3</sub> Nitridation and N<sub>2</sub>O RTA Treatment" Transactions on electron devices VOL. 48, NO. 5, MAY (2001)

- [38] C.H. Chen, Y.K. Fang, C.W. Yang, Y. S. Tsair, M.F. Wang, L. G. Yao, S.C. Chen, C.H. Yu, and M.S. Liang, "The 1.3~1.6 nm oxide equivalent gate dielectrics with nitrided oxide prepared by NH<sub>3</sub> nitridation and post-deposition rapid thermal annealing for 0.1μ m and beyond CMOS technology application", Solid State Electronics (SSE), vol. 46, p. 539-544, (2002)

[39] C. T. Liu, E. J. Lloyd, T. Ma, M. Du, R. L. Opila, and S. J. Hillenius, “High performance 0.2um CMOS with 25Å gate oxide grown on nitrogen implanted silicon,”

[40] S. C. Song, H. F. Luan, C. H. Lee, A. Y. Mao, S. J. Lee, J. Gelpey, S. Marcus, and D. L. Kwong, “Ultra thin high quality stack nitride/oxide gate dielectrics prepared by in-situ rapid thermal N<sub>2</sub>O oxidation of NH<sub>3</sub>-nitrided Si,” VLSI Technol. Syst. Applica., pp. 78–81, (1999)

[41] W. Hei, Poon, V. M. C., C.W. Kok, P. J. Chan, V. A. Gritsenko, “Interface structure of ultrathin oxide prepared by N<sub>2</sub>O oxidation,” IEEE Trans. Electron Devices, vol. 50, p.1941, (2003)

