Chapter 1

Introduction

1.1 General Background

Metal-Oxide-Semiconductor Field-Effect transistor devices were proposed in 1960, the semiconductor industry had rapidly developed over four decades. The CMOS technology is main stream and plays a important role in the semiconductor due to lower standby power consumption and scaling properties. The digital circuits can be implemented completely with complementary MOSFET. As demands for electronic products increases, the silicon based integrated circuits had grown exponentially because silicon has a native oxide that is silicon dioxide. The quality of insulator layer will be major concern. According to the famous Moore's law [1], the numbers of transistors in a chip doubles every 2 or 3 years or device line features decreased at the rate of 70% every three years, and cost per function has decreased at the rate about 30% per year [2].

Driving current of the MOSFET I_{ds} can be well modeled by following equation:

$$I_{ds}=\frac{1}{2}uC_{OX}\frac{W}{L}(V_{gs}-V_t)^2$$

the term $(V_{gs}-V_t)$ is difficult to reduce because operating voltage was gradually decreased to approach lower power consumption. To achieve high performance and promote driving current, the gate length and oxide thickness continue scaling down. The barriers of gate length shrinkage are lithography limited and short channel effects. Thermal silicon dioxide has low surface trap density and low interface state density. The scaling of SiO_2 based dielectrics is no longer a practical choice when the oxide

thickness drops below 13 Å because of direct tunneling from the gate electrode [3]. Fig 1-1 shows the low standby power logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling. According to the 2004 ITRS roadmap, oxy-nitride can not meet the limit on gate leakage current density of low standby power logic circuit after Year 2006. The physical limitation of oxide thickness is caused by the quantum mechanical tunneling of carriers. Gate leakage current induced a problem of heat dissipation. As the operating frequency of microprocessors surpass 1GHz or more, heat dissipation becomes a serious issue including package materials, devices layout, process integration and so on. Recently Intel and AMD had proposed dual core processor architecture to avoid leakage current and heat dissipation.

The replacement of silicon dioxide as a gate insulator in MOS devices by materials of higher dielectric permittivity ε_r is motivated by the need of increasing the capacitance density without further reducing the physical thickness. Despite a considerable effort in this direction, the formation of a thin SiO_2 interlayer between silicon substrate and the high-k material appears to be unavoidable [4]. Most of high-k materials are not stable in direct contact with silicon and require a thin SiO_2 layer to stabilize the dielectric film on silicon substrate. Thin SiO_2 layer can improve interface states, surface roughness and electron mobility. The use of dielectric layers with high-k will give us thicker films with equivalent SiO_2 electrical thickness, and should allow us to reduce the leakage current and improve the reliability of the gate dielectric layer. Currently many experimental efforts are to investigate for alternative gate dielectric materials. Many metal oxides such as TiO_2 [5], Al_2O_3, Ta_2O_5, ZrO_2, HfO_2, La_2O_3, Y_2O_3, [6-19]etc and ferroelectric materials (e.g., PZT [20], BST, etc.) are being investigated as candidate material to replace silicon dioxide. The required material properties of alternative gate oxide can be summarized as follows.

1. Dielectric constant significantly larger than 3.9 in thin film phase.
2. Thermodynamic stability in direct contact with silicon .
3. Low diffusion constant for dopant atoms in poly-Si.
4. Large bandgap with more than 1 eV tunneling barrier for both electrons and holes in order to achieve low leakage current.
5. Low interface trap defect density, Dit $\leqq 10^{10}$-10^{11} $cm^{-1}eV^{-1}$.
6. Low defect density within oxide layer.
7. Preferably stable amorphous phase to avoid grain boundary problem.

Table 1-1 illustrates Material requirement of high-k dielectrics. For most high-k materials, the higher dielectric constant comes at the expense of narrow band gap. The lower barrier height for tunneling tend to compensate the benefit of the higher dielectric constant. Even though there are many materials with significantly high k values, many of them are not suitable for gate dielectric applications since they do not satisfy several of these necessary conditions. For example, TiO_2 has a higher k value of 80-100 but has a small bandgap of 3.5 eV and band offset of 0.05 eV. Most other ferroelectric materials such as $SrTiO_3$ with very high dielectric constants have the same problem of small potential barrier.[21] Table 1-2 shows material properties comparison of Al_2O_3, ZrO_2 ,HfO_2.

High-k oxide film have been deposited by a variety of methods, including atomic layer deposition chemical vapor deposition (ALDCVD), physical vapor deposition (PVD), metallic organic chemical vapor deposition (MOCVD), RF and DC sputter, photo-assisted CVD, Jet CVD, electrochemical deposition, etc. The main consideration which high-k materials are applied on manufacture is throughput, uniformity and cost. High-k materials which replace silicon dioxide are avoidable, but it is not clear that what method of high-k film deposition will be the main stream and adopted on manufacture.

1.2 Motivation

Over the last decades, the minimum feature size of microelectronic devices has been continuously reduced. As the device scaling continues down to deep submicron scales, fundamental physical limits of device materials are becoming critical barrier. Recently, aluminum oxide and hafnium oxide had been proved as promising candidates for the gate dielectrics due to their higher dielectric constant, superior thermal stability, and leakage current by order of magnitude, but encountered the integrated issues such as charge trapping shifted the flat band and mobility degradation.

From the high-k standpoint, Al_2O_3 is inferior to HfO_2 and ZrO_2 (k~25). Despite this, the Al_2O_3 dielectric is an extremely promising candidate in terms of its chemical and thermal stability as well as its high barrier offset. The energy band gap of Al_2O_3 is about 8.3 eV, which is higher than HfO_2, ZrO_2, Ta_2O_5. Band alignment determines the barrier height for electron and hole tunneling from gate or silicon substrate. For SiO_2, the energy band gap is almost 9 eV, and the barrier height of electron is 3.1 eV and the barrier height of hole is 4.5 eV. The barrier height of Al_2O_3 for electron and hole is 2.9 eV and 4.3 eV, respectively. Al_2O_3 is possessed of high free energy of reaction with Si (64.4 kcal/mole) and high heat of formation (399 kcal/mole). The energy band gap of HfO_2 is about 6.02 eV, which is higher than Si_3N_4, TiO_2, Ta_2O_5. The barrier height of HfO_2 for electron and hole is 1.6 eV and 3.3 eV, respectively.

Of particular interest is its compatibility with the conventional process of integrating complementary metal oxide semiconductor, which involves high temperatures above 1000℃. Consequently, high–k materials having a high

crystallization temperature are best for this process to suppress leakage current. The Al_2O_3 gate dielectric has already been integrated in sub-100nm FETs [22][23].

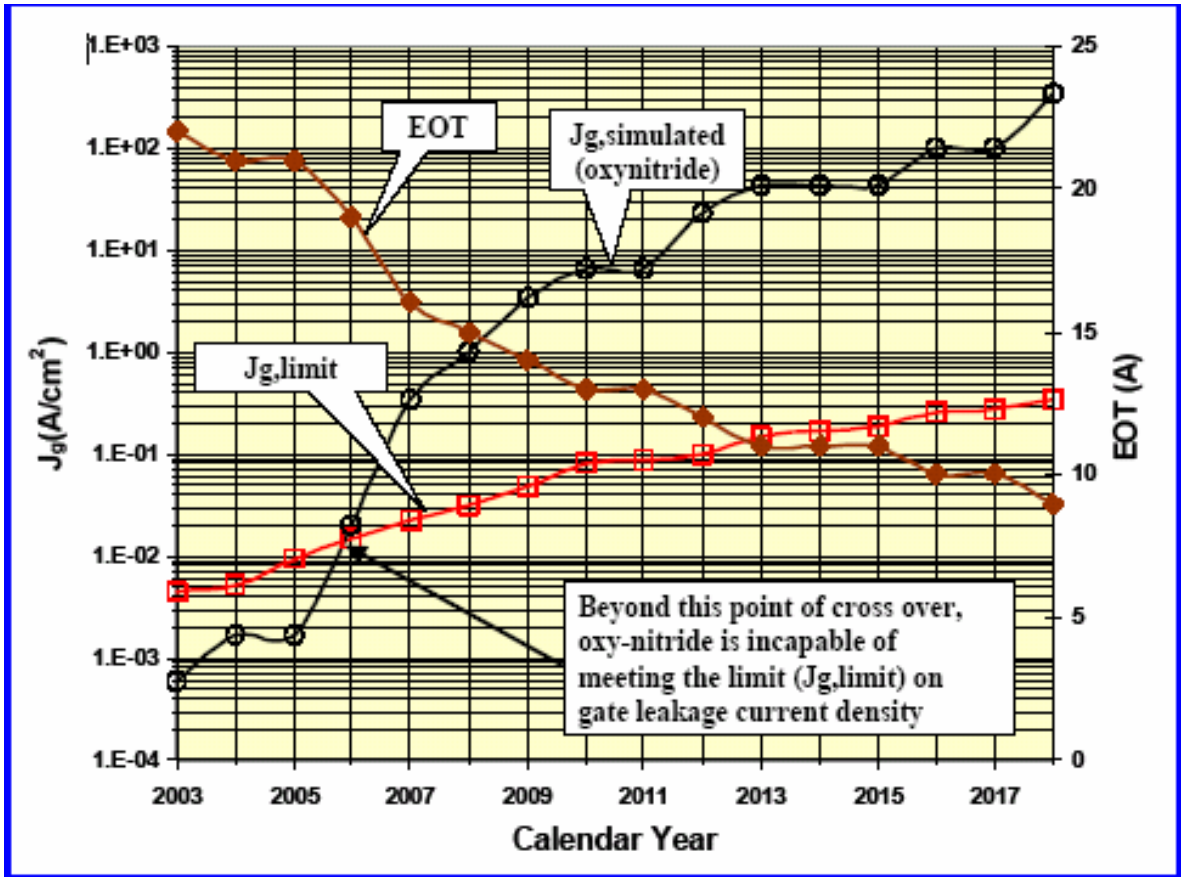

Fig. 1-1: LSTP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling.

Criteria	Requirements
EOT scalability <10Å	Dielectric constant > 15
Negligible FIBL effect	Dielectric constant < 60
Leakage current < 1 A/cm2 @ 1V	Bandgap > 5 eV Barrier height > 1 eV
Thermal stability	No silicidation and reduction
Hysteresis	< 20 mv
Dispersion	< 1 %/decade
Interface state density	< 1011 /eVcm2
Mobility	> 85 % of SiO2
Reliability	> 10 years

Table 1-1: Material requirements of high-k dielectrics

Aspect	Property		
	Al_2O_3	ZrO_2	HfO_2
Bandgap (eV)	8.3	5.82	6.02
Barrier Height to Si (eV)	2.9	1.5	1.6
Dielectric Constant	8-11.5	~25	~30
Dielectric Strength (MV/cm)	>1.0		2-4.5
Heat of Formation (Kcal/mol)	399	261.9	271
ΔG for Reduction ($MO_x + Si \rightarrow M + SiO_x$)	64.39	42.326	47.648
Thermal expansion coefficient ($10^{-6}K^{-1}$)	6.7	7.01	5.3
Lattice Constant (Å) (5.43 Å for Si)	4.7-5.2	5.1	5.11
Self Diffusion Coefficient @ 900℃	1.5048×10^{-7}	6.0009×10^{-10}	2.8227×10^{-17}

Table 1-2: Material properties comparison of Al_2O_3, ZrO_2 ,HfO_2