國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

次世代快閃記憶體之氨氣氮化底多晶矽上多晶矽層間高介電常數介電質特性

Characteristics of the Inter-Poly High-κ Dielectrics on NH_3-Nitrided Bottom Poly-Si for Next Generation Flash Memories

研 究 生：李宗翰 Tsung-Han Li

指導教授：羅正忠 博士 Dr. Jen-Chung Lou

中華民國九十四年六月

次世代快閃記憶體之氨氣氮化底多晶矽上
多晶矽層間高介電常數介電質特性

Characteristics of the Inter-Poly High-κ Dielectrics on NH_3-Nitrided Bottom Poly-Si for Next Generation Flash Memories

研 究 生：李宗翰　　Student : Tsung-Han Li

指導教授：羅正忠 博士　　Advisors : Dr. Jen-Chung Lou

國 立 交 通 大 學
電子工程學系 電子研究所
碩 士 論 文

A Thesis
Submitted to Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of
Master of Science
in Electronic Engineering
June 2005
Hsinchu, Taiwan, Republic of China

中華民國 九十四 年 六 月

次世代快閃記憶體之氨氣氮化底多晶矽上

多晶矽層間高介電常數介電質特性

研究生：李宗翰　　　　　　　　　　　　　　指導教授：羅正忠 博士

國立交通大學　電子工程學系　電子研究所

摘要

隨著系統晶片（SOC）的發展，持續降低互補式金氧半（CMOS）場效電晶體元件中的閘極介電層及非揮發性記憶體（non-volatile memories）中的複晶矽層間介電層（inter-poly dielectric）厚度以提高元件密度及降低操作電壓變得十分重要。為了滿足以上的需求並獲得較低的漏電流及較高的可靠度，利用高介電常數材料（high-κ）來取代二氧化矽（SiO_2）變成是不可或缺的趨勢。

本篇論文研究沉積後高溫退火（post-deposition annealing）溫度對有機金屬化學氣相沉積（metal organic chemical vapor deposition）之高介電常數材料三氧化二鋁（Al_2O_3）及二氧化鉿（HfO_2）複晶矽層間電容的影響。實驗結果顯示，對三氧化二鋁及二氧化鉿複晶矽層間電容，不論是漏電流、電子捕捉率或崩潰電荷，900°C和 800°C分別是最佳化條件。因此，等效氧化層厚度為 5 奈米及 3 奈米的三氧化二鋁和二氧化鉿將是45奈米及32奈米世代以下堆疊式快閃記憶體的絕佳候選複晶矽層間介電質。

Characteristics of the Inter-Poly High-κ Dielectrics on NH_3-Nitrided Bottom Poly-Si for Next Generation Flash Memories

Student : Tsung-Han Li Advisors : Dr. Jen-Chung Lou

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

Abstract

For the system-on-chip (SOC) application, a continuously scaling of the gate dielectrics for complementary metal oxide semiconductor (CMOS) and inter-poly dielectrics (IPDs) for electrically-erasable programmable read-only-memory (EEPROM) and stacked-gate flash memory is needed to obtain high density and low operation voltage. To meet the above requirements and exhibit low leakage current as well as good reliability, the replacement of high-κ materials for SiO_2 have become indispensable.

In this thesis, we investigated the effects of post-deposition annealing (PDA) temperature on the electrical properties and reliability characteristics of metal-organic chemical vapor deposition (MOCVD) aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) inter-poly capacitors. For Al_2O_3 and HfO_2 inter-poly capacitors, samples

exhibit optimal quality in terms of leakage current, electron trapping rate and charge-to-breakdown (Q_{BD}) when annealed at 900°C and 800°C respectively. As thin as 5nm and 3nm equivalent oxide thickness (EOT) of Al_2O_3 and HfO_2 IPD is suitable to meet the requirement of 45nm and 32nm generation stacked-gate flash memories respectively.

誌　謝

兩年的碩士生涯終於在認真忙碌的學習與同學的歡笑聲中結束了，首先要感謝我的指導教授羅正忠博士，在老師諄諄教誨與勉勵之下，讓我在做人做事與學術研究上都有了受益終身的收穫與啟發，特此向羅老師呈上最衷心的感謝。另外要特別感謝陳永裕、陳世璋、謝文斌三位學長，謝謝你們在學業與專業研究上提供這許許多多的指導與協助，在生活中如兄長般的照顧與關愛更讓我感到無比的溫暖，當實驗遇到困難時不遺餘力地幫我解決問題，讓我順利地完成了研究所的課業。還要感謝彥廷、祐慈、昶維、雁雅、明衡以及其他實驗室的同學，也感謝國源、佳寧還有各位學弟，兩年來大家一起努力，互相幫助，更共同擁有歡樂的時光，我知道這將是我人生中美好的回憶。在這裡也要對國家奈米實驗室以及裡面勞苦功高的研究人員、工程師們致上深深的謝意，因為你們熱心地提供專業的意見與幫助，讓實驗能順利的進行。

最後要對我的父母、家人說聲謝謝，這麼多年來，你們總是默默耕耘，讓我沒有後顧之憂地完成我的學業，雖然你們從未提起片言隻字，卻讓我深深體會到這份親情的可貴與感動，謝謝你們。

Contents

Abstract (in Chinese) I

Abstract (in English) II

Acknowledgements IV

Contents V

Table Captions VII

Figure Captions VIII

Chapter 1 Introduction 1

1.1 Background 1

1.2 Motivation 4

1.3 Organization of the Thesis 8

Chapter 2 Effects of PDA Temperature on the Electrical Properties of Al_2O_3 IPD with NH_3 nitridation 13

2.1 Introduction 13

2.2 Experimental Details 14

2.3 Results and Discussions 15

2.3.1 Basic Electrical Properties 15

2.3.2 Electric Field and Leakage Current Density Characteristics 16

2.3.3 Reliability Characteristics 16

2.4 Summary 18

Chapter 3 Effects of PDA Temperature on the Electrical Properties of HfO_2 IPD with NH_3 nitridation ………………………………………... 27

3.1 Introduction 27

3.2 Experimental Details 29

3.3 Results and Discussions 30

3.3.1 Basic Electrical Properties 30

3.3.2 Electric Field and Leakage Current Density Characteristics 30

3.3.3 Reliability Characteristics 31

3.4 Summary 32

Chapter 4 Conclusions and Recommendations for Future Works ………….. 43

4.1 Conclusions 43

4.2 Recommendations for Future Works 44

References 46

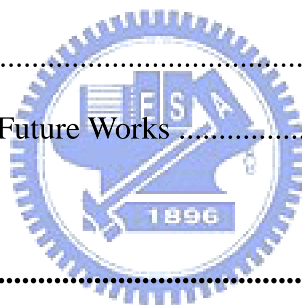


Table Captions

Chapter 1

Table 1.1 Materials properties of high-κ dielectrics, Al_2O_3, ZrO_2 and HfO_2

Table 1.2 Comparisons of deposition technique: sputtering, ALD, MOCVD and MBE

Chapter 2

Table 2.1 EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values of the Al_2O_3 inter-poly capacitors with surface NH_3 nitridation under positive and negative CCS at various PDA temperatures in N_2 ambient

Chapter 3

Table 3.1 EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values of the HfO_2 inter-poly capacitors with surface NH_3 nitridation under positive and negative CVS at various PDA temperatures in N_2 ambient

Chapter 4

Table 4.1 Comparison of 800ºC PDA HfO_2 IPD and 900ºC PDA with 900ºCPEA Al_2O_3 IPD samples in terms of EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values

Figure Captions

Chapter 1

Fig. 1.1 Scaling limits of various gate dielectrics as a function of the technology specifications for low stand-by power technologies.

Fig. 1.2 Leakage current density and EOT projection of nitrided oxides from ITRS roadmap 2004 update.

Fig. 1.3 A schematic diagram of typical MOCVD system structure.

Chapter 2

Fig. 2.1 Cross-sectional view of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 2.2 Key process steps of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 2.3 (a) *C-V* curves and (b) *J-E* characteristics of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 2.4 The Weibull distributions of the effective breakdown field of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities.

Fig. 2.5 The Weibull distributions of the leakage current density of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities as the gate bias is 6MV/cm.

Fig. 2.6 (a) Q_{BD} Weibull distributions and (b) the corresponding curves of gate voltage shift of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures when CCS of 5mA/cm^2 is applied in positive polarity.

Fig. 2.7 (a) Q_{BD} Weibull distributions and (b) the corresponding curves of gate voltage shift of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures when CCS of 5mA/cm^2 is applied in negative polarity.

Fig. 2.8 Band diagrams of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation under (a) positive and (b) negative gate voltage biased to the Poly-II.

Chapter 3

Fig. 3.1 Band alignment of typical high-κ dielectrics.

Fig. 3.2 Cross-sectional view of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 3.3 Key process steps of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 3.4 (a) *C-V* curves and (b) *J-E* characteristics of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 3.5 Equivalent oxide thickness of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 3.6 Comparison of EOT between Al_2O_3 and HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

Fig. 3.7 The Weibull distributions of the effective breakdown field of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities.

Fig. 3.8 The Weibull distributions of the leakage current density of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities as the gate bias is 6MV/cm.

Fig. 3.9 The Weibull distributions of the leakage current density of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities as the gate bias is 5V.

Fig. 3.10 Q_{BD} Weibull distributions of HfO_2 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures under (a) positive and (b) negative polarities.

Fig. 3.11 Curves of gate current density shift of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative constant voltage stress.

CHAPTER 1

Introduction

1.1 Background

As the scaling rule keeps going, the dimension of gate oxide for complementary metal oxide semiconductor (CMOS) has decreased dramatically for the past decade. The integrated circuit technology nowadays makes devices with high density and low operation voltage for the system-on-chip (SOC) application. To meet such requirements like high performance (speed), low static (off-state) power and a wide range of power supply and output voltages [1], we have to perform a calculated reduction of the dimensions of the fundamental active device in the circuit just like what "Moore's law" indicated, doubling the circuit density about every two or three years since 1980 [2]-[4]. And this trend results in a dramatic expansion in technology and communication markets including the market associated with high-performance microprocessor and low static-power applications, such as wireless systems. Just like what we already knew, the key element of keeping the scaling rule of Si-based metal-oxide-semiconductor field effect transistor (MOSFET) going is the materials and resultant electrically properties associated with the dielectric employed to isolate the transistor gate from the Si channel for decades: silicon dioxide (SiO_2). We can benefit several key advantages in CMOS processing including a thermodynamically and electrically stable high-quality Si-SiO_2 interface as well as superior electrical

isolation properties by using thermally grown amorphous SiO_2 as the gate dielectric. ~10^{10} cm^{-2} defect charge density, ~10^{10} $cm^{-2}eV^{-1}$ midgap interface state density and 15 MV/cm hard breakdown field are routinely obtained and therefore expected in spite of dimensions. These outstanding electrical properties clearly present a significant challenge for any other alternative gate dielectric candidates [5], [6].

As the time past, there have been several major evolutions in silicon digital logic technology. CMOS technology became the most important digital logic technology for all IC industry, owing to its low standby power dissipation and scaling potential. The scaling of oxide thickness has long been recognized as one of determinant factor for devices scaling. High driving current and thereby improved performance can be achieved by reducing the oxide thickness. At the current rate of progressing, Fig. 1.1 indicates the imperative need for a nitrided oxide (SiO_xN_y) and high dielectric constant (κ) gate dielectrics for low standby power application after the year 2002 and 2006, respectively [7]. However, the direct tunneling current increases exponentially by about one order of magnitude for every 0.2nm ~ 0.3nm reduction in oxide thickness. This additional leakage current not only causes increased power dissipation but also affect the circuit functionality due to the decreased operation margins.

For this reason, several alternative materials for silicon dioxide are currently being investigated. Ultrathin nitrided oxides are, at this moment, the best choices to replace pure SiO_2 [8]-[14]. Figure 1.2 shows the expected equivalent oxide thickness (EOT) trends from the published 2004-ITRS roadmap. It indicated that nitrided oxides can extend SiO_2 limitation to 2006 without massive change in production technologies. Nitrided oxides have several properties superior to those of conventional thermal SiO_2, and it deserves to mention the suppression of boron penetration from the poly-Si gate and enhanced reliability. Nitrogen also reduces hot-electron-induced degradation [15].

The dielectric constant of the oxynitride increases linearly with the percentage of nitrogen from κ (SiO_2) = 3.9 to κ (Si_3N_4) = 7.8 [16], though one should note that most SiO_xN_y films grown currently by thermal methods are lightly doped with N (< 10 at.%) and therefore have a dielectric constant only slightly higher than that of pure SiO_2. The other potential candidates to replace silicon dioxide are high-κ materials, including aluminum oxide (Al_2O_3), hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) etc [17]-[20]. The most important advantage of high-κ dielectric is the several orders reduction of magnitude of leakage current compared to SiO_2 at the same EOT. However, in device performance point of view, a suitable gate dielectric candidate should also meet the other requirements, including high thermal stability, high carrier mobility, small oxide charges, good stress immunity and CMOS compatible.

On the other hand, high-κ dielectrics are paid much attention on the flash memory applications [21]-[27].The thickness of inter-poly dielectric (IPD) and tunnel dielectric (TD) in stacked-gate flash memory had met intrinsic limitation [28]. It is not sufficient to meet the stringent data retention requirement of IPD while applying thermal or CVD oxynitride technologies due to the unavoidable leakage current [29]-[32]. By increasing the floating gate coupling ratio, high-κ IPD can lead to a high electric field across tunnel oxide (TOX) even at very low control gate voltage. For the tunnel dielectric engineering of stacked-gate flash memories, the issue is closely related to dielectric material selection itself. Flash tunnel dielectric has two roles. One is a barrier to suppress charge leakage under read and retention. Second role is a charge transfer path. In order to avoid trap-assisted tunneling via one trap site, the minimum TOX thickness of conventional FG structure will be limit to 8 nm. This limits the tunnel SiO_2 scaling and program/erase voltage reduction. Nitrided oxides have been intensively studied, but so far only 5 to 10 times improvement for low field

leakage is achieved [33]. This is not enough, because it only achieves 1 nm reduction even with heavy nitridation.

To successfully employ the high-κ IPD and TD into flash memory, one must take charge retention issues into consideration and make sure that the barrier height (φ_B) between Si and the new adopted high-κ dielectrics should be larger than 1.5eV for effectively suppressing the loss of floating gate charges through electron thermal emission [33]. Usually, dielectrics with higher κ inherently have lower φ_B. Therefore a trade-off between dielectric constant and barrier height is inevitably required in trying to implement the high-κ dielectrics in flash memories.

1.2 Motivation

Fast low-power nonvolatile memories are required for future wireless communication products. In the recent flash memory technologies, short program/erase times and operating voltage reductions are the most important issues to realize high speed/low power operation [28], [34]-[36]. For EEPROM and flash memory devices, the IPD requires a high charge-to-breakdown (Q_{BD}), high breakdown field and low leakage current to obtain good data retention characteristics [37]-[39]. It is not sufficient to meet the stringent data retention requirement of IPD while applying thermal or CVD oxynitride technologies due to the unavoidable leakage current [29]-[32], [40]. In order to accomplish this without a trade-off between low power and high speed operations, high coupling ratio should be achieved by increasing the floating gate capacitance [34], [35], [41]-[48].

There are three different approaches can be used to increase coupling ratio. First,

decrease the IPD thickness. Oxide/nitride/oxide (ONO) multi-layered films had been extensively investigated and frequently used as the dielectric layer in the flash memory devices and other applications [49]-[51]. However, decreasing the thickness of the IPD to increase the coupling ratio may cause serious leakage and reliability problems which are fatal in the retention time of flash memories. Secondly, increase the area of the IPD capacitor. High capacitive-coupling ratio cell [41]-[43], 3-dimension inter-poly dielectric [45], and hemisphere grain [46], [47] had been proposed to effectively increase the capacitance area and lower the control gate bias. Although the coupling ratio of above mentioned cell structure could be dramatically improved, they must be fabricated with many additional process steps for fabrication such complex structures and be difficult to control well. The final approach is to increase the dielectric constant (κ) of IPD materials [22], [23], [27], [52]-[59]. Therefore, it is straightforward and effective to incorporate alternative high dielectric constant (high-κ) materials on nonvolatile memories to replace oxide/nitride/oxide IPD for increasing floating gate capacitance without increasing cell area and complexity of fabrication while suppressing charge loss. By increasing the floating gate coupling ratio, high-κ IPDs can lead to a high electric field across tunnel oxide even at very low control gate voltage.

Recently, aluminum oxide (Al_2O_3) [17], [60]-[62] and hafnium oxide (HfO_2) [20], [63]-[66] had been proved as promising candidates for the gate dielectrics of sub-0.1 μm device due to their higher κ, relatively high φ_B and superior thermal stability, shown in Table 1.1. Thanks to the high dielectric constant and high thermal stability, Al_2O_3 and HfO_2 are suitable to be integrated into stacked-gate flash memories. Nonetheless, the effects of these kinds of high-κ dielectrics on flash memories are seldom investigated. To further realize the dielectric properties of these

high-κ dielectrics, some reliability issues such as breakdown field, charge trapping and temperature-dependence behaviors are extensively studied for both gate dielectric and flash memories applications.

Many deposition methods such as physical vapor deposition (PVD), metal-organic chemical vapor deposition (MOCVD), atomic layer chemical vapor deposition (ALCVD) [67], [68], and molecular beam epitaxial method (MBE), etc. have been employed to prepare high-κ IPDs. The pros and cons of each deposition techniques are demonstrated in Table 1.2. For industrial application, PVD and MBE are not appropriate tools for high-κ film deposition. Since MOCVD has the advantage of superior step coverage, high deposition rate, good controllability of composition, excellent uniformity of film thickness over large area, we, therefore, choose the MOCVD technology as our tool to deposit thin high-κ IPDs. A detail schematic structure is shown in Fig. 1.3. The MOCVD chamber is equipped with a turbomolecular pump and a liquid injection system, which has four independent-controlled injectors. The latter is consisted of a liquid pump to pump the precursors through a hot nickel frit with a proper rate because the pump is unreliable at low pump rates. The vapors are carried with a 200sccm flow of Ar to a gas distribution ring which is located at a proper distance from the substrate. In contrast to the conventional bubble system, the liquid injection is with sufficient temperature window to alleviate the thermal aging of the precursor. This is because the precursor remains in liquid state at room temperature until it is pumped into the vaporizer and injected into the deposition chamber. However, the precursor should be kept at long-term chemical stability in solvent and non-reactive with other precursors solvent [69], [70]. The components of the vaporizer, the gas ring and the connecting tube are maintained at a temperature of 190°C with heating tapes and blankets, while the

substrate temperature is controlled at 500ºC with quartz-halogen lamps and a thermocouple. A rotating suspensor is used for uniform heating during processing. A flow of 100sccm N_2 is maintained throughout the deposition cycle. The base pressure of the MOCVD chamber is ~10^{-8}Torr. The deposition pressure of the deposition is at the 5mTorr where the gas-phase collisions are scarce.

As many reports indicated, the direct contact of high-κ materials and Si-substrate will be imperfect and debatable. The dominance of the Si MOSFETs over competing technologies has largely been attributed to the high quality of thermally grown SiO_2 and the resulting Si/SiO_2 interface [71]. The Si/SiO_2 interface is known to have a very low density of interface states (D_{it}~2×10^{10} ststes/cm^2) arising from unsaturated surface bonds and other electrically active imperfections [71]. Interface states lead to degradation of on-current, since carrier mobility is limited by scattering at the interface due to the strong vertical electric field present in the channel. For maintaining the excellent transport properties at the Si interface, a possible method to suppress the interfacial layer thickness is to passivate the Si surface before the high-κ IPD deposition. Generally, there are many methods to passivate the Si surface such as surface nitridation, nitrogen-contained ambient annealing, or nitride deposition as the bottom layer. Nitridation of the Si surface using NH_3 treatment before the deposition of high-κ materials has been shown to be effective in achieving the low EOT and preventing the boron penetration [72], [73]. However, this technique results in higher interface charges which leads to higher hysteresis and reduced channel mobility [74]. The NH_3 treatment would nitridize the Si surface to form a silicon nitride layer [75]-[77]. Silicon nitride is a superior barrier for H_2O and oxygen, and it can suppress oxygen to diffuse into Si substrate [72]. After the NH_3 treatment, a thin silicon nitride (Si_xN_y) layer (~10 Å) was deposited and measured by optical measurement system (Ellipsometer). As reports, nitridation of the Si surface is prior to the deposition of

high-κ gate dielectrics and it shows the result to achieve the low EOT and increase reliability by making the interface smoother [78].

1.3 Organization of This Thesis

There are four chapters in this thesis. In chapter 1, we present a conceptive introduction to describe the background of the semiconductor technology and discuss the possible issues that we may meet during the dimension scaling down. In addition, we would concern about the hopeful solutions to overcome the physical limits in the ITRS, discuss and explain the reasons for high-κ IPD application in the nonvolatile flash memories.

In chapter 2, the effects of post-deposition annealing (PDA) temperature on inter-poly characteristics of MOCVD Al_2O_3 dielectrics are examined. The basic electrical properties, electric field, leakage current, and reliability characteristics are presented and discussed.

In chapter 3, the effects of PDA temperature on inter-poly characteristics of MOCVD HfO_2 dielectrics are examined. The basic electrical properties, electric field, leakage current, and reliability characteristics are presented and discussed.

Finally, in chapter 4, the conclusions are made and the recommendations describe the topics which can be further researched.

Table 1.1 Materials properties of high-κ dielectrics, Al_2O_3, ZrO_2 and HfO_2.

	High-κ Dielectrics		
	Al_2O_3	**ZrO_2**	**HfO_2**
Bandgap (eV)	**8.3**	**5.82**	**6.02**
Barrier Height to Si (eV)	**2.9**	**1.5**	**1.6**
Dielectric Constant	**9**	**~ 25**	**~ 25**
Heat of Formation (Kcal/mol)	**399**	**261.9**	**271**
ΔG for Reduction ($MO_x + Si \rightarrow M + SiO_x$)	**63.4**	**42.3**	**47.6**
Thermal expansion coefficient ($10^{-6}\ {}^{o}K^{-1}$)	**6.7**	**7.01**	**5.3**
Lattice Constant (Å) (5.43 Å for Si)	**4.7 - 5.2**	**5.1**	**5.11**
Oxygen Diffusivity at 950°C (cm^2/sec)	**5×10^{-25}**	**1×10^{-12}**	**$\sim10^{-12}$**

Table 1.2 Comparisons of deposition techniques: sputtering, ALD, MOCVD and MBE.

Physical Vapor Deposition (PVD)	Chemical Vapor Deposition (CVD)		Epitaxial Method
	MOCVD	ALDCVD	
Pros： 1. Convenient for new materials screening. 2. Easy to fabricate experimental data. 3. Low cost for ownership.	Pros： 1. superior step coverage. 2. High deposition rate. 3. Good controllability of composition. 4. Uniformity of film thickness over large area.	Pros： 1. Better thin film quality than PVD or CVD. 2. Excellent coverage and conformity.	Pros： 1. Permit single crystal, high-k dielectric system.
Cons： 1. Planar, line-of-sight process, damage. 2. Not likely to be used in ULSI gate process. 3. Poor conformity, especially for high aspect ratio.	Cons： 1. Hard to deposit ultra-thin films. 2. Poorer conformity than ALCVD. 3. C-, H-, OH-impurity contamination.	Cons： 1. Low throughput. 2. Mechanism-related surface sensitivity. 3. Chemistry-limited final products (only binary materials are available now.)	Cons： 1. Require submonolayer control. 2. Poor throughput for ULSI standard. 3. UHV tool and the cost of maintenance.

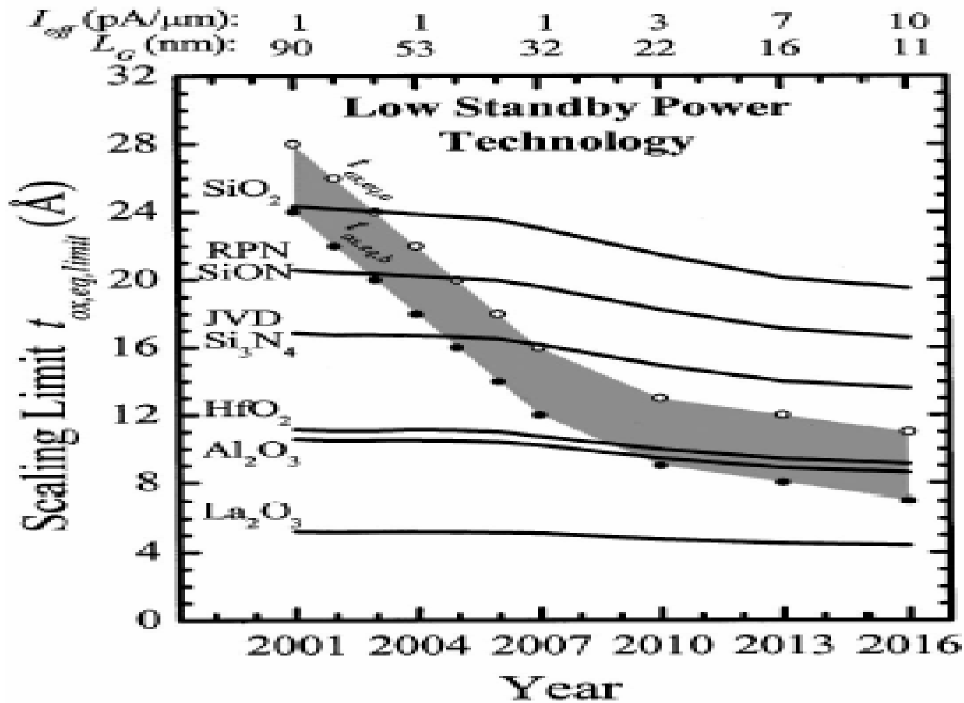


Fig. 1.1 Scaling limits of various gate dielectrics as a function of the technology specifications for low stand-by power technologies [Ref. 7].

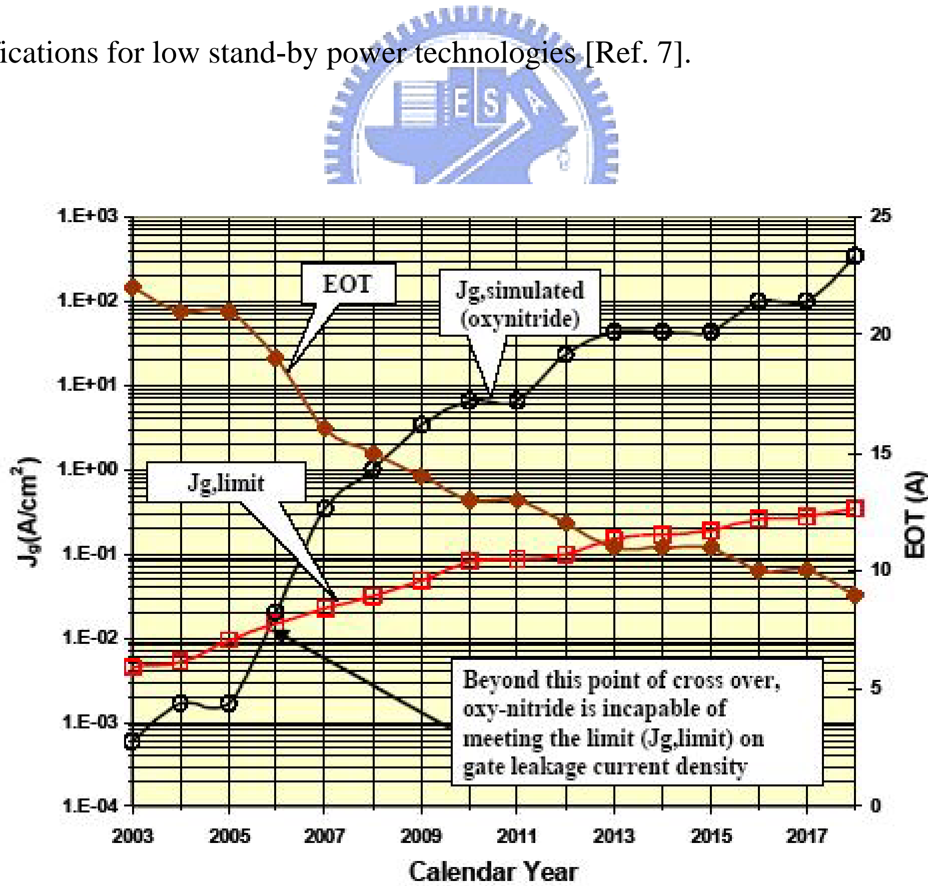


Fig. 1.2 Leakage current density and EOT projection of nitrided oxides from ITRS roadmap 2004 update.

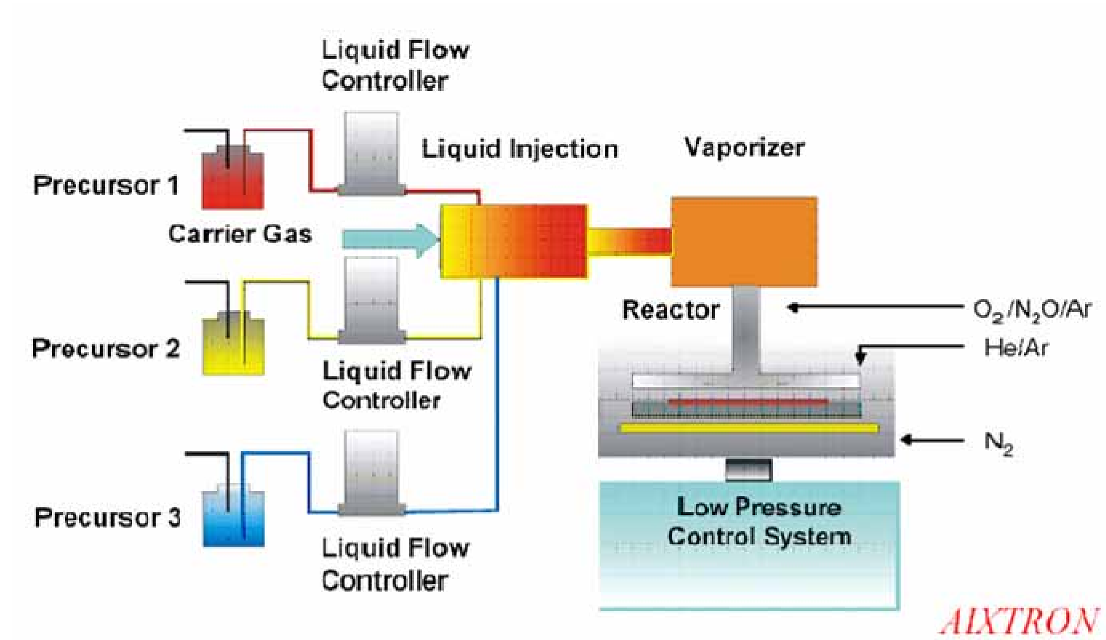


Fig. 1.3 A schematic diagram of typical MOCVD system structure.

CHAPTER 2

Effects of PDA Temperature on the Electrical Properties of Al_2O_3 IPD with NH_3 Nitridation

2.1 Introduction

With the scaling down of thickness of the inter-poly dielectrics (IPD), the quality of the dielectric becomes very critical for the application of the EEPROM and Flash nonvolatile memories. Lower leakage of the dielectric means longer data retention time. As many reports indicated that high-κ IPDs with surface NH_3 nitridation have been shown improved electrical properties [21]-[23]. Among those potential candidates, aluminum oxide (Al_2O_3) is the most attractive for IPD application in nonvolatile flash memories because of its higher conduction band offset with respect to the underlying poly-Si electrode and its higher permittivity with respect to Si_3N_4 [17], [21], [57], [71], [79], [80]. On the other hand, it is found that the incorporation of nitrogen on the bottom poly-Si surface can not only reduce leakage current by one order of magnitude, but also enhance the breakdown field and the charge-to-breakdown (Q_{BD}) as well [23]. This is ascribed to the resultant smoother interface between the dielectric and the floating gate by surface nitridation and less electron traps in the bulk [23]. However, the Q_{BD} is unfortunately quite low. Moreover, the effects of post-deposition annealing (PDA) temperature on the electrical properties

and reliability characteristics of MOCVD Al_2O_3 inter-poly capacitors with surface NH_3 nitridation are studied in this chapter. The electrical properties of the Al_2O_3 IPD are influenced by the PDA temperature. The optimum is 900ºC Al_2O_3 IPD in terms of leakage current, electron trapping rate and Q_{BD}.

2.2 Experimental Details

The n^+-polysilicon/Al_2O_3 IPD/n^+-polysilicon capacitors were fabricated on 6-inch p-type (100)-oriented silicon wafers. Silicon wafer was thermally oxidized at 950ºC to grow a 2000Å buffer oxide. 2000Å bottom polysilicon film (Poly-I) was deposited on the buffer oxide by low pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620ºC and subsequently implanted with phosphorous at 5e15cm^{-2}, 20keV, then activated with RTA at 950ºC for 30s. Prior to the growth of Al_2O_3 IPDs, the native oxide covering Poly-I was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides. The surface of Poly-I prepared in this matter was known to be contamination-free and terminated with atomic hydrogen. After being wet cleaned and dipped in HF solution, all samples were subjected to ammonia (NH_3) nitridation in the LPCVD furnace at 800ºC for 1 hour. Then, 10nm Al_2O_3 IPDs were deposited by MOCVD system at 500ºC. Annealing of Al_2O_3 IPDs was carried out by rapid thermal annealing (RTA) at temperatures ranging from 800ºC to 1000ºC in an N_2 atmosphere for 30s. Subsequently, a 2000Å top polysilicon layer (Poly-II) was deposited by LPCVD system and implanted with phosphorous at 5e15cm^{-2}, 20keV. Dopants were then activated with RTA at 950ºC for 30s. Finally, 5000Å TEOS oxide passivation and

Al metal pads were defined. It is worthy to mention that we took one of the 900ºC PDA samples annealed again at 900ºC in N_2 atmosphere followed by the dry etching step, called post-etching annealing (PEA). The cross-sectional view and key process steps of Al_2O_3 inter-poly capacitor with surface NH_3 nitridation and post-deposition nitrogen annealing are shown in Figs. 2.1 and 2.2, respectively.

The equivalent oxide thickness (EOT) was obtained from the high frequency (10 kHz) capacitance-voltage (*C-V*) measurement using a Hewlett-Packard (HP) 4284 LCR meter. The electrical properties and reliability characteristics of the inter-poly capacitors were measured using a HP4156C semiconductor parameter analyzer.

2.3 Results and Discussions

2.3.1 Basic Electrical Properties

Figure 2.3 (a) shows the high frequency *C-V* curves (10kHz) and the corresponding EOT of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation annealed at 800ºC to 1000ºC. The EOT increases as PDA temperature rising up to 900ºC, which can be ascribed to the thick interfacial layer (IL) growth. As the PDA temperature continually increases to 1000ºC, in spite of the thickest IL, Al_2O_3 film may partially crystallize and slightly increase permittivity, smaller EOT value is therefore obtained as compared to 900ºC PDA samples. However, the differences of the EOT among these samples are less than 3Å, which can be ascribed to both the effects of surface NH_3 nitridation and extremely low oxygen diffusivity of Al_2O_3 film. Figure 2.3 (b) presents the *J-E* characteristics of the Al_2O_3 inter-poly capacitors with NH_3 nitridation at various PDA temperatures under both polarities. It is found that the

large leakage current of 1000ºC PDA sample may be the proof of crystallization. We also found that 900ºC PDA with additional 900ºC post-etching annealing (PEA) sample can effectively reduce the low-field leakage current than other samples, which is helpful to suppress charge loss from the floating gate. It can be explained by the reduced damage generated by ion bombardment during the Poly-II patterning. In addition, it is worthy to mention that polarity dependence can be observed in gate leakage current curves, the leakage current in negative polarity is smaller than that in positive polarity due to asymmetric band diagram.

2.3.2 Electric Field and Leakage Current Density Characteristics

Figure 2.4 shows the breakdown characteristics of Al_2O_3 inter-poly capacitors with NH_3 nitridation at various PDA temperatures under both polarities. Effective breakdown field exhibits nearly independent on PDA temperatures. Figure 2.5 compares the Weibull distributions of the leakage current of Al_2O_3 inter-poly capacitors at various PDA temperatures with NH_3 nitridation in both polarities as the magnitude of gate bias is 6MV/cm. Once again, 1000ºC PDA sample has large leakage current caused by partially crystallization, and 900ºC PDA with 900ºC PEA sample has better performance in preventing charge loss from floating gate.

2.3.3 Reliability Characteristics

Figure 2.6 demonstrates (a) Q_{BD} Weibull distributions and (b) the corresponding curves of gate voltage shift of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures when constant current stress of $5mA/cm^2$ is applied in positive polarity. In Fig. 2.6 (a), the smaller Q_{BD} value of 1000ºC PEA sample in

positive polarity is attributed to its thicker interfacial layer. The interfacial layer becomes thicker when post-deposition annealing temperature rises, then the voltage drop across interfacial layer will increase and result in stronger electric field. The increase in the gate voltage indicates that the primary mechanism responsible for the long-term wear-out in Al_2O_3 film is the creation of electron traps under positive polarity, as shown in Fig. 2.6 (b). We also found that Al_2O_3 inter-poly capacitors annealed at 900ºC with additional 900ºC PEA exhibits smaller trapping rate than other conditions and this phenomenon indicates improved film quality ,which is consistent with the result of suppressed gate leakage current shown in Fig. 2.3. We believe that additional 900ºC post-etching annealing can reduce damage generated by ion bombardment during the Poly-II patterning and further improve Al_2O_3 inter-poly capacitors characteristics such as leakage current and stress-induced trapping rate. However, it is totally different situation in negative polarity. Figure 2.7 shows (a) Q_{BD} Weibull distributions and (b) the corresponding curves of gate voltage shift of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures when constant current stress of 5mA/cm^2 is applied in negative polarity. In Fig. 2.7 (a), although thickness of interfacial layer increases as PDA temperature rising, there is no apparent difference in Q_{BD} for negative polarity. This fact reveals that the thickness of Al_2O_3 film dominate breakdown mechanism, i.e. bulk breakdown. In Fig. 2.7 (b), hole trapping is observed, which can ascribed to the electron-hole pairs generation caused by electron impact after injection from Poly-II to Poly-I under negative bias. Then holes jumped to valence band and were trapped in the Al_2O_3 bulk when they injected back to Poly-II. Such mechanism is called anode hole injection (AHI) [81], [82]. The other mechanism for hole trapping is injection of accumulation hole of Poly-I. The similar trapping rate in negative polarity is in agreement with the result of identical charge-to-breakdown as shown in Fig. 2.7 (a). Band diagrams of Al_2O_3 inter-poly

capacitors with surface NH_3 nitridation under (a) positive and (b) negative gate voltage biased to the Poly-II are demonstrated in Fig. 2.8 (a) and (b) respectively.

2.4 Summary

The effects of PDA temperature on the electrical properties and reliability characteristics of the Al_2O_3 inter-poly capacitors with surface NH_3 nitridation are evaluated in this chapter. It was found that the electrical properties of Al_2O_3 IPD strongly depend upon the PDA temperature. 900℃ annealing is the best condition for the Al_2O_3 IPD electrical characteristics in terms of leakage current, trapping rate and Q_{BD}. Moreover, additional post-etching annealing is beneficial to improve Al_2O_3 thin film quality because it can reduce the defects generated during the Poly-II patterning. The results apparently demonstrate Al_2O_3 IPD with surface nitridation, optimized PDA temperature and another 900℃ PEA can effectively reduce charge transfer between control gate and floating gate, better retention and disturb characteristics are expected by replacing ONO IPD to Al_2O_3 IPD. The Al_2O_3 dielectric with surface NH_3 nitridation, 900℃ post-deposition and post-etching annealing thus appears to be very promising for future flash memory devices. Table 2.1 lists several physical and electrical parameters, including EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values of the Al_2O_3 IPDs with surface NH_3 nitridation annealed at various temperatures.

Table 2.1 EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values of the Al_2O_3 inter-poly capacitors with surface NH_3 nitridation under positive and negative CCS at various PDA temperatures in N_2 ambient.

PDA Temp. (°C)	EOT (Å)	E_{BD} (MV/cm)		Jg@6MV/cm (nA/cm^2)		63% QBD (mC/cm^2)	
		positive	negative	positive	negative	positive	negative
As-dep	55.6	18.4	19.1	20.4	24.5	5880	560
800	56.0	18.3	18.8	15.8	13.2	4300	570
900	57.0	18.3	18.6	13.8	13.2	6750	690
1000	56.2	18.5	19.0	490.0	2089	3800	700
900 with 900 PEA	55.5	18.0	18.8	6.0	3.1	6570	610

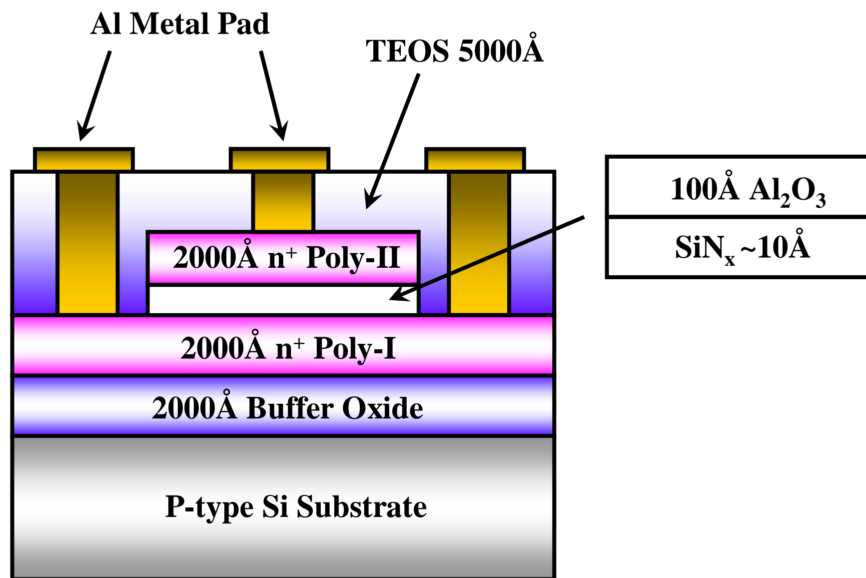


Fig. 2.1 Cross-sectional view of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

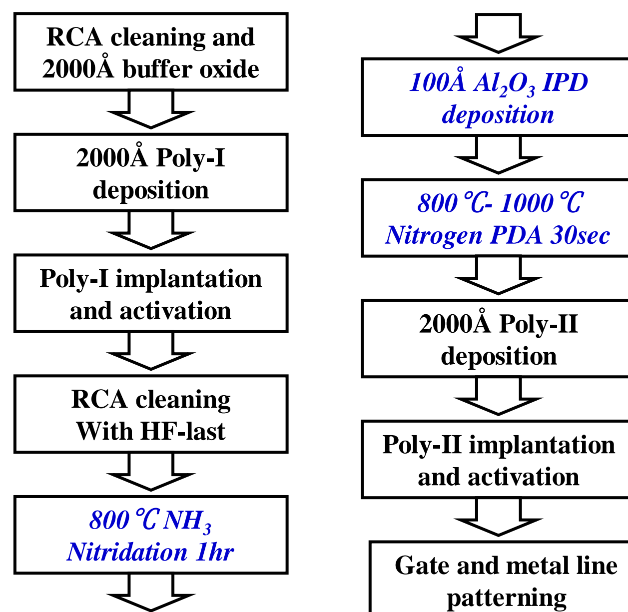
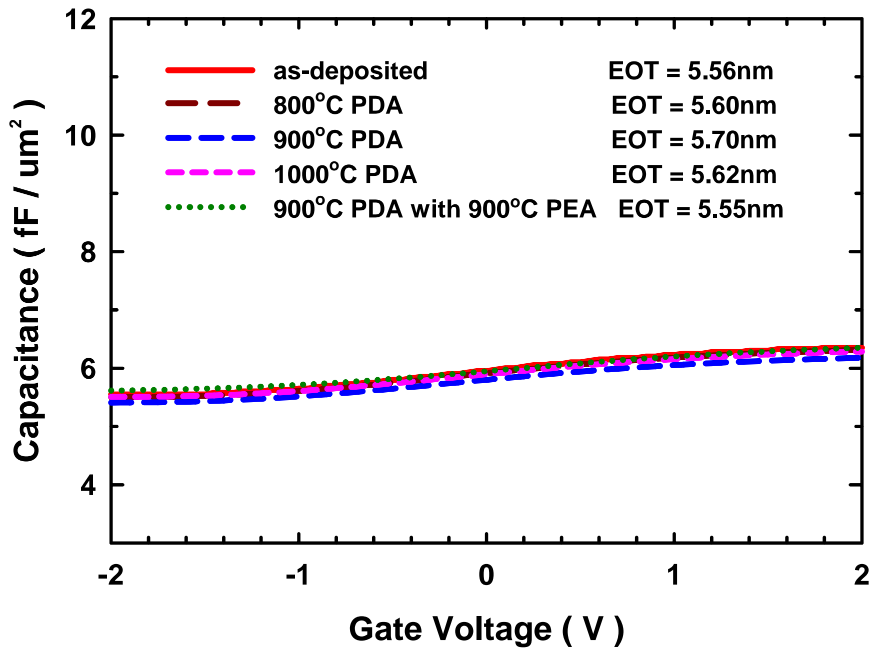
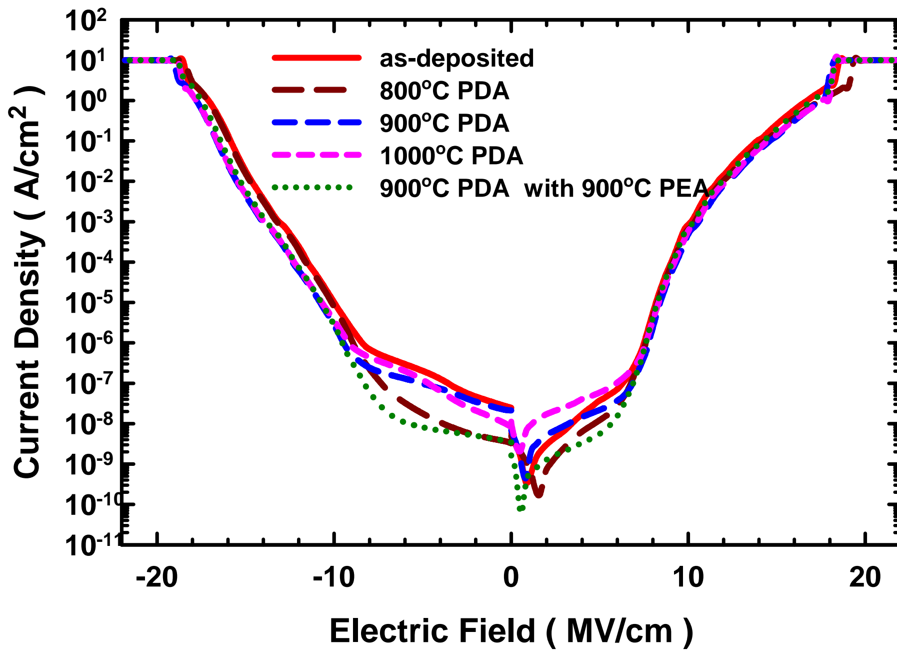


Fig. 2.2 Key process steps of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

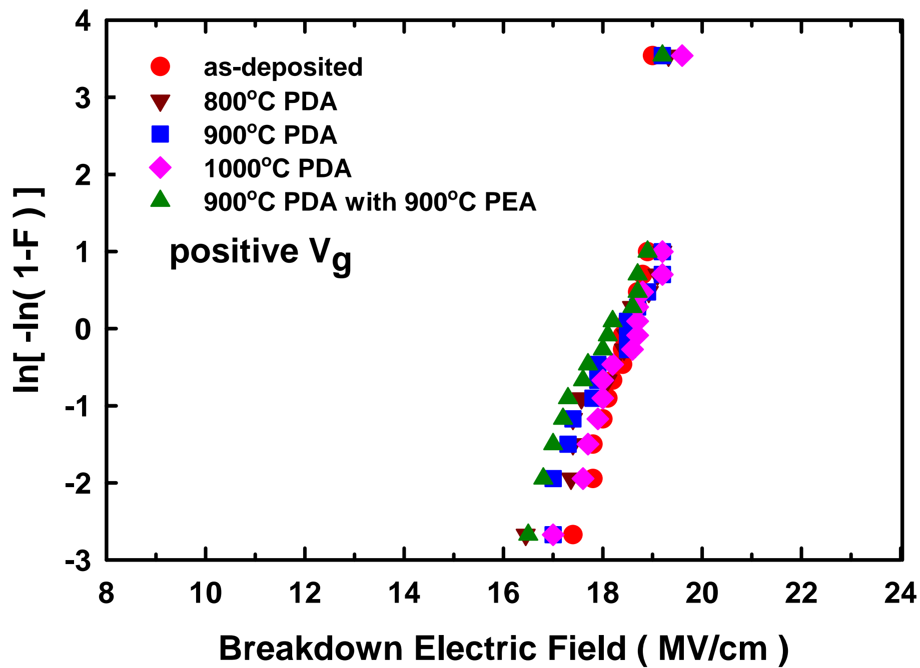


(a)

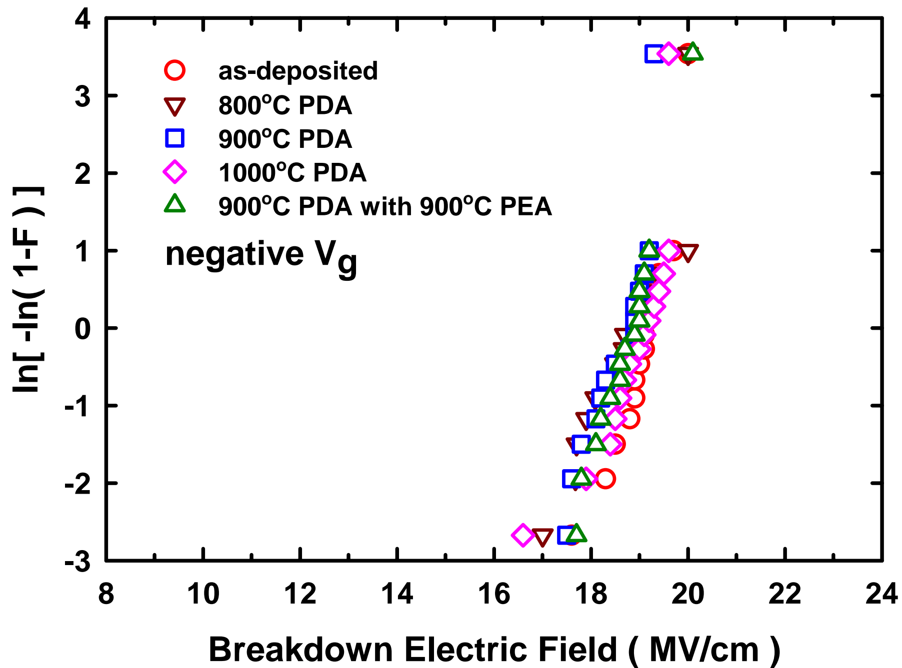


(b)

Fig. 2.3 (a) *C-V* curves and (b) *J-E* characteristics of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

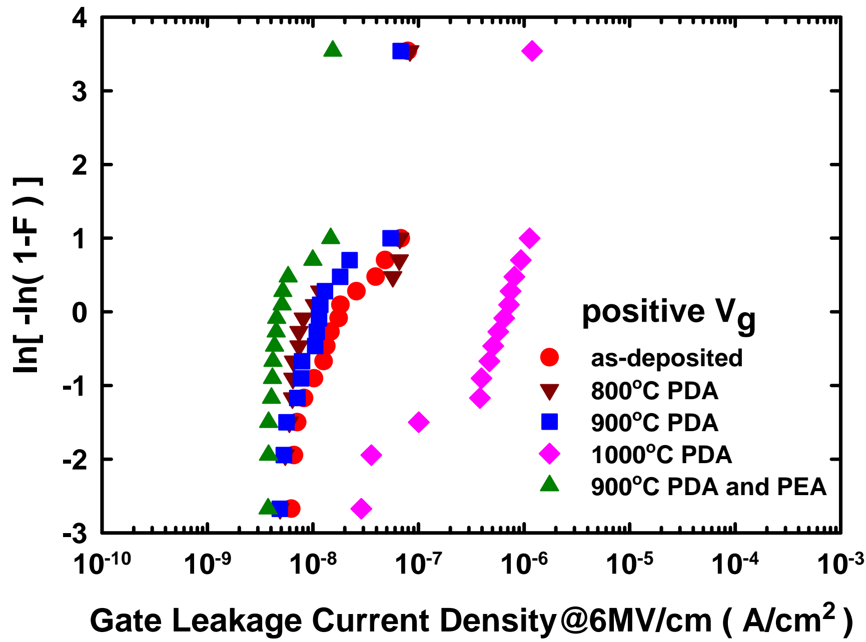


(a)

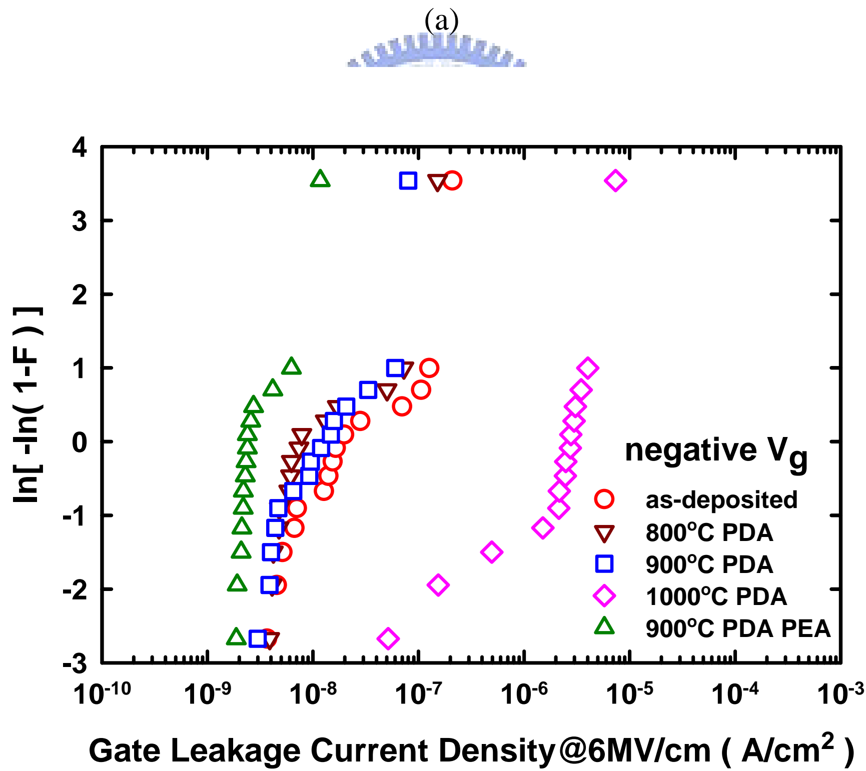


(b)

Fig. 2.4 The Weibull distributions of the effective breakdown field of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities.

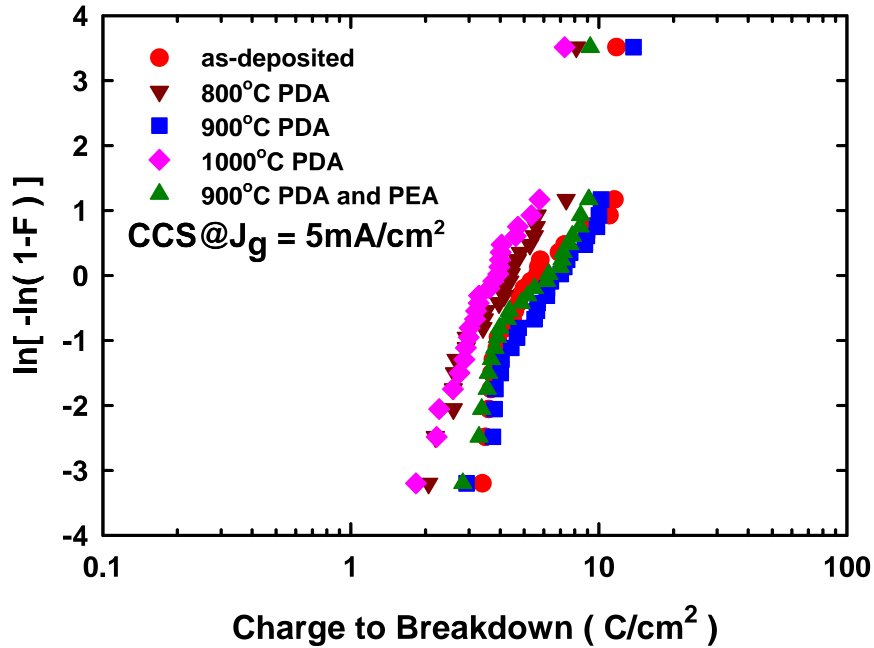


(a)

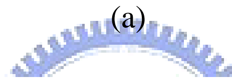


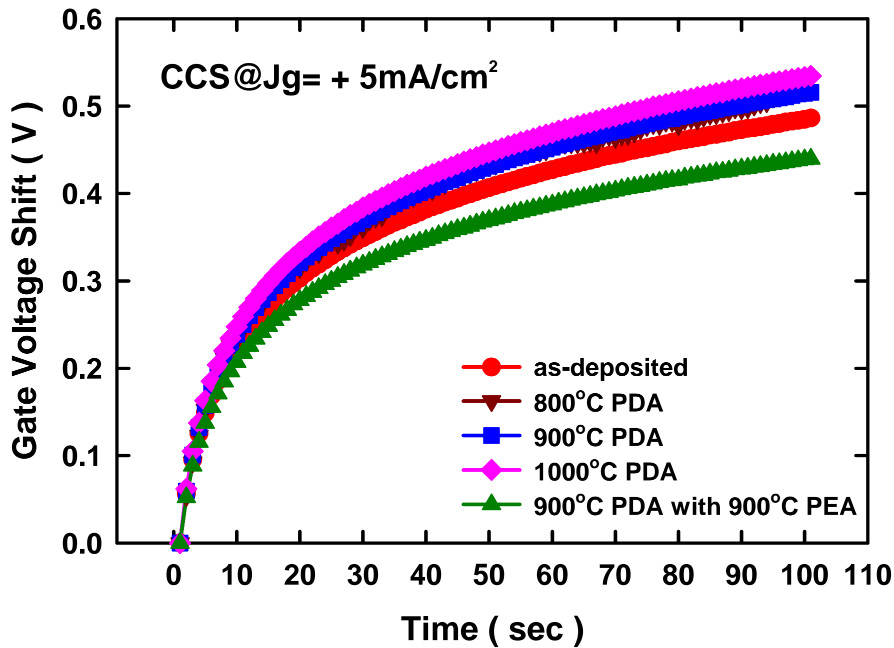
(b)

Fig. 2.5 The Weibull distributions of the leakage current density of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities as the gate bias is 6MV/cm.



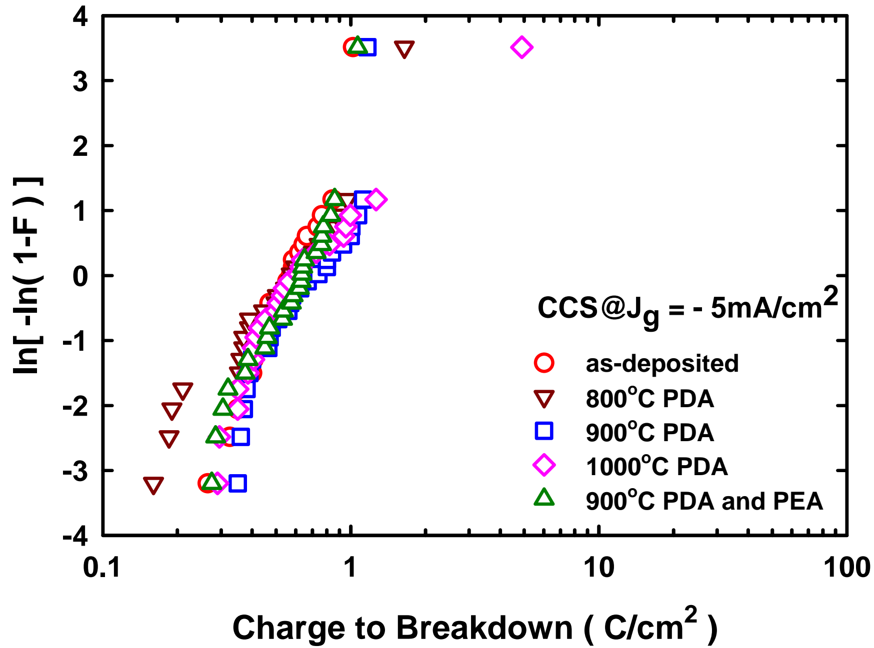
(a)



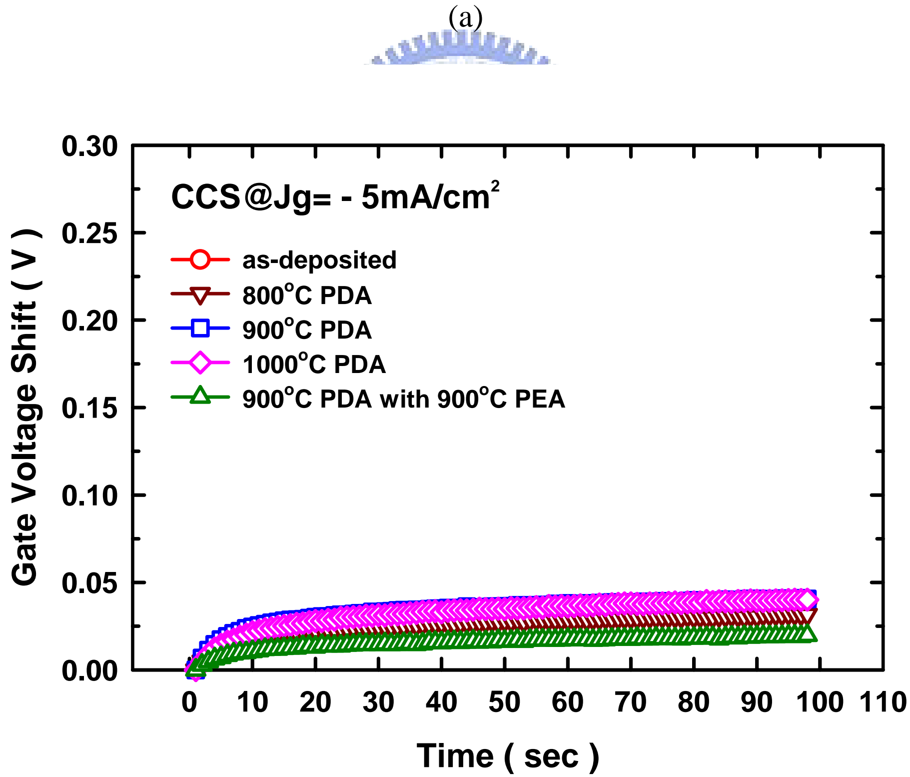


(b)

Fig. 2.6 (a) Q_{BD} Weibull distributions and (b) the corresponding curves of gate voltage shift of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures when CCS of $5mA/cm^2$ is applied in positive polarity.



(a)



(b)

Fig. 2.7 (a) Q_{BD} Weibull distributions and (b) the corresponding curves of gate voltage shift of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures when CCS of $5mA/cm^2$ is applied in negative polarity.

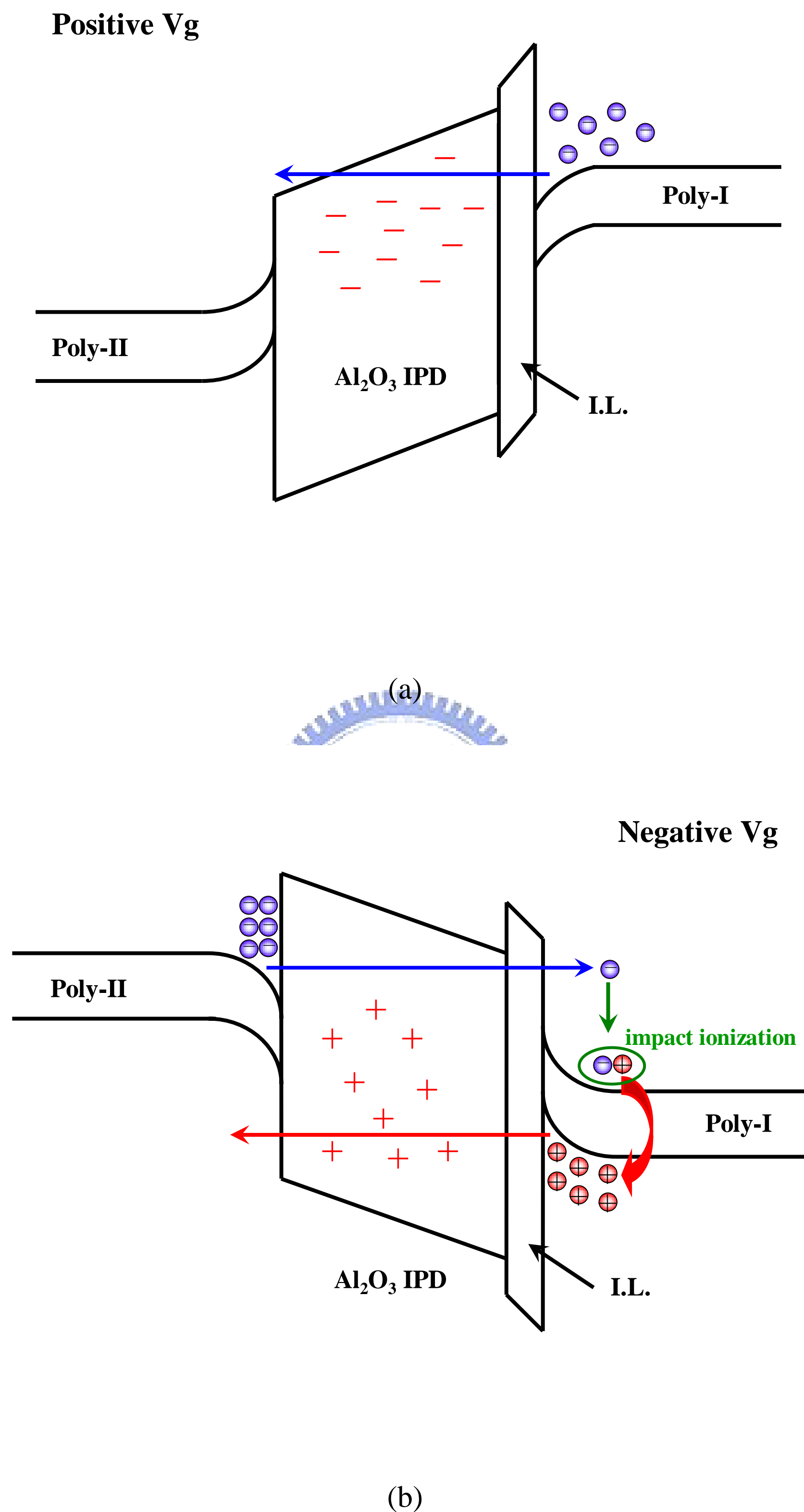


Fig. 2.8 Band diagrams of Al_2O_3 inter-poly capacitors with surface NH_3 nitridation under (a) positive and (b) negative gate voltage biased to the Poly-II.

CHAPTER 3

Effects of PDA Temperature on the Electrical Properties of HfO_2 IPD with NH_3 Nitridation

3.1 Introduction

Recently, HfO_2 has gained much attention as promising insulator. The reasons are briefly listed as follows.

(1) Suitable high dielectric constant：

The reported dielectric constant of HfO_2 is about 25~30. This magnitude of κ-value is higher than that of Si_3N_4 (κ~7) and Al_2O_3 (κ=8~11.5). It is not high enough to induce severe fringing-induced barrier lowering effect.

(2) Wide bandgap：

In general, as the dielectric constant increases, the bandgap decreases. The narrower bandgap would increase leakage current through thermal emission. The energy bandgap of HfO_2 is about 5.68eV, which is higher than the other high-κ materials such as ZrO_2, Si_3N_4 and Ta_2O_5.

(3) Acceptable band alignment：

Band alignment determines the barrier height for electron and hole tunneling

from gate or Si substrate. For SiO_2 the band offset of conduction band and valence band is ~9eV, and the barrier height for electrons is 3.1eV and the barrier height for holes is 4.7eV. The high band offset for both electron and hole has the benefit of low leakage current. Figure 3.1 shows the calculated band offsets for most high-κ dielectrics [83]. For HfO_2, barrier height for electron and hole is 1.6eV and 3.3eV, respectively. This band alignment is acceptable for nonvolatile memory requirement and better than other high-κ materials such as Ta_2O_5 [33].

(4) High free energy of reaction with Si：

For HfO_2, the free energy of reaction with Si is about 47.6 kcal/mole at 727ºC (see Table 1.1), which is higher than that of TiO_2 and Ta_2O_5. Therefore, HfO_2 is a more stable material on Si substrate as compared to TiO_2 and Ta_2O_5.

(5) High heat of formation：

Among the elements in IVA group of the periodic table (Ti, Zr, Hf), Hf has the highest heat of formation (271 kcal/mole). Unlike other silicides, the silicide of Hf can be easily oxidized. And it means that Hf is easy to be oxidized to form HfO_2 and the oxide of Hf is usually stable on Si substrate.

(6) Superior thermal stability with poly-Si：

Unlike ZrO_2, HfO_2 shows a good thermodynamic stability with poly-Si [84], [85]. The HfO_2 would not react easily with poly-Si in high temperature as ZrO_2 [86].

According to these profits discussed above, we choose HfO_2 as one of the major high-κ IPDs in our investigation for next decade flash memories.

3.2 Experimental Details

The n^+-polysilicon/HfO_2 IPD/n^+-polysilicon capacitors were fabricated on 6-inch p-type (100)-oriented silicon wafers. Silicon wafer was thermally oxidized at 950ºC to grow a 2000Å buffer oxide. 2000Å bottom polysilicon film (Poly-I) was deposited on the buffer oxide by low pressure chemical vapor deposition (LPCVD) system using SiH_4 gas at 620ºC and subsequently implanted with phosphorous at 5e15cm^{-2}, 20keV, then activated with RTA at 950ºC for 30s. Prior to the growth of HfO_2 IPDs, the native oxide covering Poly-I was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides. The surface of Poly-I prepared in this matter was known to be contamination-free and terminated with atomic hydrogen. After being wet cleaned and dipped in HF solution, all samples were subjected to ammonia (NH_3) nitridation in the LPCVD furnace at 800ºC for 1 hour. Then, 10nm HfO_2 IPDs were deposited by MOCVD system at 500ºC. Annealing of HfO_2 IPDs was carried out by rapid thermal annealing (RTA) at temperatures ranging from 600ºC to 1000ºC in an N_2 atmosphere for 30s. Subsequently, a 2000Å top polysilicon layer (Poly-II) was deposited by LPCVD system and implanted with phosphorous at 5e15cm^{-2}, 20keV. Dopants were then activated with RTA at 950ºC for 30s. Finally, 5000Å TEOS oxide passivation and Al metal pads were defined. The cross-sectional view and key process steps of HfO_2 inter-poly capacitor with surface NH_3 nitridation and post-deposition nitrogen annealing are shown in Figs. 3.2 and 3.3, respectively.

The equivalent oxide thickness (EOT) was obtained from the high frequency (10kHz) capacitance-voltage (*C-V*) measurement using a Hewlett-Packard (HP) 4284 LCR meter. The electrical properties and reliability characteristics of the inter-poly

capacitors were measured using a HP4156C semiconductor parameter analyzer.

3.3 Results and Discussions

3.3.1 Basic Electrical Properties

Figure 3.4 (a) and (b) show the high frequency *C-V* curves (10kHz) and the current density-effective electric field (*J-E*) characteristics of HfO_2 inter-poly capacitors with surface NH_3 nitridation annealed at 600ºC to 1000ºC, respectively. The low capacitance and suppressed leakage current of 1000ºC PDA sample can be ascribed to its thicker EOT, shown in Fig. 3.5. Lower post-deposition annealing temperature won't cause large difference in the oxygen diffusivity between HfO_2 and Al_2O_3 film. When annealing temperature is high as up to 1000ºC, due to the high oxygen diffusion coefficient of HfO_2, shown in Table 1.1, oxygen can easily penetrate the HfO_2 film and react with the layer beneath HfO_2 film to form thick interface layer. This effect can be clearly observed in Fig. 3.6. Compared to the low oxygen diffusivity of Al_2O_3 film, oxygen can penetrate all the way through HfO_2 film to form interface layer at high temperature. So, the higher the post-deposition annealing temperature is, the thicker the interface will be formed. As HfO_2 is not a good oxygen diffusion barrier, the control of oxygen concentration and temperature would be very critical when we apply HfO_2 film as the inter-poly dielectric in production line.

3.3.2 Electric Field and Leakage Current Density Characteristics

Figure 3.7 depicts the Weibull distributions of the effective breakdown field of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen

annealing under (a) positive and (b) negative polarities. In both polarities, the effective breakdown field of the 800ºC PDA annealed HfO_2 IPD is obviously higher than those of as-deposited and 600ºC PDA samples. And we believe this is due to the improved thin film quality of 800ºC PDA sample. Since HfO_2 IPD annealed at 1000°C will oxidize underlying Poly-I more effective than others, both large effective breakdown field and degraded Weibull slope can be explained by thicker interfacial layer and poor interface morphology. Figure 3.8 demonstrates the Weibull distributions of the leakage current of HfO_2 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures in both polarities as the gate bias is 6MV/cm. The magnitude of the leakage current in both polarities is almost the same, about 10^{-7}A/cm^2 in spite of different PDA temperature. The leakage current of as-deposited and 600ºC annealed samples goes up enormously to 10A/cm^2 when the gate bias increases as high as to 5V (about 15.6MV/cm), however there is only three order of magnitude enhancement in the leakage current of 800ºC PDA sample, as shown in Fig. 3.9. The extreme high leakage current density of as-deposited and 600ºC annealed samples stands for their breakdown, and this fact will retard their application to the flash memories [28]. The relatively low leakage current of 1000ºC PDA sample is due to its thicker EOT and thus lower electric field (about 11.3MV/cm) as compared with that of 800ºC PDA sample.

3.3.3 Reliability Characteristics

Figure 3.10 shows Q_{BD} Weibull distributions of HfO_2 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures under (a) positive and (b) negative polarities. The EOT of 800ºC PDA sample is almost the same as those of as-deposited and 600ºC annealed sample, however, a two order magnitude of

enhancement in Q_{BD} can be observed. This fact indicates that post-deposition temperature of 800ºC can effectively improve thin film quality of HfO_2 bulk. On the other hand, according to percolation model [87], [88], stress-induced defects must get in a continuous line to form a leakage path. The 1000ºC PDA sample will have larger Q_{BD} and Weibull slope because of its thicker EOT. Figure 3.11 presents curves of gate current density shift of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative constant voltage stress (CVS) of 1V gate voltage. Electron trapping is observed in both polarities. As PDA temperature increases, electron trapping rate can be suppressed, which means improved film quality. However, the reason for small gate leakage current shift of 1000ºC PDA sample is totally different with others. Voltage drop across HfO_2 IPD will be decreased as the thickness of interfacial layer increasing, which will cause the reduction of the electric field across HfO_2 IPD in 1000ºC PDA sample, reduced leakage path formation and therefore larger Q_{BD} is obtained.

3.4 Summary

The effects of PDA temperature on the electrical properties and reliability characteristics of the HfO_2 inter-poly capacitors with surface NH_3 nitridation are evaluated in this chapter. It was found that the electrical properties of HfO_2 IPD strongly depend upon the PDA temperature. 800ºC annealing is the best condition for the HfO_2 IPD electrical characteristics in terms of EOT scaling, leakage current, electron trapping rate and Q_{BD}. On the other hand, the high oxygen diffusivity of HfO_2 film will result in thick I.L. growth, retarding EOT scaling. As the result, the control of oxygen concentration and temperature would be very critical when we apply HfO_2

film as the inter-poly dielectric in flash memories. Table 3.1 lists several physical and electrical parameters, including EOT, breakdown electric field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values of the HfO_2 IPDs with surface NH_3 nitridation annealed at various temperatures.

Table 3.1 EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values of the HfO_2 inter-poly capacitors with surface NH_3 nitridation under positive and negative CVS at various PDA temperatures in N_2 ambient.

PDA Temp. (ºC)	EOT (Å)	E_{BD} (MV/cm)		Jg@6MV/cm (nA/cm^2)		63% QBD (mC/cm^2)	
		positive	negative	positive	negative	positive	negative
As-dep	31.3	12.86	13.63	162	278	0.9	1.0
600	31.1	13.37	14.60	245	355	0.33	0.76
800	32.2	19.69	20.24	245	550	103	16
1000	42.3	20.14	21.75	110	309	172	11.5

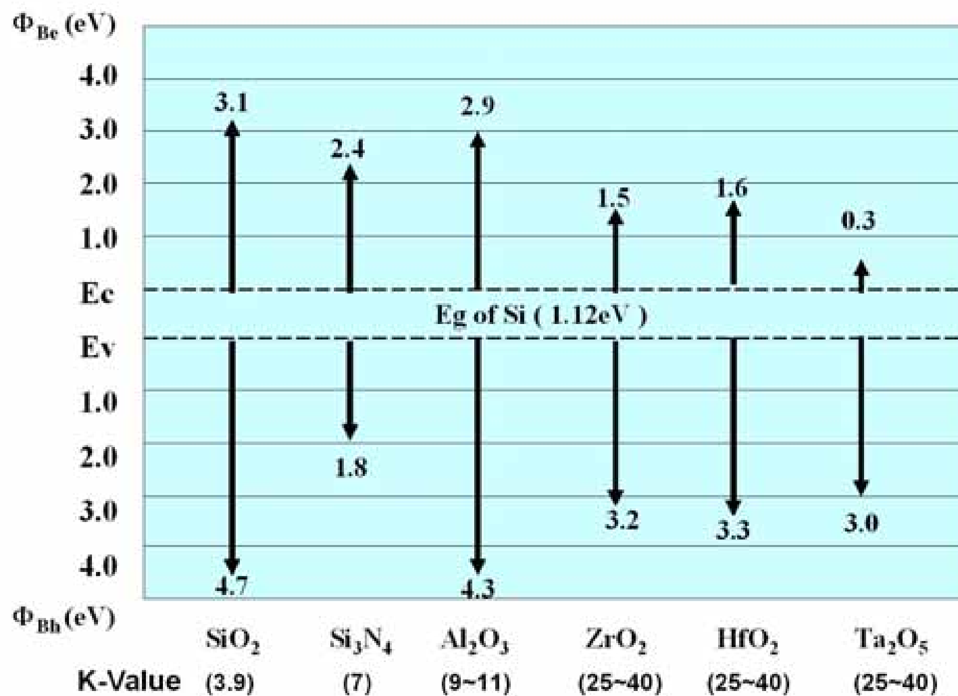


Fig. 3.1 Band alignment of typical high-κ dielectrics.

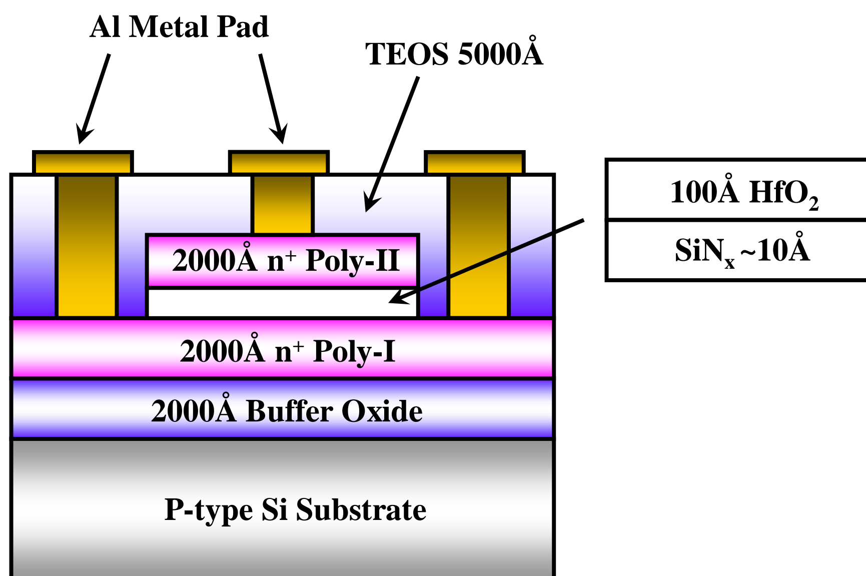


Fig. 3.2 Cross-sectional view of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

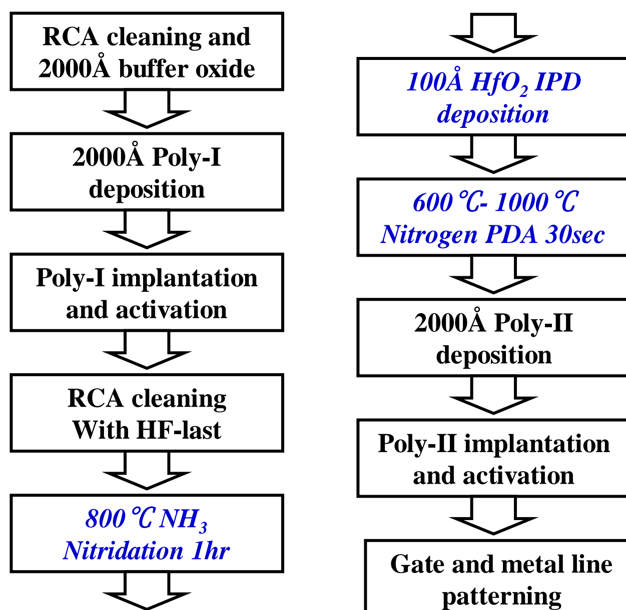
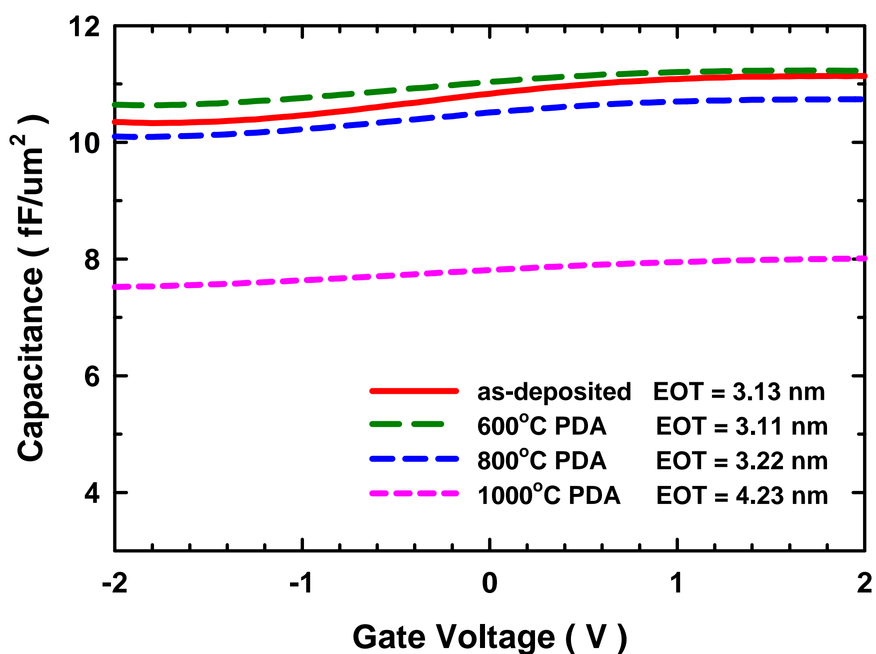
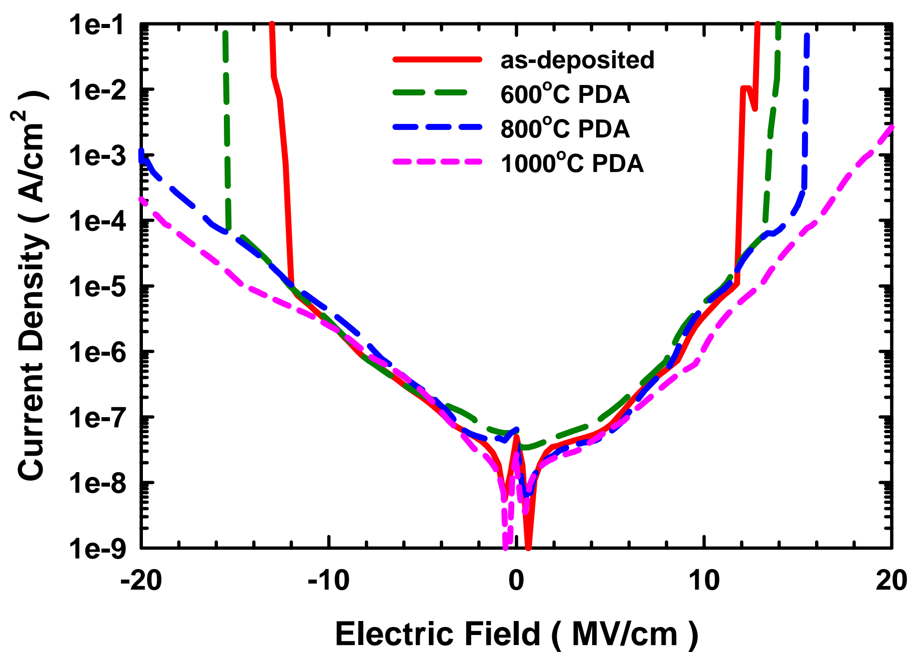


Fig. 3.3 Key process steps of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.



(a)



(b)

Fig. 3.4 (a) *C-V* curves and (b) *J-E* characteristics of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

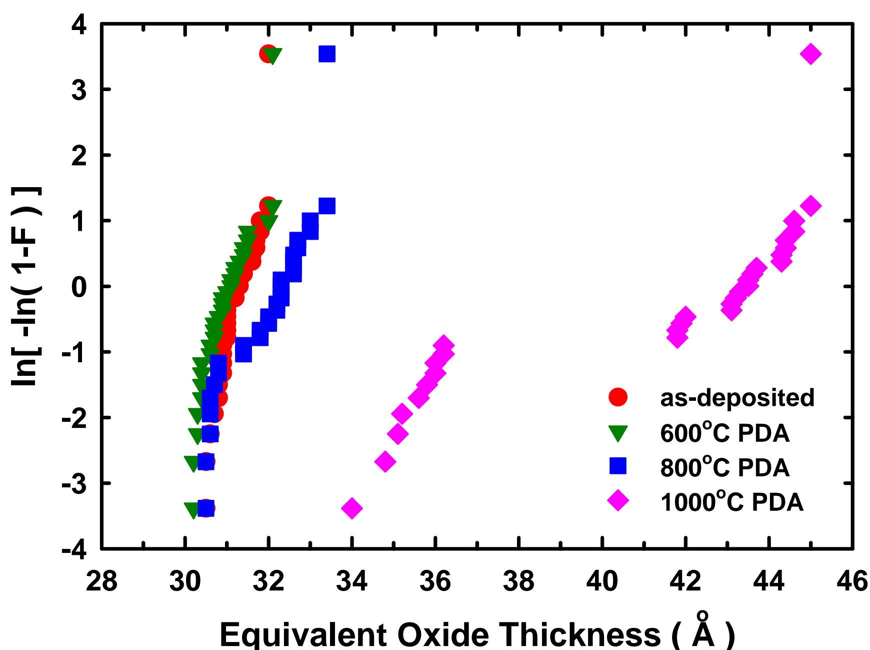


Fig. 3.5 Equivalent oxide thickness of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.

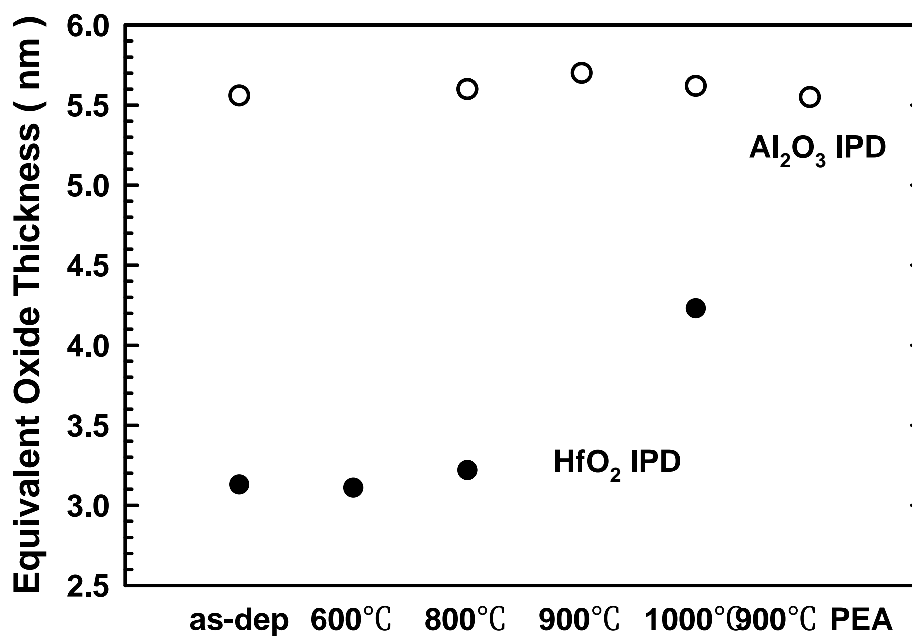
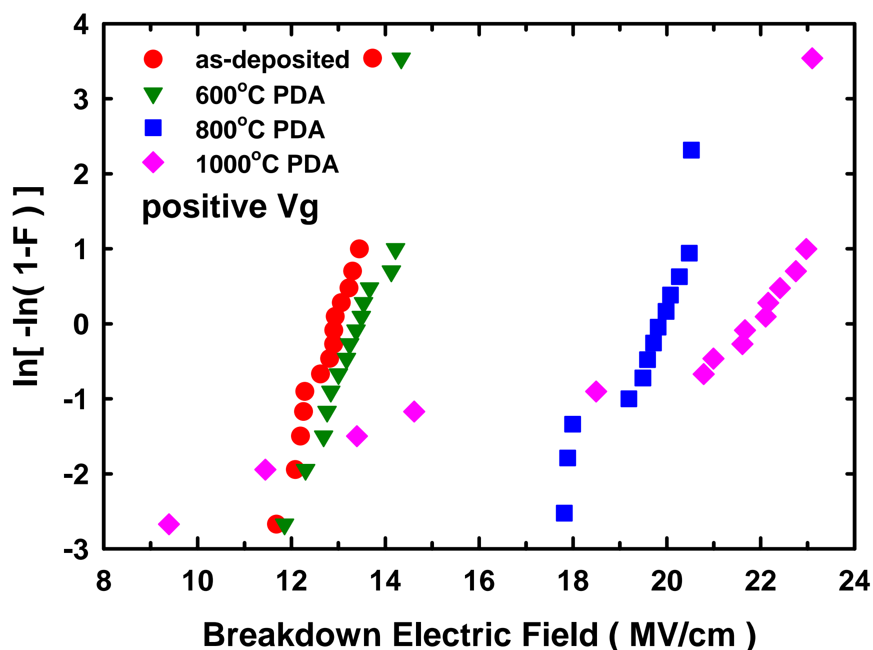
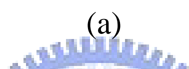
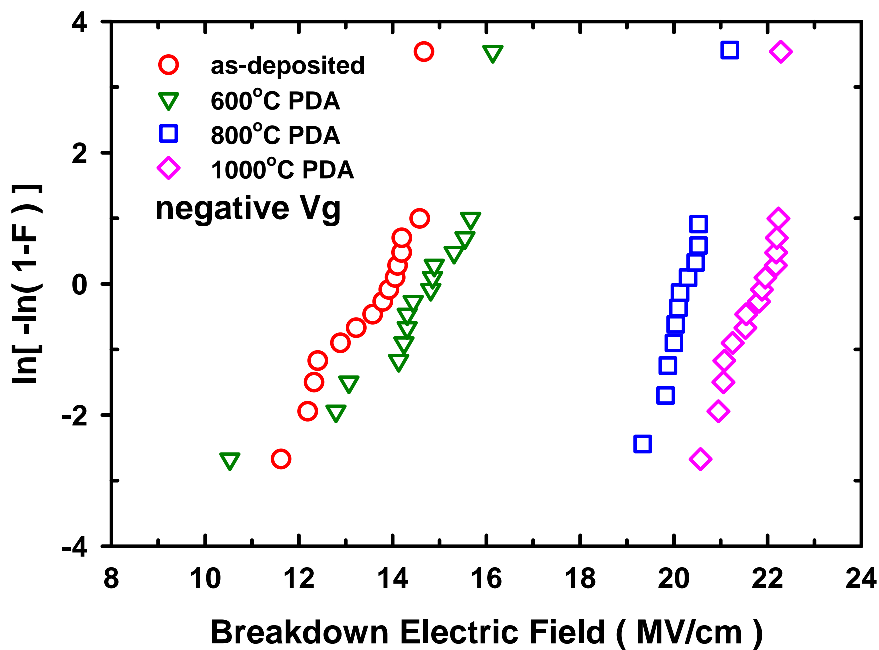


Fig. 3.6 Comparison of EOT between Al_2O_3 and HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing.



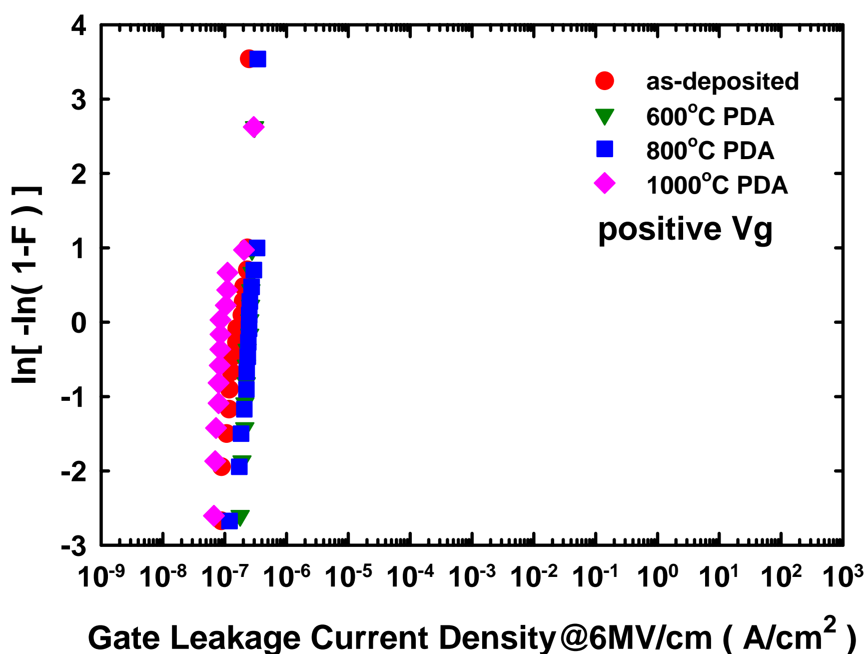
(a)



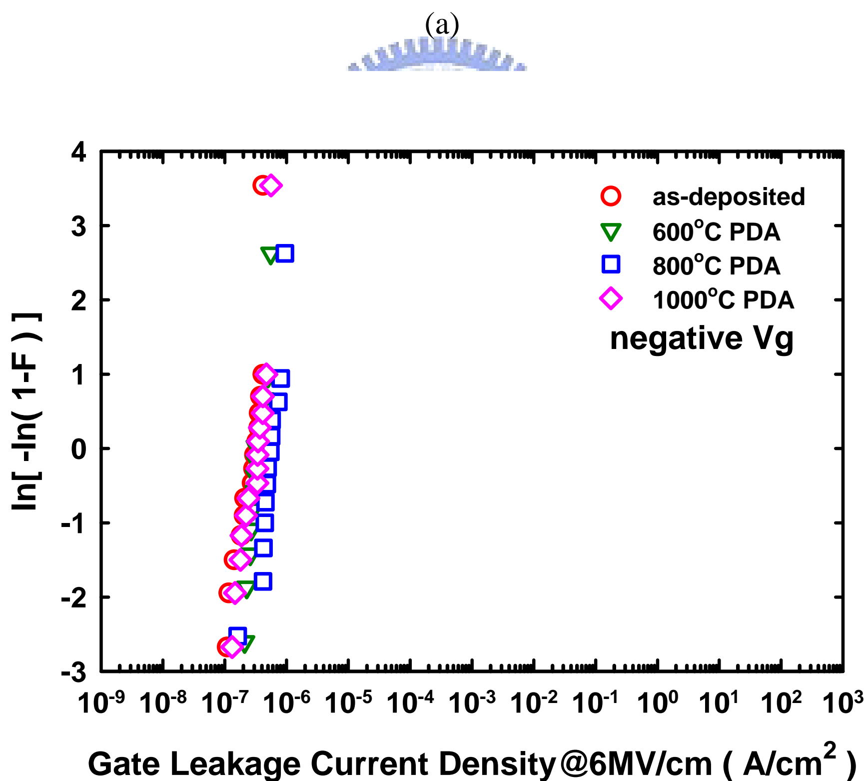


(b)

Fig. 3.7 The Weibull distributions of the effective breakdown field of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities.

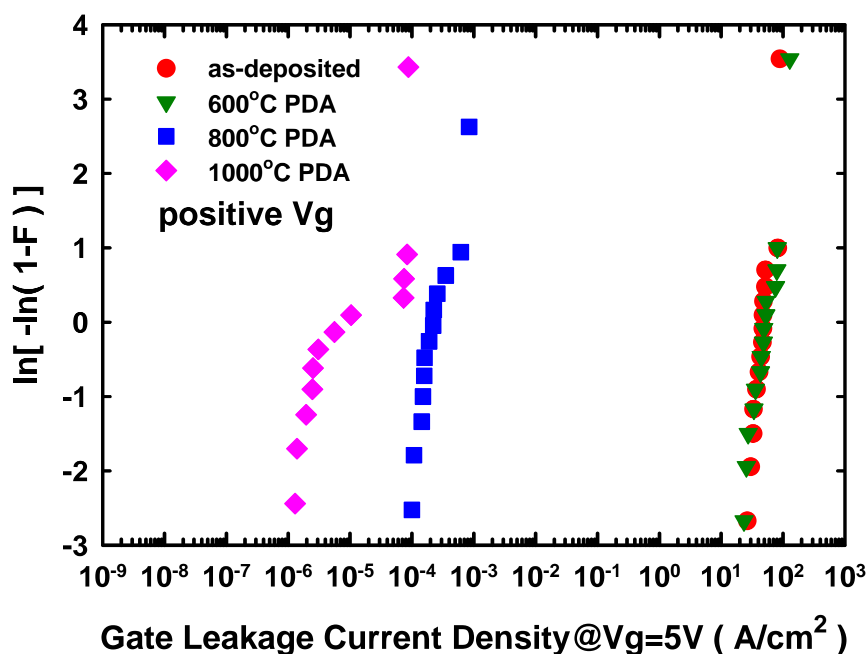


(a)

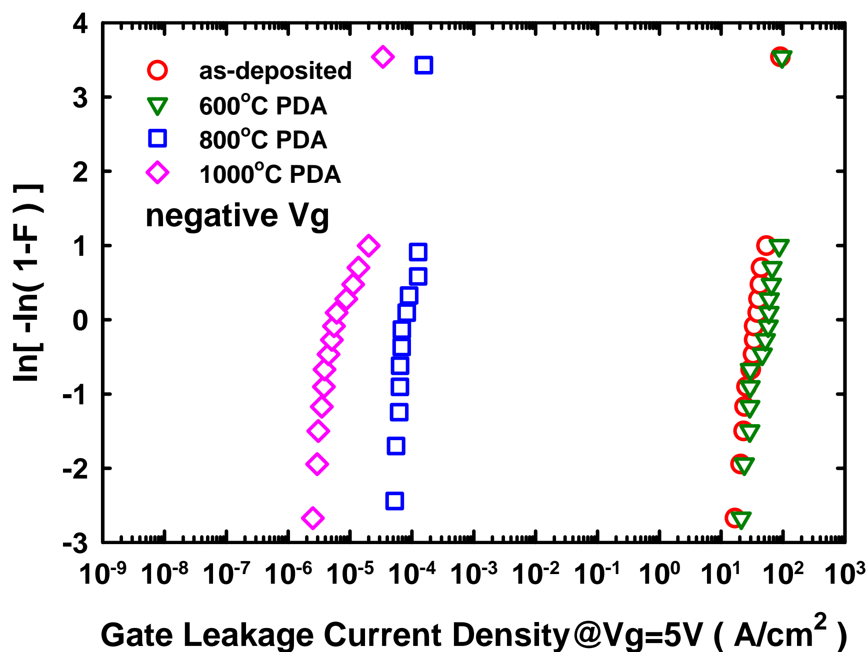


(b)

Fig. 3.8 The Weibull distributions of the leakage current density of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities as the gate bias is 6MV/cm.

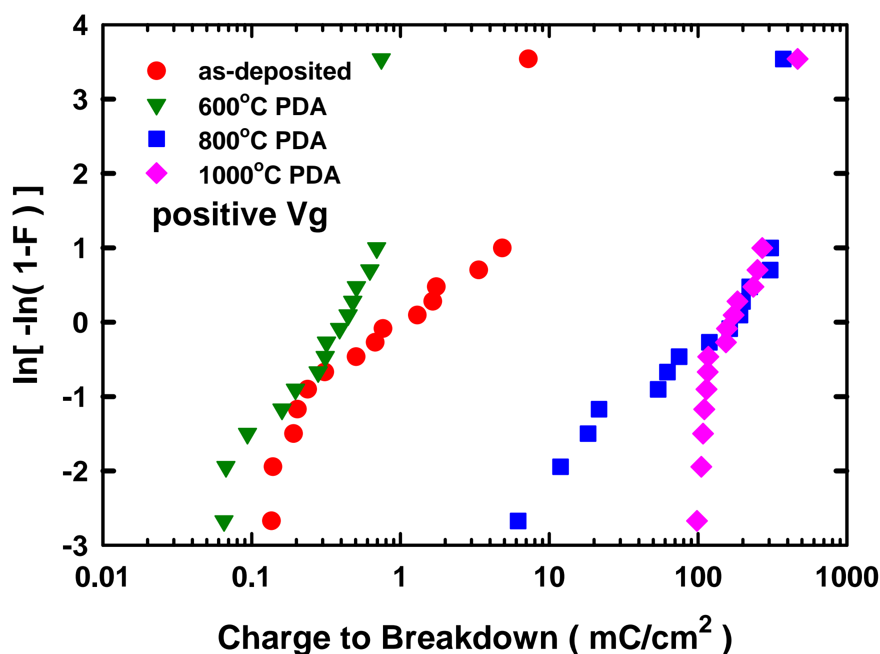


(a)

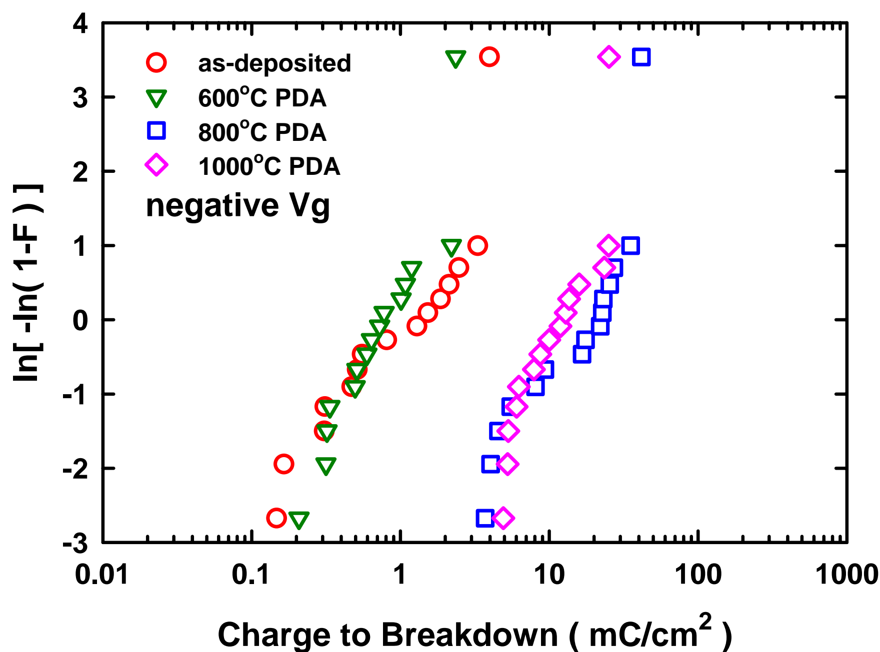


(b)

Fig. 3.9 The Weibull distributions of the leakage current density of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative polarities as the gate bias is 5V.

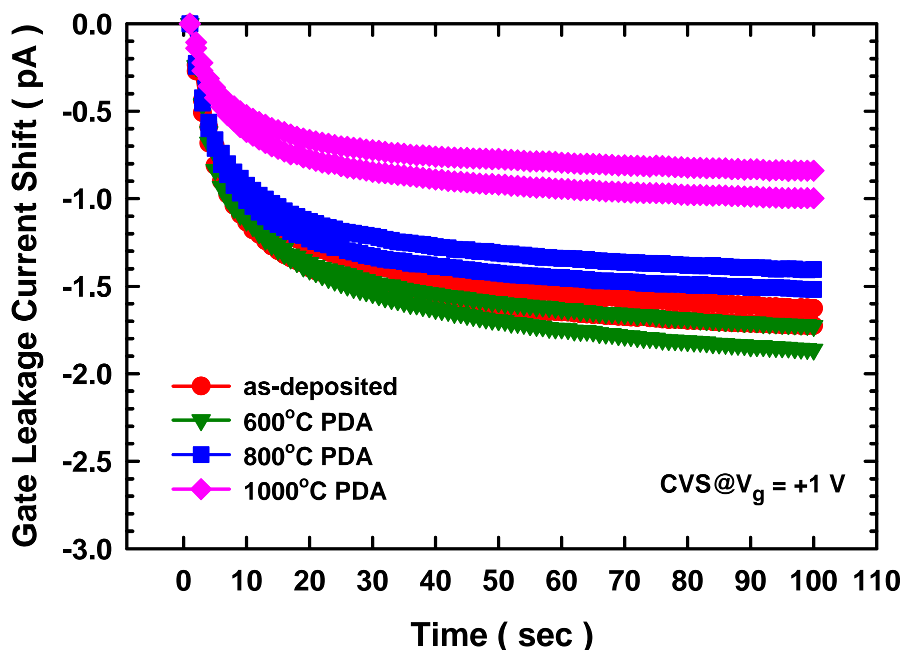


(a)

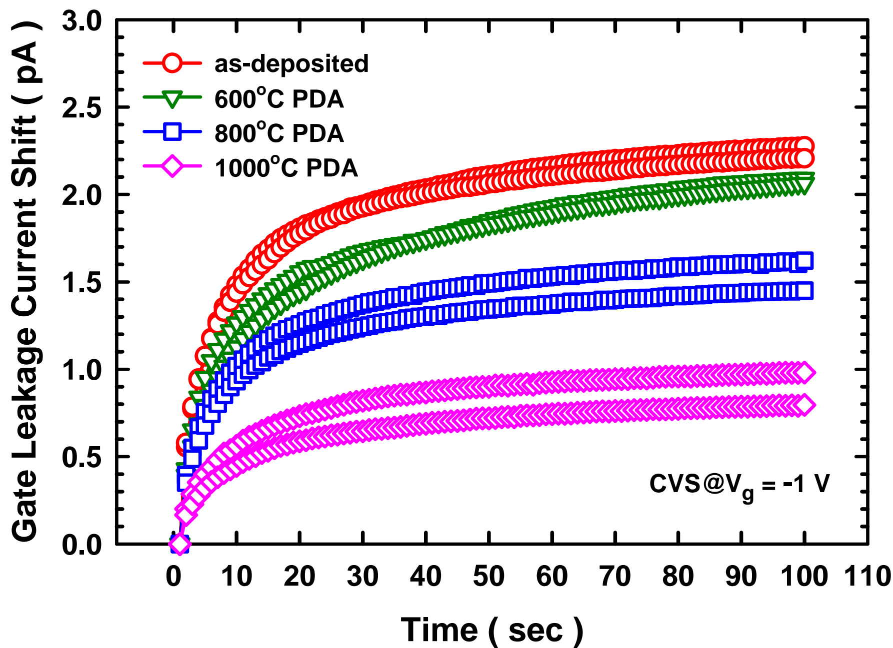


(b)

Fig. 3.10 Q_{BD} Weibull distributions of HfO_2 inter-poly capacitors with surface NH_3 nitridation at various PDA temperatures under (a) positive and (b) negative polarities.



(a)



(b)

Fig. 3.11. Curves of gate current density shift of HfO_2 inter-poly capacitors with surface NH_3 nitridation and post-deposition nitrogen annealing under (a) positive and (b) negative constant voltage stress.

CHAPTER 4

Conclusions and Recommendations for Future Works

4.1 Conclusions

According to SIA roadmap, oxide thickness small than 20Å is necessary for deep sub-quarter micron devices. However, pure SiO_2 can't meet the requirement due to the large tunneling current. In our study, it was found that the electrical properties of Al_2O_3 and HfO_2 IPD strongly depend upon the PDA temperature. The PDA temperature up to 1000ºC may cause Al_2O_3 film crystallization and thus poor quality. Additional 900ºC PEA is beneficial to improve thin film quality because it can reduce the damage generated during the Poly-II patterning. For HfO_2 IPD, since HfO_2 is not a good oxygen diffusion barrier, the control of oxygen concentration and temperature would be very critical when we apply it as the inter-poly dielectric in the flash memories. 800ºC and 900ºC annealing are the best condition for the HfO_2 and Al_2O_3 IPD respectively. Table 4.1 lists the comparison of 800ºC PDA HfO_2 IPD and 900ºC PDA with 900ºCPEA Al_2O_3 IPD samples in terms of EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values.

4.2 Recommendations for Future Works

1. More HRTEM images to evidence thickness variation and interfacial layer reaction.

2. More physical analyses to quantitatively understand film composition.

3. Fully Fabricated stacked-gate flash memories with high-κ inter-poly dielectrics to study the device characteristics, including program/erase speed, retention time and charge loss mechanism.

Table 4.1 Comparison of 800ºC PDA HfO_2 IPD and 900ºC PDA with 900ºCPEA Al_2O_3 IPD samples in terms of EOT, effective breakdown field, 6MV/cm-biased leakage current density and 63%-failure Q_{BD} values.

IPD material	EOT (Å)	E_{BD} (MV/cm)		Jg@6MV/cm (nA/cm^2)		63% QBD (mC/cm^2)	
		(+)	(−)	(+)	(−)	(+)	(−)
800ºC PDA HfO_2	**32.2**	**19.7**	**20.2**	**245**	**550**	**103**	**16**
900ºC PDA with 900ºCPEA Al_2O_3	**55.5**	**18.0**	**18.8**	**6.0**	**3.1**	**6570**	**610**

References

[1] T. Hori, *Gate Dielectrics and MOS ULSIs*, p. 43.

[2] G. Bavvarani, M. R. Wordeman and R.H. Rennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," *IEEE Trans. Electron Devices*, vol. 31, no. 4, p. 452, Apr. 1984.

[3] P. A. Packan, "Device physics: pushing the limits," *Science*, vol. 285, p. 2079, 1999

[4] T. H. Ning, "Silicon technology directions in the new millennium," in *Proc. Int. Reliab. Phys. Symp.*, 2000, p. 1.

[5] M. T. Bohr, "Technology development strategies for the 21st century," *Appl. Surf. Sci.*, vol. 100-101, p. 534, July 1996.

[6] Y. Taur, D. Buchanan, W. Chen, D. J. Frank, K. I. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. C. Wann, S.J. Wind, and H.-S. Wong, "CMOS scaling into the nanometer regime," in *Proc. IEEE*, vol. 85, no. 4, p. 486, Apr. 1997.

[7] Y.-C. Yeo, T.-J. King and C. Hu, "Direct tunneling leakage current and scalability of alternative gate dielectrics," *Appl. Phys. Lett.*, vol. 81, no. 11, p. 2091, Sep. 2002.

[8] H. Hwang, W. Ting, B. Maiti, D. L. Kwong and J. Lee, "Electrical characteristics of ulthathin oxynitride gate dielectrics prepared by rapid thermal oxidation of silicon in N_2O," *Appl. Phys. Lett.*, vol. 57, no. 10, p. 1010, Sep. 1990.

[9] M. Bhat, L. K. Han, D. Wristers, J. Yan, D. L. Kwong and J. Fulford, "Effect of chemical composition on the electrical properties of NO-nitrided SiO_2," *Appl. Phys. Lett.*, vol. 66, no. 10, p. 1225, Mar. 1995.

[10] S. V. Hattangady, H. Niimi and G. Lucovsky, "Controlled nitrogen incorporation at the gate oxide surface," *Appl. Phys. Lett.*, vol. 66, no. 25, p. 3495, June 1995.

[11] W. L. Hill, E. M. Vogel, V. Misra, P. K. McLarty and J. J. Wortmsn, "Low pressure rapid thermal CVD of oxynitride gate dielectrics for N-channel and P-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 43, no. 1, p. 15, Jan. 1996.

[12] T. Hori, "Nitrided gate-oxide CMOS technology for improved hot-carrier reliability," *Microelectron. Eng*., vol. 22, p. 245, 1993.

[13] E. P. Gusev, H.-C. Lu, E. L. Garfunkel, T. Gustafsson and M. L. Green, "Growth and characterization of ultrathin nitrided silicon oxide films," *IBM J. Res. Develop*., vol. 43, p. 265, 1999.

[14] M. Fujiwara, M. takayanagi, T. Shimizu and Y. Toyoshima, "Extending gate dielectric scaling limit by NO oxynitride：design and process issues for sub-100nm technology," in *IEDM Tech. Dig*., 2000, p. 227.

[15] E. Cartier, D.A. Buchanan and G. J. Dunn, "Atomic hydrogen-induced interface degradation of reoxidized-nitrided silicon dioxide on silicon," *Appl. Phys. Lett*., vol. 64, no. 7, p. 901, Feb. 1994.

[16] D. M. Brown, P. V. Gray, F. K. Heumann, H. R. Philipp and E. A. Taft, "Properties of $Si_xO_yN_z$ films on Si," *J. of Electrochem. Soc*., vol. 115, p. 311, 1968.

[17] D. A. Buchanan, E. P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M. A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R. J. Fleming, P. C. Jamison, J. Brown and R. Amdt, "80nm poly-silicon gated n-FETs with ultra-thin Al_2O_3 gate dielectric for ULSI applications," in *IEDM Tech. Dig*., 2000, p.223.

[18] S.-J. Ding, H. Hu, C. Zhu, M. F. Li, S. J. Kim, B. J. Cho, D. S. H. Chan, M. B. Yu, A. T. Du, A. Chin and D. L. Kwong, "Evidence and understanding of ALD HfO_2-Al_2O_3 laminate MIM capacitors outperforming sandwich counterpart," *IEEE Electron Device Lett*., vol. 24, no. 10, p. 681, Oct. 2004.

[19] J. C. Wang, S. H. Chiao, C. L. Lee, T. F. Lei, Y. M. Lin, M. F. Wang, S. C. Chen, C. H. Yu and M. S. Liang, "A physical model for the hysteresis phenomenon of

the ultrathin ZrO_2 film," *J. Appl. Phys*., vol. 92, no. 7, p. 3936, Oct. 2002.

[20] B. Tavel, X. Garros, T. Skotnicki, F. Martin, C. Leroux, D. Bensahel, M. N. Séméria, Y. Morand, J. F. Danlencourt, S. Descombes, F. Leverd, Y. Le-Friec, P. Leduc, M. Rivoire, S. Jullian and R. Pantel, "High performance 40nm nMOSFETs with HfO_2 gate dielectric and polysilicon damascene gate," in *IEDM Tech. Dig*., 2002, p. 429.

[21] W. -H. Lee, J. T. Clemens, R. C. Keller and L. Manchanda, "A novel high κ inter-poly dielectric (IPD), Al_2O_3 for low voltage/high speed flash memories: erasing in msecs at 3.3V," in *VLSI Tech. Symp. Dig*., 1997, p. 117.

[22] Y. Y. Chen, C. H. Chien and J. C. Lou, "High quality Al_2O_3 IPD with NH_3 surface nitridation," *IEEE Electron Device Lett*., vol. 24, no. 8, p. 503, Aug. 2003.

[23] Y. Y. Chen, C. H. Chien and J. C. Lou, "Characteristics of the inter-poly Al_2O_3 dielectrics on NH_3-nitrided bottom poly-Si for next-generation flash memories," *Jpn. J. Appl. Phys*., vol. 44, no. 4A, p. 1704, 2005.

[24] T. Sugiyama, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi and H. Tanaka, "Novel multi-bit SONOS type flash memory using a high-κ charge trapping layer," in *VLSI Tech. Symp. Dig*., 2003, p. 27.

[25] B. Govoreanu, P. Blomme, J. Van Houdt and K. De Meyer, "Simulation of nanofloating gate memory with high-κ stacked dielectrics," in *Simulation of Semiconductor Processes and Devices*, 2003, p. 299.

[26] D.-W. Kim, T. Kim and S. K. Banerjee, "Memory characterization of SiGe quantum dot flash memories with HfO_2 and SiO_2 tunneling dielectrics," *IEEE Trans. Electron Devices*, vol. 50, no. 9, p. 1823, Sep. 2003.

[27] Y. Y. Chen, J. C. Lou, T. H. Perng, C. W. Chen and C. H. Chien, "The impact of high-κ inter-poly dielectrics (IPD) on the programming/erasing performances of stacked-gate flash memories," in *Electron Devices and Materials Symposia*, 2003, p. 42.

[28] *The International Technology Roadmap for Semiconductors*, 2004 update ed.,

Semiconductor Industry Assoc.

[29] L. Faraone and G. Harbeke, "Surface roughness and electrical conduction of oxide/polysilicon interfaces," *J. Electrochem. Soc.*, vol. 133, no. 7, p. 1410, July. 1986.

[30] S. Mori, E. Sakagami, H. Araki, Y. Kaneko, K. Narita, Y. Ohshima, N. Arai and K. Yoshikawa, "ONO inter-poly dielectric scaling for nonvolatile memory applications," *IEEE Trans. Electron Devices*, vol. 38, no. 2, p. 386, Feb. 1991.

[31] C. S. Lai, T. F. Lei and C. L. Lee, "The characteristics of polysilicon oxide grown in pure N_2O," *IEEE Trans. Electron Devices*, vol. 43, no. 2, p. 326, Feb. 1996.

[32] T. M Pan, T. F. Lei, W. L. Yang, C. M. Cheng and T. S. Chao, "High quality interpoly-oxynitride grown by NH_3 nitridation and N_2O RTA treatment," *IEEE Electron Device Lett.*, vol. 22, no. 2, p. 68, Feb. 2001.

[33] K. Yoshikawa, "Research challenges for next decade flash memories," *Int. Electron Devices and Materials Symposia*, 2000, p. 11.

[34] Y. Yamaguchi, E. Sakagami, N. Arai, M. Sato, E. Kamiya, K. Yoshikawa, H. Meguro, H. Tsunoda and S. Mori, "ONO interpoly dielectric scaling limit for non-volatile memory devices," in *VLSI Tech. Symp. Dig.*, 1993, p. 85.

[35] J. D. Bude, A. Frommer, M. R. Pinto and G. R. Weber, "EEPROM/flash sub 3.0 V drain-source bias hot carrier writing," in *IEDM Tech. Dig.*, 1995, p. 989.

[36] S. Ueno, H. Oda, N. Ajika, M. Inuishi and H. Miyoshi, "Optimum voltage scaling methodology for low voltage operation of CHE type flash EEPROMs with high reliability, maintaining the constant performance," in *VLSI Tech. Symp. Dig.*, 1996, p. 54.

[37] C. Cobianu, O. Popa and D. Dascalu, "On the electrical conduction in the interpolysilicon dielectric layers," *IEEE Electron Device Lett.*, vol. 14, no. 5, p. 213, May. 1993.

[38] T. One, T. Mori, E. Ajioka and T. Takayashiki, "Studies of thin poly-Si oxides for E and E2PROM," in *IEDM Tech. Dig.*, 1985, p. 380.

[39] J. C. Lee and C. Hu, "Polarity asymmetry of oxides grown on polycrystalline silicon," *IEEE Trans. Electron Devices*, vol. 35, no. 7, p. 1063, July 1988.

[40] L. Faraone, "Thermal SiO_2 films on n^+ polycrystalline silicon: electrical conduction and breakdown," *IEEE Trans. Electron Devices*, vol. 33, no. 11, p. 1785, Nov. 1986.

[41] Y. S. Hisamune, K. Kanamori, T. Kubota, Y. Suzuki, M. Tsukiji, E. Hasegawa, A. Ishitani and T. Okazawa, "A high capacitive-coupling ratio (HiCR) cell for 3V-only 64 Mbits and future memories," in *IEDM Tech. Dig.*, 1993, p. 19.

[42] M. Kato, T. Adachi, T. Tanaka, A. Sato, T. Kobayashi, Y. Sudo, T. Morimoto, H. Kume, T. Nishida and K. Kimura, "A 0.4-um^2 self-aligned contactless memory cell technology suitable for 256-Mbit flash memories," in *IEDM Tech. Dig.*, 1994, p.921.

[43] T. Takeshima, H. Sugawara, H. Takada, Y. Hisamune, K. Kanamori, T. Okazawa, T. Murotani and I. Sasaki, "A 3.3V single-power-supply 64Mb flash memory with dynamic bit-line latch (DBL) programming scheme," in *ISSCC Tech. Dig.*, 1994, p. 148.

[44] Y. Yamauchi, M. Yoshimi, S. Sato, H. Tabuchi, N. Takenaka and K. Sakiyam, "A new cell structure for sub-quarter micron high density flash memory," in *IEDM Tech. Dig.*, 1995, p. 267.

[45] T. Kobayashi, N. Matsuzaki, A. Sato, A. Katayama, H. Kurata, A. Miura, T. Mine, Y. Goto, T. Morimoto, H. Kume, T. Kure and K. Kimura, "A 0.24-um^2 cell process with 0.18-um width isolation and 3-D interpoly dielectric films for 1-Gb flash memories," in *IEDM Tech. Dig.*, 1997, p. 275.

[46] H. Shirai, T. Kubota, I. Honma, H. Watanabe, H. Ono and T. Okazawa, "A 0.54 um^2 self-aligned, HSG floating gate cell (SAHF cell) for 256 Mbit flash memories," in *IEDM Tech. Dig.*, 1995, p. 653.

[47] T. Kitamura, M. Kawata, I. Honma, I. Yamamoto, S. Nishimoto and K. Oyama, "A low voltage operating flash memory cell with high coupling ratio using horned floating gate with fine HSG," in *VLSI Tech. Symp. Dig.*, 1998, p. 104.

[48] J.-D. Choi, J.-H. Lee, W.-H. Lee, K.-S. Shin. Y.-S. Yim. J.-D. Lee, Y.-C. Shin, S.-N. Chang, K.-C. Park, J.-W. Park and C.-G. Hwang, “A 0.15 um NAND flash technology with 0.11 um^2 cell size for 1 Gbit flash memory,” in *IEDM Tech. Dig*., 2000, p. 767.

[49] N. Matsuo and A. Sasaki, “Electrical characteristics of oxide-nitride-oxide films formed on tunnel-structured stacked capacitors,” *IEEE Trans. Electron Devices*, vol. 42, no. 7, p. 1340, July 1995.

[50] S. Holland, “An oxide-nitride-oxide capacitor dielectric film for silicon strip detectors,” *IEEE Trans. Nuclear Science*, vol. 42, no. 8, p. 423, Aug. 1995.

[51] C. L. Cha, E. F. Chor, H. Gong, A. Q. Zhang and L. Chan, “Breakdown of reoxidized nitrided oxide (ONO) in flash memory devices upon current stressing,” in *IEEE Electron Devices Meeting*, Hong Kong, 1997, p. 82.

[52] S. J. Lee, C. H. Lee, Y. H. Kim, H. F. Luan, W. P. Bai, T. S. Jeon and D. L. Kwong, “High-κ gate dielectrics for sub-100 nm CMOS technology,” in *International Conference on Solid-State and Integrated-Circuit Technology*, 2001, p. 303.

[53] C. B. Oh, H. S. Kang, H. J. Ryu, M. H. Oh, H. S. Jung, Y. S. Kim, J. H. He, N. I. Lee, K. H. Cho, D. H. Lee, T. H. Yang, I. S. Cho, H. K. Kang, Y. W. Kim and K. P. Suh, “Manufacturable embedded CMOS 6T-SRAM technology with high-κ gate dielectric device for system-on-chip application,” in *IEDM Tech. Dig*., 2002, p. 423.

[54] M. Cho, H. B. Park, J. Park, S. W. Lee, C. S. Hwang, G. H. Jang and J. Jeong, “High-κ properties of atomic-layer-deposited HfO_2 films using a nitrogen-containing $Hf[N(CH_3)_2]_4$ precursor and H_2O oxidant,” *Appl. Phys. Lett*., vol. 83, no. 26, p. 5503, Dec. 2003.

[55] M. Heyns, S. Beckx, H. Bender, P. Blomme, W. Boullart, B. Brijs, R. Carter, M. Caymax, M. Claes, T. Conard, S. De Gendt, R. Degraeve, A. Delabie, W. Deweerdt, G. Groeseneken, K. Henson, T. Kauerauf, S. Kubicek, L. Lucci, G. Lujan, J. Mentens, L. Pantisano, J. Petry, O. Richard, E. Rohr, T. Schram, W. Vandervorst, P. Van Doorne, S. Van Elshocht, J. Westlinder, T. Witters, C. Zhao, E. Cartier, J. Chen, V. Cosnier, M. Green, S. E. Jang, V. Kaushik, A. Kerber, J.

Kluth, S. Lin, W. Tsai, E. Young, V. Manabe, Y. Shimamoto, P. Bajolet, H. De Witte, J. W. Maes, L. Date, D. Pique, B. Coebegrachts, J. Vertommen and S. Passefort, “Scaling of high-κ dielectrics towards sub-1nm EOT,” in *VLSI Tech. Symp. Dig*., 2003, p. 247.

[56] A. S. Oates, “Reliability issues for high-κ gate dielectrics,” in *IEDM Tech. Dig*., 2003, p. 923.

[57] S. K. Kim and C. S. Hwang, “Atomic-layer-deposited Al_2O_3 thin films with thin SiO_2 layers grown by in-situ O_3 oxidation,” *J. Appl. Phys*., vol. 96, no. 4, p. 2323, Aug. 2004.

[58] D. L. Kwong, “CMOS integration issues with high-κ gate stack,” in *International Symp. on the Phys. and Failure Analysis of Integrated Circuit*s, 2004, p. 17.

[59] C. C. Fulton, T. E. Cook, G. Lucovsky and R. J. Nemanich, “Interface instabilities and electronic properties of ZrO_2 on silicon,” *J. Appl. Phys*., vol. 96, no. 5, p. 2665, Sep. 2004.

[60] Y. Tanida, Y. Tamura, S. Miyagaki, M. Tamaguchi, C. Yoshida, Y. Sugiyama and H. Tanaka, “Effect of in-situ nitrogen doping into MOCVD-grown Al_2O_3 to improve electrical characteristics of MOSFETs with polisilicon gate,” in *VLSI Tech. Symp. Dig*., 2002, p. 190.

[61] S. Saito, Y. Shimamoto, S. Tsujikawa, H. Hamamura, O. Tonomura, D. Hisamoto, T. Mine, K. Torii, J. Yugami, M. Hiratani, T. Onai and S. Kimura, “Impact of oxygen-enriched SiN interface on Al_2O_3 gate stack an innovative solution to low-power CMOS,” in *VLSI Tech. Symp. Dig*., 2003, p. 145.

[62] J. B. Kim, D. R. Kwon, K. Chakrabarti, C. Lee, K. Y. Oh and J. H. Lee, “Improvement in Al_2O_3 dielectric behavior by using ozone as an oxidant for the atomic layer deposition technique,” *J. Appl. Phys*., vol. 92, no. 11, p. 6739, Dec. 2002.

[63] B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi and J. C. Lee, “Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application,” in *IEDM Tech. Dig*., 1999, p. 133.

[64] S. J. Lee, H. F. Luan, T. S. Jeon, W. P. Bai, Y. Senzaki, D. Roberts abd D. L. Kwong, "Performance and reliability of ultra thin CVD HfO_2 gate dielectrics with dual poly-Si gate electrodes," in *VLSI Tech. Symp. Dig*., 2001, p.133

[65] H. Y. Yu, J. F. Kang, J. D. Chen, C. Ren, Y. T. Hou, S. J. Whang, M. F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, A. Du and D. L. Kwong, "Thermally robust high quality HfN/HfO_2 gate stack for advanced CMOS devices," in *IEDM Tech. Dig*., 2003, p. 99.

[66] S. B. Samavedam, L. B. La, J. Smith, S. Dakshina-Murthy, E. Luckowski, J. Schaeffer, M. Zavala, R. Martin, V. Dhandapani, D. Triyoso, H. H. Tseng, P. J. Tobin, D. C. Gilmer, C. Hobbs, W. J. Taylor, J. M. Grant, R. I. Hegde, J. Mogab, C. Thomas, P. Abramowitz, M. Moosa, J. Conner, J. Jiang, V. Arunachalam, M. Sadd, B. Y. Nguyen and B. White, "Dual-metal gate CMOS with HfO_2 gate dielectric," in *IEDM Tech. Dig*., 2002, p. 433.

[67] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Ki, J. S. Jeon, K. H. Cho, H. S. Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, "Effects of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-Al_2O_3 gate dielectric," in *IEDM Tech. Dig*., 2000, p. 645.

[68] H. Hu, C. Zhu, X. Yu, A. Chin, M. F. Li, B.J. Cho, D. L. Kwong, P. D. Foo, M. B. Yu, X. Liu and J. Winkler, "MIM capacitors using atomic-layer-deposited high-κ $(HfO_2)_{1-x}(Al_2O_3)_x$ dielectrics," *IEEE Electron Device Lett*., vol. 24, no. 2, p. 60, Feb. 2003.

[69] A. C. Jones, *Chemical Vapor Deposition*, **4**, 169(1998)

[70] J. F. Roeder, T. H. Baum, S. M. Bilodeau, G. T. Stauf, C. Ragaglia, M. W. Russell and P. C. Van Buskirk, "Liquid-delivery MOCVD: chemical and process perspectives on ferro-electric thin film growth," *Adv. Mater. Opt. Electron*., vol. 10, no. 3, p. 145, 2000.

[71] G. D. Wilk, R. M. Wallace and J. M. Anthony, "High-κ gate dielectrics: current status and materials properties considerations," *J. Appl. Phys*., vol. 89, no. 10, p. 5243, May 2001.

[72] Rino Choi, C. S. Kang, B. H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan and J. C. Lee, "High-quality ultra-thin HfO_2 gate dielectric MOSFETs with TaN electrode and nitridation surface preparation," in *VLSI Tech.*

Symp. Dig., 2001, p. 15.

[73] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y.-J. Jeon, C. S. Kang, B. H. Lee, R. Nieh and J. C. Lee, “Dopant penetration effects on polysilicon gate HfO_2 MOSFETs,” in *VLSI Tech. Symp. Dig*., 2001, p. 131.

[74] H.-J. Cho, D. G. Park, I.-S. Yeo, J.-S. Roh and J. W. Park, “Characteristics of TaO_xN_y gate dielectric with improved thermal stability,” *Jpn. J. Appl. Phys*., vol. 40, p. 2814, 2001.

[75] H.-J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan and J. C. Lee, “Novel nitrogen profile engineering for improved TaN/HfO_2/Si MOSFET performance,” in *IEDM Tech. Dig*., 2001, p. 30.2.1.

[76] A. L. P. Rotondaro, M. R. Visokay, J. J. Chambers, A. Shanware, R. Khamankar, H. Bu, R. T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M. J. Bevan, T. Grider, J. McPherson and L. Colombo, “Advanced CMOS Transistors with a novel HfSiON gate dielectric,” in *VLSI Tech. Symp. Dig*., 2002, p. 148.

[77] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo and A. Nishiyama, “Thermally stable ultra-thin nitrogen incorporated ZrO_2 gate dielectric prepared by low temperature oxidation of ZrN,” in *VLSI Tech. Symp. Dig*., 2001, p. 459.

[78] T. M. Pan, T. F. Lei and T. S. Chao, “Robust ultrathin oxynitride dielectrics by NH_3 nitridation and N_2O RTA treatment,” *IEEE Electron Device Lett*., vol. 21, no. 8, p. 378, Aug. 2000.

[79] J. Robertson, “Band offsets of wide-band-gap oxides and implications for future electronic devices,” *J. Vac. Sci. Technol. B*., vol. 18, no.3, p. 1785, May 2000

[80] E. P. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. C. Jamison, D. A. Neumater, M. Copel, M. A. Gribelyuk, H. Okorn-Schmidt, C. D’Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L. A. Ragnarsson, P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta and A. Ajmera, “Ultrathin high-κ gate stacks for advanced CMOS devices,” in *IEDM Tech. Dig*., 2001, p. 451.

[81] K. F. Schuegraf and C. Hu, "Hole injection SiO2 breakdown model for very low voltage lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, no. 5, p. 761, May 1994.

[82] I. C. Chen, S. Holland, K. K. Young, C. Chang and C. Hu, "Substrate hole current and oxide breakdown," *Appl. Phys. Lett*., vol. 49, no. 11, p. 669, 1986.

[83] J. C. Lee, "Ultra-thin gate dielectrics and high-κ dielectrics," IEEE EDS vanguard series of independent short courses.

[84] L. Kang, K. Onishi, Y. Jeon, B. H. Lee, C. Kang, W. J. Qi, R. Nieh, S. Gopalan, R. Choi and J. C. Lee, "MOSFET devices with polysilicon on single-layer HfO_2 high-κ dielectrics," in *IEDM Tech. Dig*., 2000, p. 35.

[85] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts and D. L. Kwong, "High quality ultra-thin CVD HfO_2 gate stack with poly-Si gate electrode," in *IEDM Tech. Dig*., 2000, p. 31.

[86] P. S. Lyaaght, B. Foran, G. Bersuker, R. Tichy, L. Larson, R. W. Murto and H. R. Huff, "Physical characterization of high-κ gate dielectric film systems processed by RTA and spike anneal," Advanced Thermal Processing of Semiconductors, 2002. RTP 2002. 10th IEEE International Conference of 25-27 Sept. 2002 Page(s):93-98.

[87] Ernest Y. Wu and R.-P. Vollertsen, "On the Weibull shape factor of intrinsic breakdown of dielectric films and its accurate experimental determination—Part I: theory, methodology, experimental techniques," *IEEE Trans. Electron Devices*, vol. 49, no. 12, p. 2131, Dec. 2002.

[88] Ernest Y. Wu, J. Suñé and W. Lai, "On the Weibull shape factor of intrinsic breakdown of dielectric films and its accurate experimental determination—Part II: experimental results and the effects of stress conditions," *IEEE Trans. Electron Devices*, vol. 49, no. 12, p. 2141, Dec. 2002.

個人簡歷

姓名：李宗翰

性別：男

生日：民國 70 年 3 月 19 日

出生地：台灣省台北縣

學歷：

國立臺灣大學機械工程學系學士　　（88.9－92.6）

國立交通大學電子工程研究所碩士　（92.9－94.6）

碩士論文題目：

次世代快閃記憶體之氨氣氮化底多晶矽上多晶矽層間高介電常數介電質特性

Characteristics of the Inter-Poly High-κ Dielectrics on NH_3-Nitrided Bottom Poly-Si for Next Generation Flash Memories