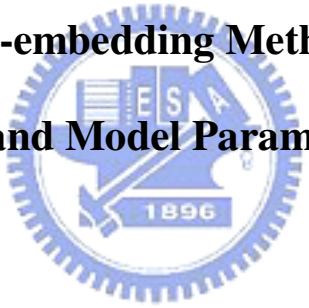
國立交通大學

電子工程學系 電子研究所

碩士論文

四極射頻金氧半電晶體於雙埠量測下的去寄生效應方法與參數萃取之研究

Study of Two-port De-embedding Method for Four-Terminal RF MOSFET and Model Parameter Extraction



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中華民國九十四年八月

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碩士論文

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中文摘要

無線通訊市場的蓬勃發展帶動了電子產品需求量的大幅上升。在激烈的競爭之下，具備低成本、高整合性、低功率的 CMOS 元件提供了射頻電路設計者一個很好的選擇。過去，晶圓廠所提供給客戶的元件樣本佈局(sample layout)中，Source 和 Body 是相連接在一起的，其所搭配的模型卡(model card)也是據此而作出。然而，電路設計者實際使用元件進行設計時，並不一定會將 S 和 B 連在一起。因此，現在晶圓廠傾向於直接提供給客戶 4-Terminal(4T)的樣本佈局，其所搭配的 model card 也是針對此情況而製作。以更符合實際上電路設計者使用元件的方式。

本論文使用 4T 的 NMOS 元件而仍置於 2-port 的 pad 之上進行 RF 量測並且進行參數粹取的工作。本研究對適合於 Two-port 量測的 de-embedding 方法以及參數萃取的方式作了一系列詳盡的探討，並提出了一系列適用於 4T NMOS 置於 2-port 的 de-embedding 以及參數萃取之方法。

此外，本論文利用軟體(Calibre-xRC)計算元件內部金屬彼此偶合的電容，並且分析元件佈局的不同對內部金屬電容的變化，探討佈局最佳化的策略。


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1896

Study of Two-port De-embedding Method for Four-Terminal RF MOSFET and Model Parameter Extraction

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Abstract

The fast development of wireless communication market increases the demand of electronic product. Under such a keen competition, CMOS transistor, which has the characteristics of low cost, high integration and low power, provides radio-frequency (RF) circuit designers an excellent choice. In the past, the Source and Body terminals of the MOS sample layout which foundries provide to customers are connected together. However it is not suitable for users. Therefore, foundries tend to provide 4-Terminal (4T) MOS sample layout to customers directly now.

In this thesis, 0.13μm process, 4T NMOS device is used for extraction but still put in 2-port pad to measure. This thesis includes a series of study and brings up a series of de-embedding and parameter extraction methods which are suitable for 4T NMOS under 2-port measurement.

This thesis utilizes software “Calibre-xRC” to calculate the interconnect capacitances coupling between device interconnect metals, and analyzes the capacitance variation to study the strategy of layout optimization.


E
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1896

Acknowledgment

感謝我的家人、朋友、以及女友一路來的支持。由於有他們的信任使我在經歷挫折之後而能重新爬起進而完成碩士學位。此論文的完成代表了他們對我的期許是值得的。

並且感謝指導教授的鞭策以及實驗室學弟們的鼎力相助 ，而能完成這份論文。此論文並非完美，但卻是兩年累積的微薄成果，希望能讓其他人有些許的用處。進而拋磚引玉，讓更多人投入此領域之研究。


E
S
A
1896

Contents


E
S
A
1896

Figure Captions

Chapter 1

Introduction

1.1 Research Motivation

With the rapid advancement of semiconductor technology, the size of transistor is scaled down aggressively to nanometer regime. Besides, because of the continuous expansion of wireless communication market, the demand of radio-frequency (RF) circuit products is increasing. In the view of circuit designers, under the consideration of high integration, low-cost of manufacture and low power, CMOS technology is an excellent choice. However, RF circuit designers usually meet a problem when designing their original circuit. When they proceed to simulate in advance, the simulated result and the measured result are always inconsistent. It means a feasible product needs to be built on the foundation of several tape-out fails. RF circuit designers have to rely on their intuition which is accumulated from experience, and fine tune their circuit and experience several times repeat tape-out to get a feasible product finally. But this kind of process will cost considerable and take much time. The reason that causes the mismatch of simulation and measurement is the inaccuracy of device model.

When a transistor is operated at radio-frequency, the parameters in original model are not enough to describe the transistor's performance. For this reason, a practicable way is to put some external elements in original model equivalent circuit to make this expansive model equivalent circuit sufficient to describe real

performance of device. These external elements include Gate resistance (R_G), Drain resistance (R_D), Source resistance (R_S), substrate components and some inductances and capacitances. We call them parasitic resistance, inductance, and capacitance.

The research motivation of this thesis is that we hope to build a reasonable model equivalent circuit. According to some numerical analysis, we can get the values of these parasitic components. Furthermore, we analyze these parasitic components physically, and explain their physical characteristics. Final, when the model is import to simulation software, the simulated result and measured result are coincident.

1.2 Thesis Organization

The theme of this thesis is the development of parasitic RLC extraction methods, the equivalent circuit analysis and verification for 4 terminals sub-μm MOSFET.

In Chapter 2, I will introduce the influence of interconnect capacitance and how to minimize it by layout optimization. In Chapter 3 to Chapter 5, the extraction methods adopted in this study will be described. Some necessary modifications have been done to conform to our test-key in which the equivalent circuit, numerical analysis, and equation derivation will be provided. The extraction method is built and verified for 0.13μm RF CMOS technology.

It is continuous from Chapter 3 to Chapter 5. In Chapter3, I introduce the measurement set and explain the de-embedding methods. Besides, according to my specific consideration, there is some minor modification on the de-embedding method.

In Chapter 4, I elaborate every extraction method of each parameter I extract. It includes my consideration and revision to make the extraction suitable for my test-key. In Chapter 5, I demonstrate all extracted parameters and their curves from measured data. After that, I analyze their characteristics and bring up a new extraction method of Gate and Drain resistance. Finally, in Chapter 6, I explain the appropriate, reformed layout and extraction for next tape-out. This thesis can provide an extraction reference for others research workers.


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1896

Chapter 2

Interconnect Capacitance

2.1 Introduction

A NMOS transistor is composed of p-substrate, n+ doped source and drain regions, n+ poly-Gate, and so on. A circuit designer will put the transistor in his circuit and use metal to connect it with other devices. Based on MOSFET layout analysis, we see that both metal-to-metal and metal to contact introduce interconnect coupling capacitances. Because they belong to device, they are more complicated to be analyzed and extracted than the general inter-metal coupling capacitance introduced by back-end process as pure interconnection lines.

If the transistor is not very small, and the circuit is not operated at very high frequency, these capacitances can be neglected because they are too small compared with intrinsic capacitances. However, if the transistor is very small, and the operating frequency is very high, these capacitances should not be neglected because of the small intrinsic capacitances and the small impedance across the interconnect capacitance. Please see Fig.2-1. (The impedance across capacitance is $1/\omega C$)

In this Chapter, I name the capacitance with a suffix “m”. It means the interconnect capacitance is coupled between metals inner device.

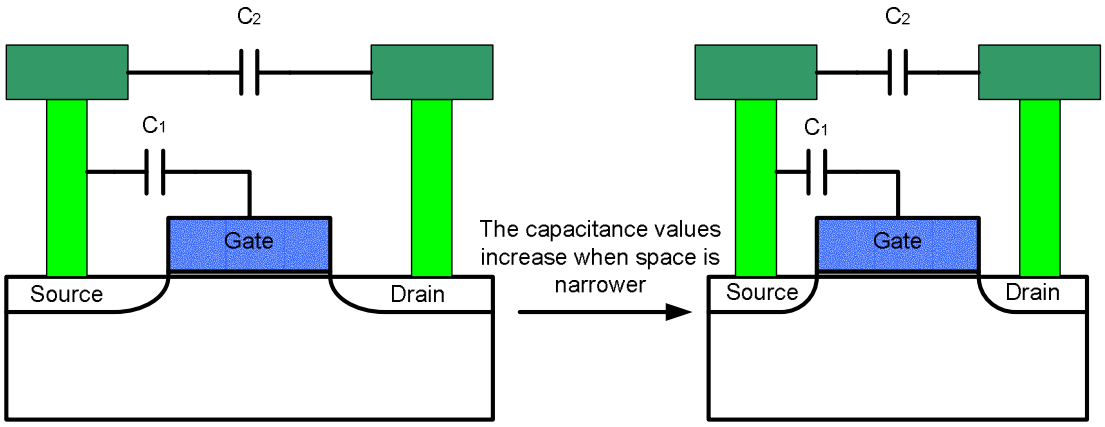


Figure 2 - 1: the interconnect capacitance chart

These capacitances will affect the performance of MOS. For example, f_T, the cut-off frequency, is a parameter to know how fast this transistor can operate. There is a rough formula can estimate f_T: $\mathbf{f_T \cong \frac{g_m}{C_{gs}+C_{gd}}}$ when C_{gs} increase, f_T decreases.

It shows the fact that when device is very small, interconnect capacitance will degrade the performance.

2.2 Layout Analysis and Optimization Strategy

Fig.2-2 and Fig.2-4 are the layout of NMOS transistor before and after layout optimization. Now I analyze their interconnect capacitance from the view of their structure to explain that after optimization, the interconnect capacitance effect decreases. The cross-section views of the layout before and after optimizing are showed in Fig.2-2 and Fig.2-3.

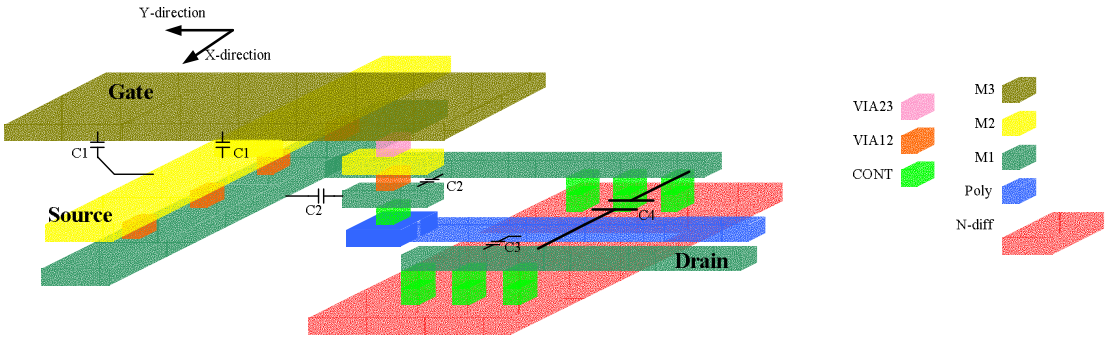


Figure 2 - 2: the cross-section view of NMOS before optimizing

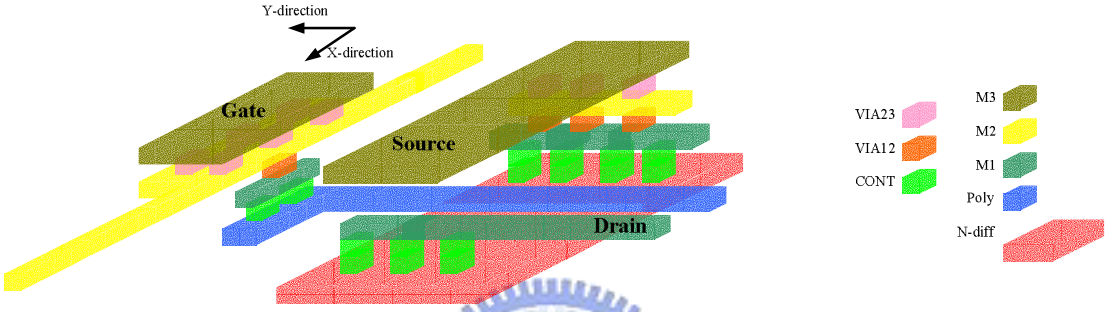


Figure 2 - 3: the cross-section view of NMOS after optimizing

2.2.1 Gate to Source Coupling Capacitance - C_{gs_m}

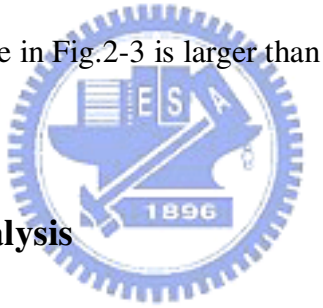
The gate to source coupling capacitance (C_{gs_m}) in Fig.2-2 is mainly contributed from the first element Gate-M3 and Source-M2 coupling and the second element from Gate-M1 and Source-M1 coupling. But, in Fig.2-3, the capacitance value decreases much because 1st: Source metal is stacked to M3, and connect to terminal in X-direction; 2nd: the Gate-poly terminator in Fig.2-3 is connect in U-shape. So the Gate-M3 doesn't overlap Source metal. Besides, Gate-M1 and Source-M1 are staggered and separated in a distance. Such a layout design decrease the interconnect C_{gs} value.

2.2.2 Gate to Drain Coupling Capacitance - C_{gd_m}

C_{gd_m} value is contributed by Gate-poly and Drain-M1 coupling. Because the layout shape of Drain doesn't change much, the C_{gd_m} values of Fig.2-2 and Fig.2-3 are closed. Because the space between Gate-poly and Drain-M1 in Fig.2-2 is wider than in Fig.2-3, C_{gd} value in Fig.2-3 is larger than in Fig.2-2.

2.2.3 Drain to Source Coupling Capacitance - C_{ds_m}

C_{ds_m} value is mainly contributed by Drain-M1 and Source-M1 coupling. When the transistor is smaller, the space between Drain-M1 and Source-M1 is narrower. And it explains that C_{ds_m} value in Fig.2-3 is larger than in Fig.2-2.



2.3 Simulation result analysis

In section 2.2, Fig.2-3 layout is the optimized result of Fig.2-2 layout to reduce interconnecting coupling capacitance. To prove it, I use the software Calibre-xRC developed by Mentor-Graphic to calculate the coupling capacitance between different metals. Table 2-1 is the simulation result. The device used to be simulated is 0.13μm NMOS whose finger number is 18.

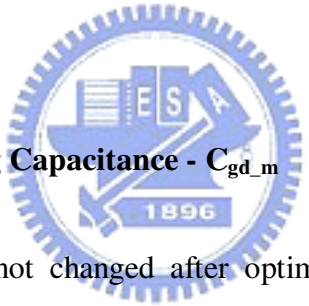
Unit: fF	C_{gs_m}	C_{gd_m}	C_{ds_m}
Before optimize	4.36988	2.1651	2.8203
After optimize	1.68503	2.3036	4.53245

Table 2 - 1: the interconnect capacitance values of NMOS whose finger number is 18 (unit:fF)

According to Table 2-1, the C_{gs_m} value decreases much, C_{gd_m} value increases little and C_{ds_m} value increases much.

2.3.1 Gate to Source Coupling Capacitance - C_{gs_m}

Compare Tab.2-2 and Tab.2-3, we can find that before layout optimizing, interconnect C_{gs_m} is mainly contributed by (1)Gate-M3 and Source-M2 overlap coupling and (2)Gate-M1 and Source-M1 sideward coupling. After layout optimizing, the overlap coupling and sideward coupling are eliminated or minimized. This layout design results in interconnect C_{gs_m} decreasing.



2.3.2 Gate to Drain Coupling Capacitance - C_{gd_m}

Drain layout shape is not changed after optimizing. The interconnect C_{gd_m} value is not changed much which is mainly contributed by Gate-poly and Source-M1 coupling.

2.3.3 Drain to Source Coupling Capacitance - C_{ds_m}

Interconnect C_{ds_m} is mainly contributed by Drain-M1 and Source-M1 sideward coupling. We hope the device size smaller, and then the space between Drain-M1 and Source-M1 will be narrower. Because device performance is not affected by C_{ds_m} much, decrease in C_{gs_m} value is chosen first in the optimization work.

Besides, Table 2-4 is the simulated interconnect capacitance between every

terminal.

	C_{gs_m}	C_{gd_m}	C_{ds_m}	C_{gb_m}	C_{db_m}	C_{bs_m}
NF=18	1.68503	2.3036	4.53245	0.200926	0.451989	0.262949
NF=36	3.0508	4.45151	9.04583	0.233144	0.833048	0.278357
NF=72	5.78234	8.74732	18.0726	0.297582	1.59517	0.309175

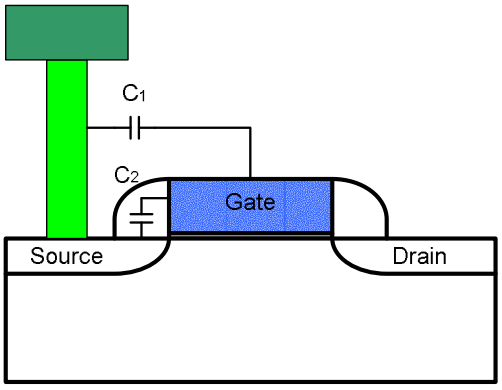
Table 2 - 2: simulated interconnect capacitance of each finger number NMOS (unit:fF)

2.4 Spacer Fringing Capacitance Analysis

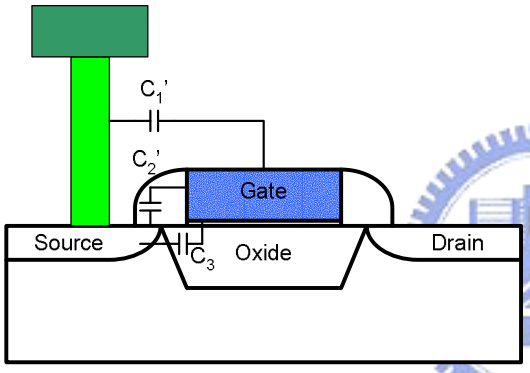
2.4.1 Introduction

Not only the metal coupling capacitance, but also the capacitances between Gate-poly and Drain/Source diffusion region through spacer should not be neglected when the device is scaled down to nanometer level.

Please see the figure showed below left, C_1 represents the coupling capacitance between Gate-poly and contact and C_2 represents the coupling capacitance through spacer. When device is not very small, the space between Gate-poly and contact is wide and C_1, C_2 values are small relative to intrinsic C_{gs}. However, because fast development of the semiconductor technology, the device size has been extreme small and the space between Gate-poly and contact has been very narrow. Therefore, C_1 and C_2 values should not be neglected.



However, there is not effective method to measure the values of these capacitances. De-embedding process at least removes the capacitance coupling higher than contact. The C_1 and C_2 in above figure are always included in extracted capacitance values. Nevertheless, we can calculate out these values by the 3-D simulation tools such as Raphael. We are not sure the accuracy of the simulated intrinsic capacitance which is coupling through the substrate. However we can simplify the device situation. We design a test-key, and the region under Poly-Gate is not channel but oxide. The cross-section view of the test-key is showed below left.



Of course it is not MOS transistor anymore but it simplify the situation of interconnect coupling because semiconductor intrinsic capacitance is excluded. Because there must been a minimum space between diffusion active region and Poly-Gate, the coupling capacitance between Poly-Gate and contact and through spacer are not the same as mentioned formerly. In the above left figure, I use C_1' and C_2' to distinguish from former ones. Furthermore, C_3 represents the coupling capacitance through the oxide under Poly-Gate.

We use RF measurement equipment to measure the s-parameters of the test-key and then extract C_{gs}, C_{gd} values from the measured data (About the RF measurement, it will be introduced in Chapter 3). In addition, we use the TCAD tool: Raphael to calculate the capacitance values. Here I name the calculated spacer capacitance with a suffix “sp”. If the measured capacitance values are close to simulated values, it means that the simulation tool: TCAD is reliable about the capacitance-in-oxide calculation.

(The materials of spacer are oxide, too)

2.4.2 Measurement and simulation analysis

"S" in the Table 2-5 represents the distance from poly edge to active region edge. Because the region under Gate-poly is oxide, the equivalent circuit is quite simple. Therefore we can extract the capacitances from the formulas:

$$C_{gg} = C_{gs} + C_{gd} = \frac{Im(Y_{11})}{\omega}$$

The extracted capacitances are showed in Table 2-5.

	S=0.07, NF=36	S=0.14, NF=36	S=0.21, NF=36
$C_{gg\_sp}=C_{gs\_sp}+C_{gd\_sp}$	0.312986	0.281111	0.285417

Table 2 - 3: the extracted C_{gg} values of test-key (unit: fF/um)

Besides, we build a device structure of test-key and import the source file to Raphael, and then simulating the sum of capacitance values which are coupled from Gate to Source and Gate to Drain.

Moreover, the extracted capacitances include interconnect capacitance because the open pad used for de-embedding just reserve the metals higher than M3. Therefore, the simulated interconnect capacitances should be added. Here I use the tool: Calibre-xRC to calculate the interconnect capacitance of the test-key. The simulated result is showed in Table.2-6.

	S=0.07	S=0.14	S=0.21
Interconnect C_{gg_m}	0.059084	0.06018	0.069056
Spacer C_{gg_sp}	0.243308	0.188227	0.164437
sum	0.302392	0.248407	0.233493

Table 2 - 4: the simulated C_{gg} values of test-key (unit: fF/um)

Comparing Table 2-5 and Table 2-6, we can find the simulated value and the measured values are close. This fact tells up that the simulation is believable and hence, the effects we analyze by the help of the tools such as interconnect capacitance and spacer capacitance are reliable.


E
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A
1896

Chapter 3

RF Measurement and De-embedding

3.1 RF Measurement

For the purpose of extracting MOS transistor parameters from measured data, on-chip RF measurement is adopted because of its accuracy. The data we get not only includes device's performance but also the influence of the pad, coaxial cable and equipment. Before we put the die in the probe station, system calibration needs to be performed first to remove the influence of equipment, signal line and make the reference plane locates at the probe tips. (Fig.3-1)

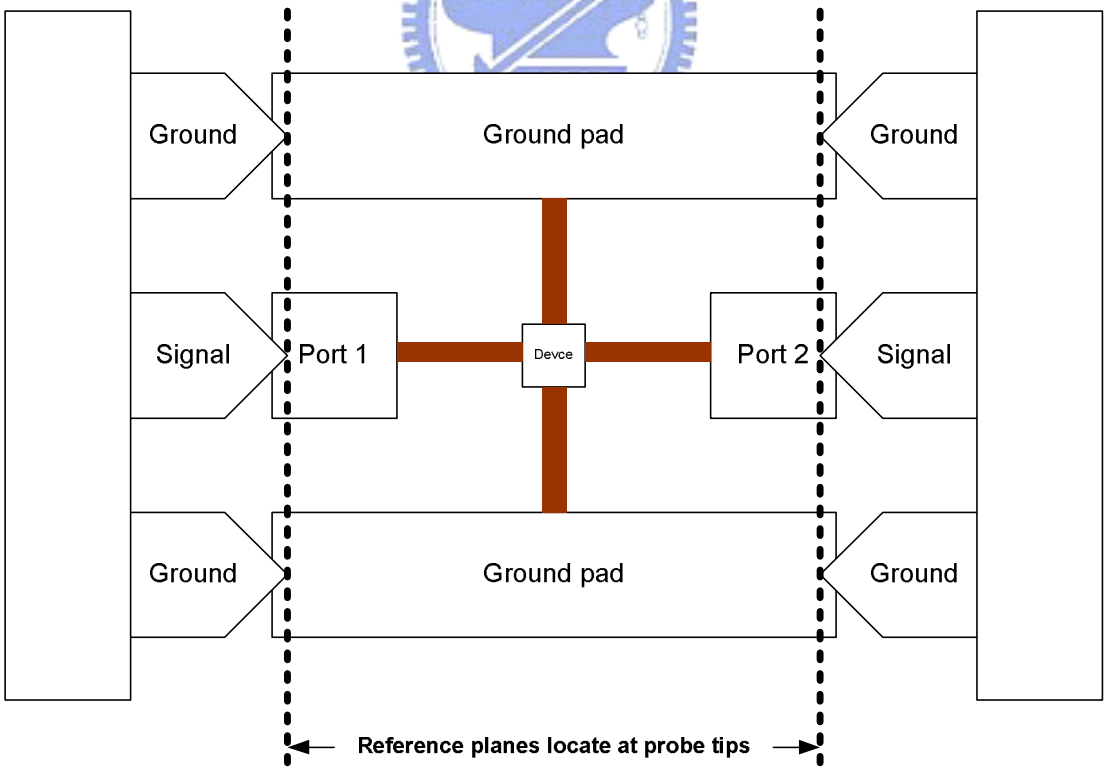


Figure 3 - 1: illustration of RF measurement for a two-port system

2-port system is adopted. (Please see Fig.3-2) It is because our measurement equipment (which will be mentioned in 3.1.2), system calibration technique and de-embedding method (which will be mentioned in 3.2) are mainly for 2-port measurement. We can still design a 4-port test patter to extract parameters, but the measurement system with special calibration techniques, and the de-embedding method are more complicated and not complete enough.

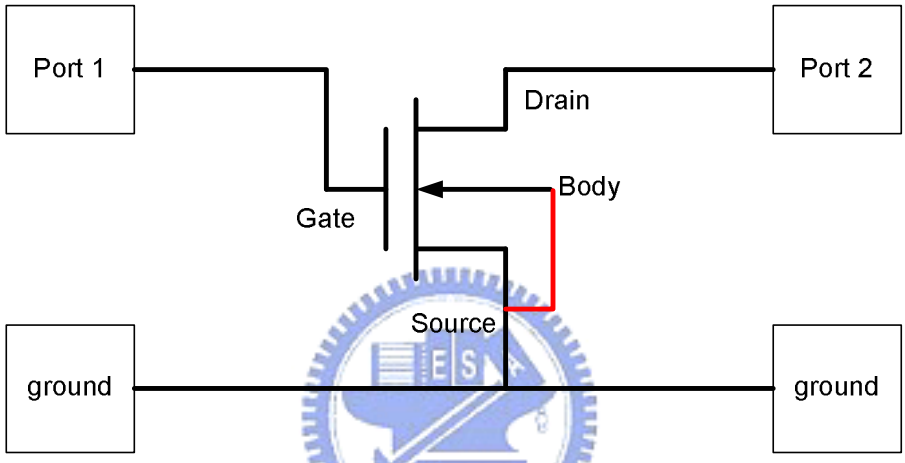


Figure 3 - 2: illustration of RF measurement for a two-port transistor

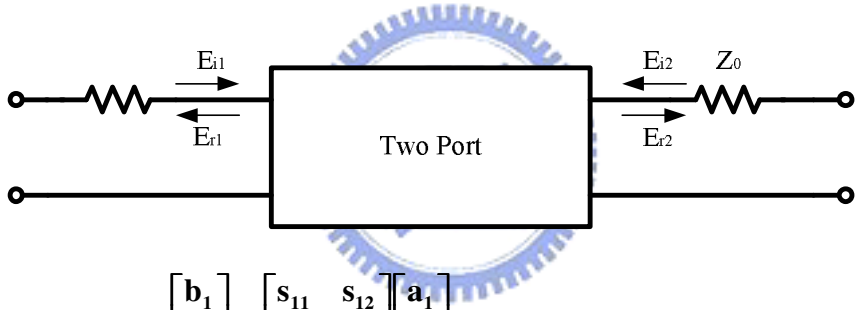
Typically speaking, the system calibration for on-wafer measurement is done by using a so-called impedance standard substrate (ISS) that can provide high-accuracy and low-loss standards for two-port calibration procedures such as short-open-load-through (SOLT) and through-reflect-line (TRL). The SOLT calibration has been widely used because it is supported by virtually every VNA. [1]

3.1.1 Two-Port Scattering Parameters

It is more suitable for two-port RF measurement to use scattering parameters

(s-parameters) to replace impedance and admittance parameters (z-, y-parameters). Because when device is operated at high frequency, it is quite difficult to provide adequate shorts or opens, particularly over a broad frequency range. Furthermore, active high-frequency circuits are frequently rather fussy about the impedance into which they operate, and may oscillate or even expire when terminated in open or short circuit. [2]

Please see the figure showed below, s-parameters defines input and output variables in terms of incident and reflected (scattered) voltage waves, rather than port voltage or current. Furthermore, the source and load termination are Z_0.



$$\begin{bmatrix} \mathbf{b}_1 \\ \mathbf{b}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{s}_{11} & \mathbf{s}_{12} \\ \mathbf{s}_{21} & \mathbf{s}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{a}_1 \\ \mathbf{a}_2 \end{bmatrix}$$

where

$$\mathbf{a}_1 = \mathbf{E}_{i1} \Big/ \sqrt{\mathbf{Z}_0}$$

$$\mathbf{a}_2 = \mathbf{E}_{i2} \Big/ \sqrt{\mathbf{Z}_0}$$

$$\mathbf{b}_1 = \mathbf{E}_{r1} \Big/ \sqrt{\mathbf{Z}_0}$$

$$\mathbf{b}_2 = \mathbf{E}_{r2} \Big/ \sqrt{\mathbf{Z}_0}$$

and

$$\mathbf{s}_{11} = \left.\frac{\mathbf{b}_1}{\mathbf{a}_1}\right|_{\mathbf{a}_2=0} = \frac{\mathbf{E}_{r1}}{\mathbf{E}_{i1}} \qquad \mathbf{s}_{12} = \left.\frac{\mathbf{b}_1}{\mathbf{a}_2}\right|_{\mathbf{a}_1=0} = \frac{\mathbf{E}_{r1}}{\mathbf{E}_{i2}}$$

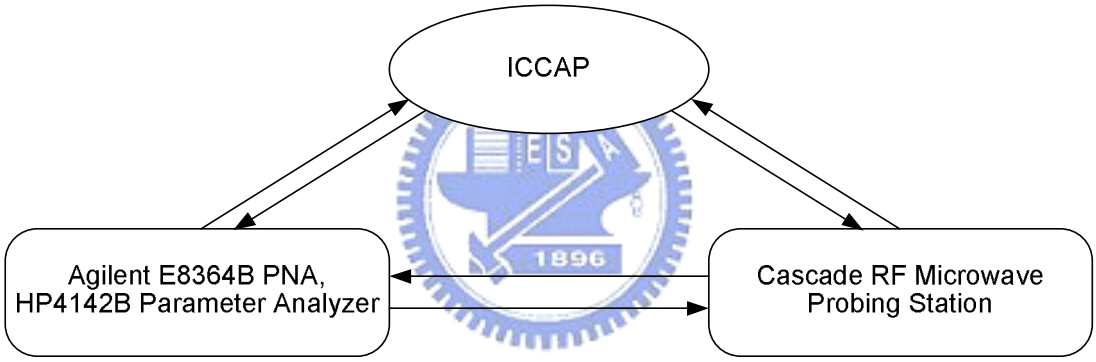
$$\mathbf{s}_{21} = \left.\frac{\mathbf{b}_2}{\mathbf{a}_1}\right|_{\mathbf{a}_2=0} = \frac{\mathbf{E}_{r2}}{\mathbf{E}_{i1}} \qquad \mathbf{s}_{22} = \left.\frac{\mathbf{b}_2}{\mathbf{a}_2}\right|_{\mathbf{a}_1=0} = \frac{\mathbf{E}_{r2}}{\mathbf{E}_{i2}}$$

The normalization by the square root of Z_0 is a convenience that makes square of the magnitude of the various a_n and b_n equal to the power of the corresponding

incident or reflected wave. s_{11} is simply the input reflection coefficient, s_{12} is the reverse transmission, s_{21} is a sort of gain and s_{22} is the output reflection coefficient. [2]

3.1.2 RF Measurement Equipment

The figure showed below illustrates our setup of HF measurement system for on-wafer RF measurements. ICCAP is used to send the commands to instruments (Agilent E8364B PNA, and HP4142B) and the probing station is to perform the measurements for a specific DUT and to gather the measured data for extraction. [1]



3.2 Two-Port de-embedding

After system calibration is accomplished, the reference plane is located at the probe tips. However, the measured data still includes the pad effects which consist of capacitive, inductive and resistive effects. Our goal is to get the measured data of "pure" device. It is necessary to remove the parasitic effect of the pads including the metal line connecting signal pad and device. There are some techniques developed to remove these pad parasitic effect which is so-called de-embedding.

3.2.1 Open pad de-embedding

The most conventional and easiest method for obtaining the "pure" transistor's measured data is to use an extra "open" pad.

When the transistor device is measured with the GSG pad, the layout is like Fig.3-3, the equivalent circuit is as Fig.3-4 and the open pad's equivalent circuit is as Fig.3-5 and Fig.3-6.

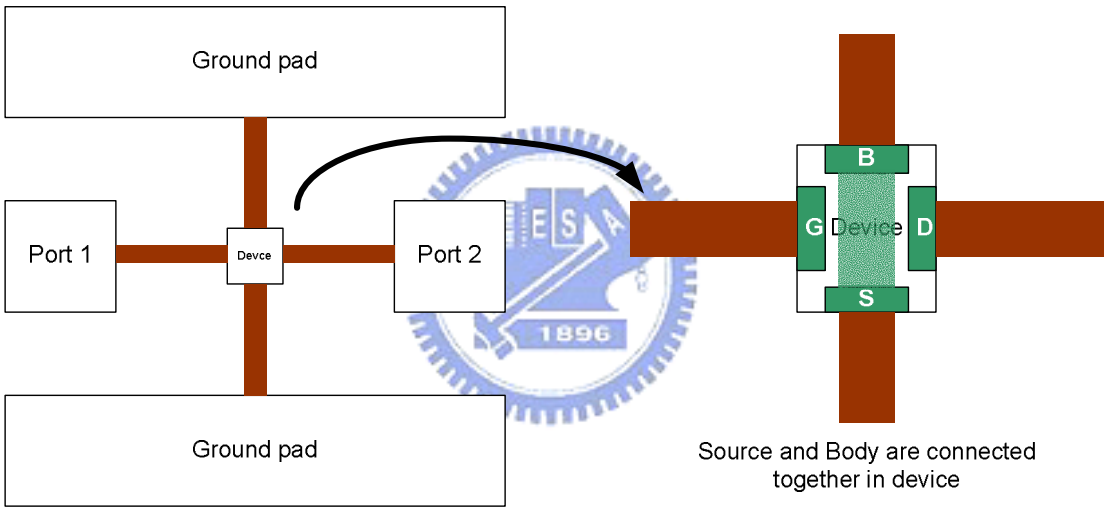


Figure 3 - 3: the illustration of device with pad (S and B are connected)

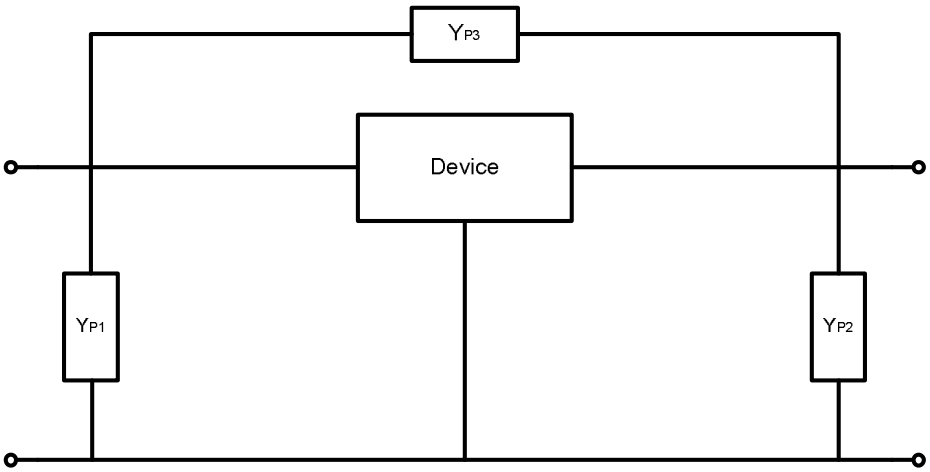


Figure 3 - 4: the equivalent circuit of device with pad

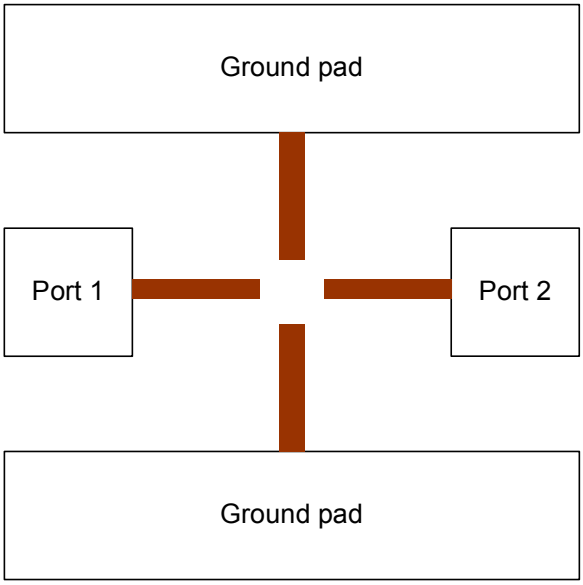


Figure 3 - 5: the illustration of open pad layout

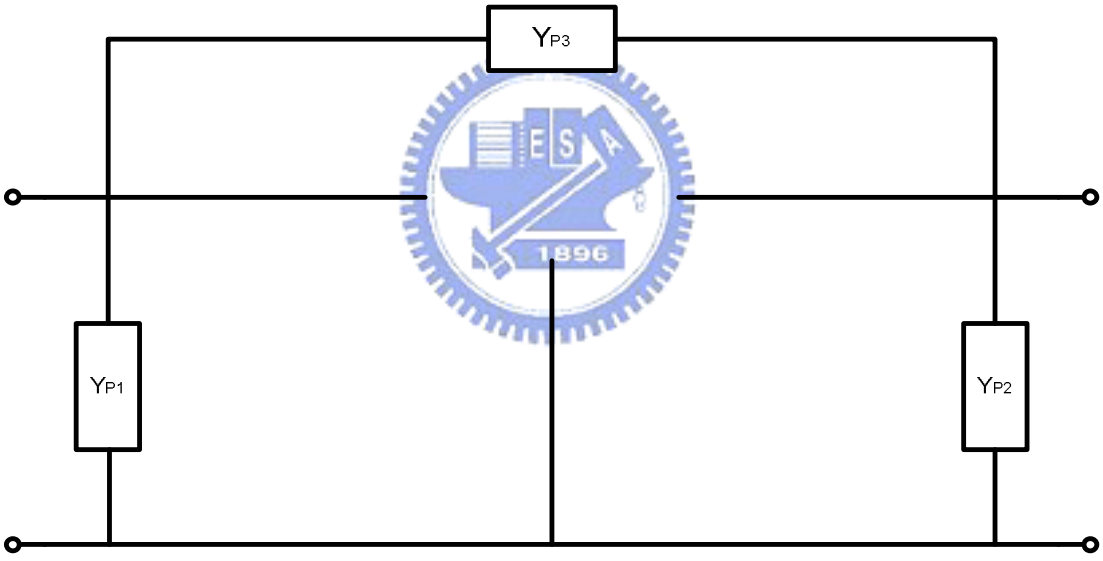


Figure 3 - 6: the equivalent circuit of open pad

After getting the measured s-parameters from device with pad and from open pad, we transform them to y-parameters and then we can get the transistor y-parameters by subtracting Y_{P1}, Y_{P2} and Y_{P3} from the measured data of transistor with pad. Theoretically, after this step, we get the pure measured data of transistor.

We name the y-parameter of device with pad "Y_{meas}", and the y-parameter of open dummy "Y_{open}", and then

$$\mathbf{Y}_{open} = \begin{bmatrix} \mathbf{Y}_{P1} + \mathbf{Y}_{P3} & -\mathbf{Y}_{P3} \\ -\mathbf{Y}_{P3} & \mathbf{Y}_{P2} + \mathbf{Y}_{P3} \end{bmatrix} \cdots\cdots\cdots (3.1)$$

$$\mathbf{Y}_{dut} = \mathbf{Y}_{meas} - \mathbf{Y}_{open}$$

3.2.2 Open, short pads de-embedding

The de-embedding method expounded in 3.2.1 has a defect that it neglects pad parasitic series effects of the connecting metal line. When device is very small, and operating frequency is very high, the resistive and inductive effect caused by the metal line should not be neglected. So it is necessary to use one more extra dummy pad such as "short" pad to remove the series parasitic components.

Under the considering of pad parasitic series effect, the equivalent circuit of device with GSG pad is as Fig.3-7. The short pad's equivalent circuit is as Fig.3-8, Fig, 3-9.

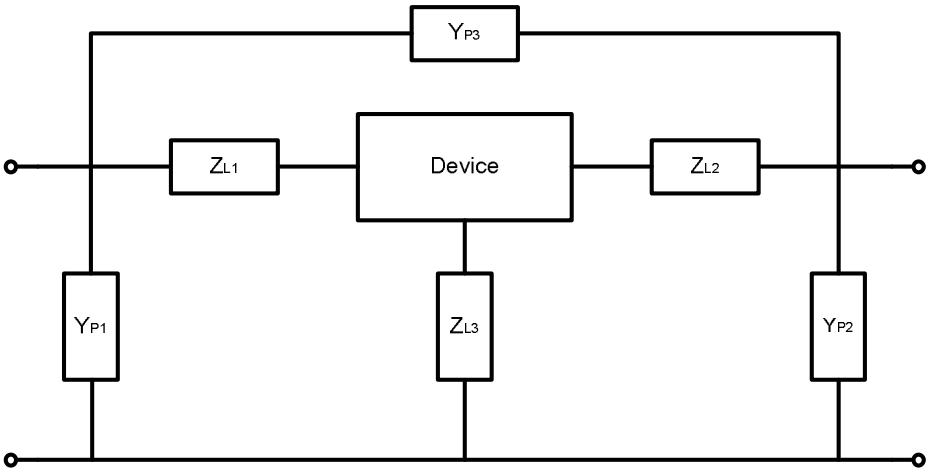


Figure 3 - 7: the equivalent circuit of device with pad

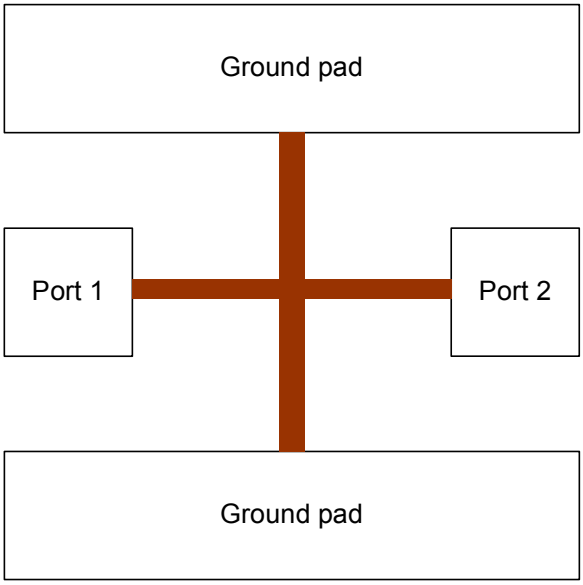


Figure 3 - 8: the illustration of short pad

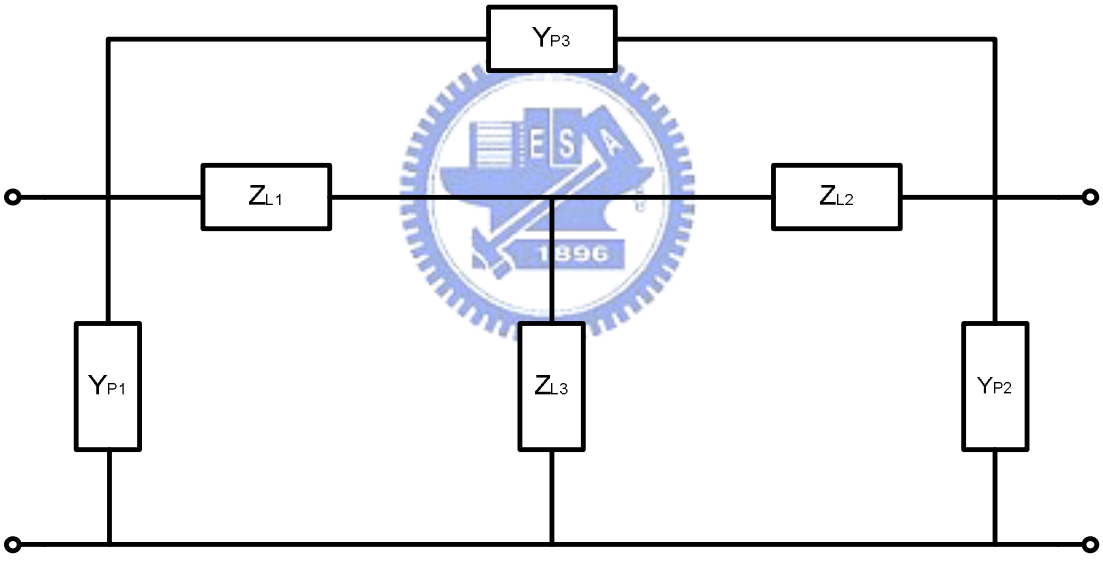


Figure 3 - 9: the equivalent circuit of short pad

The first step is to get the Y_{P1}~Y_{P3} value by measuring open pad and the method is mentioned in 3.2.1. After removing Y_{P1}~Y_{P3}, secondly, we have to remove Z_{L1}~Z_{L3}. We measure the s-parameters of short pad and transform it to y-parameter, and then use y-parameter matrix calculation to remove Y_{P1}, Y_{P2} and Y_{P3} in short pad. Finally, we transform all measured data to z-parameters and use z-parameter matrix

calculation to remove Z_{L1}, Z_{L2} and Z_{L3} in the measured data of device with pad. Please see Fig.3-10 and the equations are showed below [3].

$$\mathbf{Y}_{short} - \mathbf{Y}_{open} = \mathbf{Y}_1$$

$$\mathbf{Y}_1^{-1} = \begin{bmatrix} \mathbf{Z}_{L1} + \mathbf{Z}_{L3} & \mathbf{Z}_{L3} \\ \mathbf{Z}_{L3} & \mathbf{Z}_{L2} + \mathbf{Z}_{L3} \end{bmatrix} \cdots\cdots\cdots (3.2)$$

$$\mathbf{Y}_{meas} - \mathbf{Y}_{open} = \mathbf{Y}_2$$

$$\mathbf{Z}_{dut} = \mathbf{Y}_2^{-1} - \mathbf{Y}_1^{-1}$$

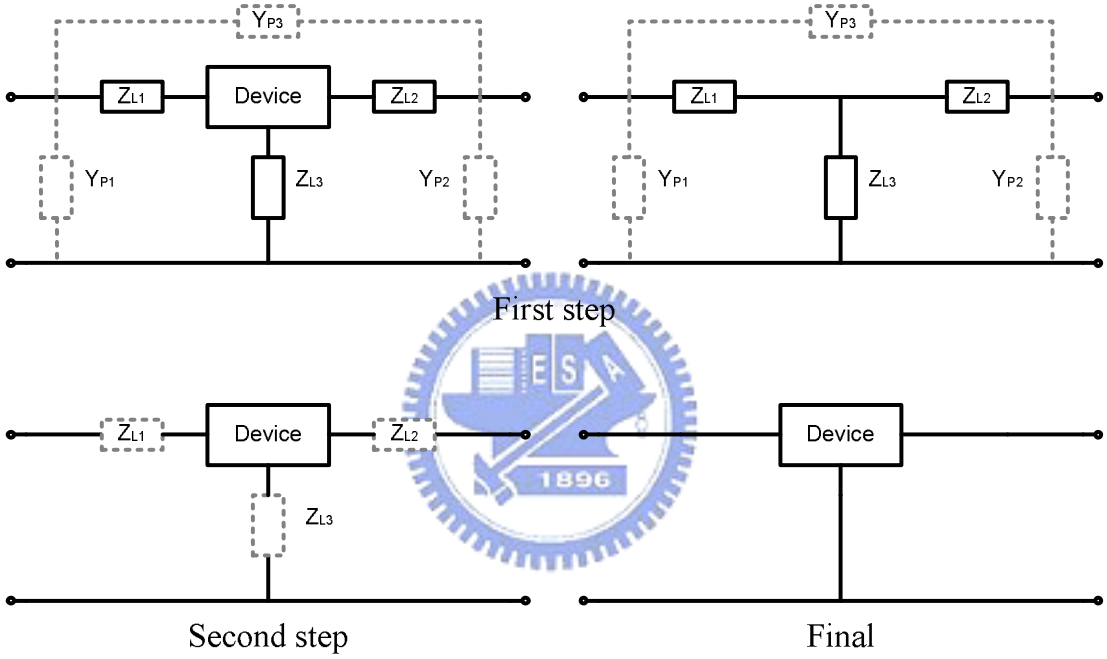


Figure 3 - 10: the illustration of de-embedding procedure

3.2.3 Revised de-embedding method for our case

The de-embedding method mentioned in 3.2.1 and 3.2.2 is based on an important fact that the transistor is under 2-port GSG pad measurement. So, it is necessary to connect Source and Body together inter device and then connect to ground pad (Fig.3-3). However, 4-terminal (Gate, Drain, Source, and Body) MOS transistor is more practical to circuit designer because it is more flexible. They would

like to connect Body terminals to ground line individually to make sure the pn-junction between p-substrate and n+ Drain in nMOS is under reverse-bias and prevent substrate affecting nMOS operation. And designer might bring into Body effect by connecting Body to other node except Source or ground to make his circuit fit specification.

Therefore, the latest sample layout which foundry provides to customers doesn't connect Source and Body inter-device. We didn't change the indigenous layout and connect the Gate, Drain to two individual signal pads and connect Source, Body to ground pads separately. (Fig.3-11)

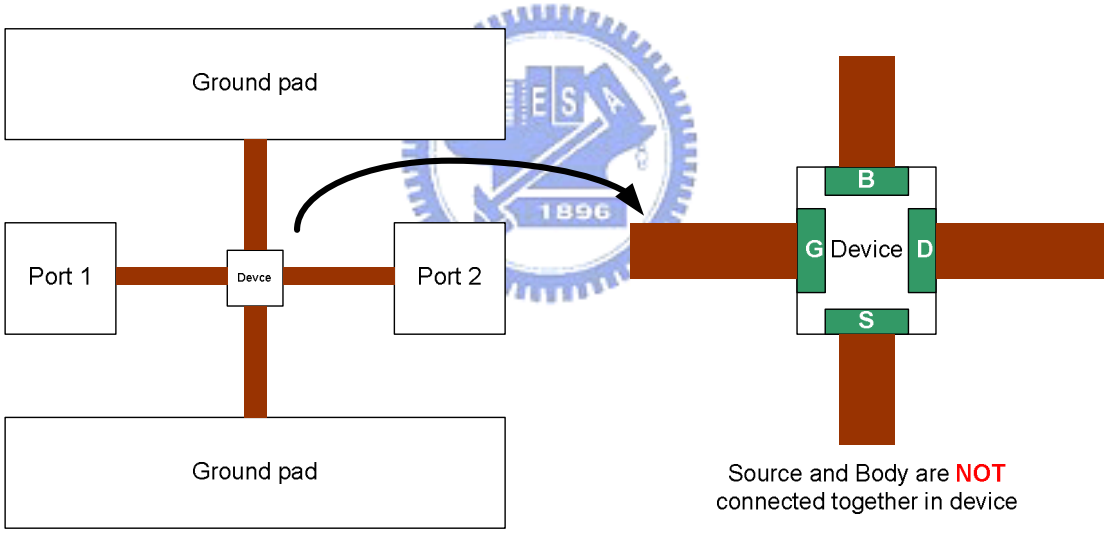


Figure 3 - 11: the illustration of device with pad (S and B are separated)

Furthermore, 4-terminal transistor under 4-port RF measurement and corresponding system calibration, de-embedding methods are continuous developed, but not matured yet and will be very complicated expectedly.

Here I provide a revised de-embedding procedure which comes from my

practical measurement experience. And it is suitable for 4-terminal transistor but under 2-port GSG pad (Fig.3-11).

The equivalent circuit of measured device with pad is as Fig.3-12. I change the characters of the pad parasitic series components for later explanation. Z_{g_ext} means the parasitic effect of the metal line connecting signal pad and Gate terminal of transistor and so do Z_{d_ext}, Z_{b_ext}, and Z_{s_ext}. If the Source and Body are connected together first and then connect to ground pad, Z_{s_ext} and Z_{b_ext} are parallel and can be represented by Z_{L3} in Fig.3-7.

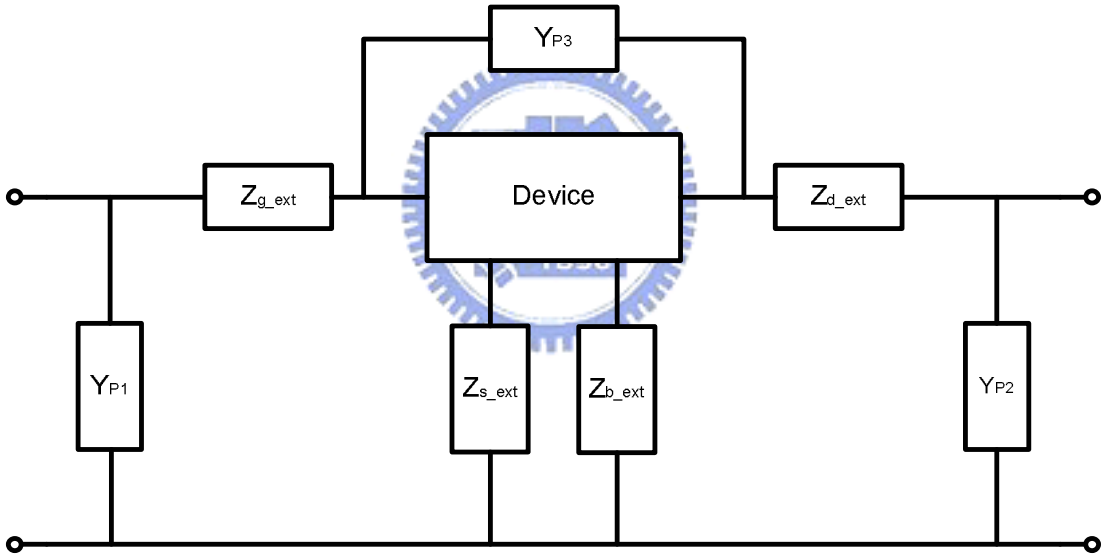


Figure 3 - 12: the equivalent circuit of device with pad (S and B are separated)

First, I extract Y_{P1}, Y_{P2}, and Y_{P3} from measured data of open pad (equation 3.1) and then subtract "just" Y_{P1} and Y_{P2} from measured data of device with pad (Fig.3-13 (a)).

Second, I extract Z_{g_ext} and Z_{d_ext} from measured data of short pad (equation 3.2)

and then subtract them from the data after first step (Fig.3-13(b)).

Third, subtract Y_{P3} from the data after second step. The reason subtracting Y_{P3} at last is the Y_{P3} is almost capacitive and contributed by near metals which are located at the end of connecting metal line of port 1 and port 2. The original equivalent circuit shows that the nodes of Y_{P3} are at the pad which contacts probe tip. It is not reasonable that they should be at the terminators of metal lines. So Y_{P3} should be subtracted at last. (Fig.3-13)

Although the metal lines connecting to Source and Body are retained, it is practicable to put external resistance or inductance to fit the measured curve. If we just use the de-embedding method mentioned in 3.3.2 which is designed under the consideration of Source and Body tied together first, it will generates an irrelevant data because of the incongruous de-embedding steps. And the model-building work cannot go on.

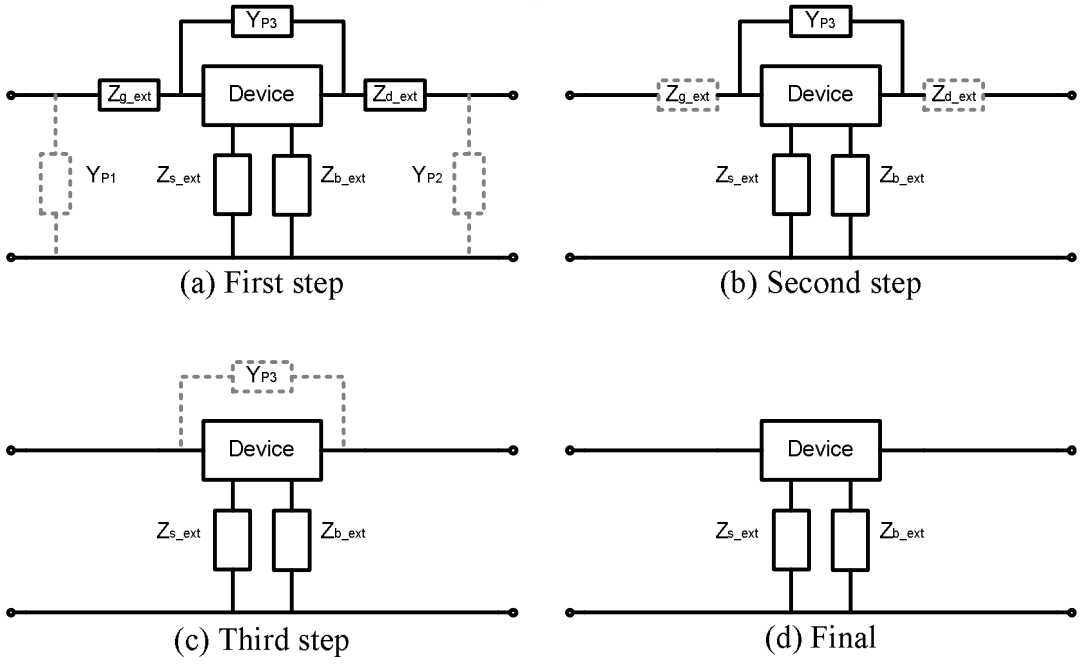


Figure 3 - 13: the revised de-embedding procedure

3.3 Extraction of PAD parasitic resistance and inductance

The Z_{L1} and Z_{L2} in Fig.3-9 are regarded the same as Z_{g_ext} and Z_{d_ext} in Fig.3-12. However, each time you raise your probe and put down again to measure, the parasitic series resistances are different. The short pad de-embedding includes measured errors innately. But de-embedding procedure is still necessary because it at least decreases much pad effects from measured data of DUT. We can just observe the pad parasitic series resistance and inductance by the short pads.

The right above figure in Fig.3-10 shows that the short pad equivalent circuit subtracting Y_{P1}, Y_{P2}. And then Z_{L1} and Z_{L2} can be extracted from the formulas which are $Z_{L1}=Z_{11}-Z_{12}$, $Z_{L2}=Z_{22}-Z_{12}$. And then

$$\mathbf{Z_{L1} = Z_{11} - Z_{12}}$$
$$\mathbf{Z_{L2} = Z_{22} - Z_{12}}$$
$$\mathbf{R_{g\_ext} = re(Z_{g\_ext}) = re(Z_{L1}),\quad L_{g\_ext} = \frac{im(Z_{g\_ext})}{\omega} = \frac{im(Z_{L1})}{\omega}} \quad \cdots\cdots\cdots\mathbf{(3.3)}$$
$$\mathbf{R_{d\_ext} = re(Z_{d\_ext}) = re(Z_{L2}),\quad L_{d\_ext} = \frac{im(Z_{d\_ext})}{\omega} = \frac{im(Z_{L2})}{\omega}}$$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Chapter 4

Model Parameters Extraction

The extraction work is divided into two steps. First, extracting parameter values and second, using these values as initial values of each component in model equivalent circuit and fine-tuning them to make the simulated curves of equivalent circuit match the measured curves. In the first step, the substrate effect is neglected to simplify the equivalent circuit and make it easier to extract most parameters. I will extract intrinsic resistances and intrinsic capacitances in $V_{gs}>V_{th}$, $V_{ds}=0$ or 1.2V and then extract substrate parameters in $V_{gs}=V_{ds}=0$. Therefore, before second step, we will have many initial values of parameters including interconnect capacitances which are expounded in Chapter 2. There is one point noticeable: in first step, the path through junction capacitance C_{jd} is neglected because we ignore substrate effect, but the path through C_{js} need to be handle carefully because the inductance L_{s_ext} makes the real part of the impedance see into node "ns" (Please see Fig.4-2) to ground is serious frequency-dependent [Appendix [a.3]].

4.1 Intrinsic Resistance

In Chapter 3, I explain the little revised de-embedding method I use. And I utilize short pad to extract the extrinsic resistances and inductances which result from the connecting metal line between Gate-port1 and Dran-port2. In this section, I will extract the resistances which belong to "intrinsic" transistor. These resistances are so-called intrinsic resistance. The extrinsic resistances have been removed after

de-embedding.

Basically, the intrinsic resistance is composed of two-parts: one is bias-independent which results from process materials such like Poly-silicon, salicide and the other is bias-dependent which results from channel characteristics.

4.1.1 Gate, Drain resistances extraction

1. V_{ds}=0, V_{gs}>V_{th}

Here I bring up a new method to extract the Gate and Drain bias-independent resistances. And then extract the channel resistance under V_{ds}=0, V_{gs}>V_{th}. In BSIM model card, channel resistance is used to model non-quasi-static (NQS) effect which is a very important parameter when device is operated at high frequency [4]. When a MOS is operated at V_{ds}=0 and V_{gs}>V_{th}, the channel is formed. If the operating frequency is very high, the region under the gate is like a distributed, uniform, resistance-capacitance (RC) transmission line.

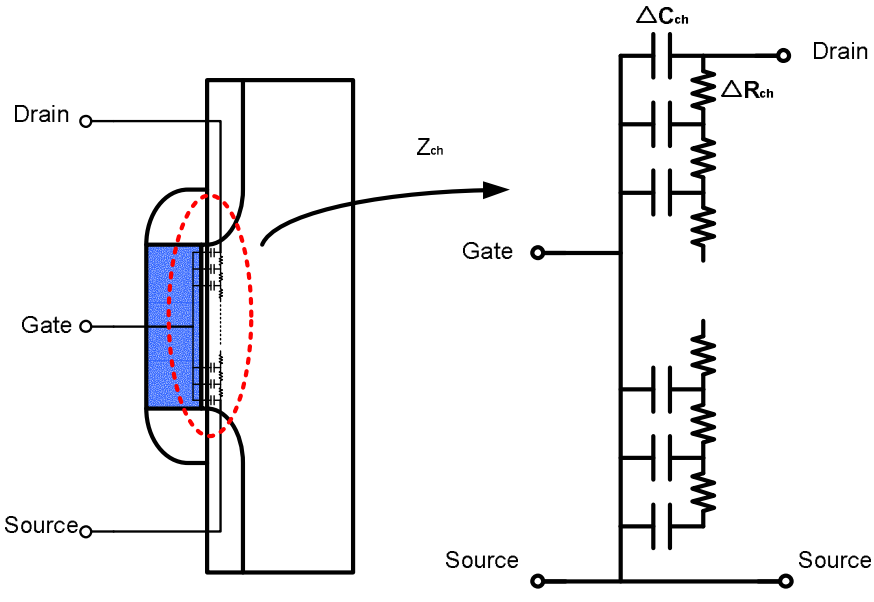


Figure 4 - 1: channel RC transmission line

In the Fig.4-1, Z_{ch} represents the two-port z-matrix of the channel which is a RC transmission line. The total capacitance under gate is C_{ch} and the total resistance is R_{ch}. We can derive the Z_{ch} matrix and the result is showed below [5]:

$$\mathbf{Z_{ch}} = \begin{bmatrix} \dfrac{\gamma L}{j\omega C_{ch}\tanh(\gamma L)} & \dfrac{\gamma L(\cosh(\gamma L)-1)}{j\omega C_{ch}\sinh(\gamma L)} \\ \dfrac{\gamma L(\cosh(\gamma L)-1)}{j\omega C_{ch}\sinh(\gamma L)} & \dfrac{2\gamma L(\cosh(\gamma L)-1)}{j\omega C_{ch}\sinh(\gamma L)} \end{bmatrix}$$

$$\gamma L = \sqrt{j\omega C_{ch} R_{ch}}$$

$$\text{If} \quad \left|(\gamma L)^2\right| = \omega C_{ch} R_{ch} << 1,$$

$$\mathbf{Z_{ch}} = \begin{bmatrix} \dfrac{1}{3}R_{ch} - j\dfrac{1}{\omega C_{ch}} & \dfrac{1}{2}R_{ch} \\ \dfrac{1}{2}R_{ch} & R_{ch} \end{bmatrix}$$

The assumption can be satisfied when the transistor length is very short and the channel opening is higher than 20% of the total channel height. It means that when V_{gs} is larger, the channel resistance will be smaller and this matrix is more appropriate [5].

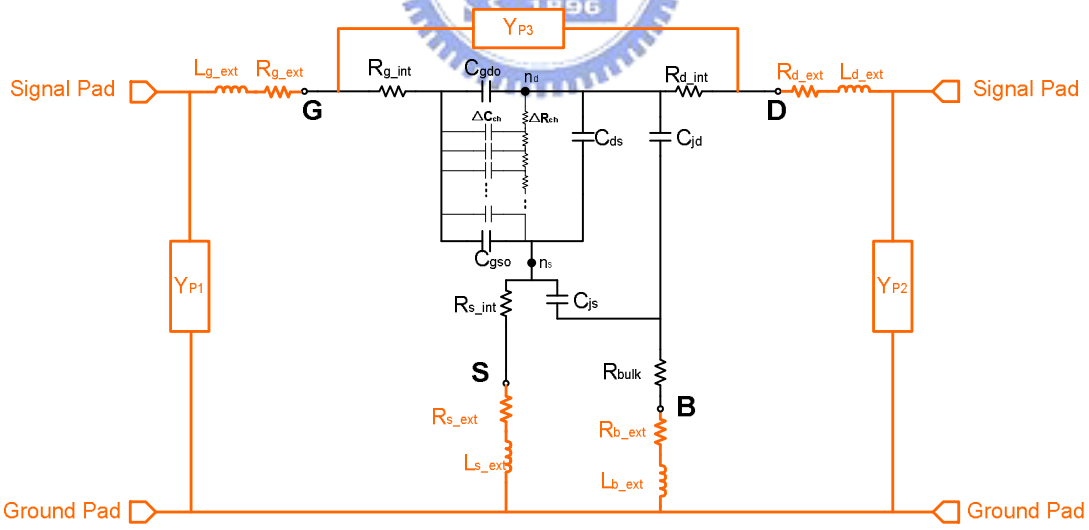


Figure 4 - 2: the equivalent circuit of transistor with gsg pad

The Fig.4-2 represents the equivalent circuit of the device with the pad. The pad part is marked with orange color. On the one hand, the parasitic series resistances and inductances are named with suffix “ext”, on the other hand, the resistances belong to

device are named with suffix “int” such as R_{g_int}, R_{d_int} and R_{s_int}. Besides the channel transmission line, the capacitances coupled between Gate-Source, Gate-Drain, and Drain-Source are named “C_{gso}”, “C_{gdo}” and “C_{ds}”. The suffix “o” means overlap. Because here we define channel capacitance C_{ch} which is always categorized to C_{gd} and C_{gs}, the surplus C_{gs} and C_{gd} mainly come from overlap capacitances which are coupling through the overlap thin oxide. Therefore, for clear identification, I name the Gate-Drain and Gate-Source coupled capacitance “C_{gdo}” and “C_{gso}”. The junction capacitances between Drain-Substrate and Source-Substrate are represented by C_{jd} and C_{js}. And the substrate is represented by a resistance “R_{bulk}”.

After de-embedding (expounded in Chapter 3), the equivalent circuit is represented by Fig.4-3. As mentioned in Chapter 3, the parasitic series resistances and inductances connecting Source-Ground and Body-Ground are retained.

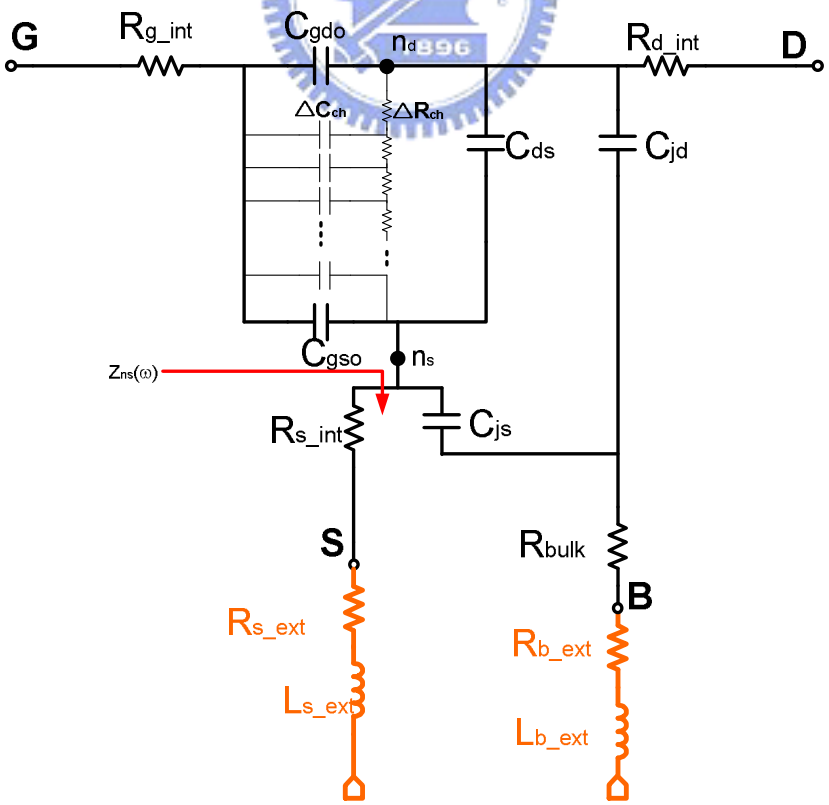


Figure 4 - 3: the equivalent circuit after de-embedding

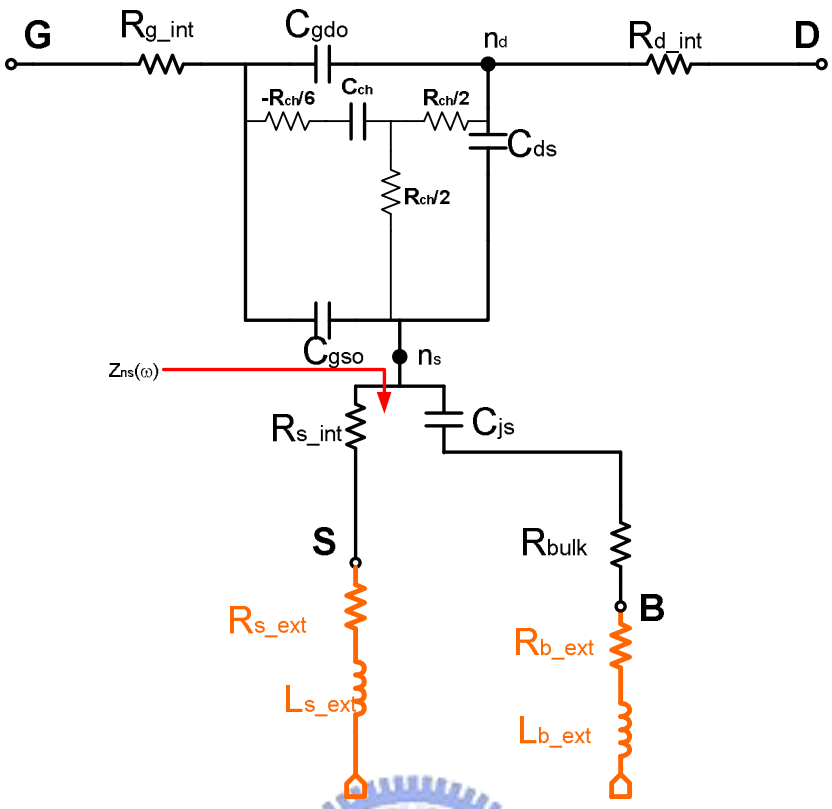


Figure 4 - 4: the equivalent circuit of mos under $V_{gs}>V_{th}$ and $V_{ds}=0$

As previously mention, the path through C_{jd} is neglected temporarily but the impedance seen into "n_s" to ground is not. This impedance is represented by Z_{ns}. According to the analysis [Appendix], the existence of L_{s_ext} will cause the real part of Z_{ns} serious frequency-dependent. The frequency-dependent components consist of L_{s_ext}, R_{s_ext} and C_{js}. Besides, the imaginary part of Z_{ns} is approximate equal to ωL_s. Therefore, the equivalent circuit becomes as Fig.4-4 and the z-parameter is showed below which has been modified for our case: [5]

$$Z=\begin{bmatrix} R_{g\_int}+\frac{1}{3}\frac{C_{ch}+3C_{ds}+3C_{gdo}}{C_{ch}+C_{gso}+C_{gdo}}R_{ch}-j\frac{1}{\omega(C_{ch}+C_{gso}+C_{gdo})}+Z_{ns}(\omega) & \frac{1}{2}\frac{C_{ch}+2C_{gdo}}{C_{ch}+C_{gso}+C_{gdo}}R_{ch}+Z_{ns}(\omega) \\ \frac{1}{2}\frac{C_{ch}+2C_{gdo}}{C_{ch}+C_{gso}+C_{gdo}}R_{ch}+Z_{ns}(\omega) & R_{d\_int}+R_{ch}+Z_{ns}(\omega) \end{bmatrix}$$

According to this matrix, I get an inspiration that we can eliminate the complex component $Z_{ns}(\omega)$by Z_{11}-Z_{12} and Z_{22}-Z_{12}. Because $V_{ds}=0$, $C_{gso}=C_{gdo}$, the formulas become:

$$\mathbf{Re(Z_{11}-Z_{12})\cong R_{g\_int}+\frac{1}{3}\frac{C_{ch}+2C_{gdo}+C_{gdo}+3C_{ds}}{C_{ch}+2C_{gdo}}R_{ch}-\frac{1}{2}R_{ch}=R_{g\_int}-\frac{1}{6}R_{ch}+\frac{1}{3}\frac{C_{gdo}+3C_{ds}}{C_{ch}+2C_{gdo}}R_{ch}}$$

$$\mathbf{Re(Z_{22}-Z_{12})\cong R_{d\_int}+R_{ch}-\frac{1}{2}\frac{C_{ch}+2C_{gdo}}{C_{ch}+C_{gso}+C_{gdo}}R_{ch}=R_{d\_int}+\frac{1}{2}R_{ch}}$$

The two equations demonstrate a good thinking for us. Now taking $Re(Z_{22}-Z_{12})$ as example. According to the formulas, $Re(Z_{22}-Z_{12})$ can be divided into two parts: one is Drain resistance (R_{d_int}) which is gate-bias-independent and the other is half channel resistance which is gate-bias-dependent.

$Re(Z_{11}-Z_{12})$ is similar to $Re(Z_{22}-Z_{12})$ except another additional frequency dependent component $\frac{1}{3}\frac{C_{gdo}+3C_{ds}}{C_{ch}+2C_{gdo}}R_{ch}$. However, this component will be explained in later Chapter 5 with measured data verification that this component is less than one-sixth R_{ch}. Consequently, $Re(Z_{11}-Z_{12})$ is approximate equal to $R_{g\_int}-\alpha R_{ch}$. "α" means a constant.

Following the thinking in last paragraph, when V_{gs} increases, the channel resistance decreases. The extracted $Re(Z_{11}-Z_{12})$ and $Re(Z_{22}-Z_{12})$ will approach to constant values, because the bias-dependent component (channel resistance) is reduced to minimum value even approaches to zero under high V_{gs}. Under this condition, the extracted $Re(Z_{11}-Z_{12})$ and $Re(Z_{22}-Z_{12})$ should only be V_{gs}-bias independent components which result from materials. Therefore, we can extract the bias-independent resistance under high V_{gs}. But we must be careful that do not give too high voltage in Gate otherwise the device will be damaged.

2. V_{ds}=1.2V, V_{gs}>V_{th}

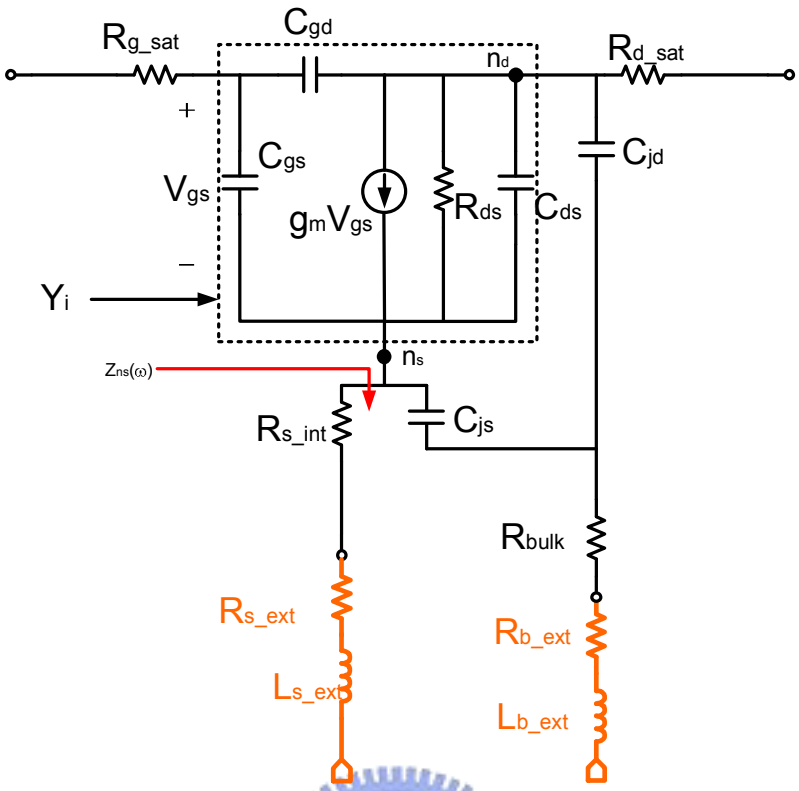


Figure 4 - 5: the equivalent circuit of mos under $V_{gs}>V_{th}$ and $V_{ds}=1.2V$

When the device is operated at saturation region ($V_{ds}=1.2V$, $V_{gs}>V_{th}$), the equivalent circuit is Fig.4-5, and here we ignore the path through the junction capacitance C_{jd} temporarily. $Z_{ns}(\omega)$ means the impedance seen into node "ns" to ground. Here the resistances are added suffix "sat" to distinguish from the resistance extracted under $V_{ds}=0$ and $V_{gs}<V_{th}$ (Fig.4-3), The components surrounded by dotted box are intrinsic components and can be represented by Y_i parameters.

$$\mathbf{Y_{11}^i = j\omega(C_{gs} + C_{gd})}$$
$$\mathbf{Y_{12}^i = -j\omega C_{gd}}$$
$$\mathbf{Y_{21}^i = g_m - j\omega C_{gd}}$$
$$\mathbf{Y_{22}^i = g_{ds} + j\omega(C_{ds} + C_{gd})}$$

And the z-parameters of the full equivalent circuit are [6]:

$$Z_{11} = R_{g\_sat} + Z_{ns}(\omega) + \frac{(Y_{22}^i)^*}{D}$$

$$Z_{22} = R_{d\_sat} + Z_{ns}(\omega) + \frac{(Y_{11}^i)^*}{D}$$

$$Z_{12} = Z_{ns}(\omega) - \frac{Y_{12}^i}{D}$$

$$D = Y_{11}^i Y_{22}^i - Y_{12}^i Y_{21}^i$$

Here, the equivalent circuit and the z-parameters have been modified little for our case. And then the Gate and Drain resistance extraction equations can be derived:

$$Re(Z_{11} - Z_{12}) = R_{g\_sat} + \frac{A_g}{\omega^2 + B}$$

$$Re(Z_{22} - Z_{12}) = R_{d\_sat} + \frac{A_d}{\omega^2 + B}$$

$$If\ \omega \to \infty$$

$$R_{g\_int} \cong Re(Z_{11} - Z_{12})$$

$$R_{d\_int} \cong Re(Z_{22} - Z_{12})$$

$$B = \left[\frac{g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}} \right]^2$$

$$A_g = \frac{C_{ds}\left[g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})\right]}{\left[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{d}s\right]^2} - \frac{g_{ds}}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}}$$

$$A_d = \frac{C_{gs}\left[g_m C_{gd} + g_{ds}(C_{gs} + C_{gd})\right]}{\left[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}\right]^2}$$

4.1.2 Source Resistance

Because of the existence of L_{s_ext} which causes some frequency dependent component in measured z-parameters, Source resistance is hard to be extracted from RF measured data. I extract source resistance from DC measurement.

Source resistance will cause g_m degradation. According to fundamental electronics, we can derive this formula:

$$g_m = \frac{g_{m0}}{1 + R_s \cdot g_{m0}} \cdots\cdots\cdots (4.1)$$

Because the Source and Body are not connected together first, the extracted

Source resistance includes the pad parasitic series resistance. ($R_s=R_{s\_int}+R_{s\_ext}$ in Fig.4-2)

4.2 Intrinsic Capacitance

4.2.1 $V_{ds}=0$, $V_{gs}>V_{th}$

When $V_{ds}=0$, $V_{gs}>V_{th}$, the equivalent circuit is like Fig.4-3. And the Z_{11}-Z_{12} has been derived in section 4.1 which is:

$$Z_{11}-Z_{12}=R_{g\_int}+\frac{1}{3}\frac{C_{ch}+3C_{ds}+3C_{gdo}}{C_{ch}+C_{gso}+C_{gdo}}R_{ch}-\frac{1}{2}\frac{C_{ch}+2C_{gdo}}{C_{ch}+C_{gso}+C_{gdo}}R_{ch}-j\frac{1}{\omega(C_{ch}+C_{gso}+C_{gdo})}$$

According the equation, the imaginary part of Z_{11} is $-\frac{1}{\omega(C_{ch}+C_{gso}+C_{gdo})}$. So we can extract the $C_{gg}=C_{ch}+C_{gso}+C_{gdo}$ value from Z_{11}:

$$C_{gg}=-\frac{1}{\omega\cdot Im(Z_{11}-Z_{12})}\cdots\cdots\cdots(4.2)$$

When $V_{ds}=0$ and $V_{gs}>V_{th}$, the channel is formed. It is like a small conductor connecting Drain and Source. Therefore, C_{ch} can be incorporated to Drain and Source. Here I define the C_{gs} and C_{gd} as:

$$C_{gd}=C_{gdo}+\frac{1}{2}C_{ch}=\frac{1}{2}C_{gg}$$

$$C_{gs}=C_{gso}+\frac{1}{2}C_{ch}=\frac{1}{2}C_{gg}$$

4.2.2 $V_{ds}=1.2V$, $V_{gs}>V_{th}$

Under this bias situation, the transistor is operated at saturation region, and its equivalent circuit is showed in Fig.4-5. C_{gg} and C_{gd} are extracted from the formulas:

$$C_{gd}=-\frac{Im(Y_{12})}{\omega},\quad C_{gg}=\frac{Im(Y_{11})}{\omega}$$

However, these extraction formulas are on a premise that after de-embedding,

the source resistance has been removed completely. In our case, there are two considerations. First: the Source parasitic series inductance is retained and make real part of $Z_{ns}(\omega)$ [appendix] increases with frequency. Second: although we can extract the capacitance at lower frequency to reduce the frequency-dependent effect of real part of $Z_{ns}(\omega)$, the real part of $Z_{ns}(\omega)$, which is approximate to Source resistance at lower frequency, is not zero. When finger number of transistor increases, the g_m value will increase and make the current flow through node "ns" increases. And then, the extracted C_{gg} and C_{gd} values are inaccurate.

So before extracting the capacitance value, I subtract the Source resistance first to make V_{ns} closer to zero and extract at lower frequency for fear of the frequency-dependent effect of $Re(Z_{ns}(\omega))$:

$$\mathbf{Z}-\begin{bmatrix}\mathbf{R_s} & \mathbf{R_s}\\ \mathbf{R_s} & \mathbf{R_s}\end{bmatrix}=\mathbf{Z^{rev}},\quad \mathbf{Y^{rev}}=(\mathbf{Z^{rev}})^{-1},\quad \textbf{then}$$

$$\mathbf{C_{gd}}=-\frac{\mathbf{Im}(\mathbf{Y_{12}^{rev}})}{\omega}\qquad \mathbf{C_{gg}}=\frac{\mathbf{Im}(\mathbf{Y_{11}^{rev}})}{\omega}\cdots\cdots\cdots\cdots\textbf{(4.3)}$$

When transistor is operated at saturation region, C_{gg} is roughly equal to $C_{gs}+C_{gd}$, therefore, $\mathbf{C_{gs}=C_{gg}-C_{gd}}$

4.3 Substrate Model

Substrate model is very important for RF model. When the device is operated at high frequency, the impedance of the junction capacitance becomes very small. Therefore, substrate resistance will affect the small-signal output characteristics of the transistor because the small-signal in substrate will go through the junction capacitance to Drain. How to model the substrate effect accurately is an important issue. Here I adopt the model equivalent circuit showed in Fig.4-6. [7]

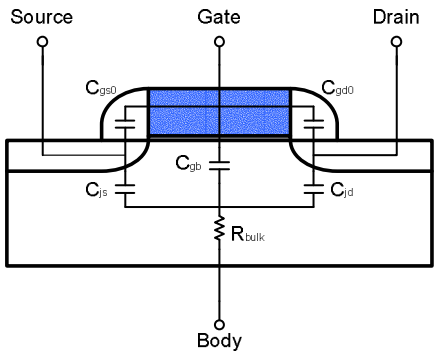


Figure 4 - 6: the equivalent circuit of mos under $V_{gs}=V_{ds}=0$

When the transistor is operated at $V_{gs}<V_{th}$ and $V_{ds}=0$, the equivalent circuit is like Fig.4-6. The substrate is represented by R_{bulk}. C_{jd}, and C_{js}. C_{jd} and C_{js} are junction capacitances and C_{gd0}, C_{gs0} represent gate-to-drain and gate-to-source capacitance. The suffix "0" means they are under zero V_{gs} bias. C_{gb} represents the sum of intrinsic and extrinsic gate-to-body capacitances. Because the device is operated at $V_{gs}<V_{th}$, most intrinsic components of the transistor are negligible. The Gate, Drain, and Source resistance are neglected here because the impedance of them is much smaller than the impedance of junction capacitance and substrate resistance [7].

After deriving the y-parameters of the equivalent circuit, we can get the extraction formulas:

$$\begin{aligned} &\mathrm{Im}(Y_{11}) \cong \omega(C_{gs0}+C_{gd0}+C_{gb}) \\ &\mathrm{Im}(Y_{12}) \cong -\omega C_{gd0} \\ &\mathrm{Re}(Y_{22}) \cong \omega^2 R_{bulk} C_{jd}^2 \\ &\mathrm{Im}(Y_{22}) \cong \omega(C_{gd0}+C_{jd}) \end{aligned} \Rightarrow \begin{aligned} C_{gd0} &\cong -\frac{\mathrm{Im}(Y_{12})}{\omega} = C_{gs0} \\ C_{gb} &\cong \frac{\mathrm{Im}(Y_{11})+2\mathrm{Im}(Y_{12})}{\omega} \\ C_{jd} &\cong \frac{\mathrm{Im}(Y_{22})+\mathrm{Im}(Y_{12})}{\omega} \\ R_{bulk} &\cong \frac{\mathrm{Re}(Y_{22})}{(\mathrm{Im}(Y_{22})+\mathrm{Im}(Y_{12}))^2} \end{aligned} \quad (4.4)$$

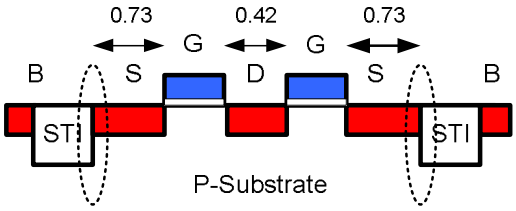
However, this extraction method doesn't match our case because our test-key retains the pad parasitic series resistances and inductances in Source and Body

terminals. The existence of inductance will seriously affect the y-parameters. The extracted parameter curve is not stable with frequency. Nevertheless, this method still supports initial values of C_{jd}, C_{jd} and R_{bulk} for us. I extract the initial values under low frequency and then do some fine-tune work to make the simulated y-parameters curves of equivalent circuit fit the y-parameter curve of measured data.

According the NMOS layout, we can figure out the junction area between Drain or Source diffusion region and Substrate. And then we can derive one capacitance from another. According to the layout, the two-side diffusion regions are Source. Besides, the areas of the two-side diffusions are little larger than others. The C_{js} can be calculated by the equation (0.73 and 0.42 are the edge length of the Drain region and two-side Source region. Please see the figure showed in the left side of next paragraph.):

$$C_{js} \cong C_{jd} \times \frac{\text{Source Area}}{\text{Drain Area}} \cong C_{jd} \times \left(\frac{\frac{N_F}{2} - 1}{\frac{N_F}{2}} + \frac{\frac{0.73}{0.42}}{\frac{N_F}{2}} \times 2\right) \cdots\cdots\cdots (4.5)$$

There is one thing noticeable that the C_{js} value should be smaller than the calculated result because one side of the diffusion region is oxide except substrate for the two-side diffusion region. Please see dotted circuit in left Figure. Therefore, this equation provides the initial value of C_{js} from C_{jd} but we have to decrease little to fine-tune the curve.



Besides, the equivalent circuit in Fig.4-6 doesn't include C_{ds} which appears in other equivalent circuit. I think the C_{ds} only comes from the interconnect capacitance.

Hence I use the value simulated by Calibre-xRC to represent C_{ds} value. It has been demonstrated in Table 2-4 in Chapter 2.

During my fine-tune process, I find that if I add two additional components to the equivalent circuit of Fig.4-6, the simulated curves will fit measured curves better. These two components are one capacitance and one resistance in series. Moreover, this series resistance and capacitance are parallel with the substrate resistance (R_{bulk} of Fig.4-6).

I conjecture that these two components come from the Deep N-Well process which is for RF design to prevent noise going through substrate. When a circuit designer arranges his circuit layout, he can put N-well layer surrounding NMOS and then put a Deep N-well layer in rectangular shape which covers the inner edge of N-well "Ring". And then, the N-well and deep N-well will be like a bowl and the p-substrate will be protected in it. The pick-up of the N-well is usually bias to the highest voltage to make the junction between p-substrate and n-well reverse-bias. This structure is designed to prevent outside noise into the p-substrate and affecting the performance of NMOS. The instruction of this structure is showed in Fig.4-7.

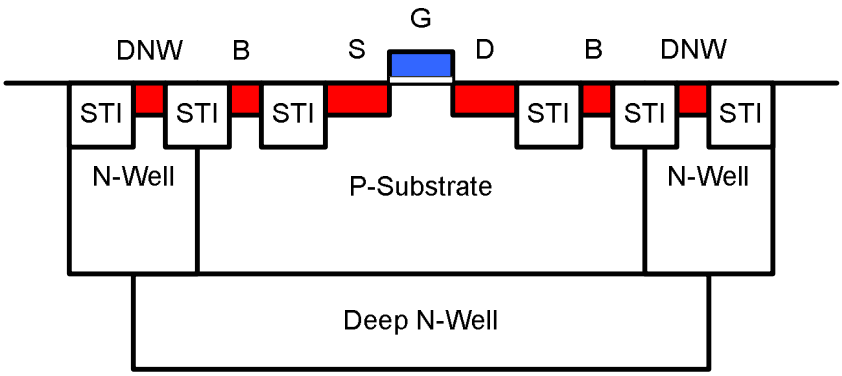


Figure 4 - 7: illustration of Deep N-well in sectional drawing

Therefore, the additional capacitance results from the junction capacitance between N-well (including Deep N-well and sideward N-well) and p-substrate. I name it "C_{dnw}". The additional resistance results from the impedance of the small-signal path in Deep N-well. I name it "R_{dnw}". Please see Fig.4-8 as the more clear illustration.

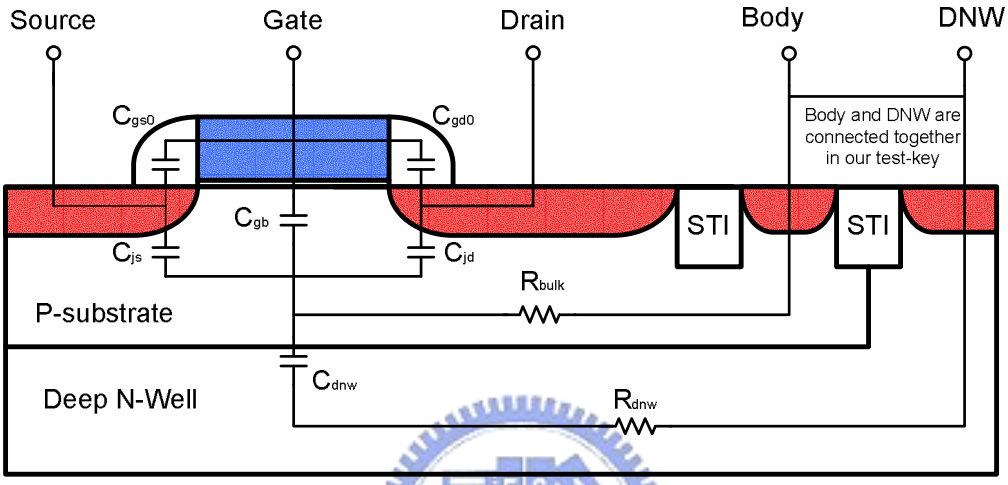


Figure 4 - 8: the equivalent circuit which is added C_{dnw} and R_{dnw}

Although I do some fine-tune work, I am not aimless. There are two basic principles: first is getting the value under low frequency to minimum the retained inductive effect; second is following the simplified equivalent circuit for Y_{22} which is showed in Fig.4-10.

I explain my substrate model extraction steps for summarization:

(1) Operating the transistor at $V_{gs}=V_{ds}=0$ and the equivalent circuit is like Fig.4-9. (R_{s_int} and R_{s_ext} are summed up to R_s which extracted in section 4.1.2; R_{b_ext}, L_{s_ext} and L_{b_ext} results from our test-key situation which is mentioned in chapter 3; Moreover, C_{dnw} and R_{dnw} are added to the circuit.)

(2) Extracting C_{gs0} and C_{gd0} and C_{gb} from the measured data according to equation 4.4. Because there is no current flowing into the node "ns", the

results of revised extraction mentioned in section 4.2 is almost the same as un-revised. However we still extract capacitance from revised extraction method because the initial values of R_{bulk} and C_{jd} are extracted at low frequency too.

(3) R_{g_int} and R_{d_int} are bias-independent because the channel doesn't exist. Their values are extracted from $Re(Z_{11}-Z_{12})$ and $Re(Z_{22}-Z_{12})$ under $V_{ds}=0$ and V_{gs} is large enough. (Please see the explanation in section 4.1.1.)

(4) According to equation 4.4 and 4.5, and calculating the R_{sub}, C_{jd} and C_{js} values. They will vary with frequency. Observing the curves, and take the values under lower frequency (about lower 3 GHz) as initial values for fine-tuning.

(5) Extracting L_{s_ext} value according to equation 4.6. (This extraction will be explained in next 4.4.) L_{b_ext} is assumed equal to L_{s_ext}.

(6) The C_{ds} value comes from simulated interconnect C_{ds} value which is discussed in chapter 2.

(7) After steps (1) to (6), we now have all initial values of parameters in Fig.4-9 except R_{dnw} and C_{dnw}. Next, we build a circuit like Fig.4-9 in software: ADS and then simulating its y-parameters. After the calculating and fine-tuning parameters, we can get these parameters final. The calculating equation is showed in Fig.4-10. Basically, the parameters which don't belong to substrate are not tuned.

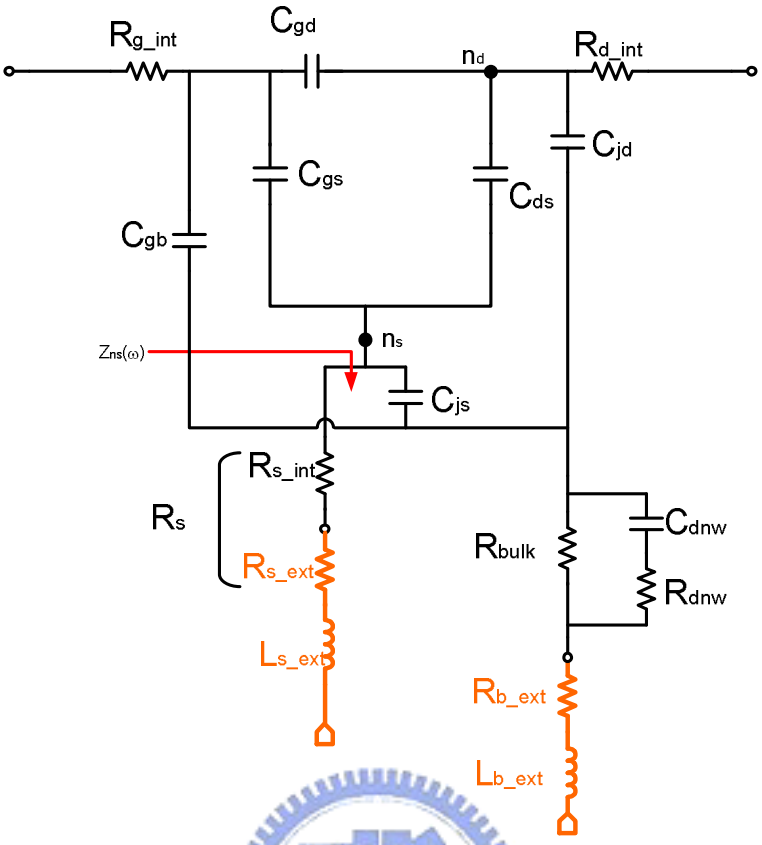


Figure 4 - 9: the equivalent circuit of NMOS under V_{gs}=V_{ds}=0V

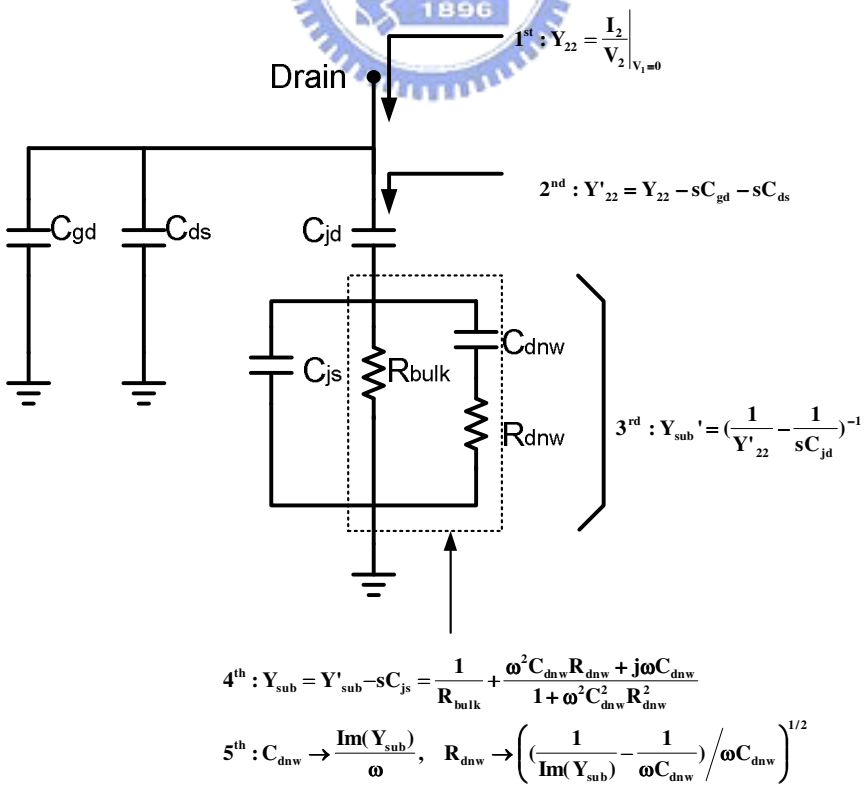


Figure 4 - 10: the R_{dnw}, C_{dnw} fine-tuning extraction process

4.4 Source Extrinsic Inductance

In Chapter 3, I expound the de-embedding procedure and mention that the pad parasitic series resistance and inductance are retained in the Source and Body terminals. In 3.3, I introduced that we can extract the pad parasitic series resistance and inductance of Gate and Drain terminals from Short and Open pads. To extract the pad parasitic inductance in Source terminal, we have to bias the device under $V_{gs}>V_{th}$ and $V_{ds}=0$ and the equivalent circuit is like Fig.4-3. To explain easier, here we can just use a small resistance R_{ch} to replace the RC transmission line in Fig.4-3. And according to the analysis in Appendix [a.3], the real part of $Z_{ns}(\omega)$ is serious frequency-dependent but the imaginary part of $Z_{ns}(\omega)$ is approximate equal to ωLs. If the finger number is larger, the C_{js} value will be larger and it will make the approximation incredible. Therefore, I extract the Source extrinsic inductance from the measured data of $N_F=18$ transistor and take the average of the imaginary part of Z_{12} at frequency=5GHz~40GHz.

The Z_{12} of Fig.4-3 which is mentioned in 4.1.1 is

$$Z_{12}=\frac{1}{2}\frac{2C_{ch}+2C_{gd}}{C_{ch}+C_{gs}+C_{gd}}R_{ch}+Z_{ns}(\omega)$$

$$\mathrm{Im}(Z_{12})=\mathrm{Im}(Z_{ns}(\omega))$$
$$\cong\frac{\omega Ls-\omega R_s^2C_{js}-\omega^3L_s^2C_{js}+\omega^3R_{bulk}^2L_sC_{js}^2}{(1-\omega^2L_sC_{js})^2+\omega^2(R_s+R_b)^2C_{js}^2}\cong\omega L_s \cdots\cdots\cdots(4.6)$$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Chapter 5

Experiment and Analysis

5.1 Pad parasitic series resistance and inductance

Theoretically, after de-embedding, the pad parasitic effect can be removed. Actually, it is hard to achieve. However, it is still a very important procedure that de-embedding can remove some critical pad parasitic effect initially such as inductive and capacitive effects.

5.1.1 Inductance

When operating frequency is very high, the thin metal line will behave as an inductance. We can extract the Gate, Drain parasitic series inductances from the short pad which subtracts the pad parasitic capacitive effect. It is mentioned in 3.3.

Besides, the source inductance extraction need to be extracted by the help of small channel resistance under $V_{gs}>V_{th}$ and $V_{ds}=0$. It is mentioned in 4.4.

The inductive effect becomes obvious when frequency is high enough. We take the average value of frequency=5GHz to 40GHz as the extracted parasitic inductance values. They are:

	Gate parasitic inductance	Drain parasitic inductance	Source parasitic inductance
Unit: pH	48.82	47.39	50.64

Table 5 - 1: extracted parasitic inductance values

5.1.2 Resistance

We take the average of the values at frequency=5GHz to 40GHz as the extracted parasitic resistance. They are:

	Gate parasitic resistance	Drain parasitic resistance
Unit: Ω	1.14	1.067

Table 5 - 2: extracted parasitic resistance values

5.2 Intrinsic resistance

According to the demonstration in section 4.1.1, the Gate and Drain resistance can be extracted from $Re(Z_{11}-Z_{12})$ and $Re(Z_{22}-Z_{12})$. They include two parts: bias-dependent and bias independent.

5.2.1 Gate, Drain resistances

1. $V_{ds}=0$, $V_{gs}>V_{th}$ (average of 15GHz~30GHz)

I name the extracted values of $Re(Z_{11}-Z_{12})$ and $Re(Z_{22}-Z_{12})$ "R_G" and "R_D". First, we see the extraction curve of R_G, (Fig.5-1). We can find that the curve is not

flat at lower frequency. It is because the extraction method expounded in 4.1.1 is under the situation that the channel is like a transmission line. If the frequency is not high enough, the RC delay in the channel is not obviously. Besides, although the channel resistance is small, and under this bias condition, we neglect the substrate effect, we have to sample the data carefully especially when extracting R_D which will be influenced by C_{jd} easily. Therefore, I sample the data at 15GHz to 30GHz and take average as the extracted value. We can find the curves of $Re(Z_{22}-Z_{12})$ become unstable when the frequency is higher than 30GHz.

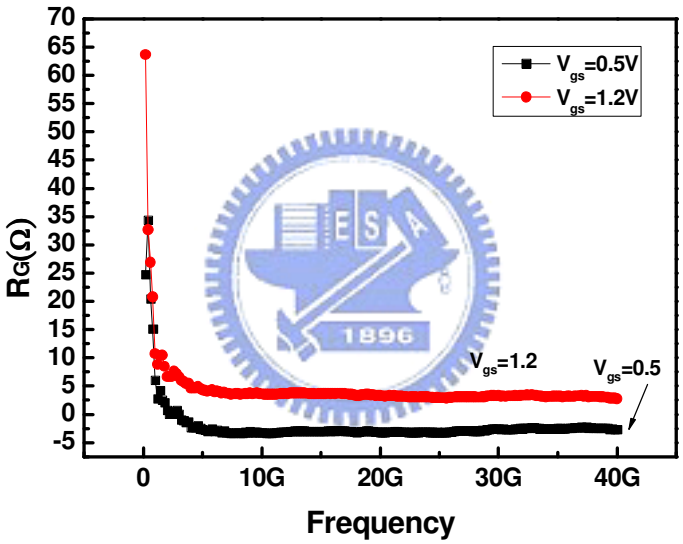


Figure 5 - 1: extracted R_G of N_F=18 NMOS under V_{ds}=0, V_{gs}=0.5 and 1.2V

The extracted R_G and R_D values under $V_{gs}>V_{th}$ and V_{ds}=0 are showed in Table 5-3 and Table 5-4.

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	-3.03	0.448	1.76	2.37	2.7	2.92	3.08	3.21
N36	-0.978	0.782	1.38	1.66	1.81	1.89	1.98	2.05
N72	-0.857	0.244	0.636	0.744	0.82	0.866	0.933	1.07

Table 5 - 3: extracted R_G values under V_{ds}=0 (unit: Ω)

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	17.271	9.771	6.94	5.603	4.854	4.39	4.081	3.866
N36	8.4	5.37	4.07	3.44	3.12	3.01	2.88	2.72
N72	3.6	1.86	1.22	0.907	0.735	0.628	0.572	0.574

Table 5 - 4: extracted R_D values under V_{ds}=0 (unit: Ω)

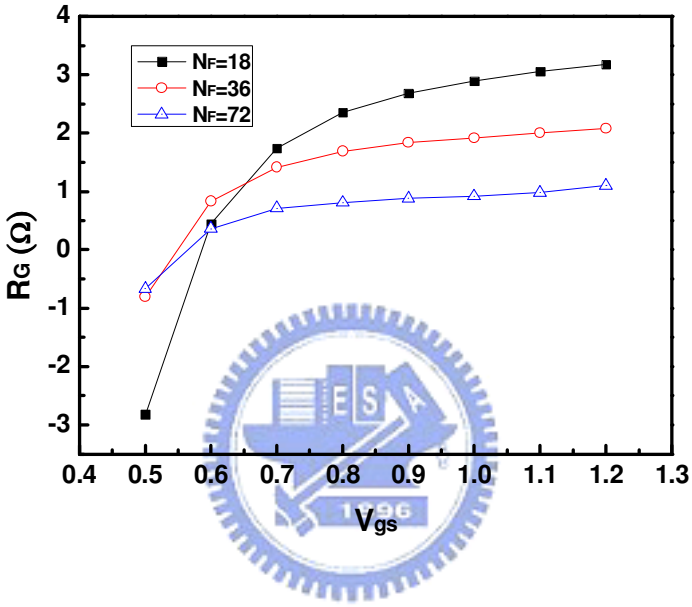


Figure 5 - 2: extracted R_G vs V_{gs} under V_{ds}=0

Now I plot the extracted R_G figure according to Table 5-3 and show in above. Observing the curves, we can find the extracted values vary with V_{gs}. We take the equation mentioned in section 4.1.1:

$$\mathbf{Re(Z_{11} - Z_{12}) \cong R_{g\_int} - \frac{1}{6}R_{ch} + \frac{1}{3}\frac{C_{gdo} + 3C_{ds}}{C_{ch} + 2C_{gdo}}R_{ch}}$$

According to this equation, we can find the real part of $Re(Z_{11}-Z_{12})$ consists of two parts: a bias-independent resistance and a bias-dependent resistance associated with channel resistance. First we check the third component in the equation. Observing the extracted C_{gg} values under V_{ds}=0, which are showed in later Table 5-8,

we can find when V_{gs} is higher than about 0.7V, the C_{gg} value approaches to a constant. In addition, the C_{gdo} value, which contributed by overlap and fringe capacitances, should be about one-third C_{gd} from experience, and under V_{ds}=0, C_{gd} is equal to half C_{gg}, therefore, C_{gdo} is about one-sixth C_{gg}. Besides, C_{ds} mainly results from interconnect capacitance and the simulated values have been showed in Table 2-4.

We take N_F=72 NMOS as example. Its C_{gg} value under V_{ds}=0, V_{gs}=1.2V is 431.1fF (later Table 5-9). The C_{gdo} value is about one-sixth C_{gg} and is 71.8fF. C_{dsm} of N_F=72 NMOS is 18fF (former Table 2-4) Therefore, we can figure out that $\frac{C_{gdo}+3C_{ds}}{C_{ch}+2C_{gdo}}$ is about 0.29. And then $\frac{1}{3}\frac{C_{gdo}+3C_{ds}}{C_{ch}+2C_{gdo}}R_{ch}$ is less than one-sixth R_{ch} surely. It means that $Re(Z_{11}-Z_{12})$ is a constant "R_{g_int}" subtracting a value associated with channel resistance. When V_{gs} increases, channel resistance decreases. Therefore, the result of a constant subtracting a smaller value is larger than before. It explains the trend of the curves in Fig.5-2 reasonably.

Therefore we can utilize this phenomenon to extract the Poly-silicon resistance which is bias-independent component associated with the materials. We can bias V_{gs} carefully little higher than V_{DD} and then the channel resistance reaches an extreme small value which can be neglected. And then R_{g_int} is equal to $Re(Z_{11}-Z_{12})$

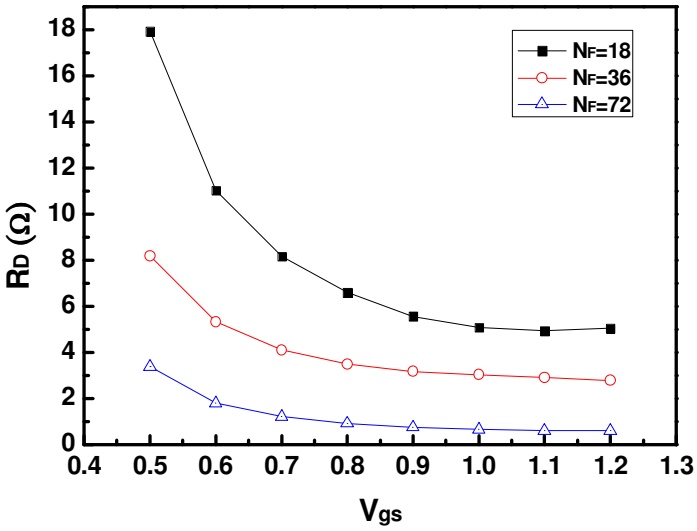


Figure 5 - 3: extracted R_D vs V_{gs} under V_{ds}=0

The above Fig.5-3 is according to Table 5-4 which is the extracted R_D plots varying with V_{gs}. First, the R_D equation mentioned in section 4.1.1 is:

$$\mathbf{Re(Z_{22} - Z_{12}) \cong R_{d\_int} + \frac{1}{2} R_{ch}}$$

According to this equation, we can explain the curves of $Re(Z_{22}-Z_{12})$ trend. When V_{gs} increases, channel resistance decreases. Therefore, the constant, R_{d_int} adds a smaller value and gets a smaller value than before. Base on the former discussion just elaborated, we can bias V_{gs} carefully little higher than V_{DD}, and then get the intrinsic Drain resistance value which is just associated with the impedance in diffusion region.

This extraction brings two benefits. First, it can exclude the measured resistance error results from the contact between probe tip and pad. Because the contact condition of each time measurement is different, the extracted resistance is influenced by it each time. However, if we can extract the bias-independent component, it must

include the resistance results from the contact. And when we build a resistance model, we can subtract this component first. And then we can be sure the left resistance is associated with channel. Therefore, second, it makes the model more physical. Originally, we always get a large values need to be fit. Now we at least can build the resistance model as like "$R_G=R_{g\_int}+R_1(V_{gs}, \omega)$" and "$R_D=R_{d\_int}+R_2(V_{gs}, \omega)$" first. And then we start to model the channel performance as the parameter "$R(V_{gs},\omega)$".

2. V_{ds}=1.2V, $V_{gs}>V_{th}$ (average of 38.2GHz~40GHz)

The R_G extraction curves under V_{ds}=0 and V_{gs}=0.5, 1.2V are showed in Fig.5-4. According to the extraction method expounded in 4.1.1, this method is reliable when the frequency is infinity. However, our measurement is limited by equipment and just up to 40GHz. But the curve is truly flatter when the frequency is higher. Here I sample the values at highest 10 frequency points which are 38.2 GHz to 40GHz.

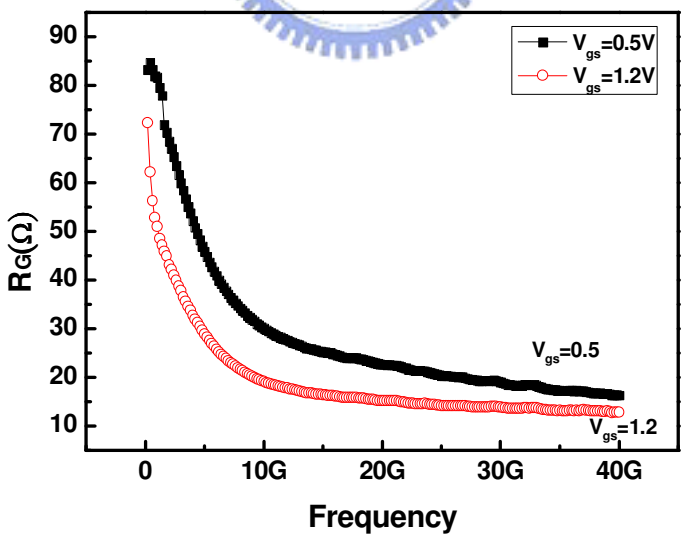


Figure 5 - 4: extracted R_G of N_F=18 NMOS under V_{ds}=1.2V, V_{gs}=0.5 and 1.2V

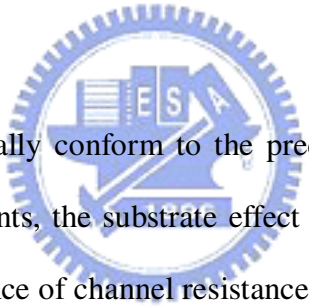
The extracted R_G and R_D values under $V_{gs}>V_{th}$ and V_{ds}=1.2V are showed in Table 5-6 and Table 5-7.

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	16.498	15.969	15.353	14.825	14.337	13.682	13.38	12.874
N36	11.209	11.156	10.9	10.615	10.323	10.017	9.702	9.366
N72	5.511	6.086	5.94	5.795	5.648	5.501	5.312	5.128

Table 5 - 5: extracted R_G values under V_{ds}=1.2V (unit: Ω)

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	30.476	28.296	26.91	26.092	25.515	25.021	24.539	24.024
N36	14.935	14.045	13.547	13.207	12.947	12.708	12.455	12.181
N72	5.934	5.487	5.267	5.117	5	4.891	4.772	4.652

Table 5 - 6: extracted R_D values under V_{ds}=1.2V (unit: Ω)



Although the curves really conform to the prediction mentioned in reference paper 4-3 and trend to constants, the substrate effect is still a latent problem. When V_{ds}=0 and V_{gs}>V_{th}, the existence of channel resistance causes a small impedance path and then the path through C_{jd} is ignorable. However, when the transistor is operated at saturation region, the small channel resistance is replaced by a current source and an extreme large resistance. Under this situation, the impedance of the path through C_{jd} might not be ignorable.

5.2.2 Source resistance

Following the extraction procedure mentioned in 4.1.2, the extracted Source resistances are showed in Table 5-8. Moreover, Fig.5-5 shows that R_s will causes I_d and g_m degradation.

Source resistance	NF=18	NF=36	NF=72
Unit: Ω	2.0798712	2.079875	2.30155

Table 5 - 7: extracted R_S values from DC measurement (unit: Ω)

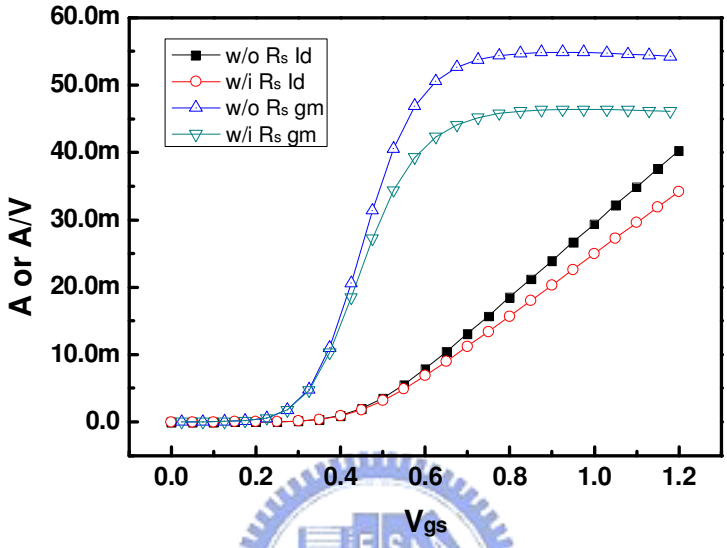


Figure 5 - 5: simulation of I_d and g_m vs V_{gs} w/i and w/o R_s

5.3 Intrinsic capacitance

5.3.1 V_{ds}=0, V_{gs}>V_{th} (average of 5GHz~15GHz)

The extracted C_{gg} curves under V_{gs}=1.0, 1.2V and V_{ds}=0 of N_F=72 transistors are showed in Fig.5-6. We observe that when the frequency increases, the curves become unstable. We have discussed in Chapter 4. In the first step of extraction work, we ignore substrate first which includes C_{jd} and R_{bulk}. (Because the L_{s_ext} exists, the C_{js} is special to un-neglected. It is discussed in Appendix). Therefore, if the frequency is very high, the C_{jd} and R_{bulk} will start to affect the y-parameters or z-parameters.

Besides, the C_{gg} will be extracted from the equation 4.2 in section 4.2.1. It is $\mathbf{C_{gg} = -\frac{1}{\omega \cdot Im(Z_{11} - Z_{12})}}$. This equation has to satisfy an assumption mentioned in Appendix [a.1] that is $\mathbf{|\gamma L|^2 = \omega R_{ch} C_{ch} << 1}$. And when finger number is larger, C_{ch} is larger. Moreover, if the frequency is too high, the assumption is not established anymore and this equation cannot be used. Therefore, in Fig.5-6, the curve of N_F=72 NMOS under high frequency becomes unstable.

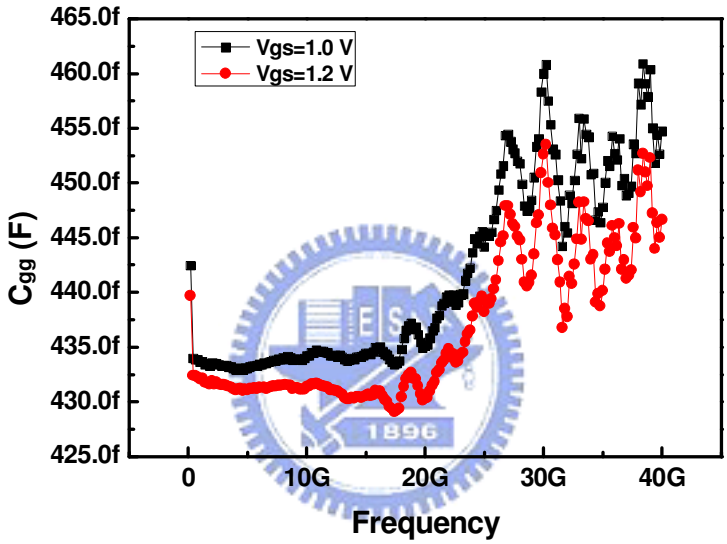


Figure 5 - 6: extracted C_{gg} of N_F=72 NMOS under V_{ds}=0 and V_{gs}=1.0V, 1.2V

Therefore, I take the average of $\mathbf{\frac{1}{\omega Im(Z_{11} - Z_{12})}}$ at frequency=5GHz~15GHz as the C_{gg} values. The extracted C_{gg} values under different V_{gs} are showed in Table 5-8.

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	105.1	109.6	111.5	112.2	112.5	112.4	112.2	111.9
N36	206.6	214.4	217.9	219.3	219.7	219.5	219.1	218.6
N72	408.6	423.8	430.5	433.4	434.2	434	432.9	431.1

Table 5 - 8: extracted C_{gg} values under V_{ds}=0V (unit: fF)

The C_{gs} and C_{gd} are equal to half C_{gg} and the values are showed in Table 5-9.

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	52.55	54.8	55.75	56.1	56.25	56.2	56.1	55.95
N36	103.3	107.2	108.95	109.65	109.85	109.75	109.55	109.3
N72	204.3	211.9	215.25	216.7	217.1	217	216.45	215.55

Table 5 - 9: extracted C_{gd} values under V_{ds}=0V (unit: fF)

5.3.2 V_{ds}=1.2V, $V_{gs}>V_{th}$

There are two problems when extracting C_{gg} under V_{ds}=1.2V and $V_{gs}>V_{th}$ which has been mentioned in section 4.2.2 First, the imaginary part of Y_{11} is decreasing when frequency is increasing because the frequency-dependence of real part of $Z_{ns}(\omega)$. Fig.5-7 is the extracted C_{gg} curves of N_F=18, 72 transistors under $V_{gs}=V_{ds}$=1.2V which are directly extracted from imaginary part of Y_{11} divided by ω. We can find that the curves are obviously decreasing when frequency is increasing. As mentioned in section 4.2.2, we can extract C_{gg} at lower frequency to make this bad effect minimum (Fig.5-8). Second, the imaginary part of Y_{11} is decreasing when the finger number of transistor is increasing because the more current flow into the node “ns” which is indicated in Fig.4-2, the node voltage is higher and causes the imaginary part of Y_{11} decreases. Therefore, even I extract C_{gg} under lower frequency as showed in Fig.5-8, the C_{gg} value of transistor whose finger number is 72 is not reasonable. It is not about 4 times of the C_{gg} value of transistor whose finger number is 18. Therefore, as mentioned in 4.2.2, I subtract R_s first from the measured z-parameters under low frequency and then transform it to y-parameters and use these y-parameters to extract

C_{gg}. Fig.5-9 is the result of revised extraction. We can find the C_{gg} values are reasonable. The R_s values are from the extraction result elaborated in Table 5-8 in section 5-2-2. The frequency range is 0.4GHz~2.2GHz, the first 10 frequency points except 0.2GHz. C_{gd} extraction has similar problem. C_{gg} and C_{gd} are extracted from equation 4.3 under 0.4GHz to 2.2GHz. The extracted C_{gg}, C_{gd}, and C_{gs} values under different V_{gs} bias are showed in Table 5-11, Table 5-12 and Table 5-13.

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	94.82	101.9	106.1	108.7	110	111.1	111.7	112.2
N36	182.5	194	201.5	205.8	208.5	210	210.9	211.4
N72	366.4	391.3	409.6	419.5	424.2	425.9	425.9	425.2

Table 5 - 10: extracted C_{gg} values under V_{ds}=1.2V (unit: fF)

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	29.07	29.15	29.31	29.55	29.89	30.23	30.66	31.13
N36	57.06	57.04	57.38	57.88	58.52	59.29	60.2	61.26
N72	116	116	116.2	117	118.2	119.7	121.7	124.1

Table 5 - 11: extracted C_{gd} values under V_{ds}=1.2V (unit: fF)

V_{gs}	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
N18	65.75	72.75	76.79	79.15	80.11	80.87	81.04	81.07
N36	125.44	136.96	144.12	147.92	149.58	150.71	150.7	150.14
N72	250.4	275.3	293.4	302.5	306	306.2	304.2	301.1

Table 5 - 12: extracted C_{gs} values under V_{ds}=1.2V (unit: fF)

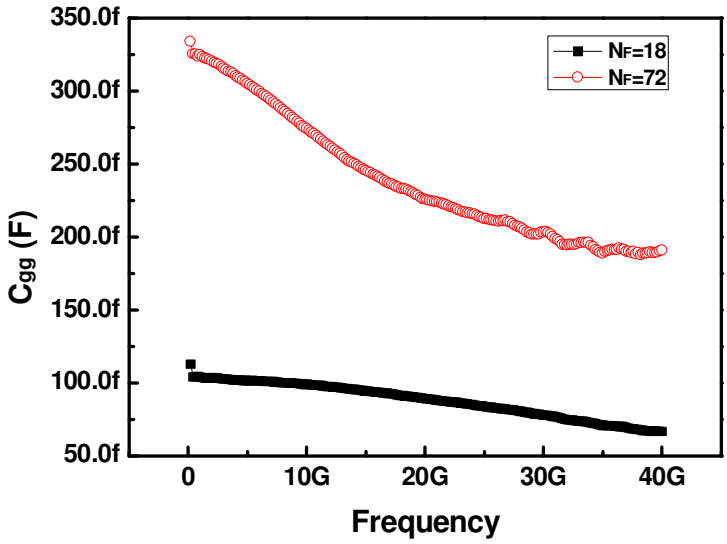


Figure 5 - 7: extracted C_{gg} of N_F=18, 72 NMOS under V_{ds}=1.2 and V_{gs}=1.2V

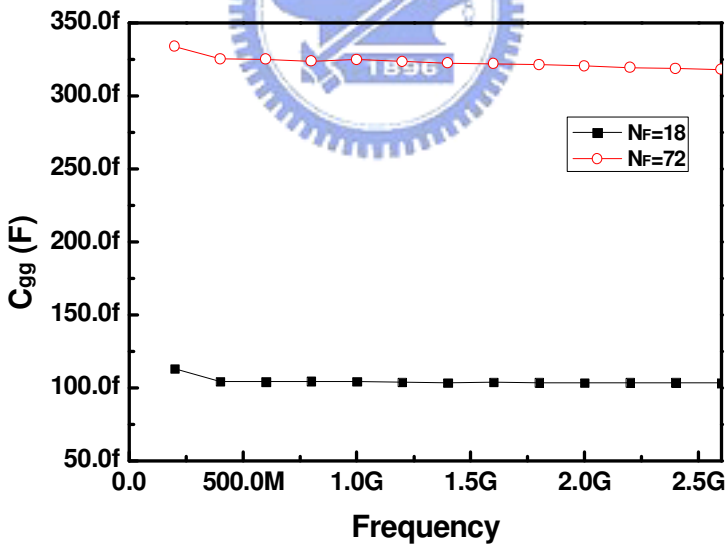


Figure 5 - 8: extract C_{gg} at lower frequency (continue Fig.5-27)

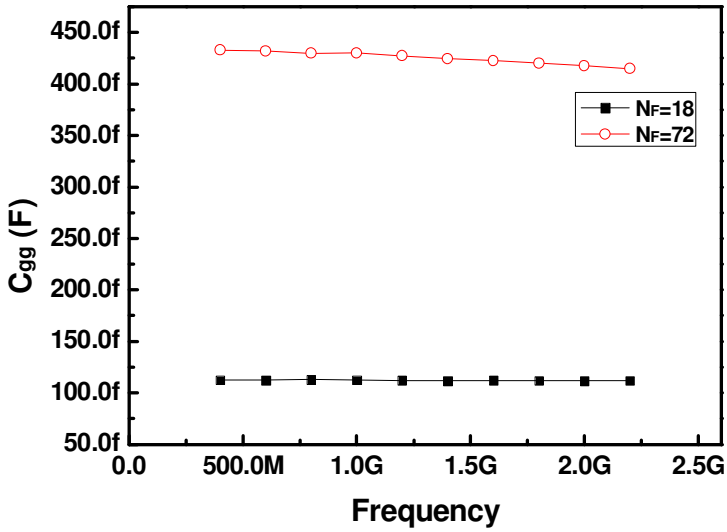


Figure 5 - 9: subtracted R_s effect first and extract C_{gg} at lower frequency (continue Fig.5-28)

5.4 Substrate Model

The equivalent circuit of NMOS under $V_{ds}=V_{gs}=0$ has been showed in Fig.4-9. C_{gg}, C_{gd0}, and C_{gb} values of different finger number NMOS are extracted according to first two equations in equation 4.4. The curves are flat up to about 20GHz. If the frequency is higher, the y-parameter curve will behave the resonant effect especially when finger number is 72. I follow the former capacitance extraction sampling frequency range which is 0.4GHz to 2.2GHz. The extracted capacitance values are showed in Table 5-13.

	C_{gg}	C_{gd0}	C_{gb}
N18	73.81	31.05	11.71
N36	141.1	61.26	18.58
N72	281.6	125.2	31.2

Table 5 - 13: extracted C_{gg}, C_{gd0} and C_{gb} under $V_{ds}=V_{gs}=0$

C_{jd} and R_{bulk} initial values come from the last two equations in equation 4.4. Taking N_F=36 NMOS as example. Please see Fig.5-10 and Fig.5-11. As I explained in section 4.3, because the retained L_{s_ext} and R_s, the R_{bulk} and C_{jd} extracted curves are not stable with frequency. However, when frequency is not very high, we can regard the impedance of inductance eliminated. Therefore, we can roughly sample the values in red dotted circuit as the initial values of R_{bulk} and C_{jd}. Moreover, C_{js} is estimated from equation 4.4 but might be tuned smaller.

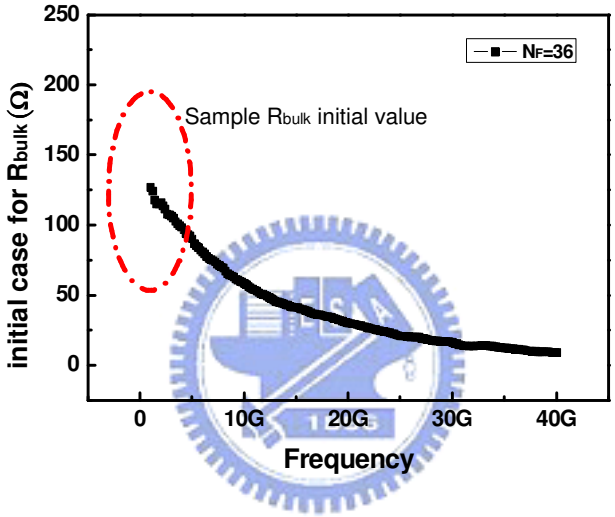


Figure 5 - 10: extract R_{bulk} initial value under V_{ds}=V_{gs}=0

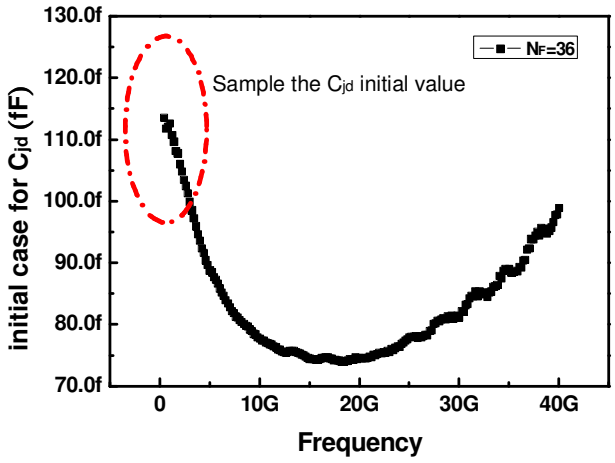


Figure 5 - 11: extract C_{jd} initial value under V_{ds}=V_{gs}=0

Besides, we refer to the values of R_s and L_{s_ext}, and estimate the values of pad extrinsic series resistance and inductance connecting to Body equal to 2ohm and 40pH, because the Body connecting metal is little wider then the Source connecting metal.

As I elaborated in section 4.3, the R_{g_int}, R_{d_int}, R_s, and L_{s_ext} are extracted from some methods. Here I omit the process. Now we get all parameters initial values except C_{dnw} and R_{dnw}. After fine-tune process which is showed in Fig.4-10, we can get the parameters showed in Table 5-14 and 5-15. Because the substrate effect influences the imaginary part of Y_{22} most, I fit $im(Y_{22})/\omega$ first. Fig.5-12 to 5-14 are the $im(Y_{22})/\omega$ curves of measurement and simulation of the equivalent circuit model showed in Fig.4-9 after adding the two new components "R_{dnw}" and "C_{dnw}". The figures include N_F=18, 36 and 72 NMOS.

	$R_{g\_int}(\Omega)$	$R_{d\_int}(\Omega)$	$R_s(\Omega)$	L_{s_ext}(pH)	C_{gs}(fF)	C_{gd}(fF)	C_{gb}(fF)	C_{ds}(fF)
NF=18	3.18	5.04	2.08	55	31.05	31.05	10.5	4.53
NF=36	2.08	2.4	2.08	55	61.26	61.26	18.58	9.05
NF=72	1.1	1.2	2.31	55	125.2	125.2	31.2	18.07

Table 5 - 14: extracted parameters of Fig.4-9

	C_{jd}(fF)	C_{js}(fF)	$R_{bulk}(\Omega)$	C_{dnw}(fF)	$R_{dnw}(\Omega)$	$R_{b\_ext}(\Omega)$	L_{b_ext}(pH)
NF=18	52	55	230	26	240	2.08	40
NF=36	105	110	120	52	120	2.08	40
NF=72	200	210	70	120	50	2.3	40

Table 5 - 15: extracted parameters of Fig.4-9

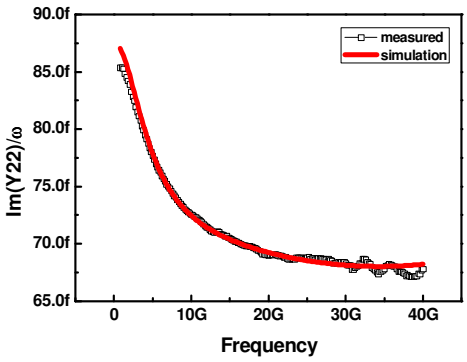


Figure 5 - 12: measured and simulated $Im(Y_{22})/\omega$ curves of N_F=18 NMOS w/i C_{dnw} and R_{dnw}

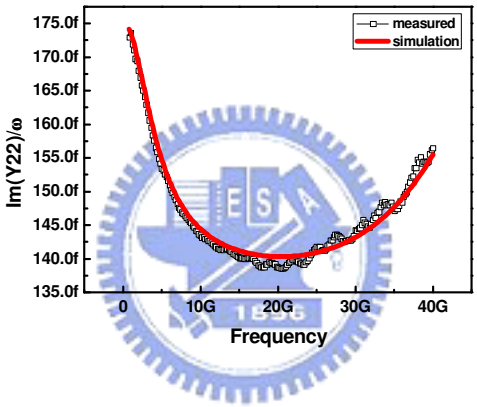


Figure 5 - 13: measured and simulated $Im(Y_{22})/\omega$ curves of N_F=36 NMOS w/i C_{dnw} and R_{dnw}

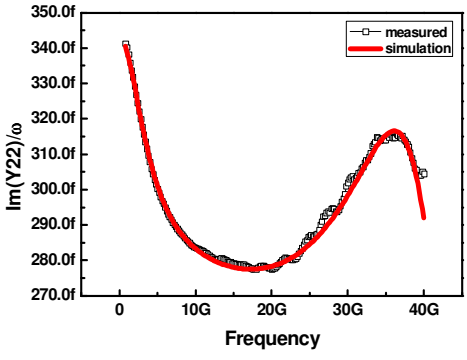


Figure 5 - 14: measured and simulated $Im(Y_{22})/\omega$ curves of N_F=72 NMOS w/i C_{dnw} and R_{dnw}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Chapter 6

Conclusion and Future Work

6.1 RF De-embedding

In Chapter 2, the interconnect capacitances are demonstrated by the help of software. In Chapter 3, the de-embedding methods to remove pad parasitic effects are discussed. The parasitic effect of pad "Y_{P3}" (Fig.3-12) is capacitive effect between two signal ports. The effect is mainly contributed by the interconnect capacitance. Moreover, when device is smaller, the capacitive effect between signal pad and ground pad which is contributed by interconnect capacitance will increase. Traditional open pad for de-embedding just retains metal layers higher than M3 (exclude M3) because the metals lower than M3 is categorized to "intrinsic" device.

To get the more "pure" intrinsic measured data of device, we can try to remove the interconnect capacitances after de-embedding. Nevertheless, although the de-embedding method can remove most pad parasitic effects to get more accurate pure device measured data, it will cost more dummy pads but not only open and short pads [9].

6.2 Parameters Extraction

After the extraction process elaborated in the thesis, we have two aspects of thinking. One is traditional 2-port RF measurement and the other is 4-port RF measurement.

In our test-key, the Source and Body are not connected together first and connect to ground pad separately. If we connect them first, it returns back to traditional 3-Terminal (3T), 2-port case. And the real part of the impedance seen into node "ns" (Fig.4-2) which is associated with L_{s_ext} will be simplified to Source resistance "R_{s_int}". Because the pad parasitic series inductance "L_{s_ext}" is removed after de-embedding, the component which causes $Re(Z_{ns}(\omega))$ increases with frequency doesn't exist. In future work, we can put a test-key under this case to verify.

Besides, there are many published papers [10], [11], [12] using other formulas to extract parameters under 2-port measurement. For example, we can also extract Gate, Drain, and Source resistances from Y-parameters except Z-parameters [10].

Relative to 2-port measurement and parameter extraction, the published papers about 4-port are fewer. But 4-port measurement and extraction is a trend because of the need of 4-T transistors for circuit designers. Even though the system calibration technique and measurement are more complex, more and more engineers devote to this research. It includes the accurate system calibration and precise measurement. Under 4-port RF measurement, the parameter extraction will be more complex than 2-port measurement. But the built model card will behave more close to reality.

6.3 Substrate Model

In this thesis, I propose two new parameters to model the effect of deep N-well and one resistance to model the effect of p-substrate.

There are several papers about substrate model are published continuously. For example, in the reference paper [10], substrate model is composed of three resistances which are showed in Fig.6-1. Besides, in accordance with the three resistance substrate model, in reference paper [13] and [14], the different authors propose different analysis. I also design a test-key to study this three resistance substrate model. In future, we can analyze the measured result of the special-designed test-key to analyze substrate effect deeper.

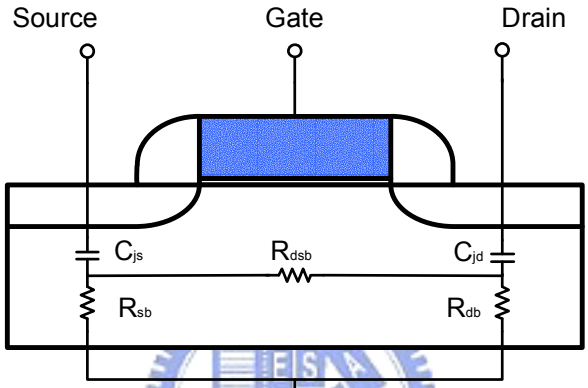

Figure 6 - 1: 3-resistances substrate model


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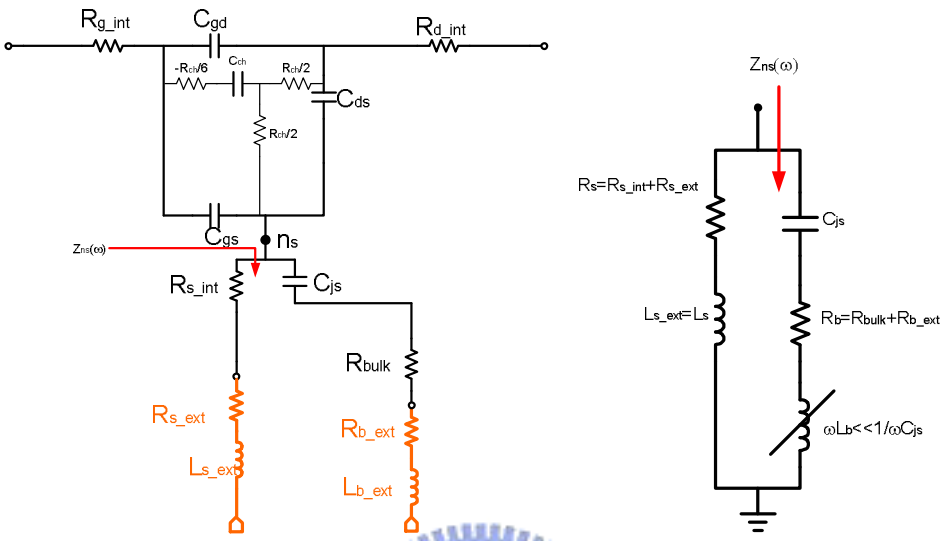
Appendix

The impedance seen into “ns” to ground



$$\mathrm{Re}(Z_{ns}(\omega)) \cong \frac{R_s + \omega^4 R_b L_s^2 C_{js}^2 + \omega^2 R_s R_b (R_s + R_b) C_{js}^2}{(1-\omega^2 L_s C_{js})^2 + \omega^2 (R_s + R_b)^2 C_{js}^2}$$

$$\mathrm{Im}(Z_{ns}(\omega)) \cong \frac{\omega L_s - \omega R_s^2 C_{js} - \omega^3 L_s^2 C_{js} + \omega^3 R_{bulk}^2 L_s C_{js}^2}{(1-\omega^2 L_s C_{js})^2 + \omega^2 (R_s + R_b)^2 C_{js}^2}$$