氮化鎵異質結構
場效電晶體之研究

研究生：陳力輔　　　　　　指導教授：　李建平 博士

國立交通大學電子工程學系 電子研究所

中 文 摘 要

本研究中，針對氮化鎵異質結構場效電晶體之結構特性，探討利用感應耦合電漿蝕刻改變閘極位置，以達成臨界電壓調整及改善元件特性之目的。蝕刻時，考慮之方向分兩部分，首先是為避免過度蝕刻導致主動區被挖穿，故蝕刻速率不可過快。其次是避免閘極在蝕刻中受到過多損傷導致特性衰減。

實驗中採用兩種不同掘入蝕刻（recess etch）條件，分別是純氯（Cl_2）蝕刻與氯氬(Cl_2/Ar)蝕刻，分別將閘極掘入(gate recess)50Å與 80Å處，臨界電壓由-7V 調整至-6V 及-4V，掘入蝕刻後分析元件特性之衰減主要受到 surface trap 及 etch damage 所導致，利用 passivation 消除 surface trap 並量測 current collapse 驗證後，可分別評估 surface trap 與 etch damage 對元件特性所造成之影響。

實驗中使用undoped $Al_{0.3}Ga_{0.7}N$/GaN HFET 閘極長度 1μm閘極寬度 50μm之元件作為比較基準，量測未加上閘極前之Vds-Id分佈判斷掘入蝕刻程度，並在元件完成後量測C-V來判斷蝕刻深度，量測元件之各項直流特性與高頻特性，並相互比較以評估掘入蝕刻所造成之影響。未經蝕刻之原始試片臨界電壓-7V，室溫下之最大通道電流高達 37mA，單位閘極寬度之電流密度達到 740mA/mm，最大外部轉導 117mS/mm，元件之崩潰電壓大於 100V扣除Pad寄生效應後之ft與 fmax分別達 7.5GHz與 13GHz。

相同尺寸之元件經過掘入蝕刻並 passivation 後，臨界電壓縮小至-4V，室溫下最高通道電流 20.55mA，單位閘極寬度之電流密度達到 411mA/mm，最大外部轉導為 112 mS/mm，崩潰電壓為 61V。在高頻特性上扣除 Pad 寄生效應後的 ft 達到 9GHz，fmax 達到 12.5GHz。

因此可明白，除了崩潰電壓亦會因 passivation 下降外，etch damage 所造成之特性影響主要是外部轉導、通道電流及崩潰電壓。

Studies of AlGaN/GaN Heterostructure Filed Effect Transistors

Student：Leaf Chen　　　　　　　　　　Advisor：Dr. Chien-Ping Lee

Institute of Electronics
National Chiao Tung University

Abstract

In this study, we focus on structure characteristics of GaN heterostructure FET Gate recess can change gate position to modify threshold voltage and to optimize device performance.During recess etching, two things are concerned. One is to avoid active layer being over etched. And therefore the etching rate can not be too fast. The other is to avoid gate being over damaged, which causes degradation of device characteristics.

In this experiment, we use two different recess etching recipes. One is pure Cl_2, which induces gate recess to reach 50Åand threshold voltage to change from -7V to -6V;the other is CL_2/Ar, which induces gate recess to reach 80Å and threshold voltage to change from -7V to -4V.After recess etching, we found that the degradation of device characteristics is mainly caused by surface trap and etching damage. Therefore, by removing surface trap with passivation, and measuring current collapse, the influences of surface trap and etch damage on device characteristics can be evaluated respectively.

In this experiment, we use undoped $Al_{0.3}Ga_{0.7}N$/GaN HFET with gate length 1 μm and gate width 50μm as the basis. Vds-Id curves of the device are measured to determine recess etching degree. After the device is completed, C-V curves are measured to determine depth of etching. We measure DC characteristics and RF performance of the device to evaluate the influence of recess etching. Threshold voltage of no recess sample is -7V, maximum channel current is 37mA under room temperature, current density of unit gate width is 740mA/mm,maximum extrinsic transconductance is 117 mS/mm. breakdown voltage >100V.After deembedding, ft is 7.5GHz and fmax is 13GHz.

Recess sample after passivation, Threshold voltage of no recess sample is -4V, maximum channel current is 20.55mA under room temperature, current density of

unit gate width is 411mA/mm,maximum extrinsic transconductance is 112 mS/mm. breakdown voltage is 61V.After deembedding, ft is 9GHz and fmax is 12.5GHz.

Therefore, etch damage influences extrinsic transconductance, channel current, and breakdown voltage of its characteristics, however, breakdown voltage also reduces due to passivation.

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