國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

利用單電荷現象研究高介電係數 CMOS 之加溫加壓回復效應與缺陷特性

Investigation of BTI Recovery Effect and Trap Properties in High-k CMOS from Single Charge Phenomena

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Abstract.

This thesis investigates post BTI (Bias Temperature Instability) stress recovery effect in high-k gate dielectric. A fast transient measurement technique is developed to retrieve the missing information during switching between stress and recovery. In small-area transistors, we measured single electron de-trapping manifested by staircase-like drain current change during PBTI (Positive BTI) recovery. By characterizing the field and temperature effects on the single charge emission time, an analytical model based on tunneling is proposed. The high-k trap density and trap activation energy are extracted.

Furthermore, the technique is applied to pMOSFETs with high-k and SiO_2 as gate

dielectric. Single hole emission is observed in both type of devices during NBTI (Negative BTI), and the responsible physical mechanism is identified to be similar to that for emission of trapped electrons. Finally, the recovery field, temperature (activation energy), and gate length effects are compared for combinations of dielectric and carrier; that is electrons in high-k nMOS, holes in high-k pMOS and holes in SiO_2 pMOS.

利用單電荷現象研究高介電係數 CMOS 之加溫加壓回復效應與缺陷特性

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摘要

本論文主要研究高介電係數 CMOS 在高溫偏壓操作(BTI)後，元件特性回復之現象。我們發展出一快速暫態的量測系統，可取得一般量測下因為施壓(stress)和回復(recovery)狀態切換太慢而忽略的資料。在小面積元件的高溫正偏壓(PBTI)實驗中，汲極電流呈現不連續的階梯變化，單一電子自陷阱釋放可明顯地量測出來。藉著描述與電場及溫度有關的單一電子發射時間，一個與穿隧效應有關的有效分析模型被提出。此高介電閘極元件之陷阱密度及陷阱活化能亦被取出。

此外，此技術亦可應用於高介電及二氧化矽之 p 型金氧半電晶體的實驗，在此兩種元件的高溫負偏壓(NBTI)實驗中，可量測到單一電洞射出，而其相關物理機制被證實與被補捉的電子釋放機制相似。最後，我們比較不同種類的元件與不同載子(電子在高介電 n 型電晶體及電洞在高介電與二氧化矽 p 型電晶體)之相關特性，例如回復電場，溫度(活化能)，還有閘極長度效應等。

Acknowledgements

I would like to express my deep gratitude to my advisor Dr. Tahui Wang for his patient guidance, encouragement and valuable discussion during the course of his study. I would like to express my sincere thanks to Chien-Tai Chan and TSMC Corporation who give me much assistance during the study of this work.

In addition, I would like to express my deepest gratitude to my friends for their continuously emotional support during the course of this study. Finally, I would like to dedicate this thesis to my parents for their support and everlasting love.

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Fig. 3.12 V_g dependence of average trapped charge emission times τ_1,τ_2 in recovery phase.(a)High-k nMOS (b)High-k pMOS (c)Oxide nMOS.

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Chapter 1
Introduction

Metal oxide semiconductor field effect transistors (MOSFETs) have been continuously scaled since they were first developed in 1960s. To date, The Silicon dioxide (SiO_2) is always chosen for MOSFETs' gate dielectrics material. With technology scaling, the thickness of gate dielectric has to be made progressively smaller.

Scaling of gate dielectric thickness is for the purpose of improving transistor performance, but it increases quantum mechanical direct tunneling leakage current [1.1]. The standby power consumption thus increases to an intolerable level. To solve this problem, high permittivity (high-k) materials are emerged as a post-SiO_2 solution [1.2]. Effort of research groups around the globe is now focusing on hafnium-based materials, exploring the nature of these materials extensively, like the film composition, process optimization, reliability assessment and analysis [1.3-1.6].

Recently, HfSiON has been successfully integrated into CMOS as gate dielectrics for low power applications, with good reliability, comparable mobility (as SiO_2) and significantly reduced gate leakage [1.4]. Figure.1.1 shows the gate leakage, J_g, for HfSiON samples used in this work, versus that for SiO_2 with several equivalent oxide thicknesses (EOT) [1.4]. The leakage is lower for the HfSiON samples, than for SiO_2 of similar EOT.

Although high-k materials have been regarded as good replacement for SiO_2 gate dielectric devices, there are still challenges for implementing high-k dielectric. One of these challenges is stress-induced V_t-instability behavior [1.7-1.10]. Compared with SiO_2, hafnium-based oxides show significant threshold voltage shift due to charging

of the pre-existing traps [1.8-1.9]. Figure.1.2 illustrates I_d-V_g characteristics of the nMOS transistor obtained after positive voltage stress for various stress times [1.11]. Stress increases the threshold voltage but it does not degrade the sub-threshold slope. Figure.1.2 leads us to the conclusion that the threshold voltage shift is due to trapping of the charges in the bulk of the dielectric.

BTI (bias temperature instability) effect was observed for SiO_2 gate dielectrics long ago [1.12]. On one hand, unlike SiO_2 where NBTI (negative bias temperature instability) in pMOS dictates lifetime extrapolation [1.13], high-k dielectric suffers from PBTI (positive bias temperature instability) in nMOS which is believed to be essentially related to charge trapping in high-k [1.14]. On the other hand, similar to NBTI in SiO_2, both PBTI degradation (charge trapping) and recovery (charge de-trapping) are being studied [1.14].

In Chapter 2, we study properties of the traps in HfSiON by characterizing single electron emission during PBTI recovery with a novel transient measurement technique. By exploring the post-stress recovery transient of drain current in small devices, an analytical model based on tunneling is developed. According to the model, high-k trap density and trap activation energy are extracted.

In Chapter 3, the drain current recovery transient in a large-area device is successfully reproduced with the analytical model developed in Chapter 2. In addition, NBTI in HfSiON and in SiO_2 are also investigated. Single charge (electron for PBTI, and hole for NBTI) emission is compared among the three conditions. Finally, we give a conclusion in Chapter 4.

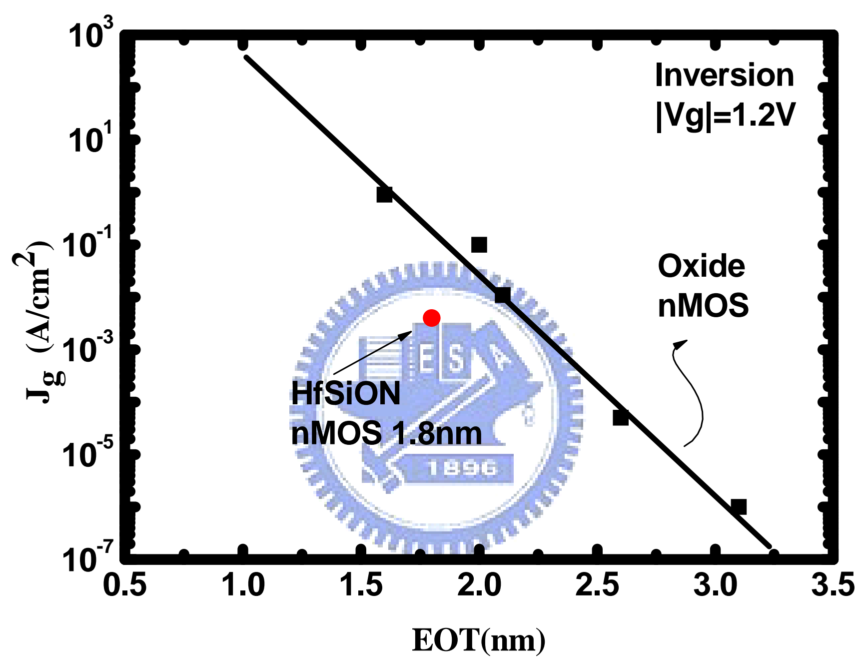


Fig.1.1 HfSiON nMOS with~2 orders gate current reduction.[1.4]

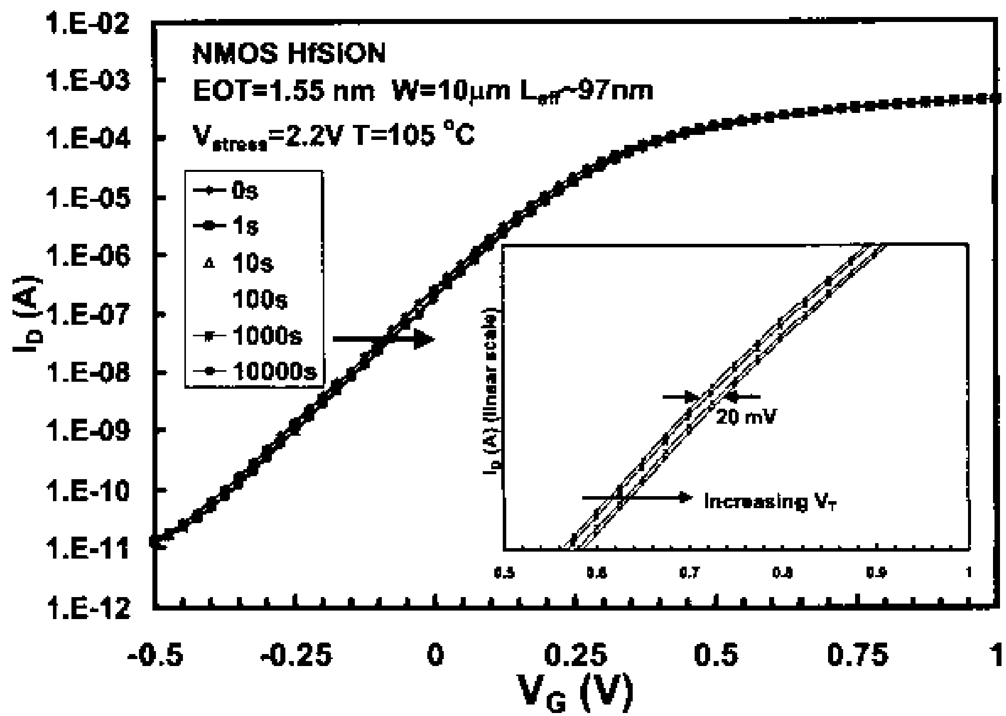


Fig.1.2 Typical I_d-V_g hysteresis (V_t instability) in high-k nMOSFET. [1.11]

Chapter 2
Single-Electron Emission of Traps in HfSiON

2.1 Introduction

The cause of BTI is believed to be essentially related to charge trapping in high-k [2.1, 2.2]. BTI is commonly characterized by stressing transistors at a high temperature and electric field, periodically interrupting the stress to monitor threshold voltage and/or drain current. The other way to investigate BTI effect is to measure post-stress recovery behavior [2.3].

To identify the charge de-trapping mechanism, a novel method for characterizing high-k gate dielectric is demonstrated, in which direct measurement of single-electron de-trapping manifested by discontinuous step-like drain current is measured. The physical path of de-trapping can be identified accordingly. An analytical model based on tunneling can predict the emission time behavior, and gives the high-k trap density.

2.2 Fast Transient Measurement

The trapped charge behavior in high-k gate dielectric is studied by “stress” and “recovery” as shown in Fig. 2.1, where the temporal evolution of drain current is recorded by a digital oscilloscope and the time delay during phase transition is minimized by high-speed switches down to μs. The sampling rate is 10^4 readings per second. Fig. 2.2 illustrates the bias conditions applied the gate and drain. During the stress phase, electrons in the inversion channel are injected into the high-k bulk traps. During the recovery phase, trapped electrons discharge. Fig. 2.3 shows the photography of our micro-second transient measurement circuit.

2.3 Single-Electron Emission Time of Traps in HfSiON

The transient measurement setup is tested on MOSFETs with SiO_2 as gate dielectric, stable current-time characteristics (Fig. 2.4) ensure that this method induces no spurious current transient.

2.3.1 Transient Recovery in Large Devices

The device has an area of 100μm*0.08μm. As shown in Fig. 2.5, after stress (V_g=0.7V, 0.2s) is removed, I_d increases with logarithmic time dependence during recovery (V_g/V_d=0.3/0.2V) and saturates to a level close to the pre-stress one, suggesting full recovery for the chosen stress condition. Notably, the observation time window extends four decades from 1ms to 10s. In traditional measurements, it takes a minimum delay for seconds between stress and recovery during which a significant portion of recovery is happening (Fig. 2.5). Transient measurement is demonstrated to be necessary for accurate analysis.

2.3.2 Single Electron Emission in Small Devices

In a large area device, the recovery I_d represents a collective effect of numerous traps in high-k and rises smoothly with recovery time (Fig. 2.5). While the same experiment (identical stress and recovery conditions) is conducted on a small (W/L=0.16μm/0.08μm) device where only a few traps are present, the recovery I_d, interestingly, exhibits a staircase-like evolution, as indicated in Fig. 2.6. In this study, each drain current step corresponds to a "single" electron de-trapping from the high-k dielectric. Interestingly, the time of occurrence for each electron de-trapping (i.e. τ_1, τ_2, and τ_3) (or referred to as emission time) increases with V_g applied in "recovery" (Fig. 2.7). Ten measurements of each V_g bias on the same device were made to take average. Furthermore, as expected, the emission time of electron de-trapping is found to decrease at elevated temperatures (Fig. 2.8). The activation energy extracted from the Arrehnius plot is about 0.18eV. The experimental results will be used to identify

the mechanism of electron de-trapping in high-k gate dielectric as discussed in the next section.

2.4 Trapped Electron Emission Mechanism

There are three possible paths for electron de-trapping as illustrated in the energy band diagram in Fig. 2.9, i.e. Frenkel-Poole (F-P) emission (path a), tunneling (path b) toward the gate electrode, and tunneling toward the Si substrate (path c). The de-trapping path (a) is ruled out, since the activation energy for F-P mechanism should be equal to the trap energy, E_t (>1eV), and the extracted E_a is only 0.18eV. The de-trapping path (b) is ruled out too since a larger V_g would accelerate the electron emission toward the gate electrode resulting in a shorter emission time. The observed trend is just the opposite (Fig. 2.7). Initially, we attempted to use direct tunneling for describing electron de-trapping. However, it fails to account for the field and temperature effect due to lack of relevant parameters in its formalism. Moreover, Leroux et al. successfully modeled hysteresis in high-k by utilizing SRH kinetics in their calculation [2.4]. Consequently, a SRH-like thermally-assisted-tunneling (TAT) is incorporated in our model and will be given in detail in the next section. Temperature dependence (Fig. 2.8) with extracted activation energy of 0.18eV confirms the role of thermal process in charge emission.

2.5 Analytical Model

An analytical model of the TAT mechanism is developed with energy band diagram and trap distance illustrated in Fig. 2.10:

$$\tau_i^{-1} = \upsilon \exp(-\alpha_{ox} T_{ox}) \exp(-\alpha_k x_1) \quad (2.1)$$

where

$$\upsilon = [N_c(1-f_c)]\upsilon_{th}[\sigma_0 \exp(\frac{-E_a}{kT})] \quad (2.1a)$$

$$\alpha_{ox} = \frac{2\sqrt{2m_{ox}^* q(E_t + \Phi_B)}}{\hbar}; \alpha_k = \frac{2\sqrt{2m_k^* qE_t}}{\hbar} \quad (2.1b)$$

Eq. (2.1) reveals the nature of tunneling for trapped electron emission time, τ_i. The pre-factor υ, a lumped parameter referred to as the "attempt-to-escape frequency" can be re-written as in Eq. (2.1a) [2.3] where N_C is the effective density-of-state in the Si conduction band, $N_C(1-f_c)$ is the amount of available states in Si substrate for out-tunneling electrons from high-k traps, σ_0 and E_a represent the trap cross-section and the activation energy. Other variables have their usual definitions. The Fermi-Dirac distribution (f_c) in the Si conduction band is a function of V_g in "recovery." A smaller recovery V_g leads to a lower surface carrier density (a smaller f_c) and thus a shorter electron emission time. As the recovery V_g drops below the threshold voltage (V_t), decrease in the emission time tends to saturate since f_c approaches zero. The electron nearest to the interface of Si substrate will be the first one for de-trapping to occur. With respect to the temperature effect, a small recovery V_g (<0.25V), where f_c~0, was chosen for measurement of the trap activation energy to exclude the temperature dependence of f_c, as shown in Fig. 2.8. The extracted activation energy from the Arrhenius plot is 0.18eV.

2.6 High-k Trap Density

The high-k trap density can be evaluated through the analytical model, Eq. (2.1). By comparing

$$\tau_1 = \upsilon^{-1} \exp(\alpha_{ox} T_{ox}) \exp(\alpha_k x_1)$$
$$\tau_2 = \upsilon^{-1} \exp(\alpha_{ox} T_{ox}) \exp(\alpha_k x_2)$$

we obtain

$$\frac{\tau_2}{\tau_1} = \exp[\alpha_k (x_2 - x_1)] \tag{2.2}$$

and the high-k trap density (N_t) is readily calculated as

$$N_t = \frac{1}{(x_2 - x_1)WL} = \frac{1}{WL \frac{1}{\alpha_k} \ln(\frac{\tau_2}{\tau_1})} \tag{2.3}$$

Eq. (2.2) predicts that the ratio of emission times (e.g. τ_2 to τ_1) is only related to the physical distance of trap sites away from the interface. Fig.2.11 indeed shows the ratio of τ_2/τ_1 (10 readings of each gate bias on the same device) is constant and independent of recovery V_g. The average high-k trap density calculated from Eq. (2.3) (assuming m^*_k ~0.18m_0 [2.5]) is $3.5*10^{17}cm^{-3}$, or equivalently, an areal density of $8.8*10^{10}cm^{-2}$. This small trap density can hardly be resolved by CP due to a comparable interface trap density [2.6]. It should be pointed out that the extracted trap density, according to Eq. (2.3), is not affected by variables such as T_{ox}, m^*_{ox} and E_a. The total available number of traps in high-k gate dielectric of each device for the stress (electron filling) condition is related to high-k thickness, trap density, and transistor size. The observed 3 electrons trapped in the nMOS after the "stress" in this study are less than the total traps (~10) as calculated from the estimated trap density and transistor size.

2.7 Gate Length Effects

The experiment was conducted on devices with different gate lengths, 0.08μm, 0.14μm, and 0.22μm. It is found that while step-like current recovery traces due to single-electron de-trapping are still observed for all lengths, the amplitude of the drain current step (ΔI_d) decreases with longer gate lengths, as shown in Fig.2.12. This trend is consistent with the Random Telegraph Signal (RTS) theory [2.7] and implies that the impact of the trapped electron in the high-k dielectric spreads over the entire channel. Thus, a single-electron emission can be observed only when the device size is small enough and the high-k is clean enough!

2.8 Modeling of PBTI Recovery Transient in a Large-area Device

In a large area device, the high-k charge de-trapping rate is

$$Q(x,t) = Q(x,0)\exp[-t/\tau(x)] \tag{2.4}$$

where $Q(x,t)=qN_t(x,t)$ is the time-dependent trapped charge density and $\tau(x)$ is described in Eq. (2.1). The threshold voltage shift ΔV_t induced by trapped electron emission can be written as

$$\Delta V_t(t) = \sum_i \frac{\Delta Q(x_i,t)}{C(x_i)} = \sum_i \frac{qN_t(x_i,0)}{\varepsilon_{HK}}(T_{HK} - x_i)[1 - \exp(\frac{-t}{\tau_i})] \tag{2.5}$$

where $C(x_i)$ is the corresponding capacitance for trapped charges located at x_i from high-k/IL interface, and ε_{HK} and T_{HK} are permittivity and physical thickness of the high-k layer respectively. For a large amount of trapped charges, the summation in Eq. (2.5) can be replaced by an integration,

$$\Delta V_t(t) = \int_0^x \frac{qN_t(x,0)}{\varepsilon_{HK}}(T_{HK} - x)\{1 - \exp[-t/\tau(x)]\}dx. \tag{2.6}$$

where $\tau(x)=A\exp(\alpha_k x)$ and $A=[N_C(1-f_c)\nu_{th}\sigma_0\exp(-E_a/kT)]^{-1}\exp(\alpha_{ox}T_{ox})$. Because the double exponential $\exp[-t/\tau(x)]=\exp[(-t/A)\exp(-\alpha_k x)]$ in the integrand changes abruptly from 0 to 1 around $x=(\alpha_k)^{-1}\ln(t/A)$, it can be approximated by a step-function:

$$\exp[(-\frac{t}{A})\exp(-\alpha_k x)] = \begin{cases} 0 & \text{for } x \le (\alpha_k)^{-1}\ln(t/A) \\ 1 & \text{for } x \ge (\alpha_k)^{-1}\ln(t/A) \end{cases} \quad (2.7)$$

This approximation translates into a "clear-cut" picture; after time t, electrons with emission times shorter than t are completely de-trapped while all of the rest remain trapped. Therefore, Eq. (2.6) is further simplified,

$$\Delta V_t(t) \approx \frac{qN_t}{\varepsilon_{HK}} \int_0^{(\alpha_k)^{-1}\ln(t/A)} (T_{HK} - x)dx. \quad (2.8)$$

The time window of interest for modeling is four decades as indicated in Fig. 2.13. According to Eq. (2.2), the time span is equivalent to a physical distance of around 10Å in high-k, or an equivalent oxide thickness (EOT) of 2Å. Therefore, the term T_{HK}-x in Eq. (2.8) is approximated as a constant, or x_{eff}, and Eq. (2.8) reduces to

$$\Delta V_t(t) \approx \frac{qN_t\overline{x_{eff}}}{\varepsilon_{HK}\alpha_k}\ln(\frac{t}{A}). \quad (2.9)$$

The corresponding recovery drain current evolution can be written as

$$\Delta I_d(t) \approx \frac{-qG_m N_t\overline{x_{eff}}}{\varepsilon_{HK}\alpha_k}\ln(\frac{t}{A}). \quad (2.10)$$

where G_m(=dI/dV) is the transconductance. Using the extracted N_t and E_a from a small device, the simulated recovery transient from Eq. (2.10) is shown in Fig. 2.13

and is in good agreement with the measured result. Eq. (2.10) also reveals that the recovery slope in Fig. 2.13 is directly correlated to the high-k trap density.

The injected electrons may fill different energy traps at larger stress V_g. In this case, the trap energy distribution should be taken into account and Eq. (2.10) is modified as follows

$$\Delta I_d(t) \propto \int_{\Delta E} \frac{-qG_m N_t(E_t)\overline{x_{eff}}}{\varepsilon_{HK}\alpha_k(E_t)} dE_t \ln(t) \tag{2.11}$$

where ΔE represents the energy range of trapped charges. $\Delta I_d(t)$ still follows log-time dependence.

Finally, the authors would like to remark that we chose a very short stress time (0.2s) in this study. The purpose is to characterize the pre-existing high-k traps only.

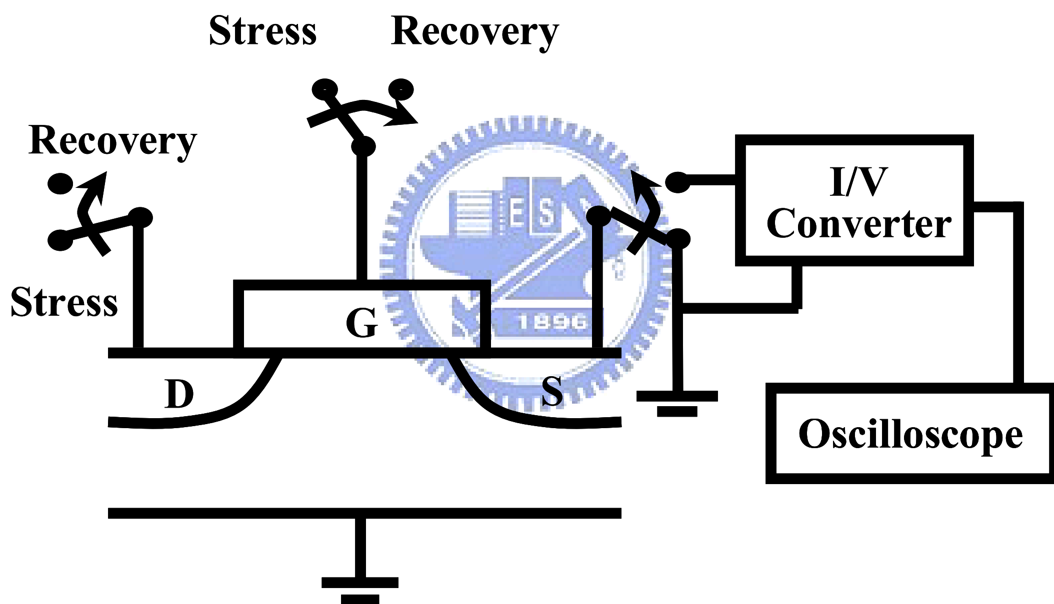


Fig. 2.1 Experimental setup to measure high-k trapped charge emission times. In stress phase, V_g=0.7V, V_d=0V for 0.1s. In recovery phase, V_g=0.25~0.55V, and V_d=0.2V, and drain current temporal evolution is recorded by an digital oscilloscope. The high-speed switches minimize the delay between phase trasition down to μs.

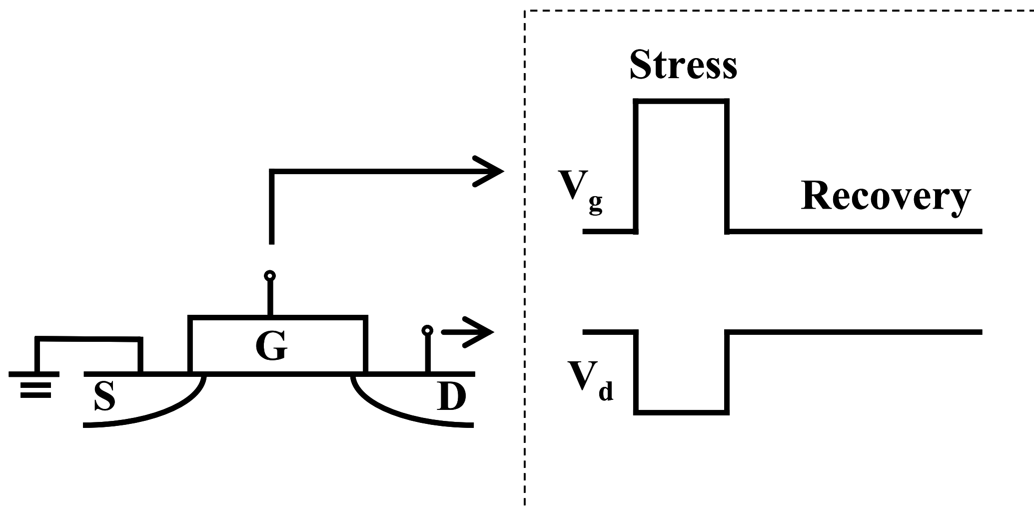


Fig. 2.2 Bias conditions for stress and recovery phases.

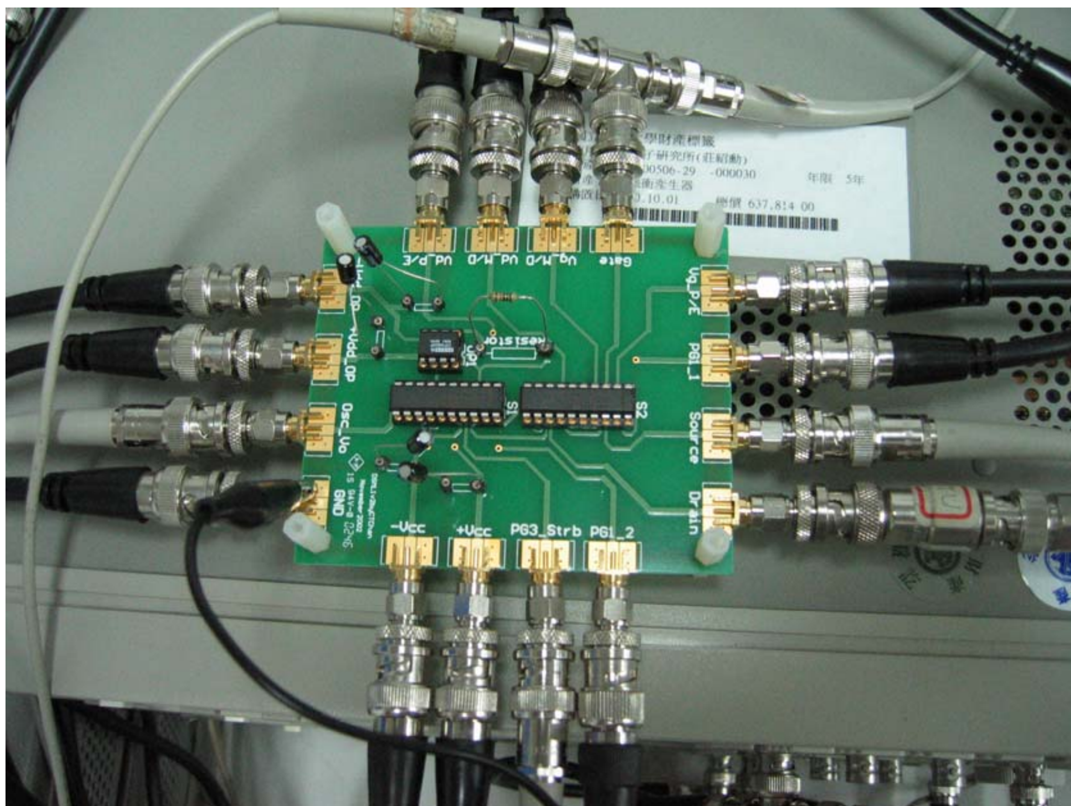


Fig. 2.3 The photograph of the micro-second measurement system used in this work.

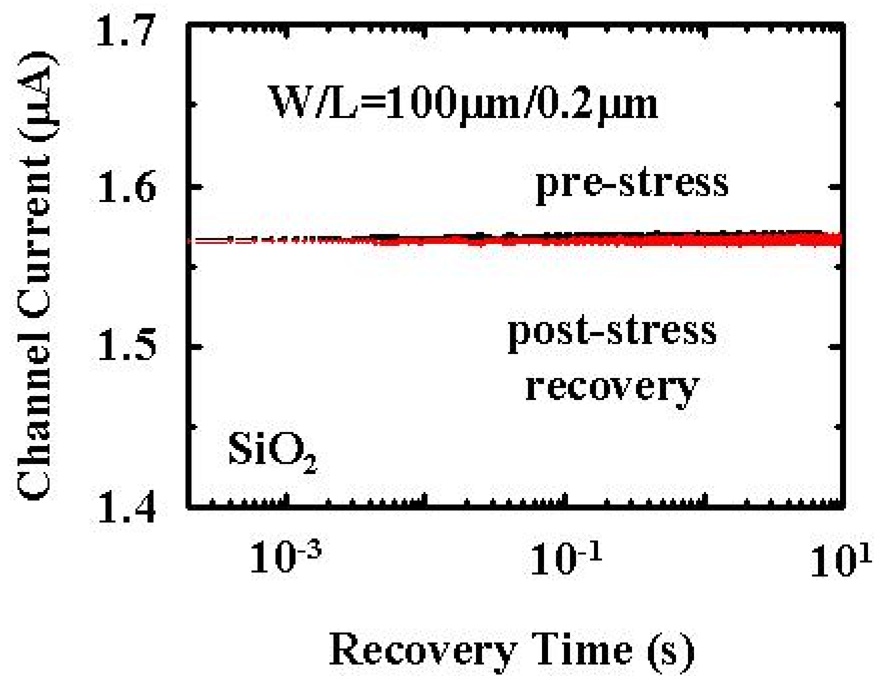


Fig. 2.4 Stable current-time characteristics in oxide gate dielectrics ensure that this method induces no spurious current transient in HK.

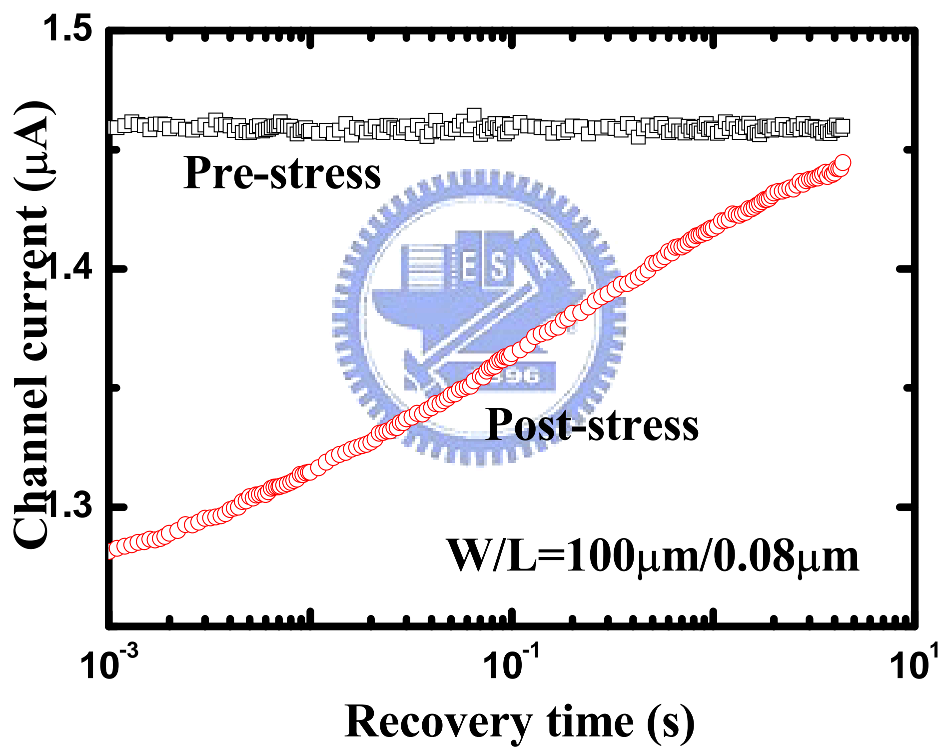


Fig. 2.5 PBTI recovery transient, usually underestimated is significant. The recovery drain current follows logarithmic time dependence.

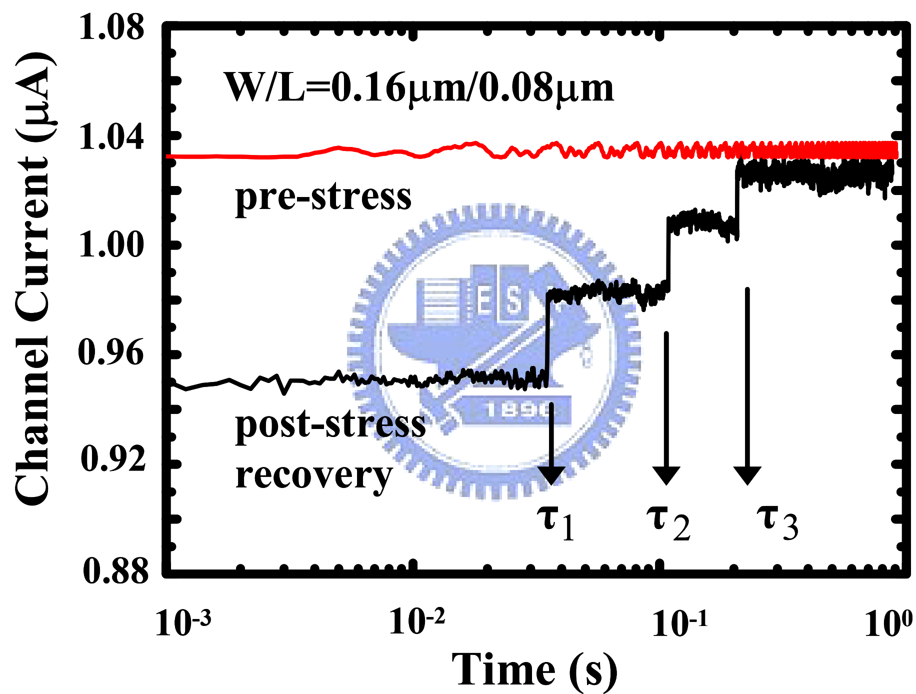


Fig. 2.6 Pre- and Post-stress current evolutions in a high-k nMOSFET with W/L=0.16μm/0.08μm. The measurement bias is V_g=0.3V and V_d=0.2V. Each current jump in the post-stress recovery corresponds to a single trapped charge escape from the high-k gate dielectric. Only three electrons are trapped during stress. The charge emission times in recovery phase are denoted by τ_1, τ_2, and τ_3 in the figure.

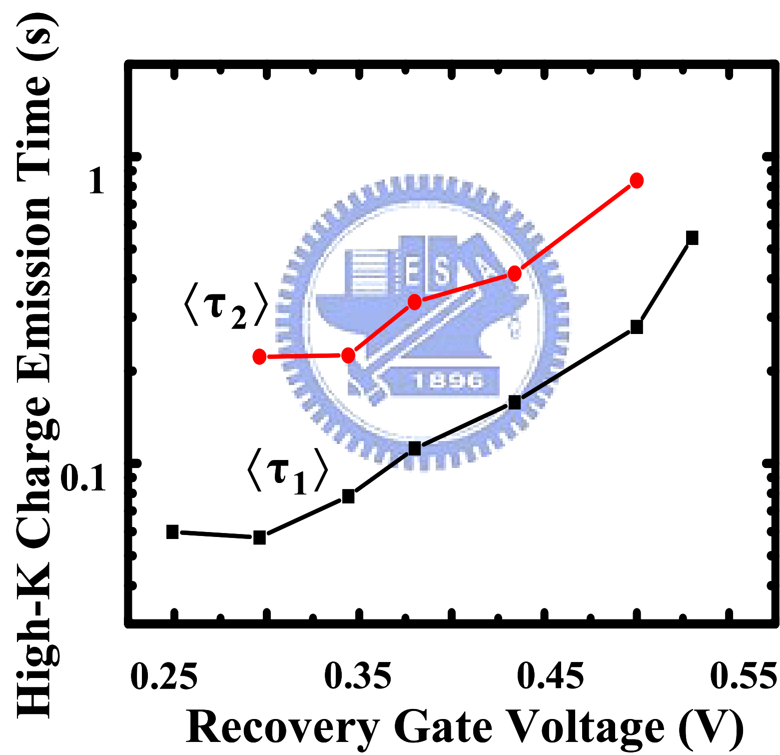


Fig. 2.7 Gate voltage dependence of averaged high-k trapped charge emission times $<\tau_1>$ and $<\tau_2>$ in recovery phase. Ten measurements on the same device are made to take average.

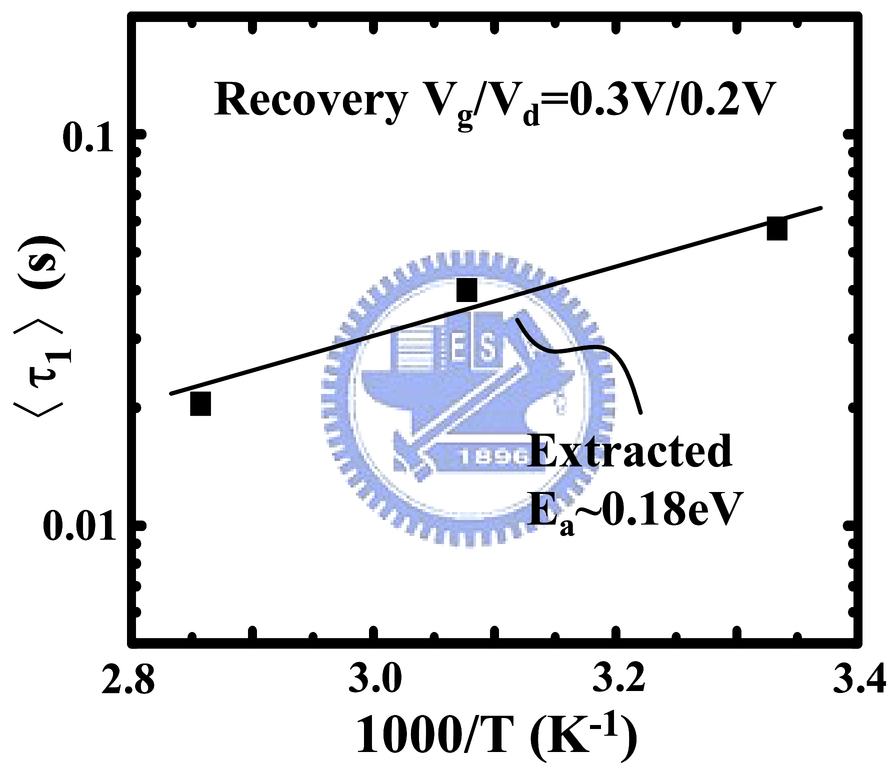


Fig. 2.8 Temperature dependence of <τ_1>. The extracted activation energy is ~0.18eV.

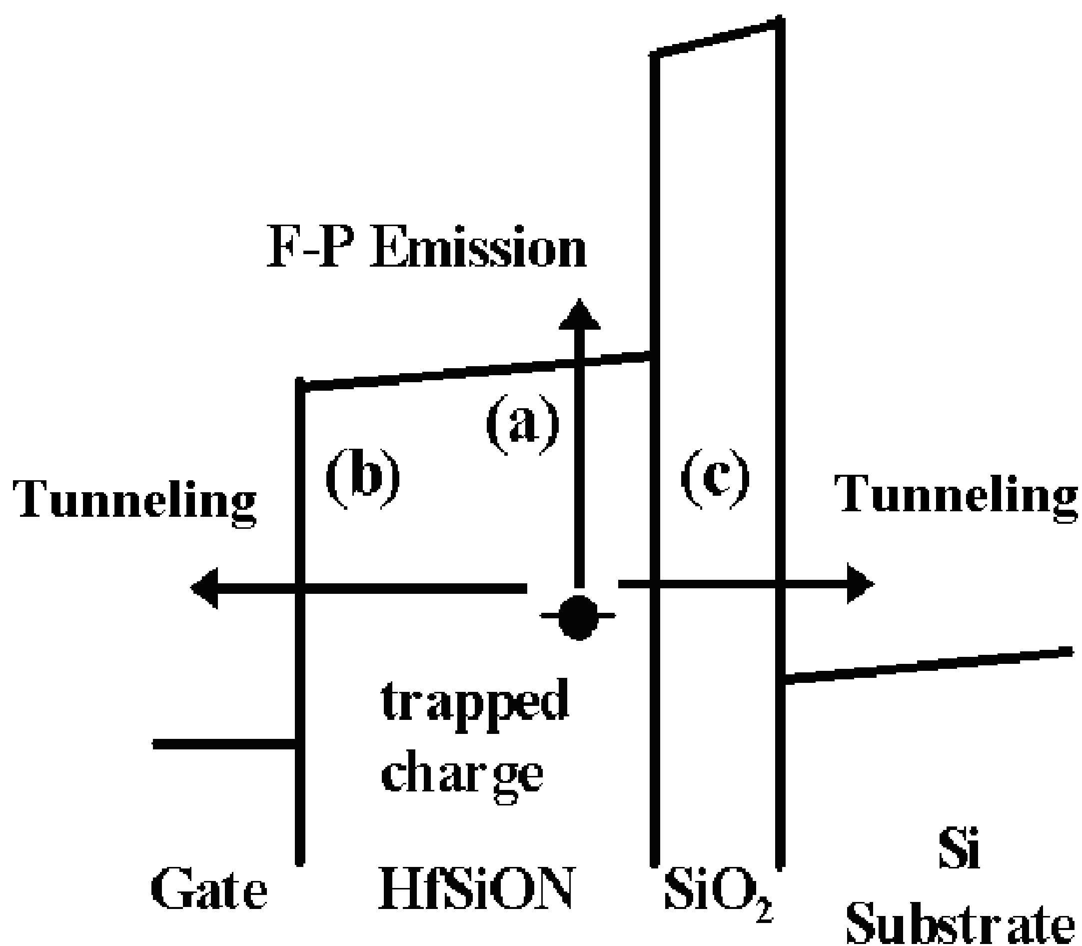


Fig. 2.9 Energy band diagram in recovery phase. Various charge escape paths are illustrated: (a) Frenkel-Poole (F-P) emission, (b) thermally-assisted-tunneling (TAT) to the gate, and (c) TAT to the Si substrate. From V_g dependence and temperature dependence of charge emission time in Fig.3 and Fig.4, only (c) should be considered.

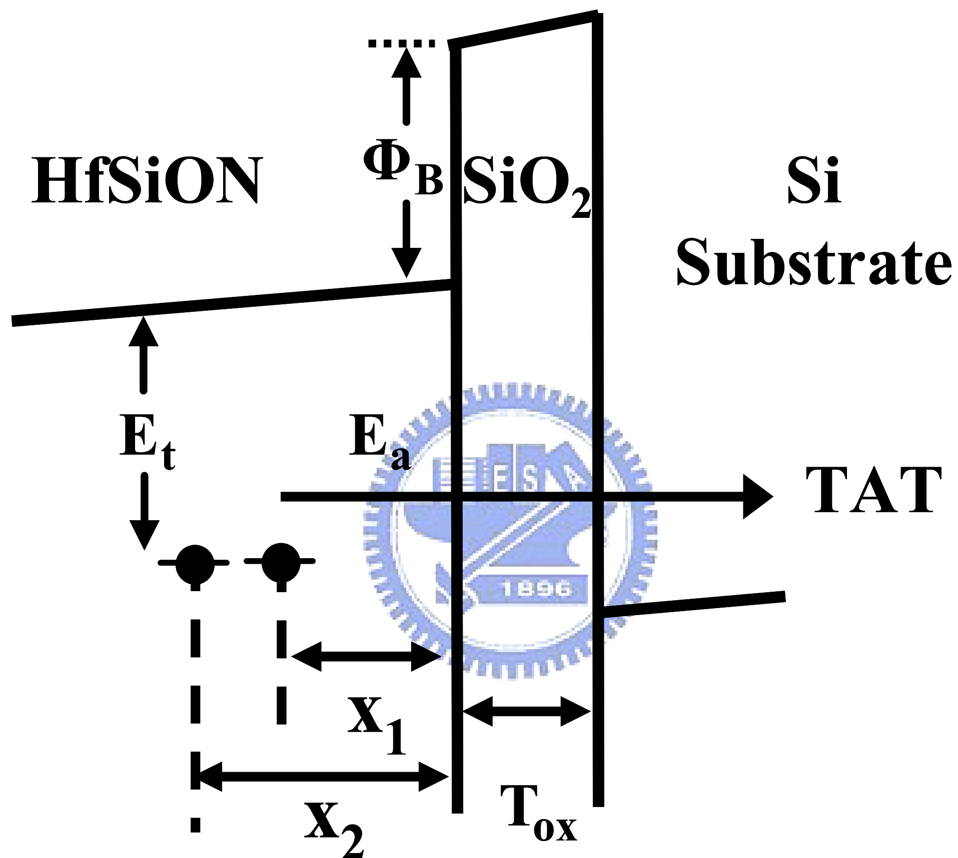


Fig. 2.10 Schematic representation of gate dielectric band diagram in recovery phase and trap positions. E_a is the activation energy for TAT, and the proposed model is described in detail in the text.

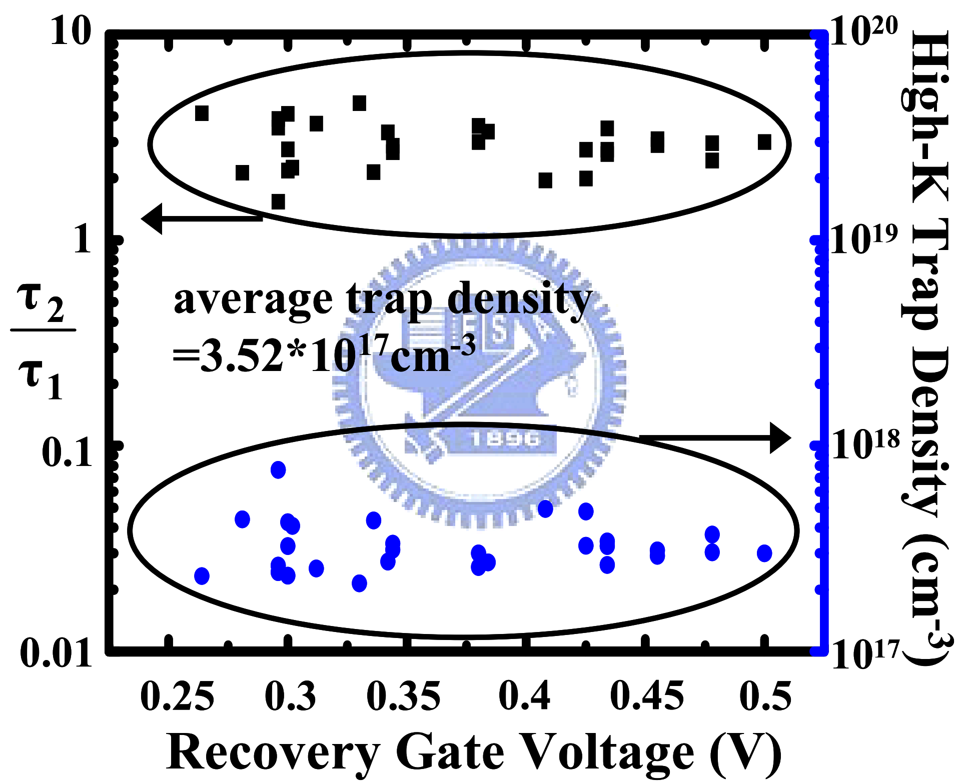
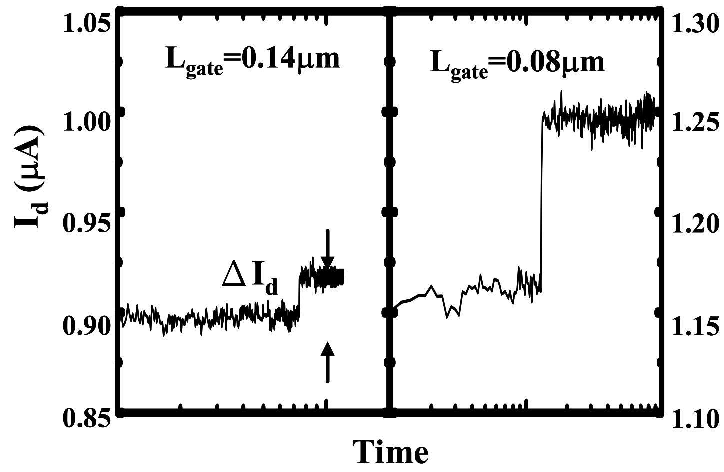
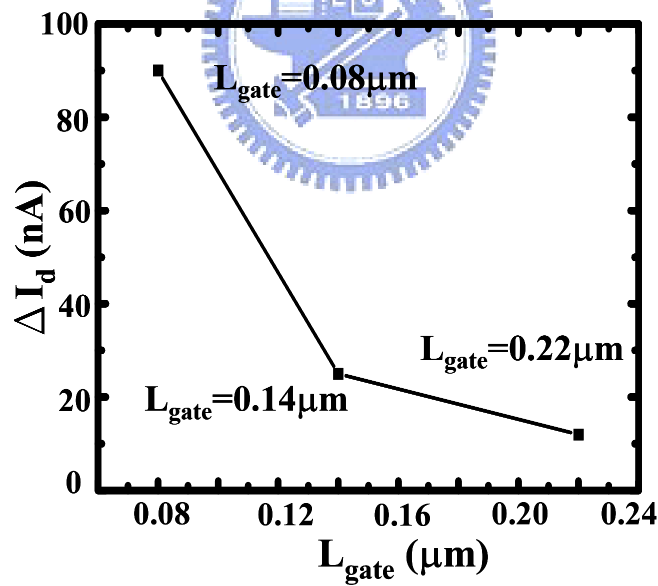


Fig. 2.11 The ratio of τ_2 to τ_1 versus gate voltage in recovery phase. Note that τ_2/τ_1 remains almost unchanged with respect to V_g. The extracted high-k trap density is also given. Totally, 10 devices are measured in the figure.



(a)



(b)

Fig. 2.12 (a) Comparison of the current jump amplitude for L_{gate}=0.08μm and for L_{gate}=0.14μm. (b) The amplitude of charge escape induced current jump versus L_{gate}.

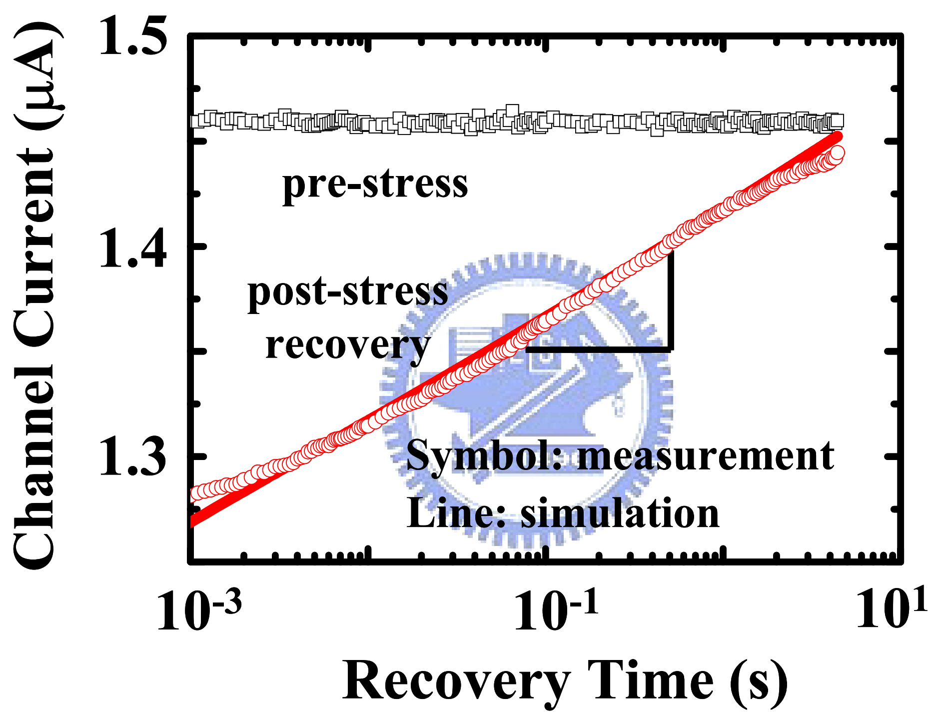


Fig. 2.13 High-k, nMOS (W/L=100μm/0.08μm), continuous recovery trace. The calculated recovery transient (line) is in good agreement with experimental result (symbols).

Chapter 3
Applications of the Transient Measurement Technique

3.1 Introduction

In Chapter 2, the electron traps in HfSiON nMOSFETs have been characterized, and based on the experimental results we proposed an analytical model responsible for high-k trapped charge de-trapping. We can accordingly evaluate the trap density either from the current quantum jumps measurement or from drain current recovery slope. The activation energy can also be extracted by de-trapping the charges at different temperatures. In this chapter, firstly, high-k degradation effect is studied by both experimental techniques (current jumps and recovery slope). We introduce a four-phase experimental procedure: stress-discharge-filling-recovery. After the high-k film is degraded, both the number of current jumps and the recovery slope for drain current change, indicating trap growth.

Secondly, the technique developed for exploring single electron phenomena is utilized to investigate properties of hole traps during NBTI recovery in pMOSFETs with high-k and SiO_2 as gate dielectric. The effects of gate length, recovery gate voltage, and temperature are compared between different carrier types (electron traps vs. hole traps) and between different materials (high-k vs. SiO_2).

3.2 High-k Degradation: A Transient Analysis

To investigate high-k degradation effect, we propose a four-phase experimental procedure: stress, discharge, filling and recovery. Fig. 3.1 illustrates the bias conditions for the four phases respectively. In the "stress" phase (Fig. 3.1a), a large

positive V_g is applied with all other terminals grounded to damage and generate additional traps in the gate dielectric. The devices are then "discharged" at a negative V_g (-1.5V, 20s), shown in Fig. 3.1b. Following that, the devices are subjected to "filling" (Fig. 3.1c) immediately followed by "recovery" (Fig. 3.1d) (fast switching by the circuit in Fig.2.1). The recovery drain current change is monitored and recorded for further analysis. The "discharge" phase is required to empty (as much as possible) the trapped charges introduced during the stress phase which may probably lead to incorrect results from the "filling" and "recovery" phases. The filling and recovery conditions are exactly identical to those in Chapter. 2 (termed as "stress and recovery" in Chapter 2, though).

Fig. 3.2 shows the recovery drain currents in high-k nMOSFETs before and after a constant voltage stress at V_g=3.5V for 500s. The device area is W*L=0.16*0.08μm^2. According to (2.3) in Chapter 2, the trap density can be obtained by two equivalent ways. One fixes the numerator as unity (one interval between two traps) and the trap density can be calculated once the ratio of emission times is known. The other fixes the denominator (here, two decades, from 0.01s to 1s) and the trap density can be calculated as well simply by counting the number of current jumps within the pre-set window. The latter is suitable for the case where the recovery patterns are complicated, or more jumps. Indicated in Fig.3.2, the pre-stress curve has only one current jump while the post-stress one has five jumps. Increase in the number of current jumps corresponds to increase in trap density as a result of constant voltage stress.

On the other hand, recovery drain current slope is demonstrated to be directly correlated to trap density in gate dielectric in Chapter 2 (section 2.8). Fig. 3.3 indicates the change in recovery slope with stress time. Again, increase in slope corresponds to increase in trap density as a result of constant voltage stress. The trap growth rate is extracted as shown in Fig. 3.4.

3.3 NBTI Recovery Transient in pMOSFETs: High-k

Fig. 3.5 illustrates the device structures used for comparison in this and the next section. The EOT is 1.8nm and 2nm for high-k and for SiO_2 respectively. Fig.3.6 shows the drain current evolution during recovery for small-area high-k pMOSFETs (W/L= 0.16μm/0.08μm). Similar to that in its nMOS counterparts, the drain current transient exhibits staircase-like current discontinuities. Each current jump here is believed due to a single trapped hole emission from traps in high-k. While the V_g for filling holes into the high-k gate dielectric is -0.8V, the V_g needed for injecting holes into SiO_2 devices (see section 3.4) is larger than -1.5V. Therefore, the possibility of de-trapped charges from the interfacial SiO_2 layer is excluded since for the V_g (-0.8V) used there is no holes injected into the interfacial SiO_2 layer. The trapped holes are de-trapped from high-k.

The dependence of charge emission times on recovery gate voltage (Fig. 3.7) and temperature (Fig. 3.8) are measured, and the trend is similar to those for trapped electrons (Chapter 2), only different in relative dependence. This confirms similar de-trapping mechanism for both trapped electrons in nMOS and trapped holes in pMOS. The extracted activation energy for trapped holes is 0.14eV, slightly smaller than that for trapped electrons (0.18eV, Fig. 2.7). The gate length effect is also measured as indicated in Fig. 3.9.

3.4 Comparison among Different Gate Dielectrics

Single hole de-trapping is observed in SiO_2-gated pMOSFETs [3.1], shown in Fig. 3.10c. The V_g and temperature effects are also measured. Fig. 3.11 compares the dependence of the current jump amplitude ($\triangle I_d$) on gate length. The recovery drain voltage is kept at 0.2V for all lengths in all devices in order to alleviate V_d effect [3.2]. For all cases, shorter devices have larger current jump amplitude. The large current

jump amplitude for electrons than holes regardless of dielectric material is probably due to smaller mobility for holes [3.2].

Fig. 3.12 shows similar recovery V_g dependence for all cases, stronger for nMOS, though. It proves that both electron and hole emission path is from gate dielectric to channel both in HfSiON and SiO_2 for the chosen charge-injection condition. Fig. 3.13 demonstrates the temperature effect of τ_1. The activation energy of HfSiON nMOS (0.18eV) and pMOS (0.14eV) are comparable, and higher in SiO_2 pMOS (0.5eV, Fig. 3.13c), indicating that the activation energy is dependent on the material type, not on the carrier type.

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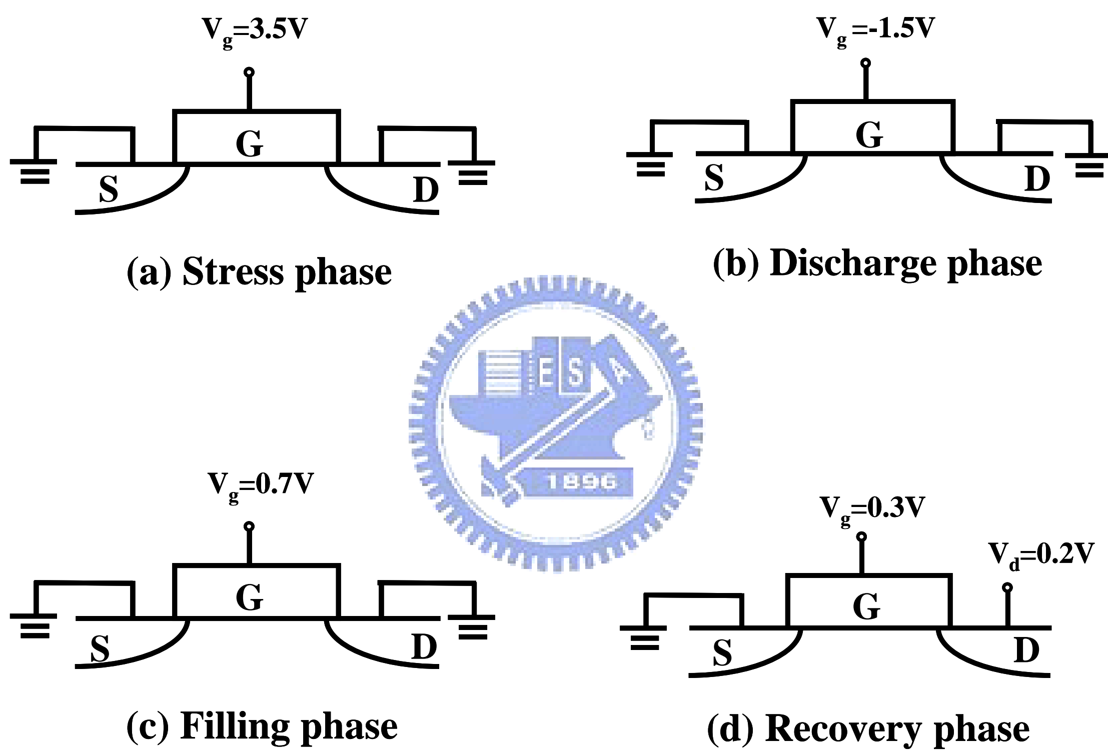

Fig. 3.1 Illustrations for four phases with bias conditions (a) stress phase, (b) discharge phase, (c) filling phase, and (d) recovery phase.

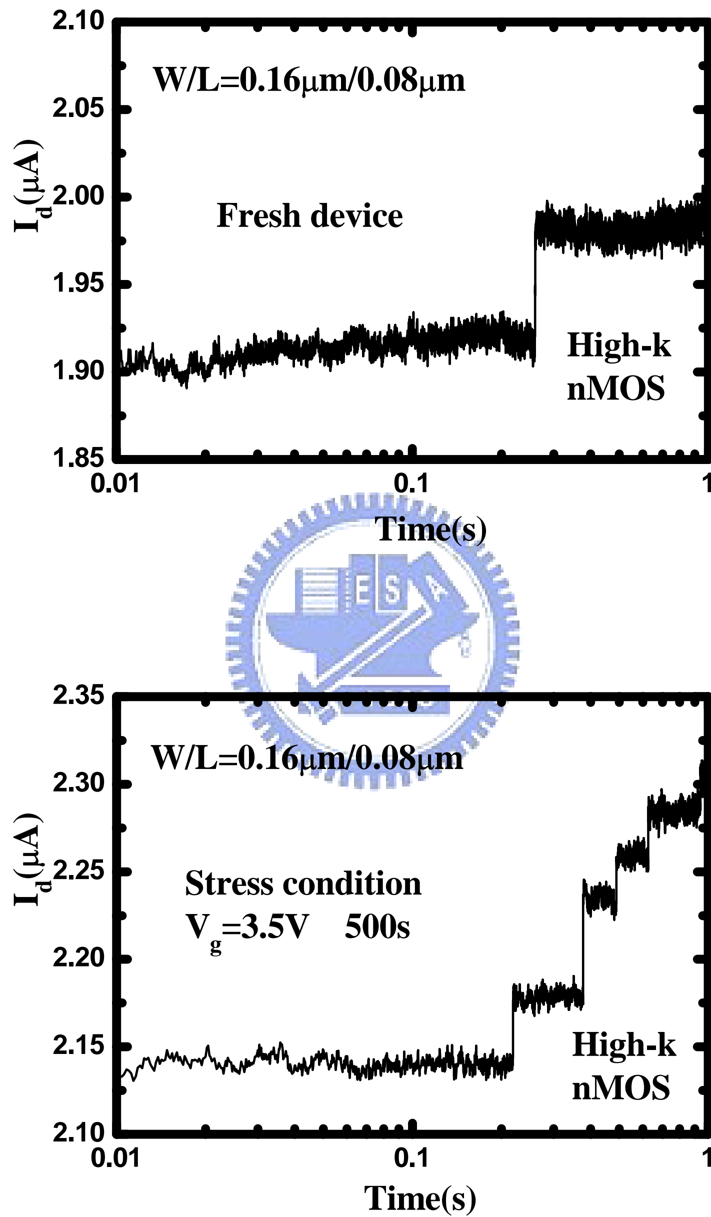

Fig 3.2 Electron quantum jump in small area devices (W/L=0.16μm/ 0.08μm) before and after positive V_g stress.

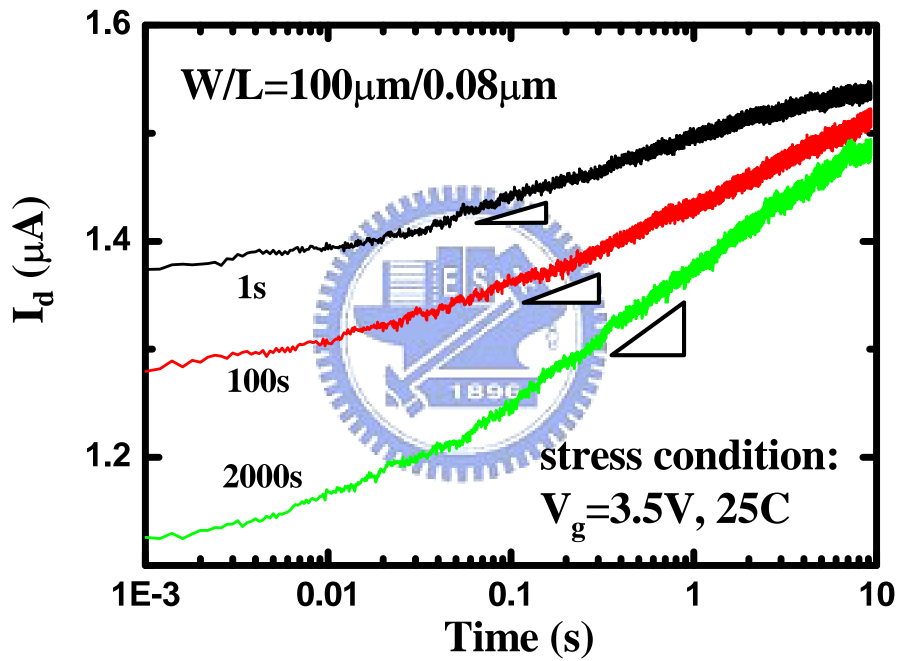

Fig 3.3 NMOS recovery I_d traces in a large area device (W/L=100μm/0.08μm). The slope increases with stress time.

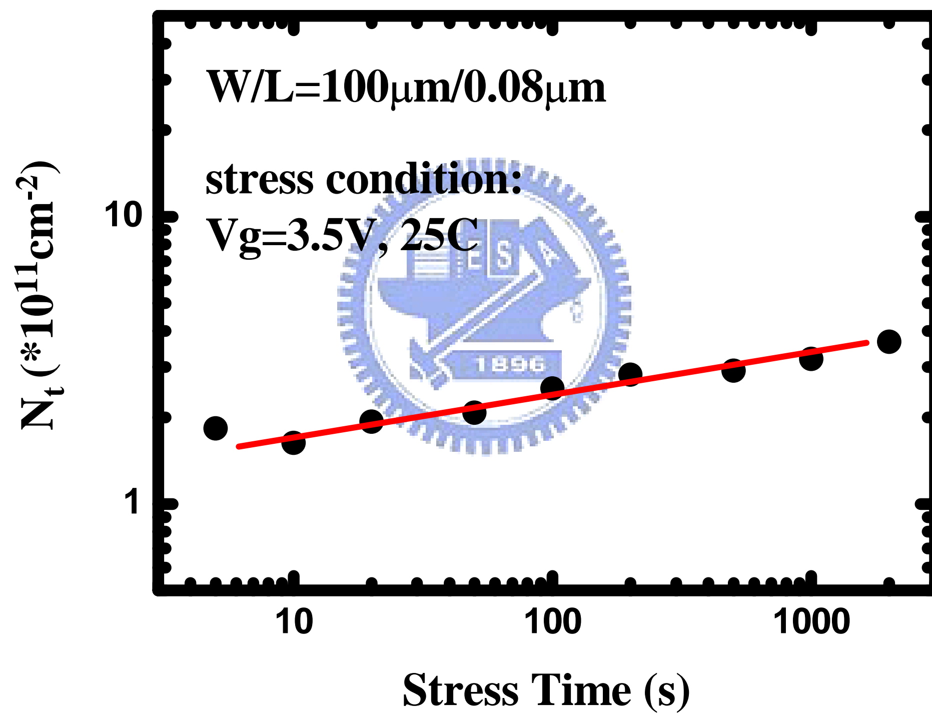

Fig 3.4 High-k trap density as a function of stress time.

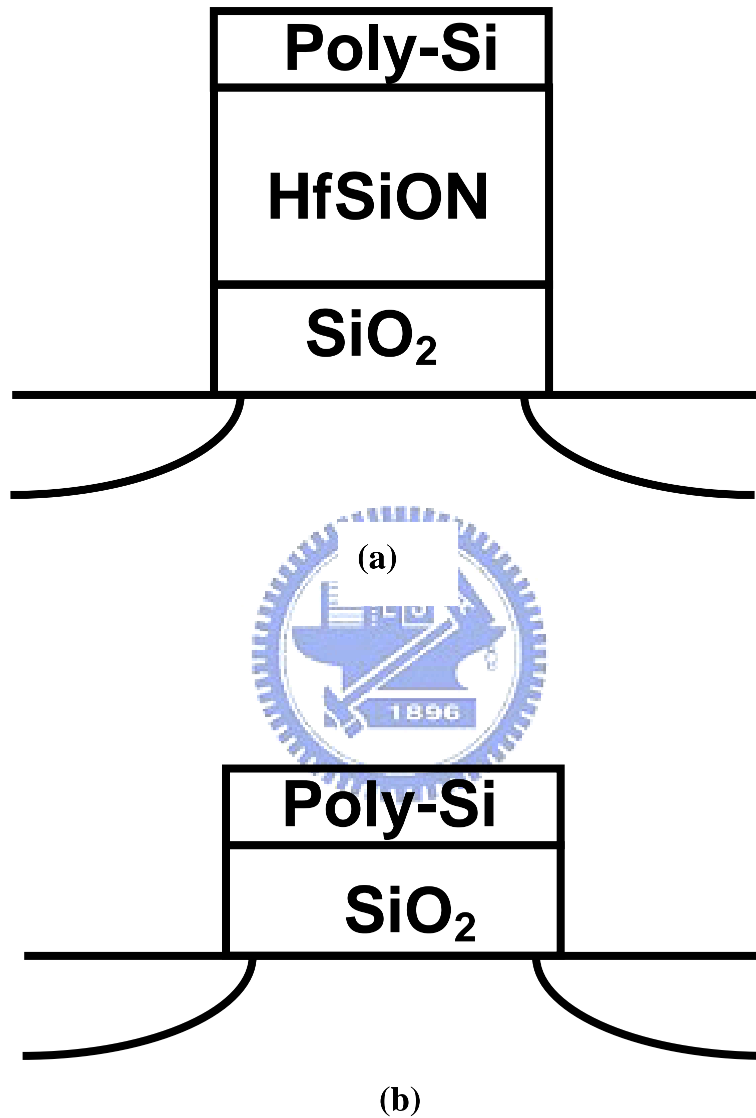

Fig 3.5 (a)the device structure of High-k with EOT=18Å
(b)the device structure of Oxide with EOT=20Å

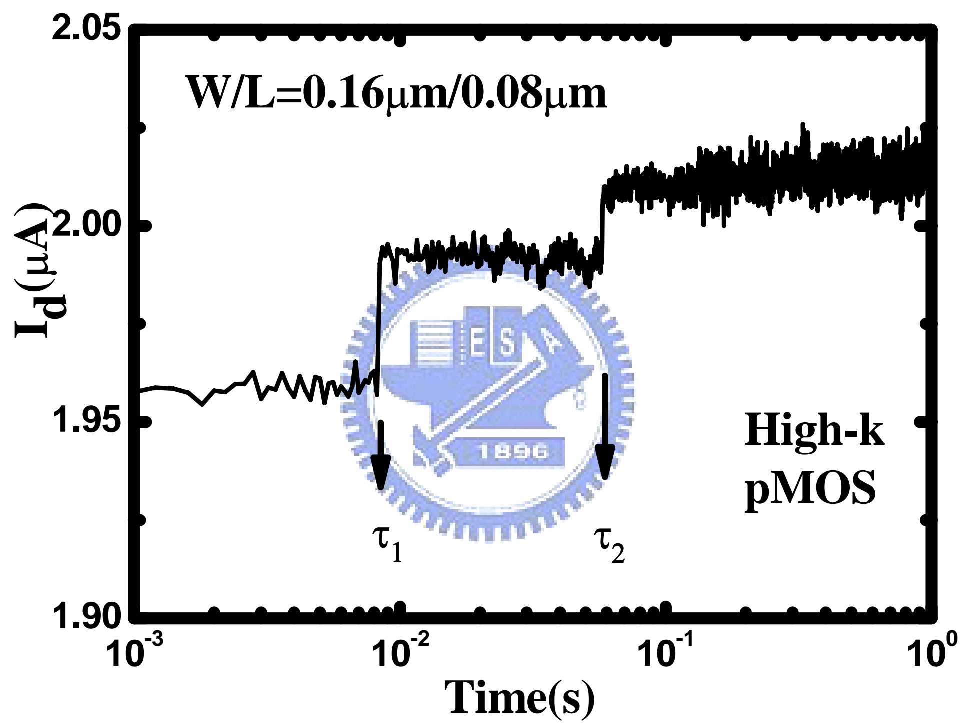

Fig. 3.6 Step-like channel current evolution during NBTI recovery in small area devices (W/L=0.16μm/0.08μm). τ_1 and τ_2 denote trapped hole emission times.

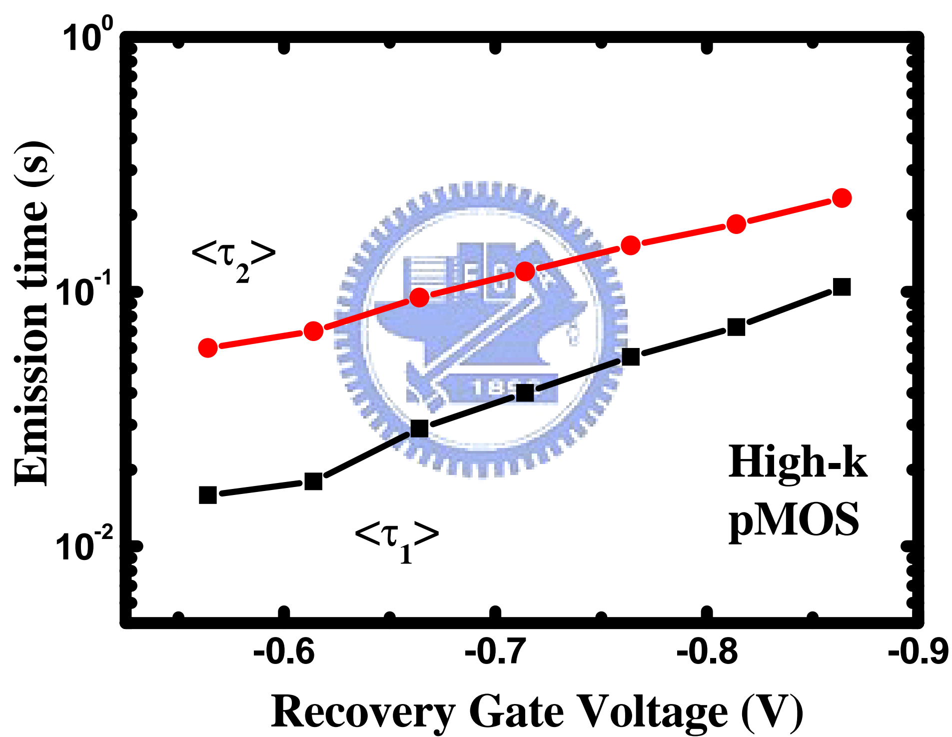

Fig. 3.7 The V_g dependence of average trapped hole emission times, τ_1 and τ_2. Ten measurements on the same device are made to take average.

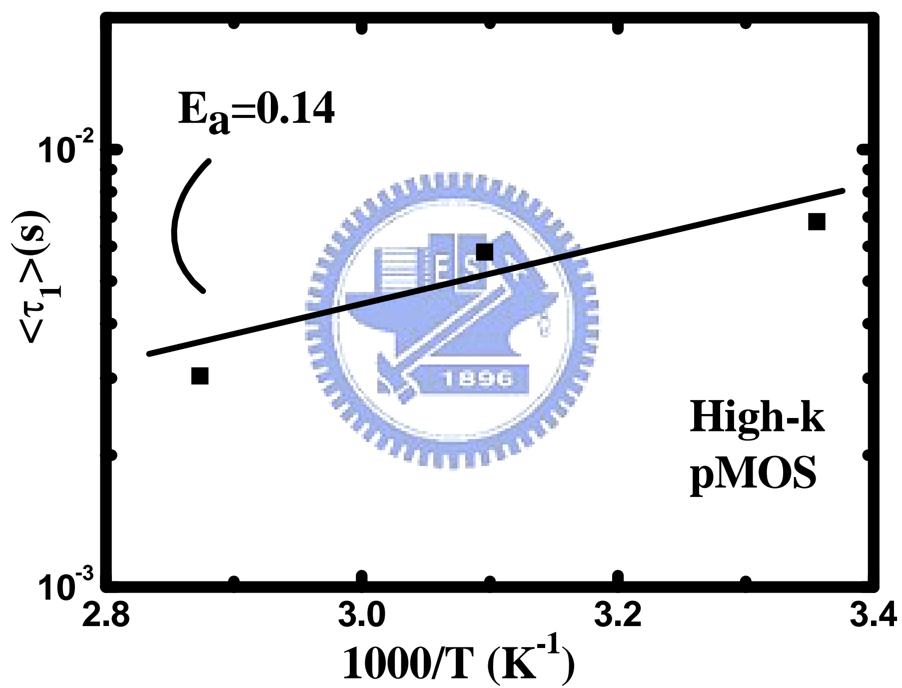

Fig. 3.8 Temperature dependence of τ_1. The extracted activation energy (E_a) from the Arrehnius plot is about 0.14eV

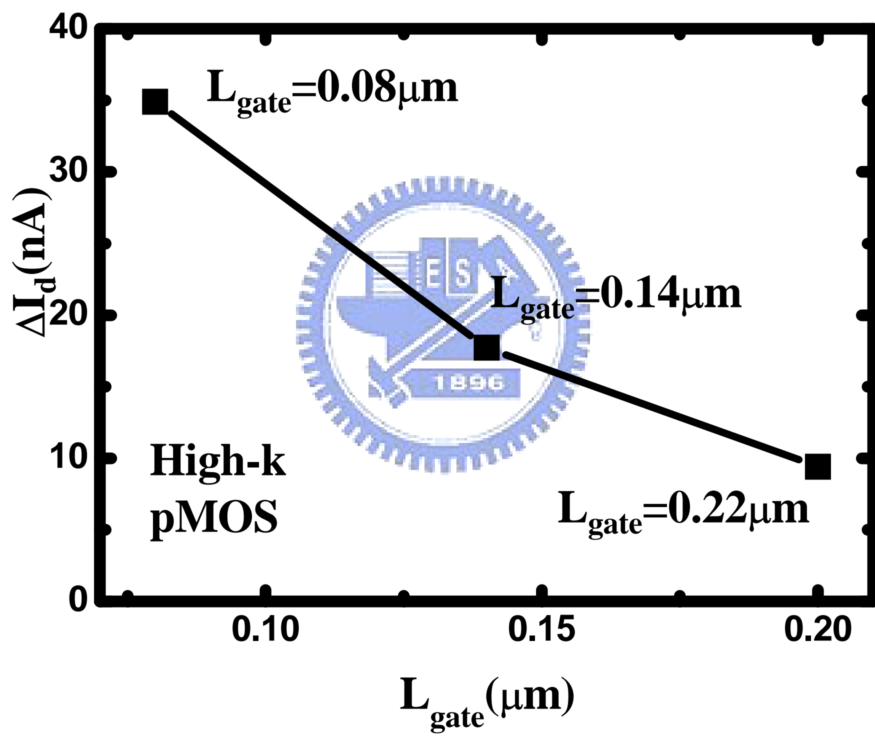

Fig. 3.9 The amplitude of measured current jump (ΔI_d) versus gate length.

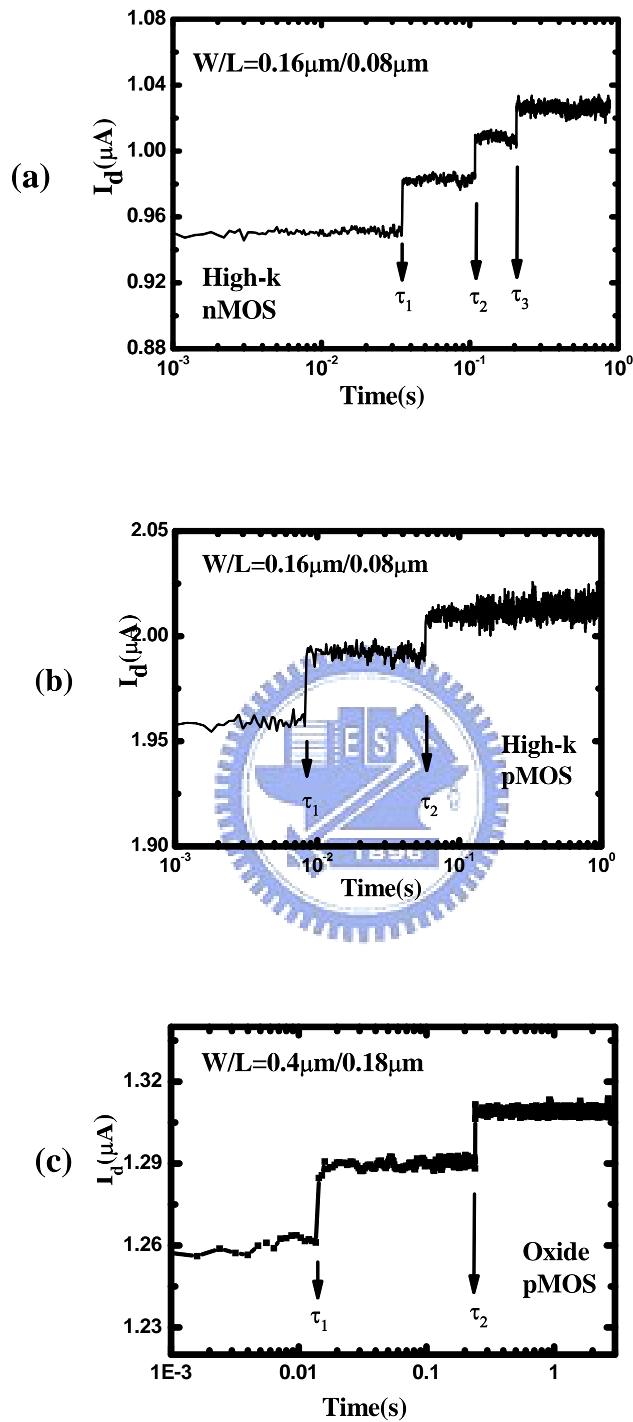

Fig 3.10 Step-like channel current evolution during recovery in (a)High-k nMOS(W/L=0.16μm/0.08μm) (b)High-k pMOS (W/L=0.16μm/0.08μm) (c)Oxide nMOS (W/L=0.4μm/ 0.18μm)

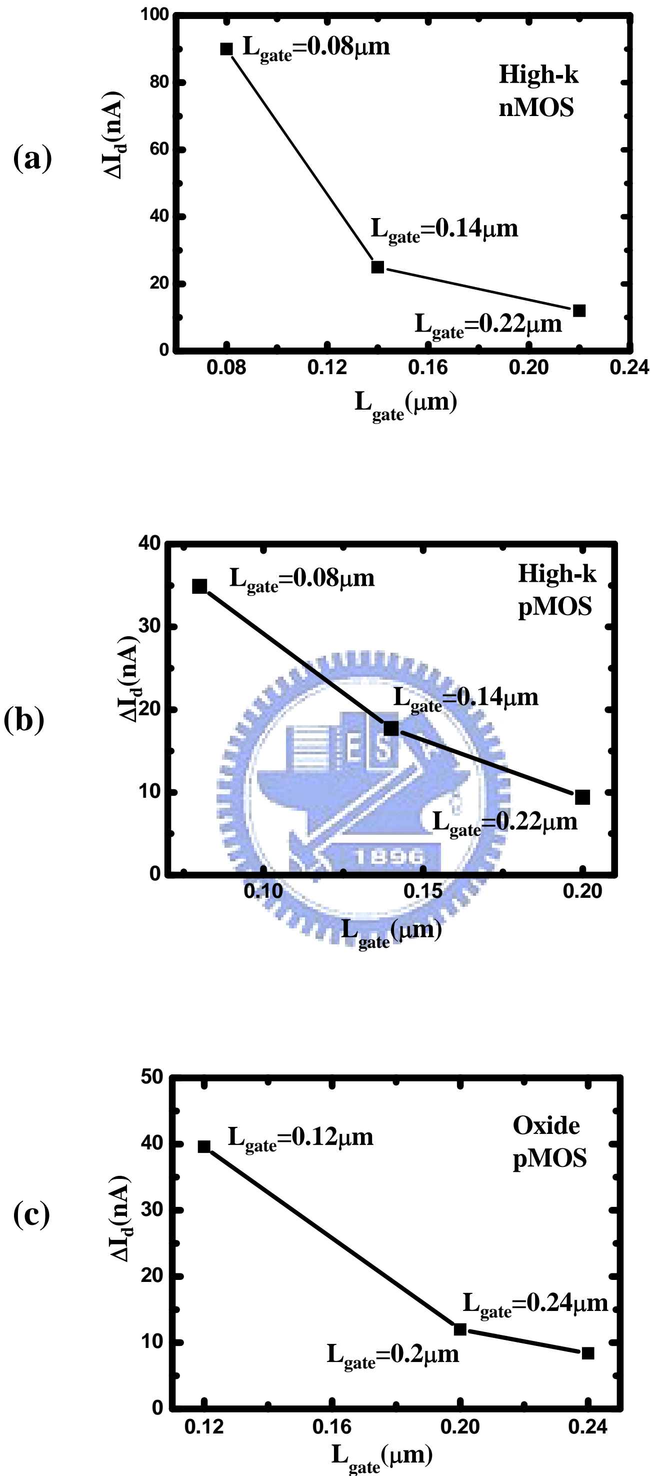

Fig 3.11 The amplitude of measured current jump($\triangle I_d$) versus gate length (a)High-k nMOS (b)High-k pMOS (c)Oxide pMOS

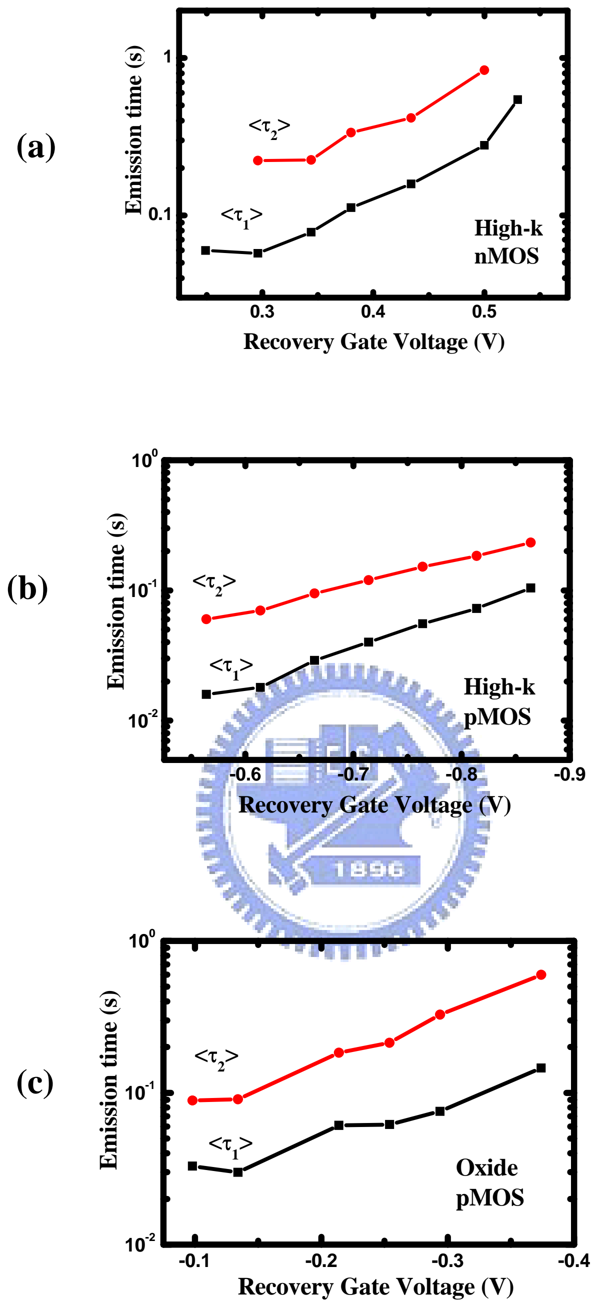

Fig 3.12 V_g dependence of average High-k trapped charge emission times τ_1,τ_2 in recovery phase.(a)High-k nMOS (b)High-k pMOS (c)Oxide nMOS.

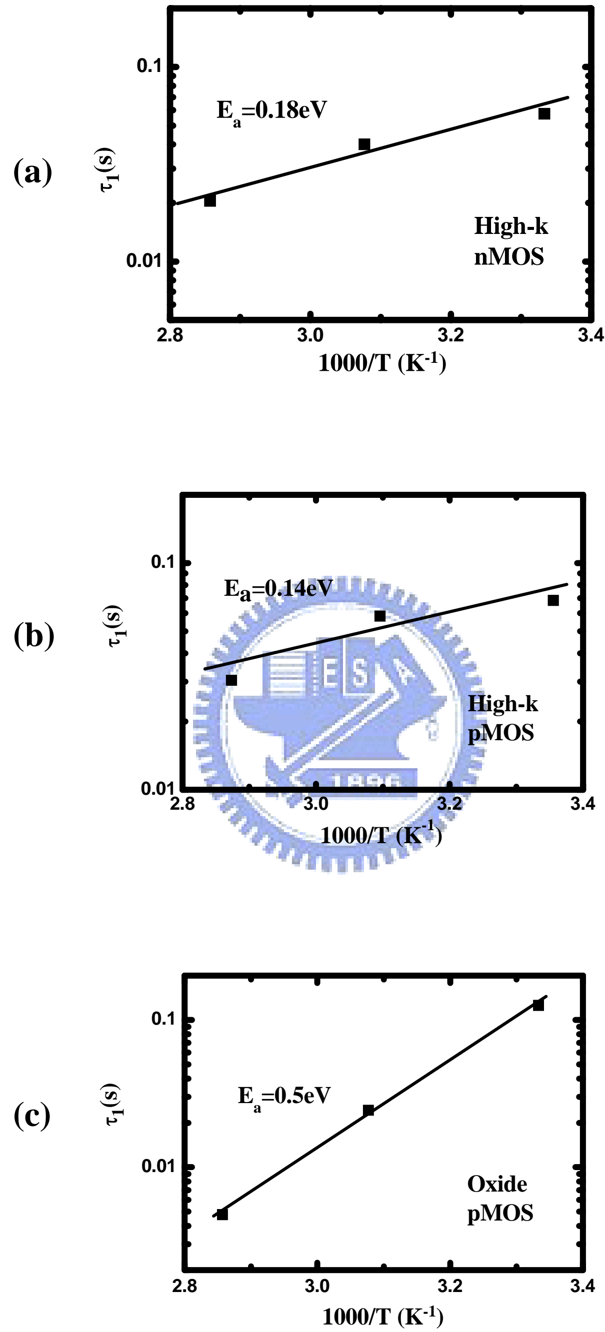

Fig 3.13 Temperature dependence of τ_1 (a)E_a of High-k nMOS= 0.18eV (b)E_a of High-k pMOS=0.14eV (c)E_a of SiO_2 pMOS=0.5eV

Chapter 4
Conclusion

A fast transient measurement setup and technique is developed in this work. The technique is firstly used to study PBTI recovery transient in HfSiON nMOSFETs. Single electron emission from traps in HfSiON gate dielectric is observed in small-size devices. Based on the characterization of recovery field and temperature effects on the single electron phenomena, a SRH-like thermally-assisted-tunneling model for trapped charge emission is proposed. The model well explains the experimental results and the prediction it makes is verified by measurement. The extracted trap activation energy is 0.18eV. Results from large- and small-size devices are well correlated. It is found that the trap density can be evaluated self-consistently from the ratio of trapped charge emission times (small devices) and from drain current recovery slope (large devices). The recovery transient for a large-area device is also well reproduced and follows logarithmic time dependence.

Furthermore, the technique is applied to pMOSFETs with high-k and SiO_2 as gate dielectric for single hole analysis. Comparison shows the emission mechanism is universal for transient electron/hole de-trapping in high-k and SiO_2. It is also found that the role of thermal process (activation energy) depends on material type (high-k or SiO_2), not on carrier type (electron or hole). The proposed technique is a powerful tool to characterize traps in gate dielectric for advanced CMOS.

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碩士論文題目:

利用單電荷現象研究高介電係數

CMOS 之加溫加壓回復效應與缺陷特性

Investigation of BTI Recovery Effect and Trap Properties in High-k CMOS from Single Charge Phenomena