國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

具有複晶矽鍺閘極與局部形變通道之 P 型金氧半場效電晶體元件製作與分析

Fabrication and Characterization of PMOSFETs with Poly-SiGe gate and Locally Strained Channel

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中 華 民 國 九 十 四 年 六 月

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FABRICATION AND CHARACTERIZATION OF PMOSFETs WITH POLY-SIGE GATE AND LOCALLY STRAINED CHANNEL

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摘 要

我們探討具有複晶矽鍺閘極、與電漿增強式化學氣相沉積氮化矽覆蓋層之 P 型金氧半場效電晶體（PMOSFETs）特性。其中，使用複晶矽鍺閘極，可以有效降低閘極空乏與硼穿透效應；而以電漿增強式化學氣相沉積之氮化矽層，可以提供通道區域內的壓縮應力。由於通道內的壓縮應力增強，P 型金氧半場效電晶體之驅動電流隨著氮化矽層厚度增加而增大。同時，我們也探討，具壓縮應變通道的金氧半場效電晶體，其負偏壓溫度不穩定特性（NBTI）。雖然氮化矽覆蓋層可以增大 P 型金氧半場效電晶體的驅動電流，但負偏壓溫度不穩定效應卻較未覆蓋氮化矽之電晶體更形嚴重。特別是在高溫條件下，氮化矽層造成的區域應力導致較多的介面狀態產生，這可能是由於通道內的應變

能量造成大量矽氫鍵結斷裂。而覆蓋氮化矽之 P 型金氧半場效電晶體，在高溫長時間的應力施加下，由於大部分的矽氫鍵結被打斷，臨界電壓與介面狀態開始呈現飽和現象。電性回復效應可以有效降低介面狀態的產生，因此動態負偏壓溫度不穩定性與交流應力也被用來模擬電路中元件的操作特性。我們觀察到，交流應力頻率強烈影響具有氮化矽覆蓋層元件之臨界電壓改變、與介面狀態產生。

Fabrication and Characterization of PMOSFETs with Poly-SiGe gate and Locally Strained Channel

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Abstract

A PMOSFET structure featuring poly-SiGe gate and plasma-enhanced CVD (PECVD) silicon nitride (SiN) capping layer was explored. Poly-SiGe gate is useful to reduce gate depletion and boron penetration, while PE-SiN is used to induce compressive strain locally inside the channel region. PMOSFET's drive current is enhanced as the thickness of SiN layer increases due to increasing compressive strain in the channel region. Negative bias temperature instability (NBTI) characteristics of PMOSFETs with compressive strain in the channel were also investigated. Although PMOSFET with SiN capping layer show enhanced drive current, its NBTI is worsened, compared to its counterpart without SiN capping layer. A lot of interface states are generated especially in high temperature stress of PMOSFET with SiN layer. This is

ascribed to a higher amount of hydrogen incorporated during SiN deposition as well as the high strain energy stored in the channel. For PMOSFET with SiN layer, under sufficient long stress time at high temperature, saturation of the threshold voltage and interface states is found, indicating that most Si-H bonds are broken. Dynamic NBTI and AC stress characteristics were used to simulate the switching operation of PMOSFETs in circuits. It is observed that the electrical passivation effect could effectively reduce the generation of interface states. Both threshold voltage shift and interface-state generation are strongly dependent on the frequency of dynamic stress for devices with SiN capping layer.

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Chapter 1
Introduction

1.1 General Background

As the channel length of MOSFETs continues to scale down, it is becoming more and more difficult to maintain high transistor performance because of mobility degradation caused by increased substrate doping. The mobility of carriers in the channel is one of the important parameters for MOSFET operation. Higher mobility helps contain power consumption by allowing the use of lower operation voltage. Moreover, the urgency of incorporating high-k gate dielectric in IC manufacturing can also be relieved. Utilizing strain engineering in the channel region to improve electron and hole mobility has been actively pursued [1,2]. Recently, MOSFETs with high bi-axial tensile channel stress by growing a Si channel layer on a relaxed SiGe substrate has been demonstrated [3,4]. Performance of both NMOSFET and PMOSFET was improved by the bi-axial tensile stress when more than 20 % Ge is incorporated in the relaxed SiGe layer. However, the yield issue associated with high threading dislocation density (typically > 10^4 cm^{-2}) of the virtual SiGe substrates represents a major obstacle for practical applications. In addition, other concerns, such as high Ge content and up-diffusion, fast diffusion of n-type dopants, and high wafer cost further blight the

situation.

In contrast, approaches that introduce uni-axial channel strain can be free from the aforementioned concerns. In this aspect, channel strain can be engineered and optimized by modifying the device processing and/or structure, including those steps involving gate capping layer (e.g., SiN), trench isolation, silicidation, and source/drain [5,6]. Electron mobility gain is similar between uni-axial and biaxial tensile strains, since both originate from the splitting of the six-fold degenerate conduction band valleys. However, uni-axial longitudinal compressive stress offers much larger hole mobility enhancement at a given stress level than the bi-axial tensile strain [7], and may have lower surface roughness scattering probability due to high out-of-plane effective mass.

It has been shown that the mechanical stress from a contact etch-stop SiN layer over the gate electrode can significantly affect the drive current [8, 9]. Depending on the deposition conditions, the SiN capping layer can generate either tensile or compressive stress [9]. It thus can be applied to the NMOS devices that benefit from tensile stress, as well as PMOS devices that benefit from compressive stress.

As CMOS technology is scaled into deep-submicron regime for higher density and speed, thinner gate oxide is required to provide sufficient current drive while the supply voltage is scaled down. Ultra-thin gate oxide (<2nm) has been reported in CMOS devices [10,11]. With such thin oxides, the poly-depletion effect (PDE) and boron

penetration have become critical issues. These technical issues impose strict limitations on the process window and may degrade device performance [12,13]. The poly-SiGe has been expected as a promising alternative gate material by taking advantage of its lower PDE and boron penetration. Process compatibility with existing Si technology has been demonstrated and significant improvements of deep-submicron PMOS transistor performance have been observed [14].

Since the melting point of SiGe is lower than that of Si, physical phenomena controlling fabrication processes, such as deposition, crystallization, grain growth, and dopant activation, occur at a lower temperature for SiGe than for Si. Thus, lower process temperature can be used for fabricating devices with poly-SiGe gate. It is thus preferable to poly-Si for various applications in technologies that have limited thermal budget tolerance.

Most important for the work presented here, the p-type work-function decreases with increasing Ge mole fraction [15~20]. Implementation of poy-SiGe gate without adjusting the channel doping profile accordingly results in an increased V_T of the resultant devices, which reduces I_{OFF}. On the other hand, for a specified V_T, the channel doping is reduced to compensate for the change in work-function of the gate electrode, the channel mobility could increase due to suppressed Coulomb scattering.

With the continuous shrinking of the MOS transistor dimensions, additional

reliability issues emerge. A number of characterization schemes, such as time- or charge-to-breakdown (T_{BD} or Q_{BD}), hot carrier stress, and negative-bias-temperature-instability (NBTI) test, have been developed to evaluate the reliability of dielectrics as well as to predict the lifetime of the MOS device.

As the oxide thickness is thinned down to the regime of 3nm or less, hot carrier effects become less important due to the reduced operation voltage [21,22]. It was recently shown that the threshold voltage shift in a PMOSFET due to negative-bias-temperature (NBT) stress becomes more and more significant as oxide is scaled down.

NBTI of p-channel MOSFETs with ultra-thin gate dielectrics has been reported as one of the most serious reliability issues due to the large threshold voltage shift and drive current degradation. The NBTI degradation may even become the major factor in limiting the device lifetime when the gate oxide thickness is scaled down to 3.5 nm and less. Despite many research efforts, detailed NBTI degradation mechanism is not yet fully understood. This is further complicated by the fact that the NBTI is affected by several other factors, such as hydrogen incorporation and boron penetration.

Conventional NBTI testing based on static experimental data. The measurements disregards the electric passivation effect of the interface traps during the operation of PMOSFETs in digital circuits, and therefore overestimates the degradations of PMOS

devices. In this aspect, results of dynamic NBTI (DNBTI) stress measurements are much closer to the situation of practical circuit operation. Therefore, it is important to investigate NBTI under such dynamic stress conditions.

1.2 Organization of This Thesis

In this study we investigate the effect of compressive strain on the performance of pMOS devices with poly-SiGe gate induced by a SiN capping layer and the associated NBTI characteristics. This thesis is divides into five chapters:

In Chapter 2, we briefly describe the process flow for fabricating the pMOS devices with the poly-SiGe gate and SiN capping layer. We also present the characterization method and the stress conditions.

In Chapter 3, we show and discuss the improvement on device performance with SiN capping layer.

In Chapter 4, the results on evaluating the static and dynamic NBTI characteristics of the devices are presented. Effects of strain on the NBTI are also discussed.

Finally important conclusions generated from our experimental results are summarized in Chapter 5. Some recommendations and suggestions for future work are also given.

Chapter 2

Device Fabrication and Measurement Setup

2.1 Process Flow

The PMOSFETs were fabricated on 6-inch n-type (100) Si wafers with resistivity of 2~7Ω-cm. Standard local oxidation of silicon (LOCOS) process was used for device isolation. Threshold voltage adjustment and anti-punch through implantation were done by implanting 80 KeV As^+ and 120 KeV P^+, respectively. After the growth of 3 nm-thick thermal gate oxide, a 150nm undoped poly-SiGe layer was deposited by low-pressure chemical vapor deposition (LPCVD), followed by gate etch process to pattern the film. The Source/Drain (S/D) junctions were then formed by B^+ implantation at 10 keV and 5×10^{-15} cm^{-2}. After a 50nm TEOS spacer formation, S/D regions were etched to a depth of 30 nm. In-situ-doped SiGe (50 nm) epitaxy was subsequently performed on the recessed S/D regions by ultra-high-vacuum chemical vapor deposition (UHVCVD). Rapid thermal anneal (RTA) was then carried out in a nitrogen ambient at 900°C for 30 sec to activate dopants in the gate, S/D, and substrate regions. Afterwards, a SiN/TEOS stack layer was deposited on the transistor by plasma-enhanced CVD (PECVD). In order to investigate the effect of SiN strain, three types of samples were fabricated with split thickness of 0, 100, and 300nm, respectively. The stress

measurement performed on a blanket Si wafer capped with a SiN of 100 nm thickness indicates that 95MPa compressive stress is induced. After contact hole etching, normal metallization scheme was carried out. The final step was a forming gas anneal performed at 400°C for 30 min to mend dangling bonds and reduce interface state density in gate oxide/Si interface. Cross sectional view of the fabricated device was showed in Fig. 2.1, and transmission electron microscopy (TEM) was shown in Fig. 2.2. PMOSFETs with three different capping layers have been fabricated as shown in Table 2.1.

2.2 Electrical Characterization and Measurement Setup

Electrical characterizations and static NBTI stressing tests were performed using an HP 4156 system. DNBTI stressing tests were performed using a Keithley 4200 system. A precision impedance meter, HP4284, was used for C-V measurements. Temperature-regulated hot chucks were controlled at temperatures ranging from 25°C to 125°C.

Split C-V method was employed to determinate the holes mobility. The electric field produced by the gate voltage is express as:

$$E_{eff} = \frac{Q_b + \eta Q_n}{K_s \varepsilon_0} \qquad (2\text{-}1)$$

$$Q_b = \int_{V_{fb}}^{V_g} C_{gb} dV_g' \qquad (2\text{-}2)$$

$$Q_n = \int_{-\infty}^{V_g} C_{gc} dV_g' \qquad (2\text{-}3)$$

where Q_b and Q_n are charge densities in depletion layer and inversion layer, respectively. The parameter η =1/3 for hole mobility. The gate-to-substrate capacitance (C_{gb}) and gate-to-channel capacitance (C_{gc}) were measured using the configurations illustrated in Fig. 2.3.

The existence of a gate leakage current may affect the accurate measurement of drain conductance. To solve this problem, we propose some new approaches as followed. The channel current is simply given by the average of the source and the drain currents. For surface carrier concentration evaluation, we have adopted a simple approach that takes drain voltage effect into account [23].

$$\mu(V_g) = \frac{L}{W} \cdot \frac{I_s(V_g) + I_d(V_g)}{2V_d} \cdot \frac{1}{2q} \cdot \left(\int_{-\infty}^{V_g} C_{gc}(V_g') dV_g' + \int_{-\infty}^{V_g - V_d} C_{gc}(V_g') dV_g' \right) \qquad (2\text{-}4)$$

The fabricated devices were subjected to bias-temperature-stress (BTS) from 25°C to 125°C. During the BTS, a negative gate bias (-3.5 V~ -4.3 V) was applied, while drain/source and substrate were all grounded, as schematically shown in Fig. 2.4.

The interface state density was evaluated using the charge pumping method. In the characterization, square-wave (f = 1MHz) voltage signals were applied to the gate with a constant pulse amplitude of 1.5 V, and a varying base voltage to tune the surface condition from inversion to accumulation. Fig. 2.5 shows the configuration of

measurement setup used in the charge pumping experiment. A MOSFET with a gate area of A_G gives the charge pumping current as:

$$I_{cp} = qA_G fN_{it} \tag{2-5}$$

Interface trap density could be evaluated by using this equation.

Oxide traps cannot respond to the Icp signal at high frequency and are categorized as slow traps. The mean interface trapped charge contributes only by ϕ_B as surface potential is roughly equal to $2\phi_B$. A simple and direct way to deduce oxide trap density (N_{ot}) is to calculate the difference between the measured ΔVth and the term contributed by ΔN_{it} from charge pumping results, using the following formula:

$$\Delta V_{th}(T) = -\frac{q\Delta N_{ot}}{C_{ox}} - \frac{q\Delta \overline{N_{it}^{Don,Acc}}(\psi_s - \phi_B(T))}{C_{ox}} \tag{2-6}$$

Therefore, ΔN_{ot} during stress cab be calculated and easily determined.

Chapter 3

Electrical Characteristics of Locally Strained PMOSFETs with Poly-SiGe gate

3.1 Brief Review of Poly-SiGe Gate Technology

Technical challenges emerge as the critical dimensions of semiconductor devices are scaled down to the deep-submicron regime in a pursuit of higher levels of integration and performance. The dual-gate process has replaced the conventional single-gate process for advanced CMOS fabrication. For dual-gate process, boron penetration through the gate oxide from the p^+-doped gate of PMOSFETs becomes a major concern. In addition, gate-depletion effect due to insufficient dopant activation at the gate/dielectric interface becomes more significant as gate oxide thickness is scaled down, and leads to the degradation of the drive current.

To alleviate the above-mentioned problems, poly-SiGe has been proposed as a promising alternate gate material to replace the conventional poly-Si gate. First, the dopant activation in poly-SiGe is better than in poly-Si for p-type gate material. Besides, the p-type poly-SiGe film has lower resistivity, reduced gate-depletion effect, and suppressed boron penetration, thanks to the higher dopant activation ratio as comparing

to poly-Si film. Mechanism of the improved boron activation is presumably caused by the local strain compensation due to the difference in atomic radii between Si and B atoms [24].

When p^+ poly-Si is substituted by p^+ poly-SiGe as the gate material for the PMOS device, the change in the gate to semiconductor work-function difference, $\Delta\Phi_{ms}$, can be approximately calculated as the difference in the energy bandgaps between the two heavily-doped materials, i.e., $\Delta\Phi_{ms} = E_G^{poly-Si} - E_G^{poly-SiGe}$. This is due to the fact that the position of the conduction band edge of the materials remains essentially unchanged regardless of the Ge incorporation. For high Ge concentration, a significant amount of stress contained in the poly-SiGe grains results in an extra reduction of the gate work-function [19]. In order to retain the threshold voltage at the reference value, one can change $\Delta\Phi_{ms}$ by reducing the channel doping. As a result, hole mobility is enhanced due to reduction of Coulomb scattering centers in the channel region. The drive current is thus increased. The subthreshold swing could also be reduced due to decrease in the depletion layer capacitance, leading to an improved I_{on}/I_{off} ratio. The reduction of the body factor results in weaker threshold voltage dependence on variations of the substrate potential.

The dopant activation temperature could be reduced owing to the lower melting

point of poly-SiGe film, and this is conducive to reducing the process thermal budget. The poly-SiGe alloy films also have good compatibility with standard CMOS processing.

3.2 Brief Review of Strained Si Technology

Rapid growth in the study of implementing strained silicon to the channel has been witnessed in the past several years. Historically, improvements on MOSFET's performance have been attained by shrinking device dimensions. However, the practical benefit of scaling is compromised as physical and economic limits are being approached, and novel solutions are being sought. The 2003 ITRS roadmap started to schedule the mobility enhancement factor by stress controls. Strain improves MOSFET drive current by altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths. Bi-axial and uni-axial strained silicon technologies are promising for enhancement of CMOS performance [25~30]. For the case of a silicon layer under bi-axial tensile strain, it is mainly implemented by the lattice mismatch with an underling relaxed SiGe layer. Note that, to avoid the generation of high amount of dislocations, thickness of the top strained Si layer must be thinner than the critical thickness that depends on the Ge content of the underlying relaxed SiGe

layer. In contrast, uni-axial strain can be engineered by modifying capping layer deposition [9][31], shallow trench isolation [32][33], source/drain material [6], silicidation [34], packing process [35], and so on. Furthermore, the behaviors of carrier mobility under uni-axial strain depend on the strength of the strain and the orientation. Electron and hole mobilities respond to the complex three-dimensional mechanical stress in different, even opposite ways, as shown in Fig. 3.1.

Several different behaviors caused by bi-axial and uni-axial stress were reported, such as the drop of mobility enhancement at high electric field and threshold voltage shift. Bi-axial strain improves electron transport more than hole transport, and vice versa for the perpendicular uni-axial strain. Uni-axial strain can be applied arbitrarily in any direction relative to the carrier transport direction. Enhancements of carrier mobility under bi-axial and uni-axial strain were induced by different factors and mechanisms.

For NMOSFETs, recent reports and theoretical calculations indicate that strained-Si under bi-axial or uni-axial tension should exhibit a higher mobility than bulk Si. The differences in electronic conduction due to bi-axial and uni-axial strain can be explained by examining the splitting of the degeneracy at the conduction band edges. The biaxial tensile strain induces splitting of degeneracy in the triangular potential well of the MOS inversion layer. This splits the six-fold degenerate Si conduction band into a

two-fold ($\Delta 2$) and a four-fold ($\Delta 4$) branches. The energy of sub-band in four-fold valley is lower than that in two-fold valley under uni-axial tensile stress, opposing to what occurs in the case of bi-axial tensile stress. The energy difference (ΔE) between $\Delta 2$ and $\Delta 4$ sub-bands determines the total population of the bands. The enhancement of uni-axial and bi-axial strained-Si caused by the splitting of conduction band can suppress inter-valley phonon scattering [36]. At high electric field, even in bulk Si NMOSFETs, the six-fold degeneracy is broken near the Si/SiO_2 interface by the confinement of carrier at surface (as shown in Fig. 3.2(a)). The two-fold sub-band is also preferentially occupied at high gate bias. Most inversion electrons are expected to reside in two-fold sub-band even for devices fabricated on bulk Si. In contrast, bi-axial tension causes nearly 100% of inversion electrons to occupy the two-fold sub-band at all gate biases. Note that the enhancement of bi-axial tension at high electrical field, albeit not as high as that at low field, is still very significant [37].

To quantify the mobility enhancement of holes, changes in the scattering and effective mass depend on the altered valence band caused by the strain. For both bi-axial tensile and longitudinal uni-axial compressive stresses, the effective mass is nearly constant over the surface energy range of a few kT below the valence band in contrast to un-strained case. The constant effective mass results since strain removes the

degeneracy and reduces the band-to-band coupling. From full-band Monte Carlo simulation [38], uni-axial compressive strained MOSFETs may have lighter in-plane effective mass thus improve hole mobility. For bi-axial tensile stress, the effective mass is heavier than un-strained case. The hole mobility enhancement is only possible through the reduction of inter-valley scattering [39]. This effect becomes significant only when the strain level is high enough (e.g., Ge > 20 %). Reducing the intra-band acoustic scattering by altering the light- and heavy-hole band density-of-states is negligible for uni-axial strain in Si, even at several hundreds of mega-pascal. On the other hand, the energy difference ΔEs (as shown in Fig. 3.2) between light-hole band and heavy-hole band was split by uni-axial stress at gamma-point (k=0) and reduces the optical phonon scattering (as shown in Fig. 3.2(b)). Significant scattering reduction requires ΔEs > 60meV (optical phonon energy in Si) [13].

Hole mobility at high vertical field with uni-axial compressive and biaxial tensile stresses would have different behaviors. Splitting of light- to heavy-hold band caused by uni-axial and biaxial stresses has no significant difference without considering surface quantization confinement. However, the splitting of light- and heavy-hole bands caused by bi-axial tensile stress would be nullified at high electric field due to surface confinement [40]. In contrast, hole mobility enhancement under uni-axial compressive

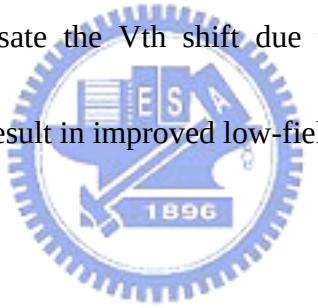
strain is not nullified by surface confinement, which represents a major advantage for MOSFETs operating at high electric fields. The splitting magnitude of the surface confinement depends on the relative magnitude of the stress altered light and heavy hole out-of-plane effective masses. Recent reports [41] showed the interesting result that the out-of-plane effective mass of light hole is heavier than heavy hole for uni-axial stress and causes the light to heavy hole band splitting to increase. On the contrary, for bi-axial stress the previously-reported out-of-plane effective mass of light hole is lighter than heavy hole and causes the band splitting to be reduced. This is why the bi-axial stress degrades hole mobility enhancement at high vertical electric fields (as shown in Fig. 3.2(c)).

The threshold voltage shift caused by bi-axial tensile stress is larger than the case with uni-axial tensile strain has been reported for NMOSFETs [42]. For PMOSFETs, larger shift of light-hole band edge under bi-axial tensile strain leads to larger shift in Vth than the case with uni-axial compressive strain [41].

3.3 Electrical Characteristics of Poly-SiGe Gate Devices

Figure 3.3 shows the cumulative probability distribution of sheet resistance for poly-Si and poly-SiGe (Ge: 20%) gates with nominally identical implant and annealing

conditions. Thickness of the films is around 150nm. As can be seen in the figure, the sheet resistance becomes lower as Ge incorporated, owing to the higher dopant activation [19]. This results in improved output characteristics for the device with poly-SiGe gate, as shown in Fig. 3.4. Figure 3.5 compares the C-V characteristics of the devices. This further confirms the fact that poly-SiGe gate could effectively suppress poly-depletion effect. Fig. 3.6 shows the mobility as a function of effective vertical electric field. PMOSFETs using poly-SiGe as gate material have no significant effect on holes mobility with the nominally identical channel doping profile. However, lowering in channel doping to compensate the Vth shift due to work-function difference in poly-SiGe-gated devices may result in improved low-field mobility.



3.4 Effects of the Strain

The stress from PE-SiN layer was first examined by probing blanket monitor sample deposited on Si wafers. We confirmed that the stress is compressive and increases monotonically with increasing thickness. The stress is around –95 MPa for 100 nm SiN. Figures 3.7(a) and 3.7(b) show the output characteristics of PMOSFETs with the identical geometry at different temperatures. Saturation current increases monotonically with increasing capping layer thickness. Figures 3.8 (a) and (b) illustrate

the Id-Vg characteristics at different temperatures. The transconductance of the devices exhibits similar trends, as shown in Figs. 3.9 (a) and (b). It should be noted that, in Fig. 3.10, there is no significant difference of the capacitance between unstrained and strained channel devices. From these results it is inferred that the holes mobility is improved by SiN capping layer.

Figs. 3.11 (a) and (b) show the percentage increase of the saturation current of the SiN-capping relative to the control devices as a function of channel lengths at 25°C and 125°C, respectively. The enhancement is less pronounced at high temperature owing to the enhanced phone scattering rate. The mobility enhancement is more significant as channel length is scaled down. Subthreshold swing of the devices seems not to be affected by the induced strain, as shown in Figs. 3.12 (a) and (b), even as operated at a raised temperature (125°C).

Figs. 3.13 (a) and (b) show the threshold voltage as a function of channel length. Fig. 3.14 illustrates the changes in threshold voltage for devices with SiN layer capping relative to that of control devices. For long channel devices (e.g., L > 2 μm), a nearly constant shift is observed in Fig. 3.14. This phenomenon could be explained by the reduction in the interface trap density extracted from charge pumping measurements, as shown in Fig. 3.15. Since the he precursors for SiN deposition are SiH_4 and NH_3, a large

amount of hydrogen species can be introduced during processing and passivate the interface states. As also can be seen in the figure, the amount of change in threshold voltage increases with decreasing channel length, especially as channel length is scaled below 1 μm. Such phenomenon is presumably caused by the splitting of valence band edges by the compressive strain that increases with decreasing channel length.

Chapter 4

Effects of SiN Capping on NBTI of PMOSFETs

4.1 Static and Dynamic NBTI

4.1.1 Brief Review of NBTI Mechanisms

For the aggressive scaling of CMOS technologies, an ultra thin gate oxide is essential to achieve high drive current under lower power operation. The integrity and reliability of such a thin gate oxide are therefore crucial for ULSI manufacturing. Recently, negative-bias-temperature instability (NBTI) has been identified as one of the major reliability concerns for deep sub-micron PMOSFETs [45]. It was observed that a large number of interface states and positive fixed charges were generated during negative-bias-temperature stressing (NBTS), resulting in a negative shift in threshold voltage showing a power-law dependence on stress time:

$$\Delta V_{th} = At^{b} \qquad (4\text{-}1)$$

This phenomenon becomes more significant as gate oxide is scaled down, and may even become the limiting factor for deep sub-micron p-channel devices. The shift in threshold voltage and degradation in transconductance have been suggested to be due to the interfacial electrochemical reactions related to the holes from the channel inversion

layer. The exponential value of the power law equation is around 0.25, which could be explained by the diffusion-controlled electrochemical reactions. Based on the $t^{0.25}$-like time evolution, a generalized reaction-diffusion model for interfacial charge formation based on the trivalent silicon and its hydrogen compounds was proposed [46].

In the Svensson model [47], an interface trap is a trivalent silicon atom with an unsaturated valence electron (dangling bond) at the Si-SiO_2 interface. It is denoted by $Si \equiv Si\bullet$ and acts as an active interface trap. A post-metal-anneal in a forming gas (typically 10% H_2 in N_2 ambient) is widely used to passivate the interface dangling bonds, and introduces a lot of hydrogen-terminated trivalent Si bonds which are electrically inactive at the actual interface. If the terminated hydrogen is released from the $Si \equiv Si - H$ bond by some dissociation mechanism, the remaining interface trivalent silicon (dangling bond) is restored as an active interface trap. Various mechanisms have been proposed for the dissociation process.

High electric fields can dissociate the silicon-hydrogen bond, according to the model [48]

$$Si_3 \equiv SiH \rightarrow Si_3 \equiv Si\bullet + H^0, \qquad (4\text{-}2)$$

where H^0 is a neutral interstitial hydrogen atom or atomic hydrogen. Recent first-principle calculations show that the positively charged hydrogen or proton H^+ is the

only stable charge state of hydrogen at the interface, and that H^+ reacts directly with the SiH to form an interface trap, according to the reaction [47]:

$$Si_3 \equiv SiH + H^+ \rightarrow Si_3 \equiv Si\bullet + H_2 . \qquad (4\text{-}3)$$

The SiH is polarized in this model such that the mobile positive H^+ migrates towards the negatively charged dipole region in the SiH molecule. The H^+ atom then reacts with the H^- to form H_2, leaving behind a positively charges Si dangling bond.

A different model considers the interaction of SiH with "hot holes" or holes near or at the Si/SiO_2 interface [46]. Dissociation involving holes is given by

$$Si_3 \equiv SiH + h^+ \rightarrow Si_3 \equiv Si\bullet + H^+ . \qquad (4\text{-}4)$$

Fig. 4.1 is a schematic view of reaction-diffusion model for N_{it} generation.

The fixed charge (Q_f) also contributes to threshold voltage shift near the SiO_2/Si interface. Q_f is a by-product of trivalent Si defect in the oxide, generated with the reaction

$$O_3 \equiv SiH + h^+ \rightarrow O_3 \equiv Si^+ + H^0 \qquad (4\text{-}5)$$

As discussed in Ref. 46, the interface trap density (N_{it}) and fixed oxide charge density (N_f) are shown to increase as:

$$\Delta N_{it} = C E_{ox}^{1.5} t^{0.25} \exp(-E_a / kT) / T_{ox} ; \qquad (4\text{-}6)$$

$$\Delta N_f = C' E_{ox}^{1.5} t^{0.14} \exp(-E_a' / kT) , \qquad (4\text{-}7)$$

here C and C' are appropriate constant values, E_{ox} is electric field in the oxide, T_{ox} is oxide thickness and aging time t. Ogawa et al. [46] found that the generation of fixed oxide charges is independent of oxide thickness, but is inversely proportional to oxide thickness for interface trap generation. This suggests that NBTI is worse for thinner oxide, but this phenomenon is not always observed and highly dependent on the process conditions.

The stable interface traps are only formed if by-product species, X, diffuses away from the interface into the oxide bulk.

$$X_{interface} \xrightarrow{diffusion} X_{bulk} \qquad (4\text{-}8)$$

while "X" could be H-related species.

As proved by Jeppson and Svensson [49], the observed $t^{0.25}$ behavior of the interface trap generation suggests the generation process is diffusion controlled. N_{it} buildup equals the total number of released H species. Hole-assisted reaction breaks interfacial SiH bonds, resulting in Nit generation:

$$\Delta N_{it} = S_N (D_X t)^n , \qquad (4\text{-}9)$$

where D_x is the diffusion coefficient of X in the oxide, time exponent n depends on the type of H species trapped and released in the oxide bulk [50].

The model that has often been invoked to explain the $t^{0.25}$ dependence of the trap

generation rates is only partially correct [46]. In fact, there may exist six regimes of the reaction-diffusion model for Nit generation [51] as shown in Fig. 4.2. During the early stress stage, the generation of interface states and hydrogen species is limited by the dissociation rate (regime1, $N_{it} \sim t^{1}$). Then, the process enters the quasi-equilibrium regime (regime2, $N_{it} \sim t^{0}$) immediately. After some stress time, the transport of hydrogen species limits the dissociation process (regime3, $N_{it} \sim t^{0.25}$). However, the reaction-controlled regime could directly merge into the diffusion-controlled regime. The rate of ΔN_{it} changes after H diffusion front reaches the SiO_2/poly interface. Either H absorption into poly ensures faster H removal and higher rate of ΔN_{it} (regime4) or H reflection from poly would result in ΔN_{it} saturation (regime5). Finally, ΔN_{it} should eventually saturate when all SiH bonds are broken (regime6).

4.1.2 Dynamic NBTI

The conventional NBTI based on static experimental data. During normal operations of digital circuits, the applied bias to the gate of PMOSFETs in a CMOS inverter is switched between “high” and “low” voltages. During “low” phase of PMOSFETs applied bias, the “electric passivation” effect may effectively reduce the interface traps generated during the “high” phase. The dynamic NBTI (DNBTI) effect greatly prolongs the lifetime of PMOSFETs operating in a digital circuit, while the

conventional static NBTI measurement underestimates the PMOSFET lifetime. Furthermore, the DNBTI effect is dependent on temperature and gate oxide thickness [52]. A physical model is proposed for DNBTI that involves the interaction between hydrogen and silicon dangling bonds [53]. According to this reaction-diffusion theory, the ΔVth is attributed to the creation of interface traps as a consequence of dissociation of Si-H bonds, and subsequent diffusion of the released hydrogen species towards the gate electrode. In the recovery process, released hydrogen re-passivates Si dangling bonds [53]. The ΔVth recovery progresses in accordance with the power law dependency as follows:

$$\Delta V_{th} = A - B \cdot t^{n}, \qquad (4\text{-}10)$$

where B/A ratio indicates the ratio of a recovery reaction coefficient to ΔVth just after NBT stress. This finding has significant impact on the determination of maximum operation voltage as well as lifetime for future scaling of CMOS devices. Therefore, it is critically important to investigate NBTI under such dynamic stress conditions.

4.2 Experimental Results and Discussion

4.2.1 Static NBTI Characterization

Figure 4.3 shows the results of NBTI stress performed at 25°C with gate overdrive bias of –3.9 V ($V_{GO} = V_G - V_{th}$). As can be seen in Fig. 4.3(a), larger change in threshold voltage shift, ΔV_{th}, is observed in the device with SiN capping layer. The shift curves show a fractional power-law dependence on time, and the exponential values with SiN-capping sample are larger than the control sample. According to the classical reaction-diffusion model, such dependence implies that NBTI is controlled by the diffusion. From Fig. 4.3(b), the maximum value of transconductance, Gm_{max}, degrades gravely in the device with SiN layer. The increase of interface trap density, ΔN_{it}, for devices with SiN capping layer are larger than that of control case, as shown in Fig. 4.3(c). The exponential value of ΔN_{it} in power-law relationship is higher for devices with SiN capping. Similar phenomenon is also observed for the generation of oxide trapped charges, ΔN_{ot}, as shown in Fig. 4.3(d).

The above results clearly indicate that the use of PECVD SiN capping may result in degraded NBTI. Two plausible origins are postulated to explain the worsen NBTI: (1) Higher density of Si-H bonds at the oxide/Si interface, since the SiN layer contains a

large amount of hydrogen species because of the use of SiH_4 and NH_3 precursor gases; (2) Higher strain energy stored in the channel. The energy may help trigger the electrochemical reactions at the interface. This is evidenced by the higher exponent value of the power-time dependence for devices with SiN capping.

Figure 4.4 shows the results after NBTI stress at 125°C. The trends are similar to those occurring at 25°C. The devices with SiN-capping have aggravated NBTI issue. It should be noted that in Fig. 4.4(a), Fig. 4.4(c) and Fig. 4.4(d), nearly saturation in ΔV_{th}, ΔN_{it} and ΔN_{ot} are observed for the device with SiN capping when the stress time is longer than 1000 sec. The NBTI is related to the amount of hydrogen species bonded at the oxide/Si interface, and ΔN_{it} should eventually saturate when nearly all Si-H bonds are broken. The disparity between the two splits is postulated to be caused by the local strain induced in the SiN capping split. The existence of strain weakens the bond strength of hydrogen species that in turn accelerates the bond-breaking process. Such phenomenon is not observed in the control devices due to the lack of high strain in the channel.

Figures 4.5 ~ 4.7 show ΔV_{th} and ΔN_{it} characteristics as a function of time under different V_{GO} at 25°C for the three splits of samples. ΔV_{th} and ΔN_{it} for all cases increase with increasing stress voltage. The exponential value of ΔV_{th} and ΔN_{it} in

power-law relationship are similar under different stress conditions in each split. Because of $\Delta N_{it} \propto E_{ox}^{1.5}$, higher V_{GO} can induce larger amount of N_{it} and degradation. Figures 4.8 ~ 4.10 illustrate ΔV_{th} and ΔN_{it} evolution under different V_{GO} aging at 125°C for the three splits of samples. The trend for ΔV_{th} at 125°C is similar to the results at 25°C. However, the exponential value of ΔN_{it} in power-law relationship decreases with increasing stress bias for the devices with SiN capping. It can be concluded that larger amounts of SiH bonds are broken by higher stress bias during early stress aging. Figures 4.11 and 4.12 illustrate the temperature dependence (Arrehenius plots) of ΔV_{th}, ΔN_{it} and ΔN_{ot} under 1000 sec stressing. The slope (activation energy) is larger for the devices with SiN capping.

4.2.2 DNBTI and AC stress

To simulate the switching operation of the device in the CMOS circuits, the gate voltage during NBTI stress is switched between negative and positive bias for all splits as shown in Figures 4.13 ~ 4.15. The condition during stress periods was for 125°C, V_{GO} = –4 V, while that for passivation periods V_G was set at several biases. Other terminals were grounded during the measurement. As can be seen in Figs. 4.13(a), 4.14(a) and 4.15(a), the ΔV_{th}, reductions of V_G = +1 V during passivation are more significant than V_G = 0 V. We found that the degradation in the stress periods worsens

when higher strain is contained in the channel. The trends in interface trap density shift are similar among the three splits, as shown in Fig. 4.13(b), Fig. 4.14(b) and Fig. 4.15(b), which have weaker dependence on the recover voltage. Because ΔN_{it} is proportionate to ΔV_{th} even at different positive biases during DNBT stressing, as shown in Fig. 4.16(a), Fig. 4.17(a) and Fig. 4.18(a), it can be concluded that ΔV_{th} is directly affected by ΔN_{it} during entire dynamic stress period. However, it should be noted that in Fig. 4.16(b), Fig. 4.17(b) and Fig. 4.18(b), the decreases in ΔV_{th} do not follow the consistent decrease in ΔS, especially for the case with passivation bias V_G = +1 V. It may be due to the electron trapping related to the positive hydrogen charges in the gate dielectric according to reactions (4-8). The B/A ratio of DNBTI is shown in Table. 4.1. The recovery reaction coefficients are similar between strained and unstrained cases.

Furthermore, the frequency dependences of NBT degradation were measured and shown in Figs. 4.19 to 4.21 with 50% duty cycle. ΔV_{th} and ΔN_{it} are plotted as a function of frequency, as shown in Fig.4.17. Both ΔV_{th} and ΔN_{it} are strongly dependent on frequency for devices with SiN capping layer. The results indicate that the stress under higher AC frequency shows less ΔV_{th} and ΔN_{it} degradation. It is due to the shortened stress time with increased frequency. It results in parts of broken SiH bonds

being recovered before entering the next stress state. Interface trap generation would be contained by increase AC stress frequency and ΔV_{th} is suppressed indirectly. Reduction in NBT degradation for strained-channel devices under AC stress is more significant than the control case, mainly because the amount of broken SiH bonds with SiN capping layer is larger than the control sample.

Chapter 5
Conclusions

5.1 Conclusions

Using poly-SiGe as gate material to fabricate PMOSFETs has numerous advantages, including reduced gate depletion effect and improved gate sheet resistance. Compressive PECVD SiN layer could significantly enhance the drive current of PMOS devices at either room or raised operating temperatures (125 °C) due to increase of hole mobility, as shown in our experiment. The degrees of mobility enhancement are enlarged as devices geometry is scaled down. Despite this merit, our results also indicate that the SiN capping may aggravate the NBTI characteristics. A high amount of hydrogen species contained in the PE-SiN layer as well as the strain energy stored in the channel may be the culprits for the worsened reliability. The interface trap density change and threshold voltage shift recover significantly during passivation periods. We've also observed that the strained channel device is influenced strongly by AC stress frequency.

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	Control sample	SiN 100nm sample	SiN 300nm sample
Passivation Layer (Capping Layer)	TEOS 300nm	SiN 100nm + TEOS 300nm	SiN 300nm + TEOS 300nm

Table 2.1 Split table of capping layer structure and thickness

	Passivation Voltage	B/A
Control	0V	0.29
	+1V	0.32
SiN 100nm	0V	0.27
	+1V	0.29
SiN 300nm	0V	0.29
	+1V	0.33

Table 4.1 B/A ratio of devices with different capping layers, at different passivation voltages during DNBTI stress

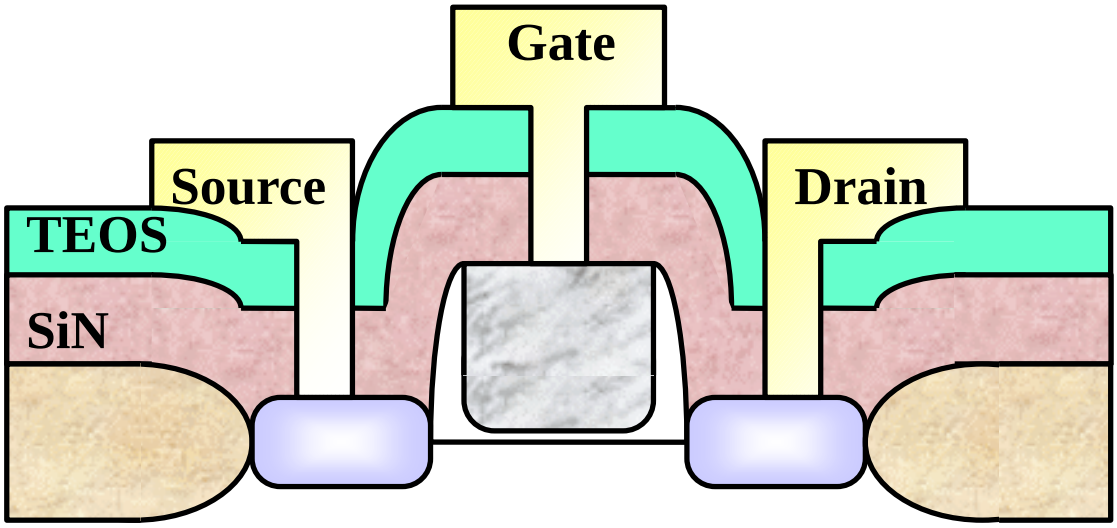


Fig. 2.1 Schematic cross section of the local strained channel PMOSFET

Fig. 2.2 TEM micrographs of device with channel length 0.55 μm

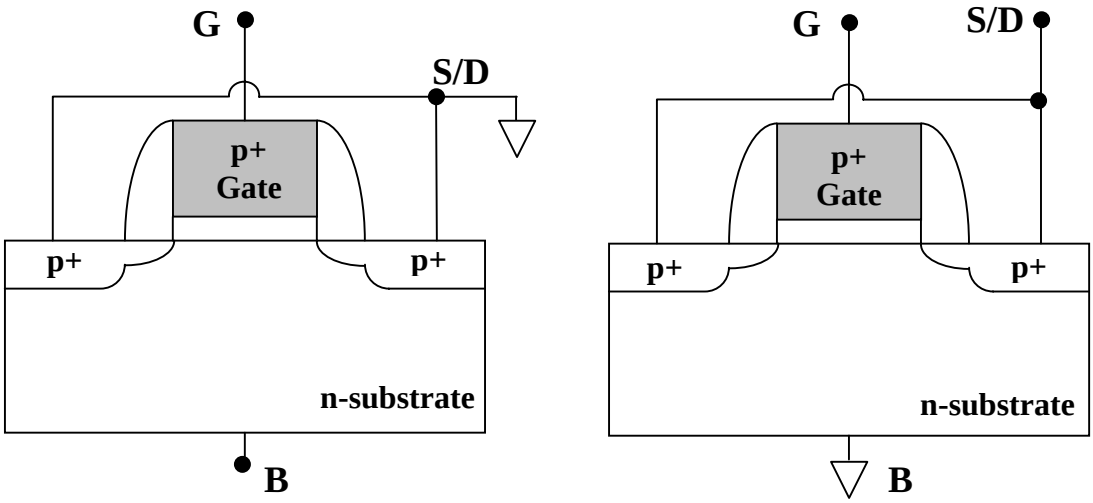


Fig. 2.3 Configuration for (a) gate-to-substrate, (b) gate-to-channel capacitance measurements

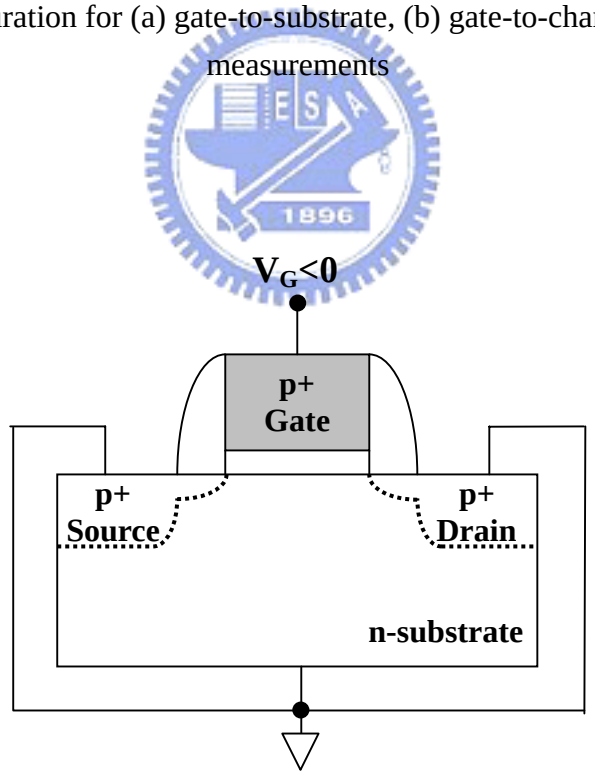


Fig. 2.4 Bias configuration of NBTI stressing

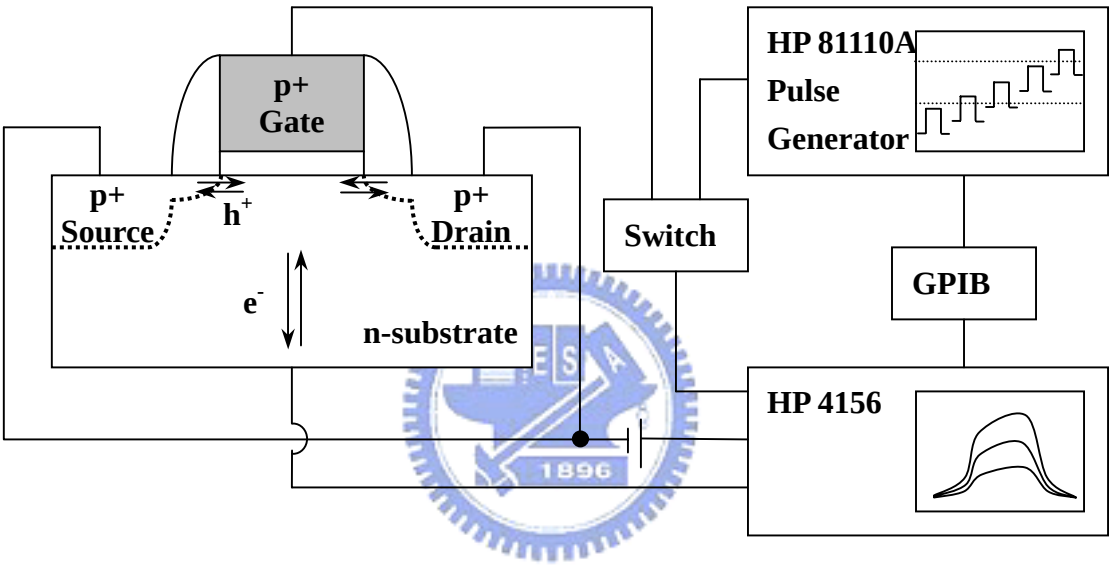
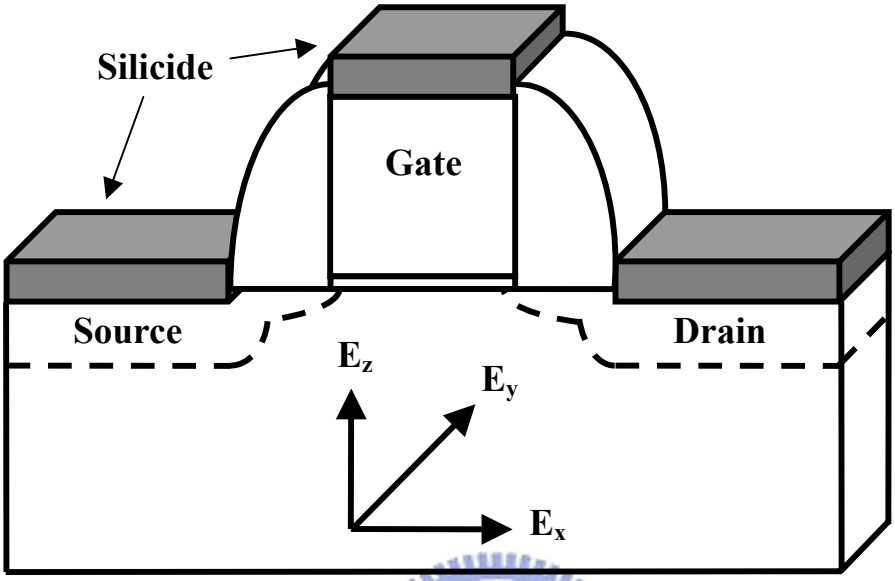


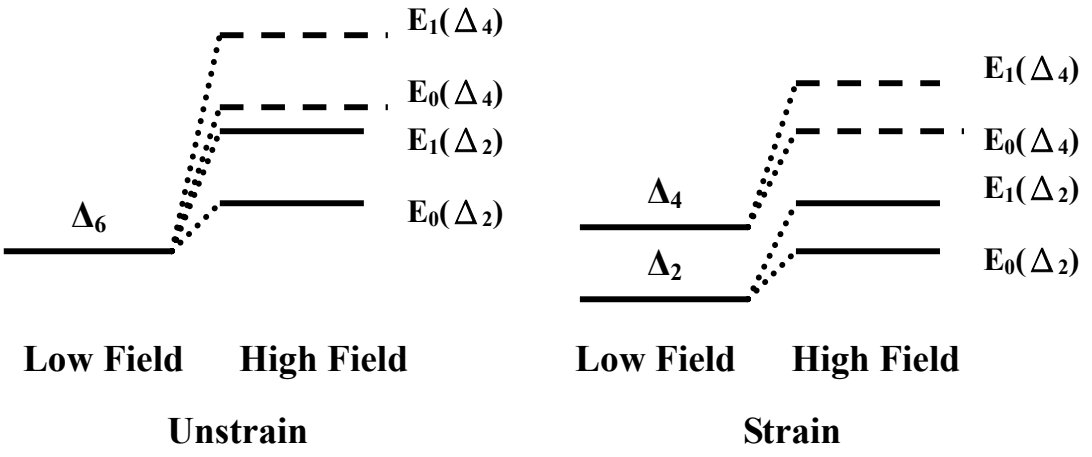
Fig. 2.5 Measurement setup in our charge pumping experiment



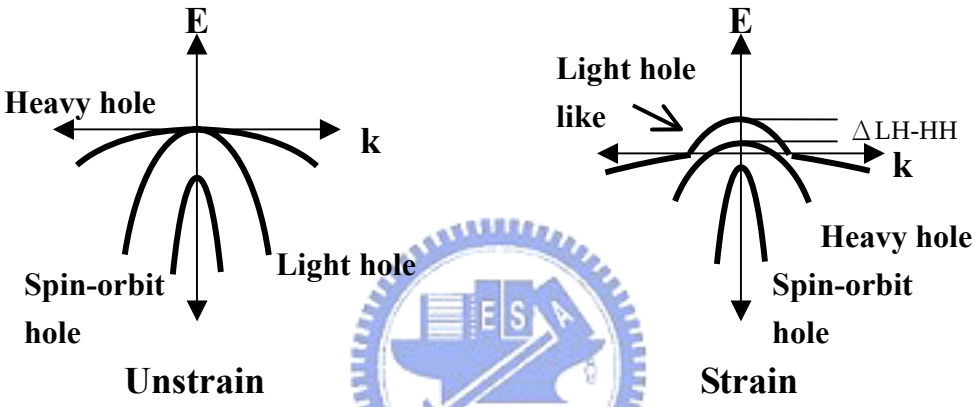
Direction of Strain Change*	CMOS Performance Impact	
	NMOS	PMOS
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

* Strain change = Increased tensile or decreased compressive strain

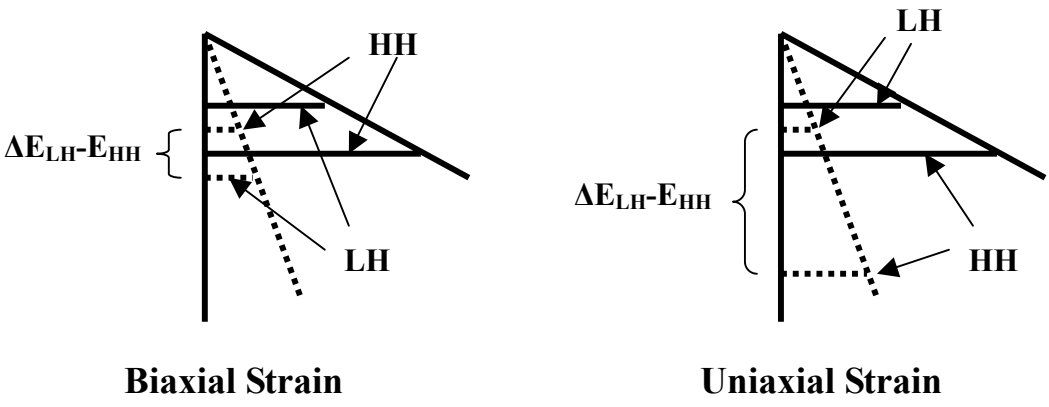
Fig. 3.1 Schematic illustration for 3D process-induced strain components [43].



(a)



(b)



(c)

Fig. 3.2 (a) Splitting of 6-fold degenerate conduction band in unstrained and biaxial tensile strained Si inversion layers [44]. (b) Schematic diagram of the valence bands in unstrained and strained Si layers [40]. (c) Splitting of light hole band and heavy hole band with biaxial and uniaxial strains in low electric field (solid line) and high electric field (dash line) [41].

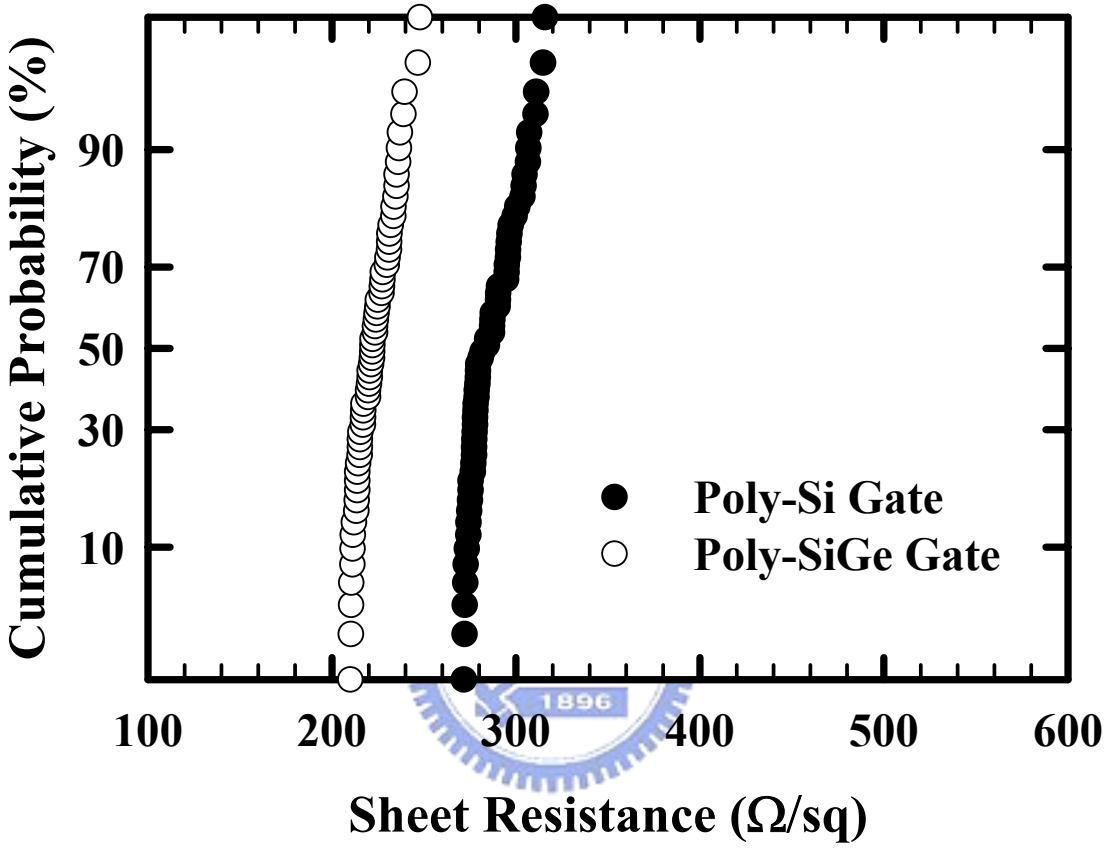


Fig. 3.3 Cumulative probability distribution of sheet resistance of poly-Si and poly-SiGe films. Both with thickness of 150nm, implanted with B implant (dose 3e15cm^{-2}, 8KeV) and anneal at 900°C 30sec.

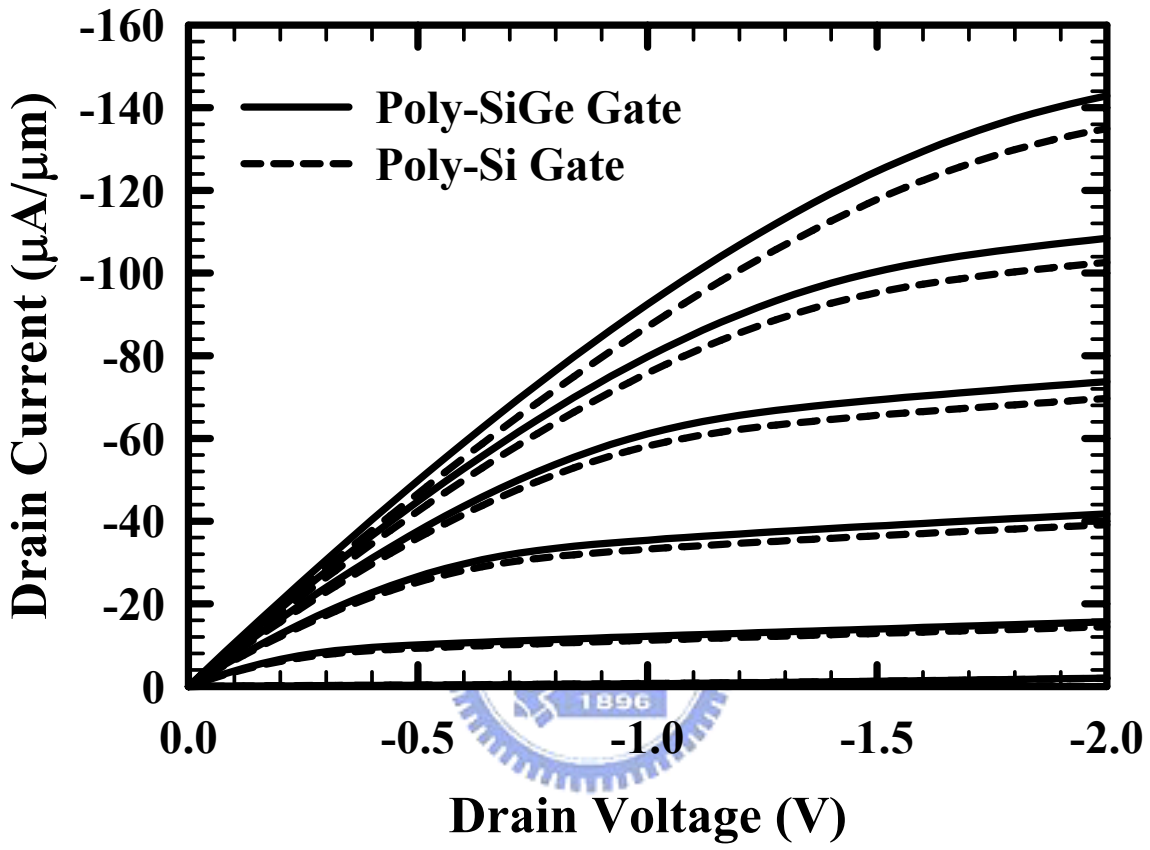


Fig. 3.4 Output characteristics of devices with poly-Si and poly-SiGe gates at 25°C and $V_G - V_{th}$= 0 ~ -2 V, step= -0.4 V, W/L= 10μm/1μm.

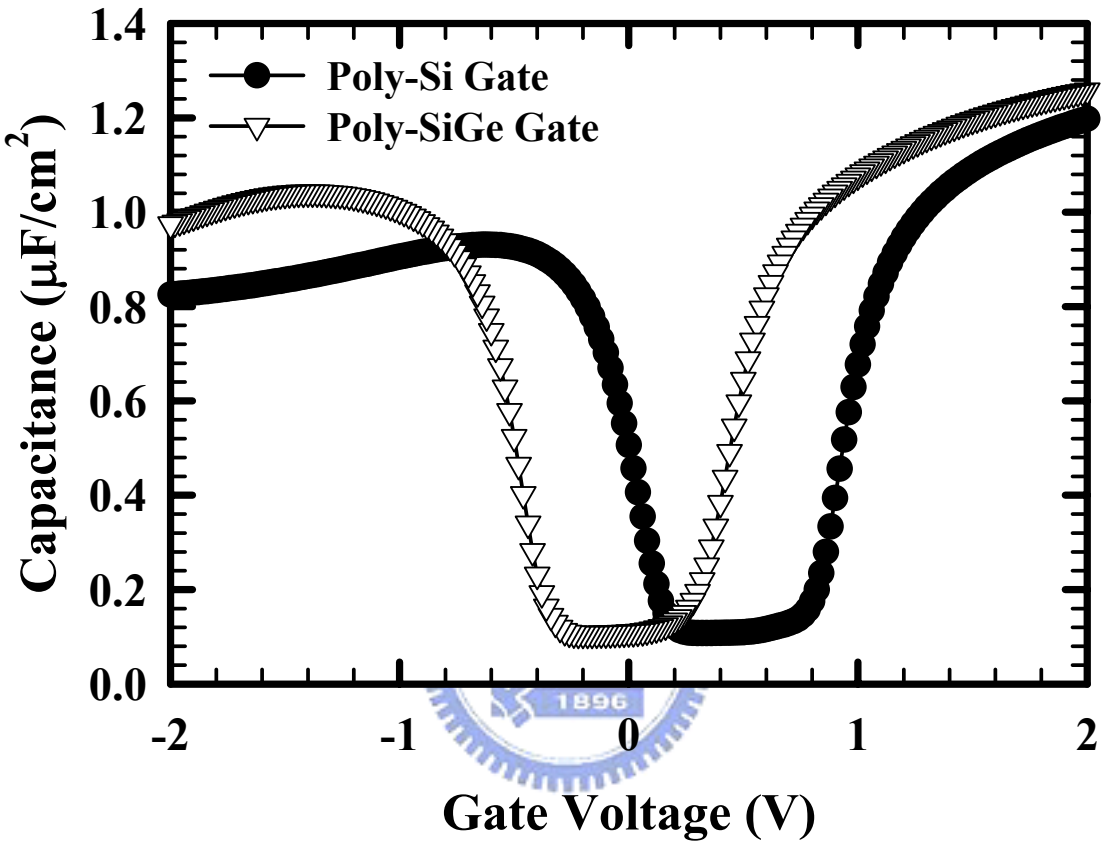


Fig. 3.5 Capacitance of devices with poly-Si and poly-SiGe gates. (W/L= 50μm/50μm)

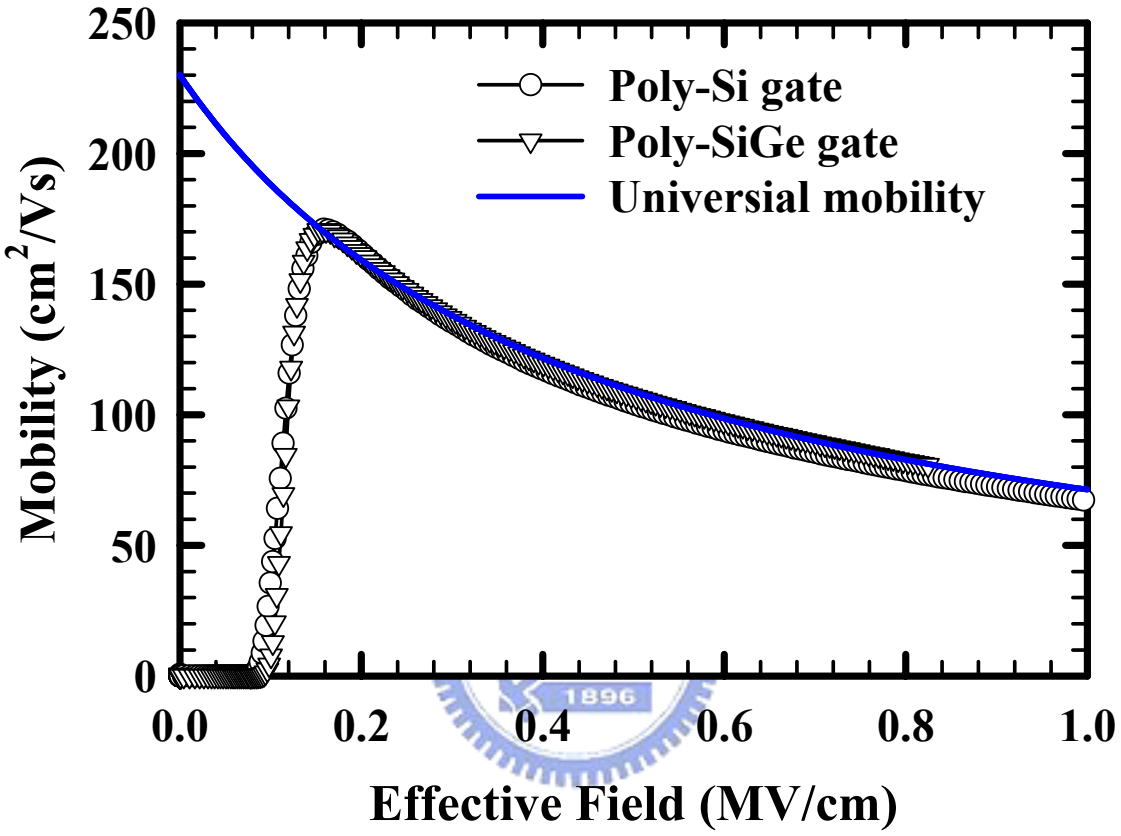
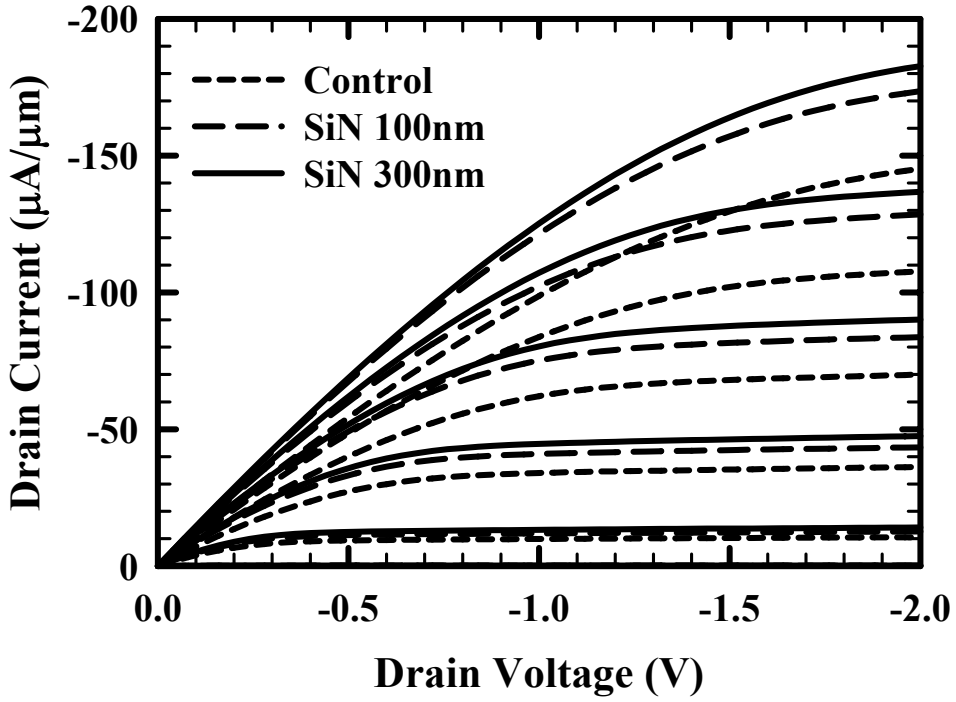
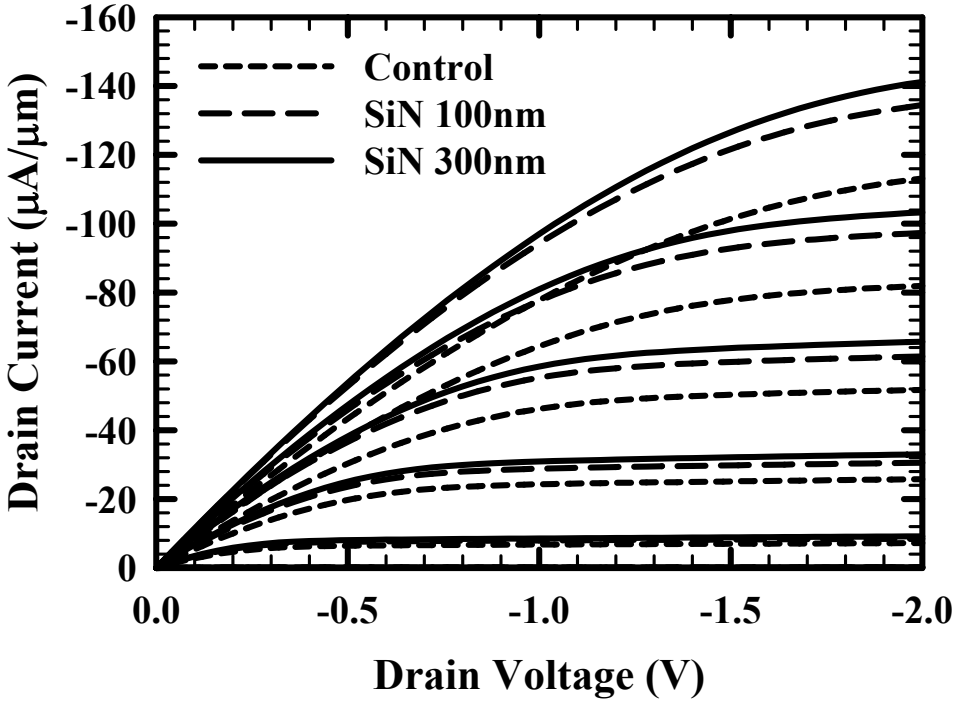


Fig. 3.6 Comparison of hole mobility among different gate materials measured by split-CV method.

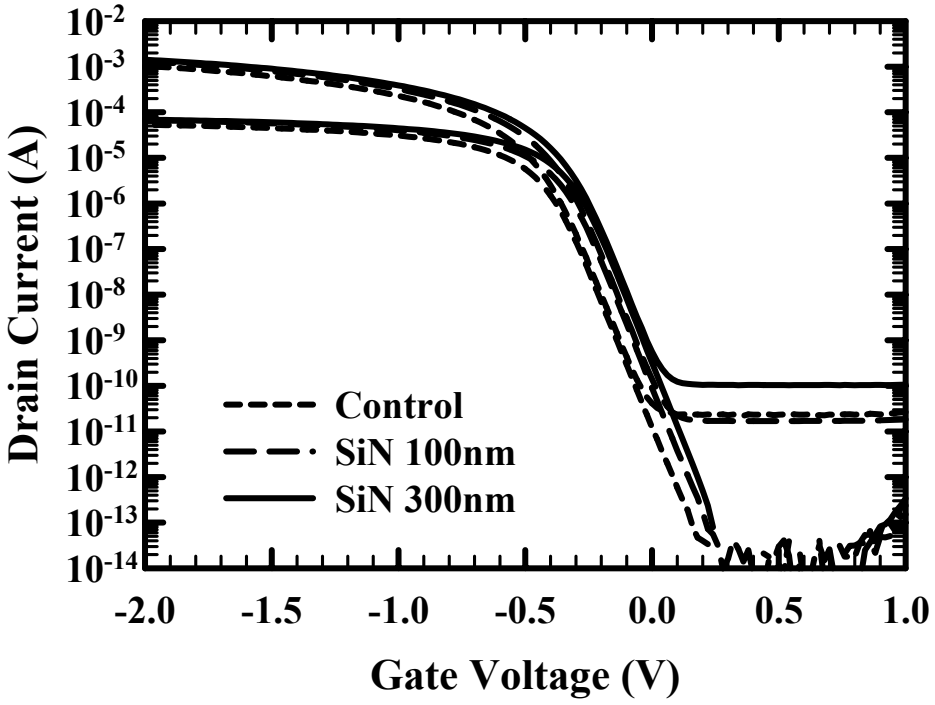


(a)

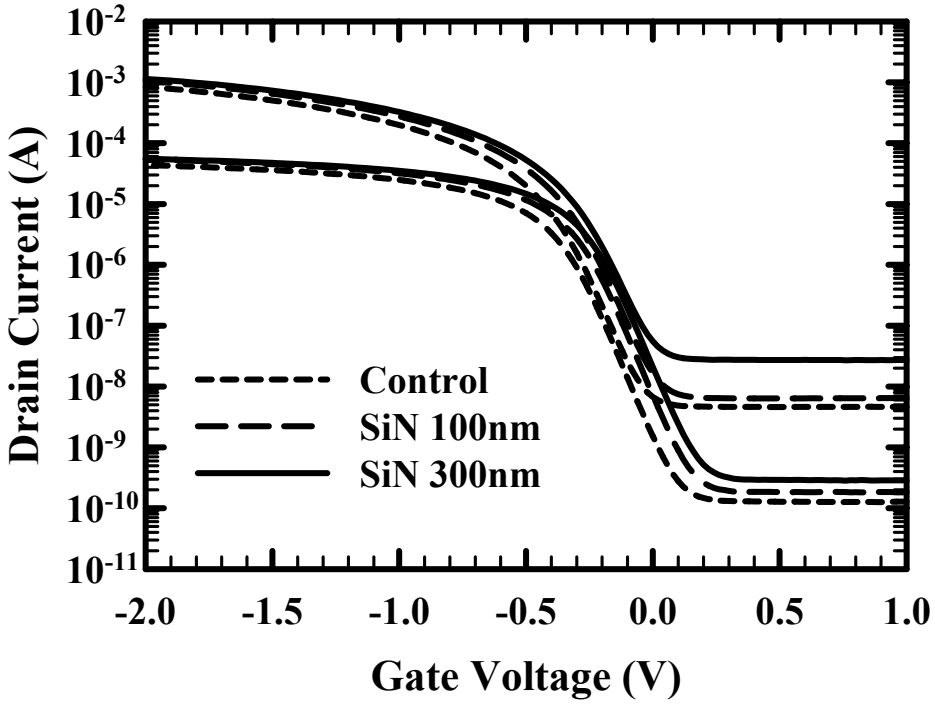


(b)

Fig. 3.7 Output characteristics of different capping layers at (a) 25°C (b) 125°C and V_G-V_{th}= 0 ~ -2 V, step= -0.4 V, W/L=10 μm/0.55μm.

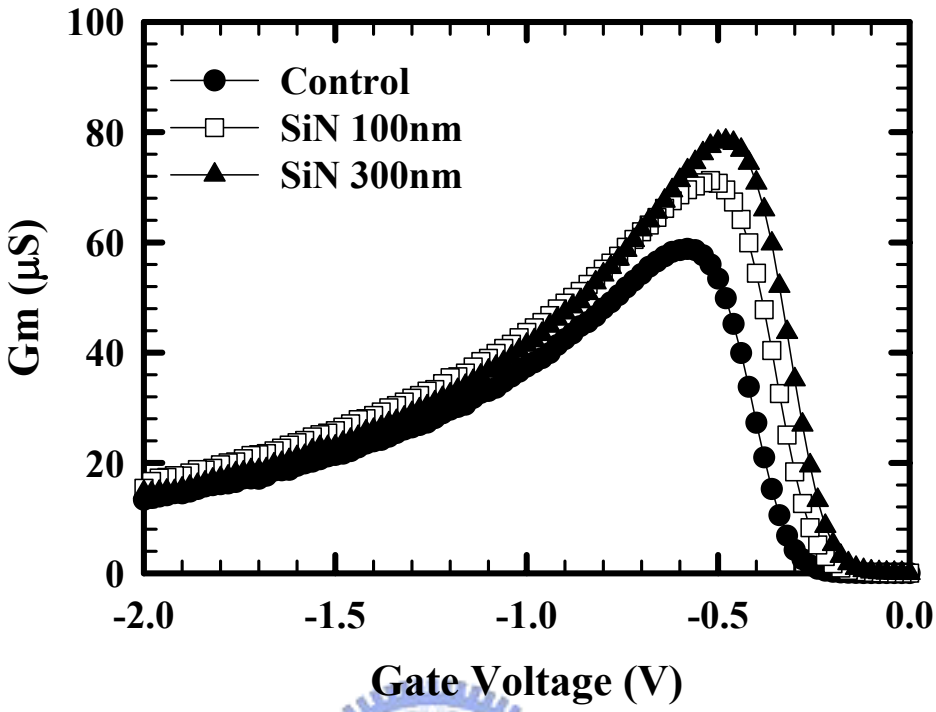


(a)

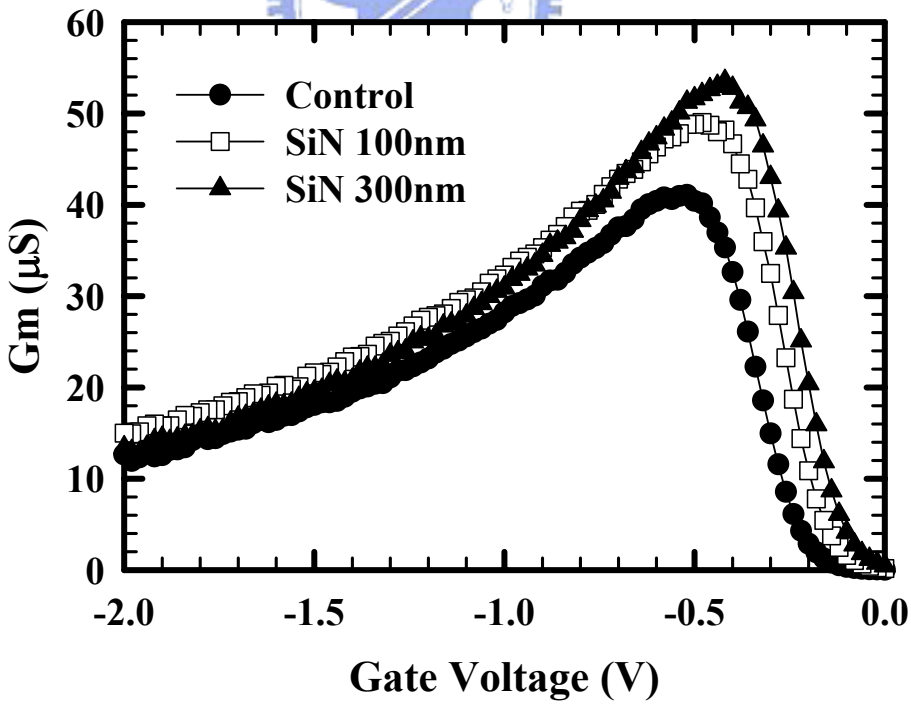


(b)

Fig. 3.8 Subthreshold characteristics of devices with different capping layers at (a)25°C (b)125°C and V_D= -0.05 V, -2 V, W/L= 10μm/0.55μm.



(a)



(b)

Fig. 3.9 Transconductance for devices with different capping layers at (a)25°C (b)125°C and V_D= -0.05 V, W/L= 10μm/0.55μm.

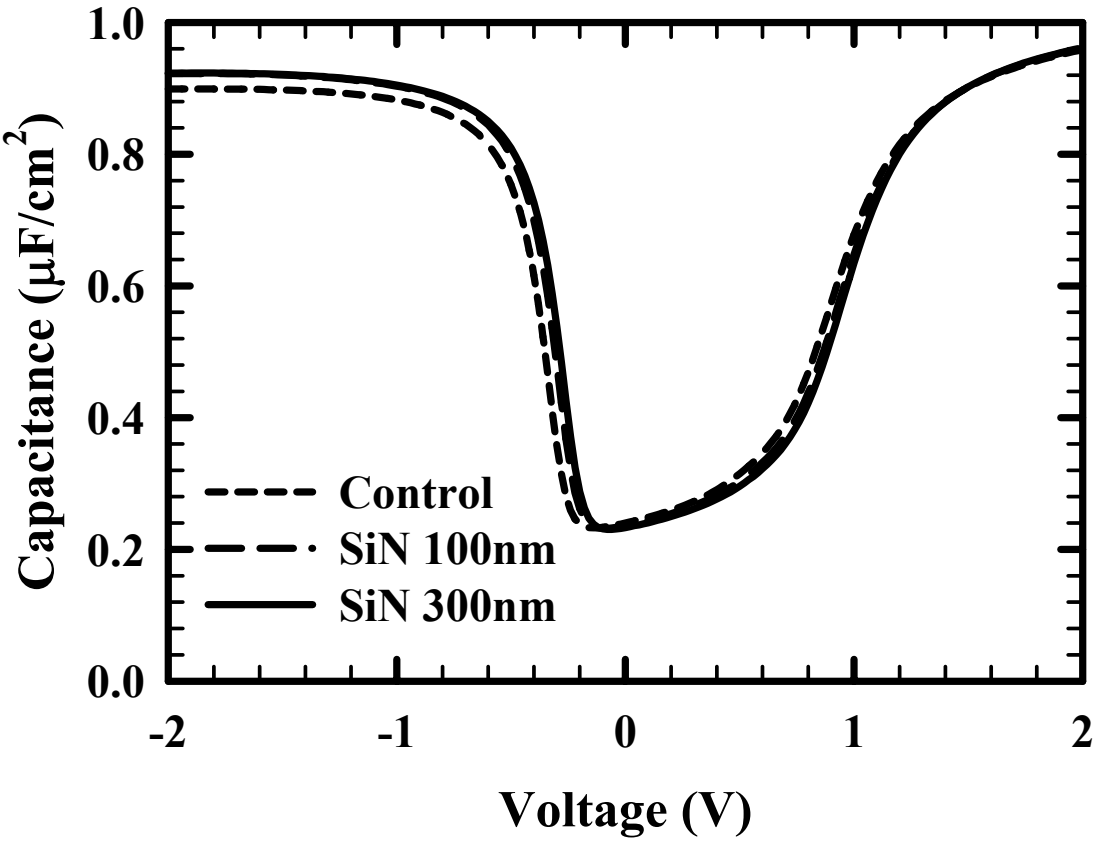
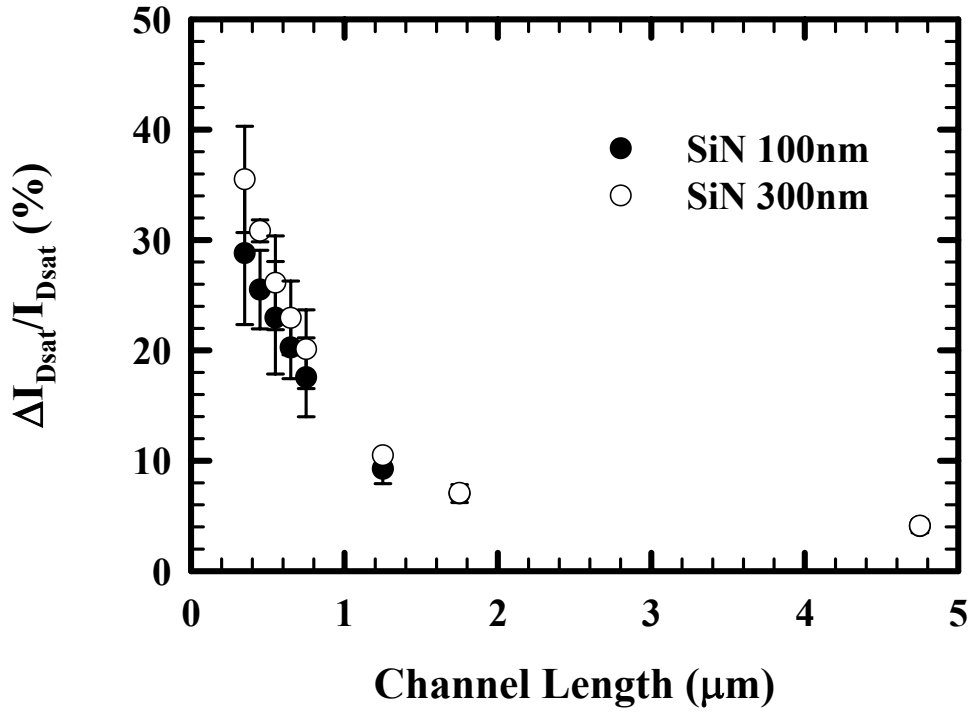
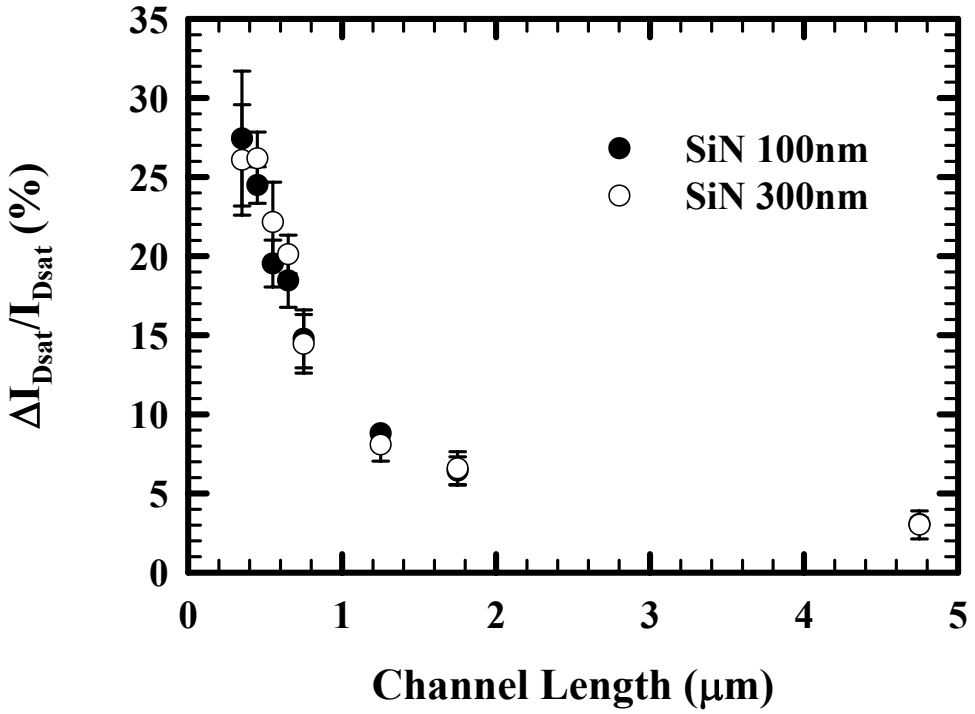


Fig. 3.10 Measured CV profile for devices with different capping layers at 25°C, W/L= 50μm/50μm.

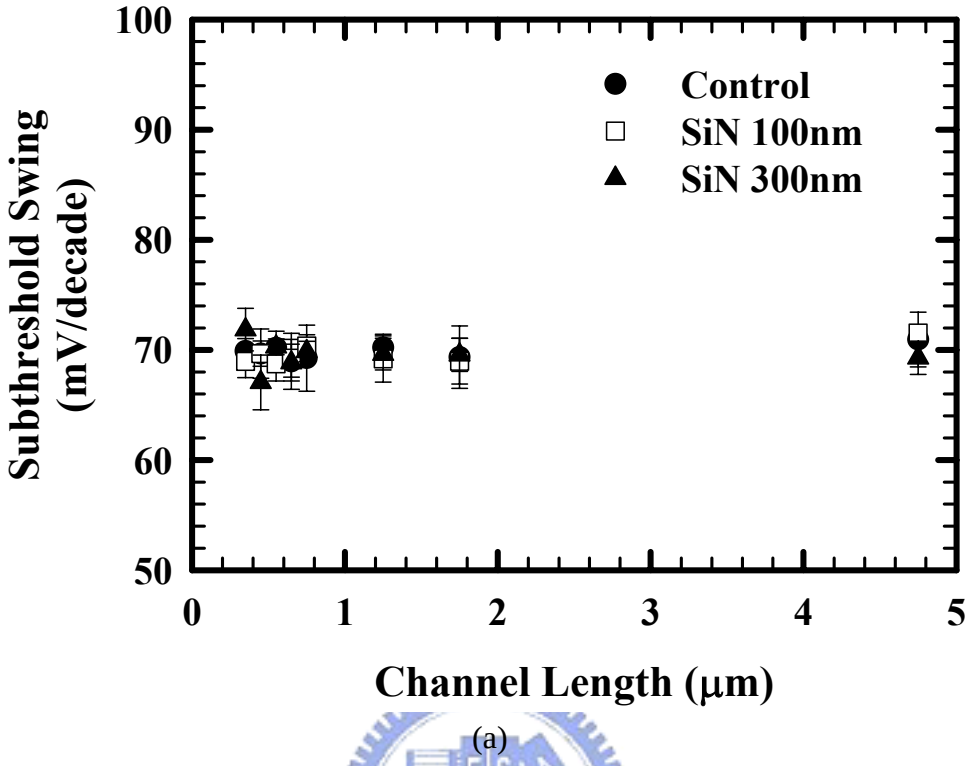


(a)

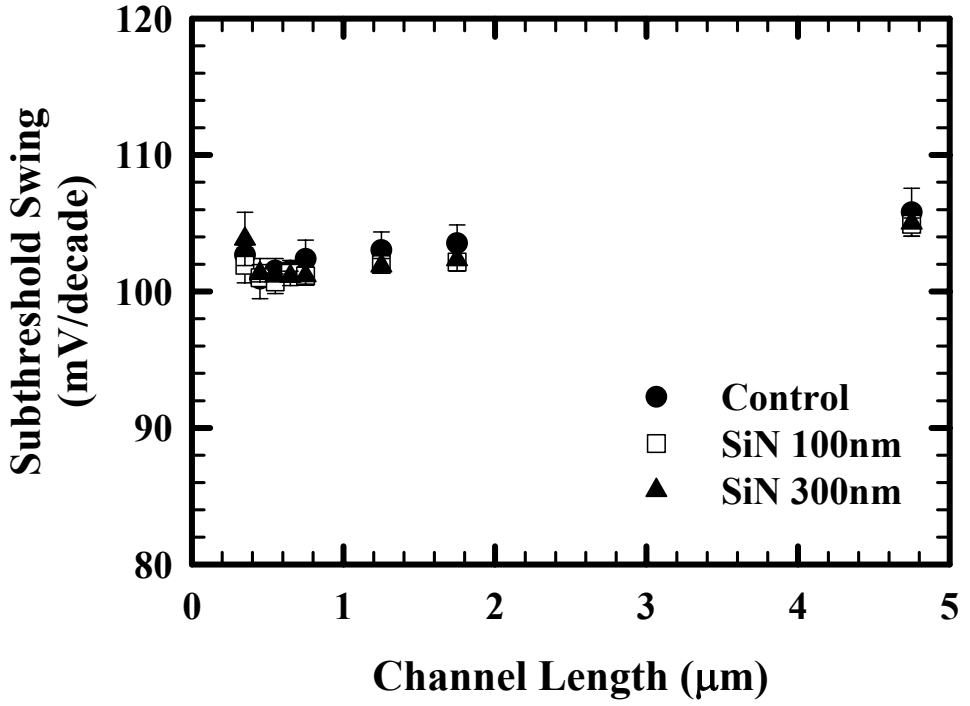


(b)

Fig. 3.11 Saturation current (V_D= -2V, V_G -V_{th}= -2V) enhancement of different SiN thickness as a function of channel length at (a) 25°C (b) 125°C

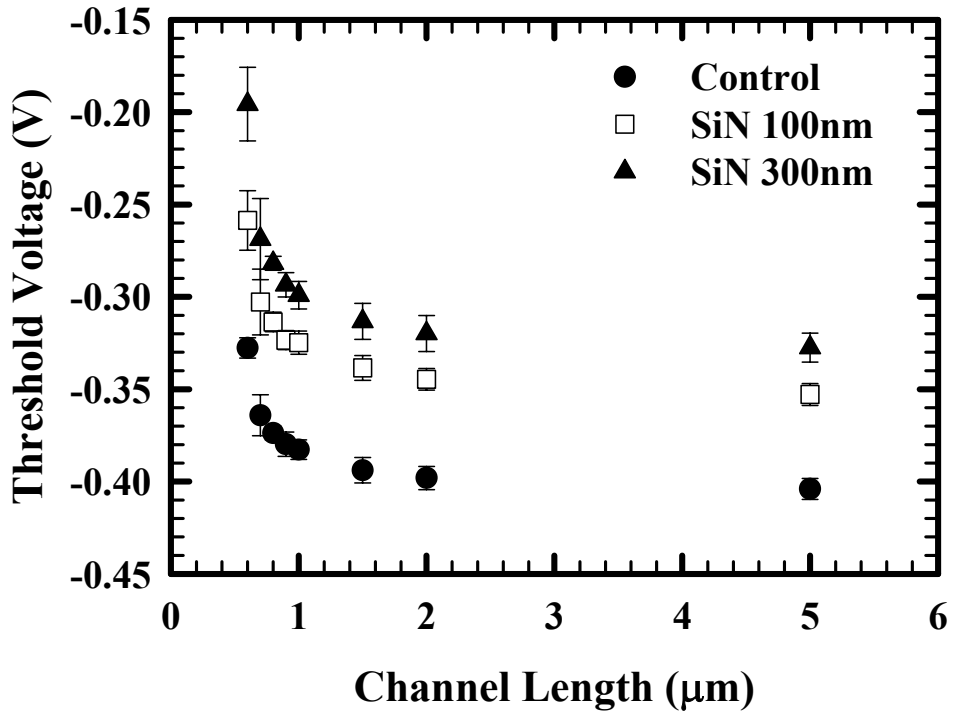


(a)

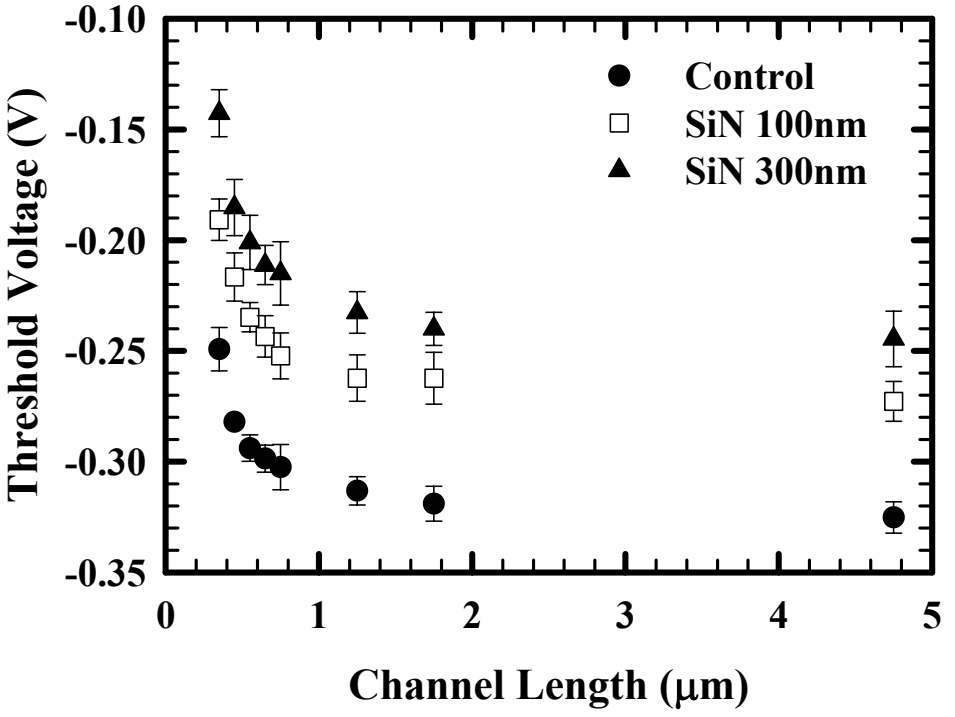


(b)

Fig. 3.12 Subthreshold swing of devices with different capping layers as a function of channel length at (a) 25°C, and (b) 125°C.



(a)



(b)

Fig. 3.13 Threshold voltage of devices with different capping layers as a function of channel length at (a) 25°C, and (b) 125°C.

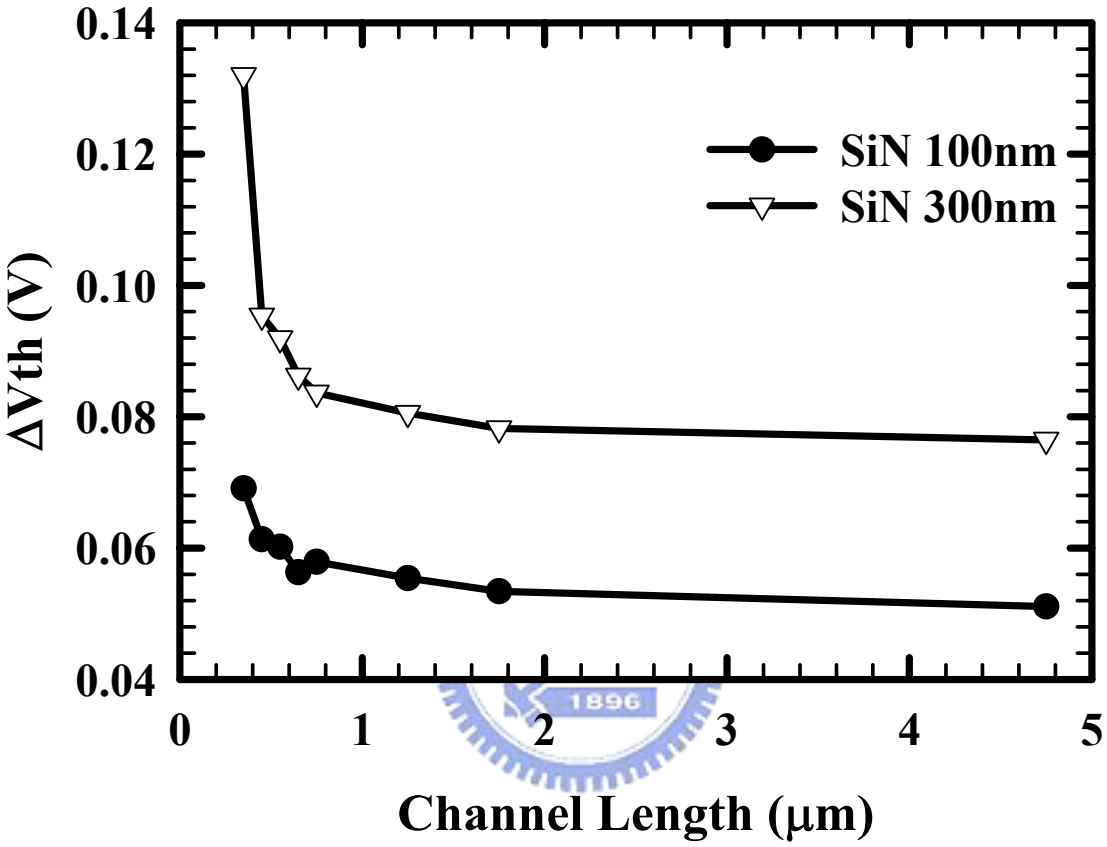


Fig. 3.14 Changes of threshold voltage for devices with different capping layers as a function of channel length at 25°C.

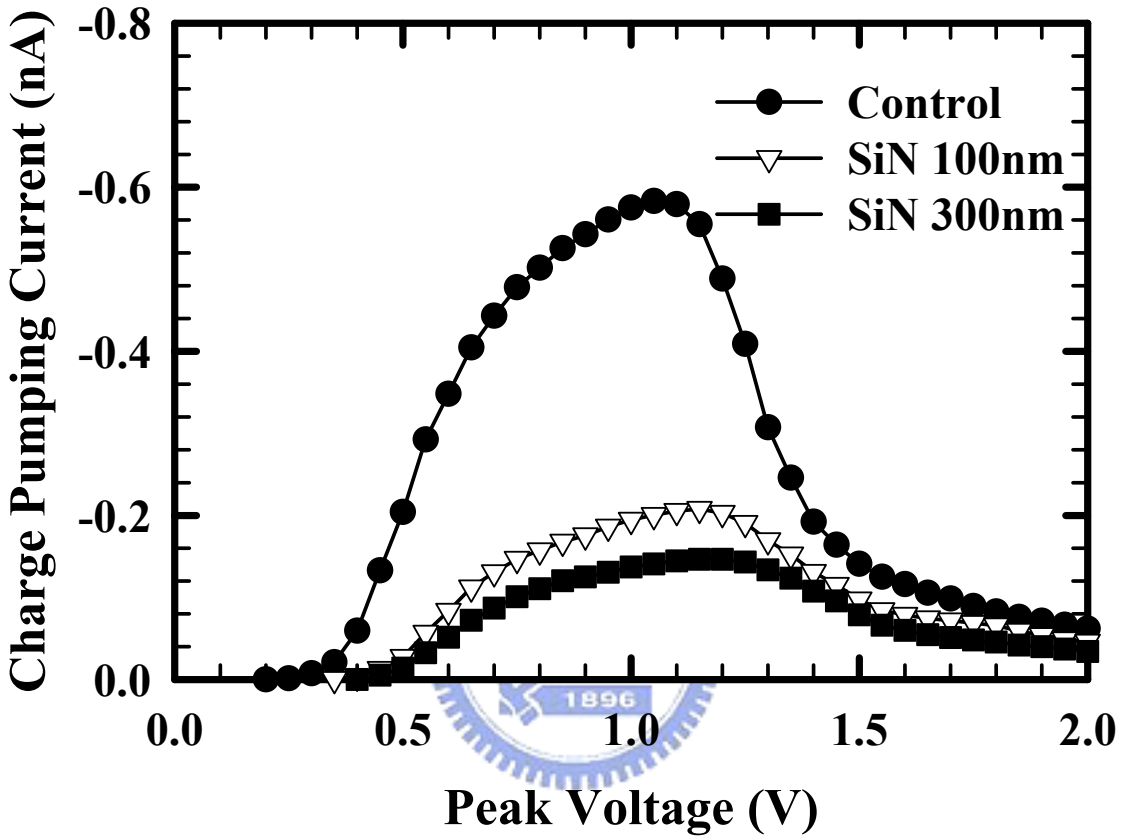


Fig. 3.15 Charge pumping current of devices with different capping layers at 25°C, W/L= 10μm/1μm, pulse amplitude= 1.5V, frequency= 1 MHz.

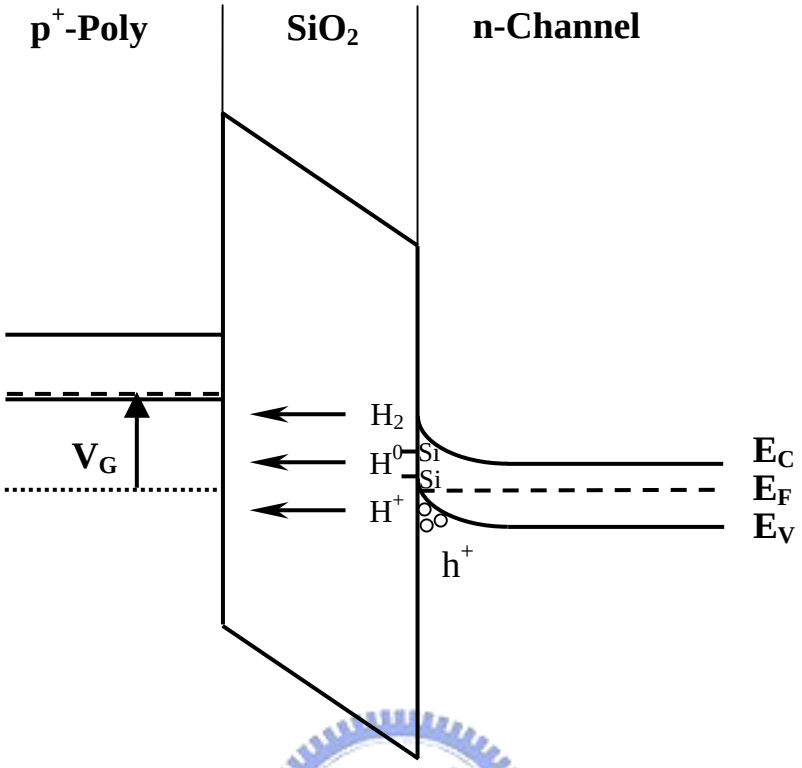


Fig. 4.1 Schematic view of the field-induced hydrogen species current through the gate oxide during negative bias aging.

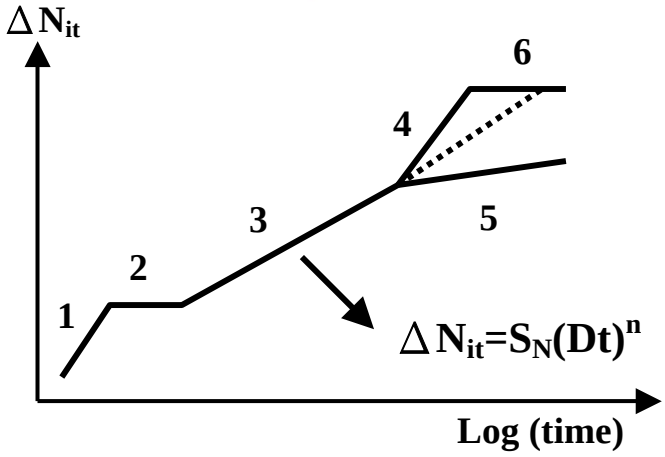
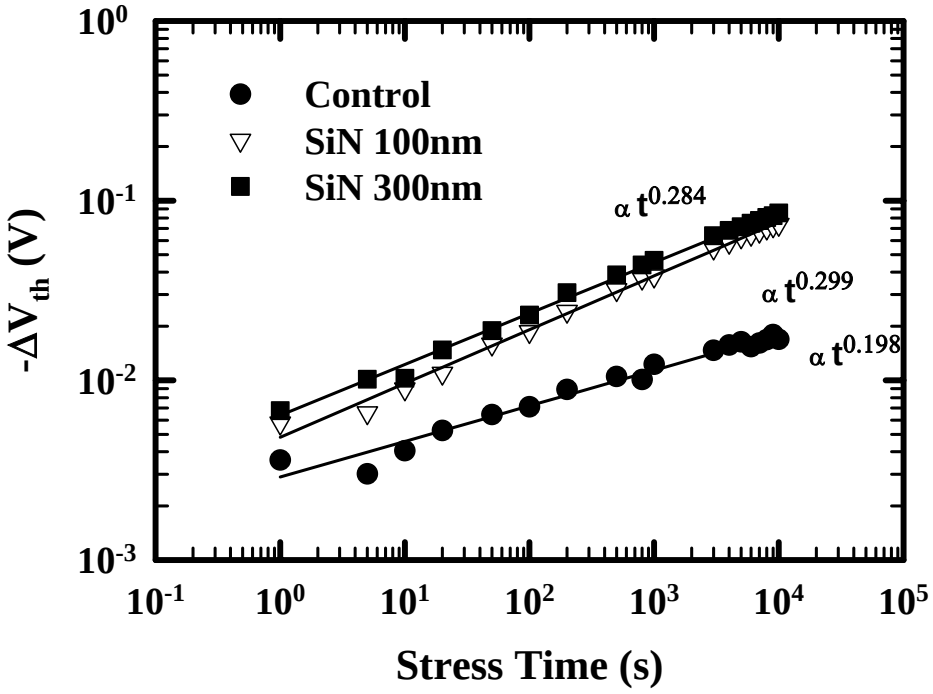
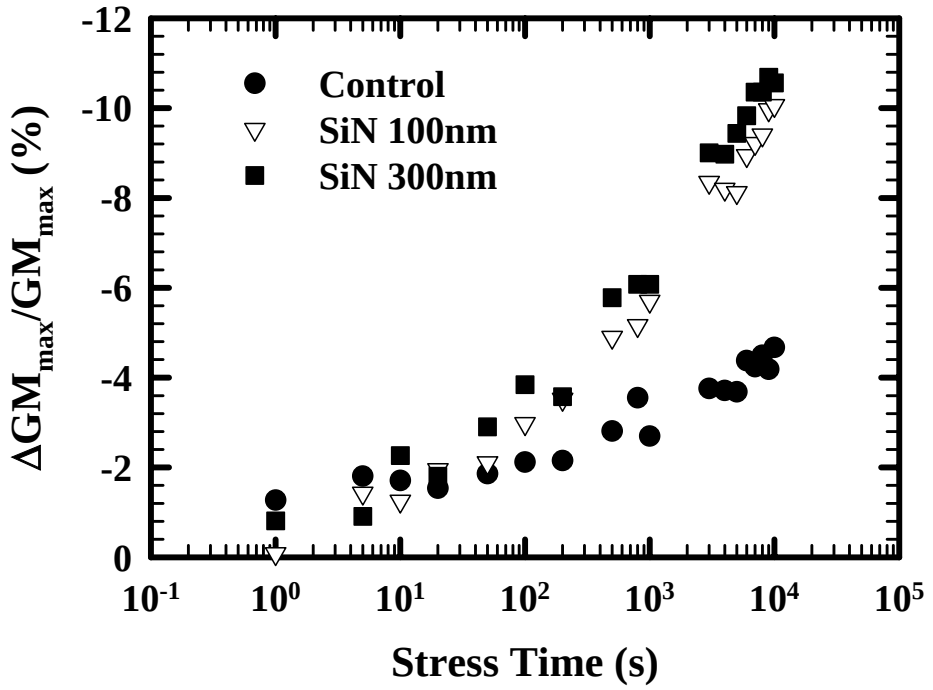


Fig. 4.2 Various phases of N_{it} buildup. 1: reaction-limited, 2: quasi-equilibrium, 3: diffusion-limited, 4: enhancement due to poly absorption, 5: saturation due to poly reflection, 6: final saturation [51].

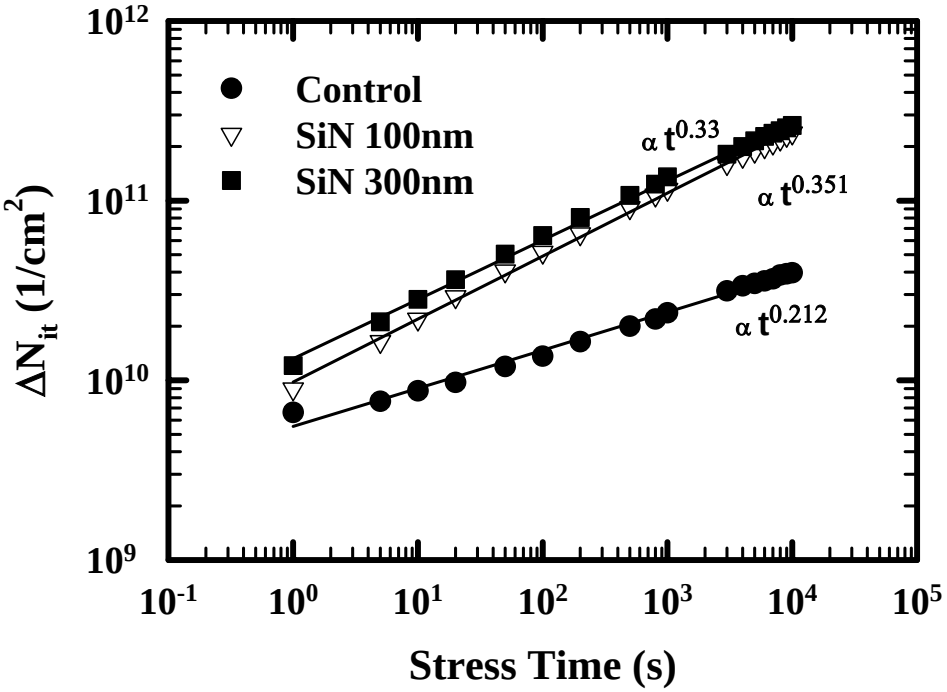


(a)

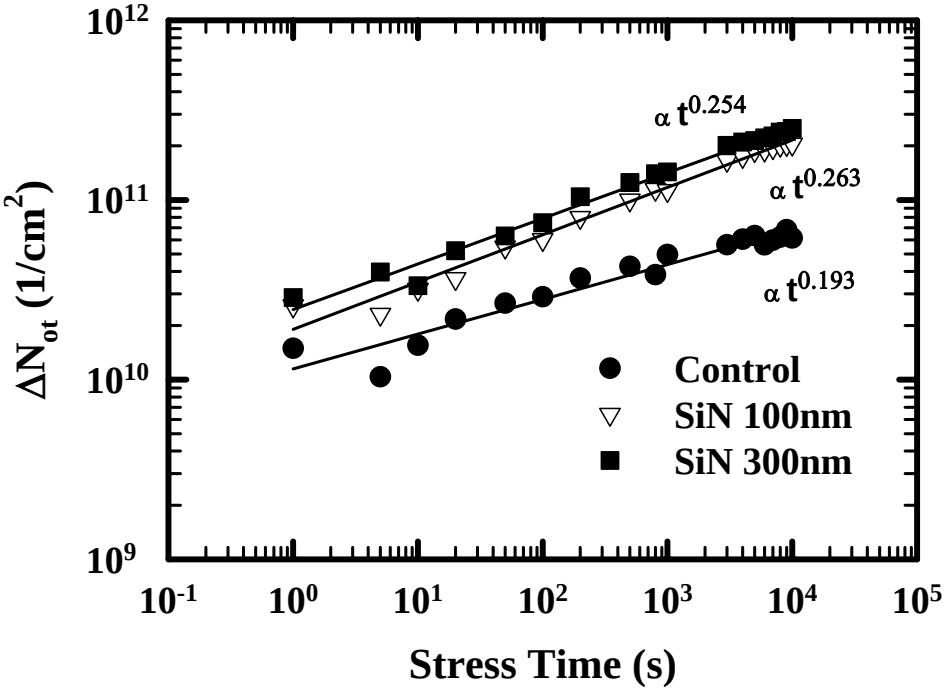


(b)

Fig. 4.3 (a) Threshold voltage shift, and (b) Transconductance degradation at 25°C during V_{GO} = –3.9 V stress aging (W/L= 10μm/0.55μm).

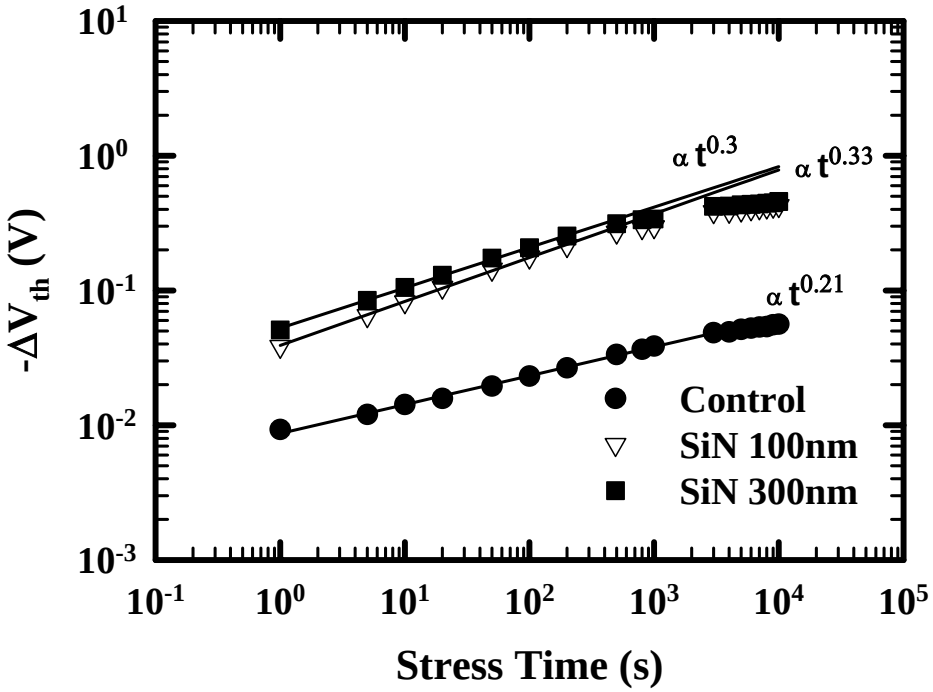


(c)

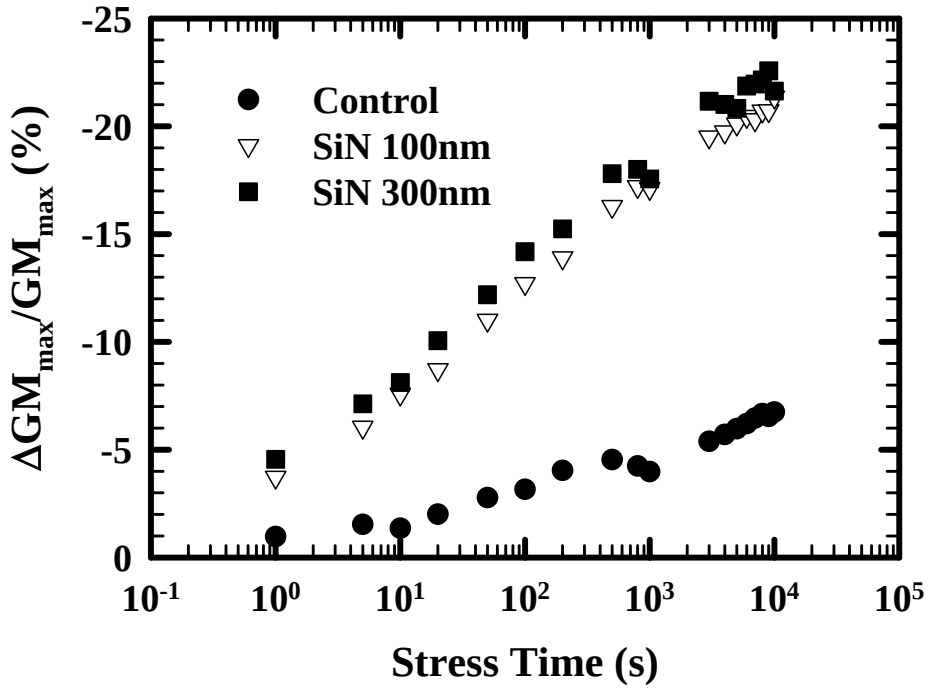


(d)

Fig. 4.3 (c) Interface trap density increasing, and (d) Oxide trap density increase at 25°C during V_{GO} = –3.9V stress aging (W/L= 10μm/0.55μm).

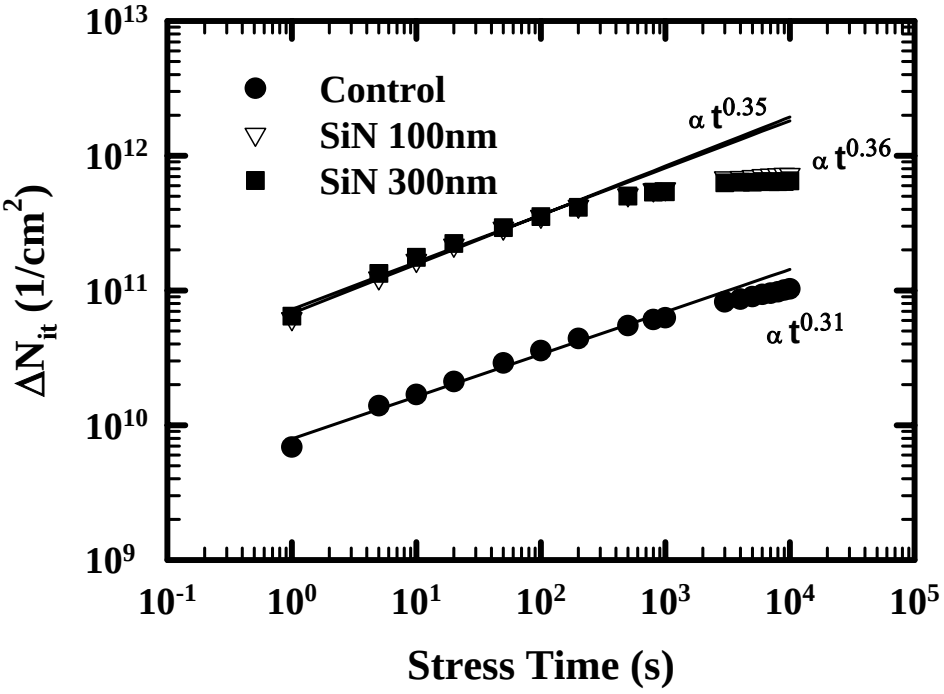


(a)



(b)

Fig. 4.4 (a) Threshold voltage shift, and (b) Transconductance degradation at 125°C during V_{GO} = –3.9V stress aging (W/L= 10μm/0.55μm).



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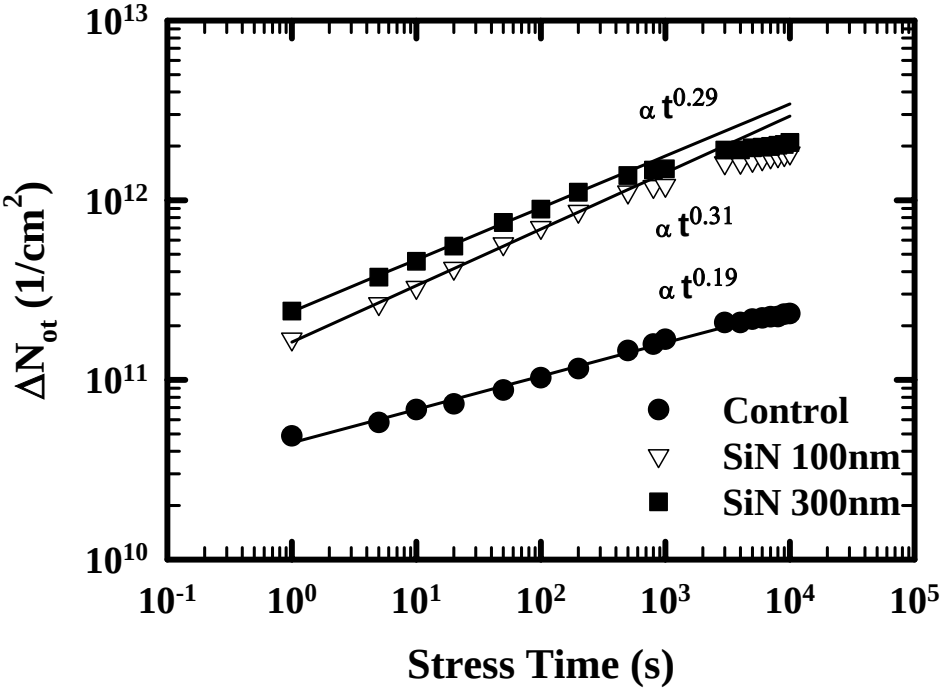
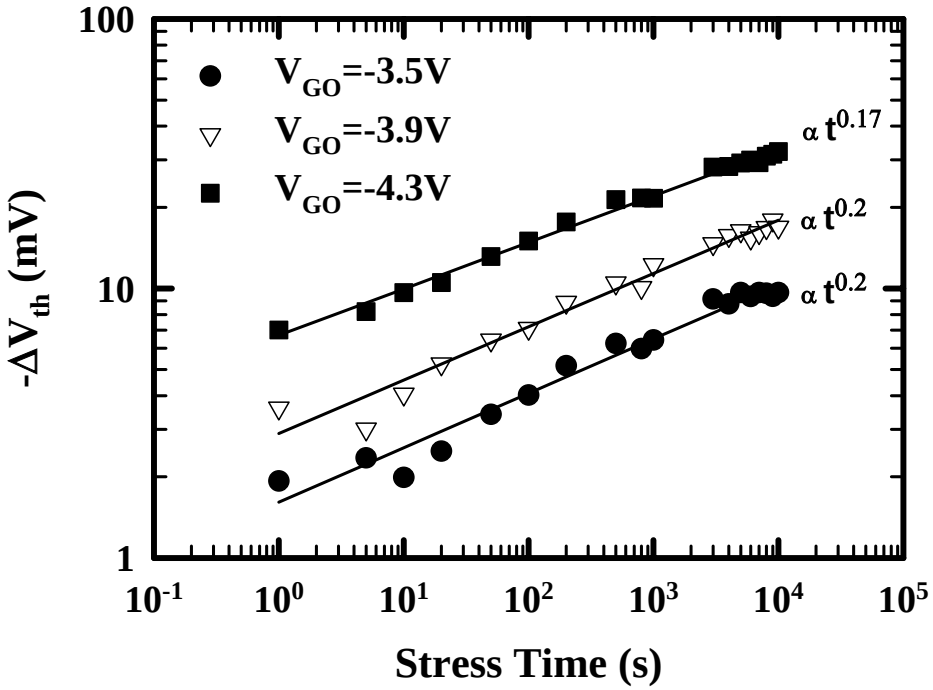
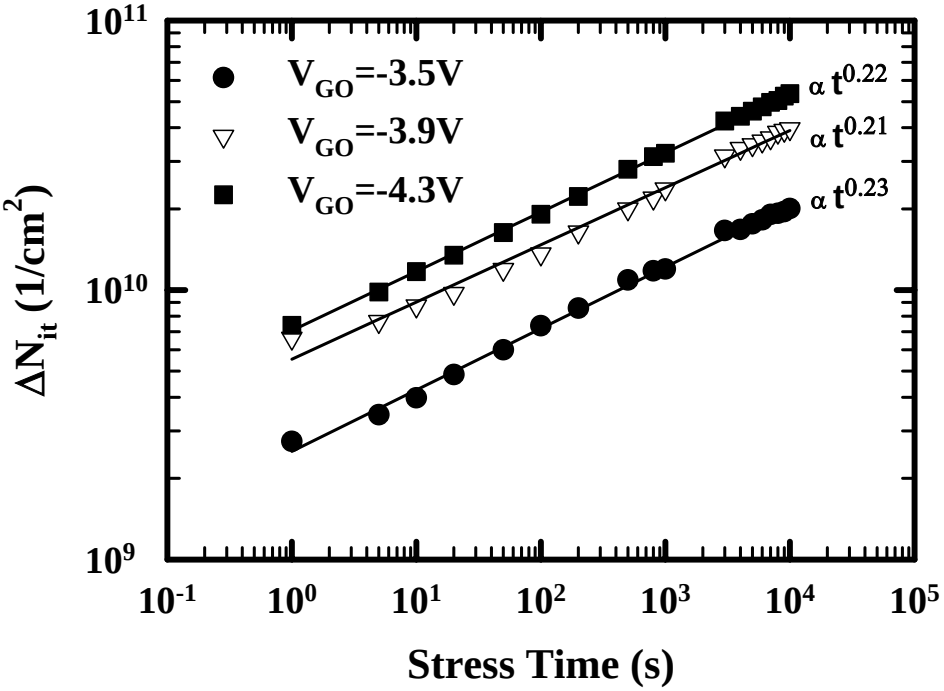


(d)

Fig. 4.4 (c) Interface trap density increase, and (d)oxide trap density increase at 125°C during V_{GO} = –3.9V stress aging (W/L= 10μm/0.55μm).

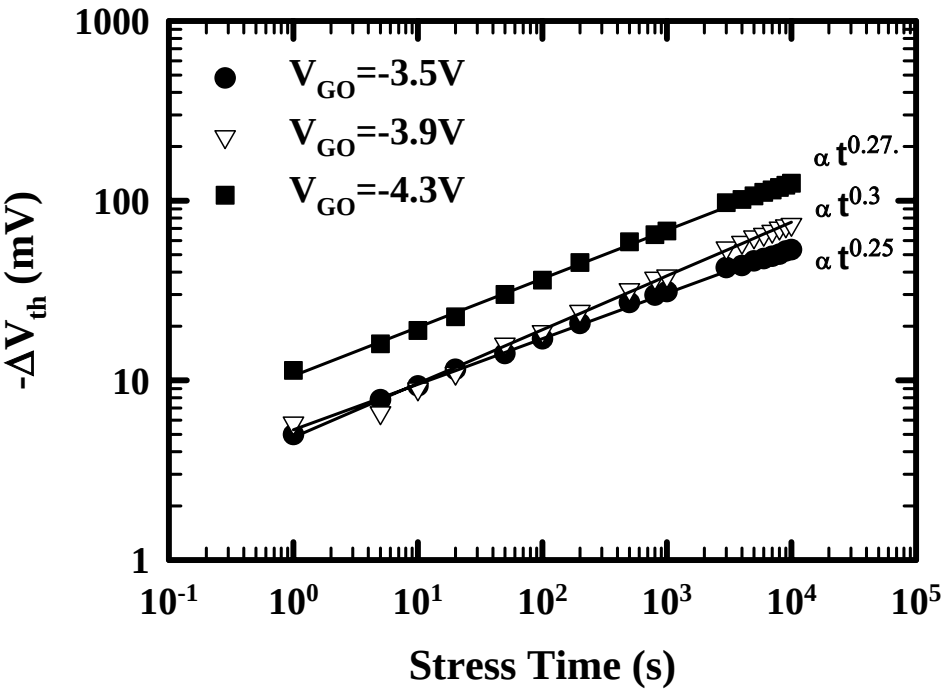


(a)

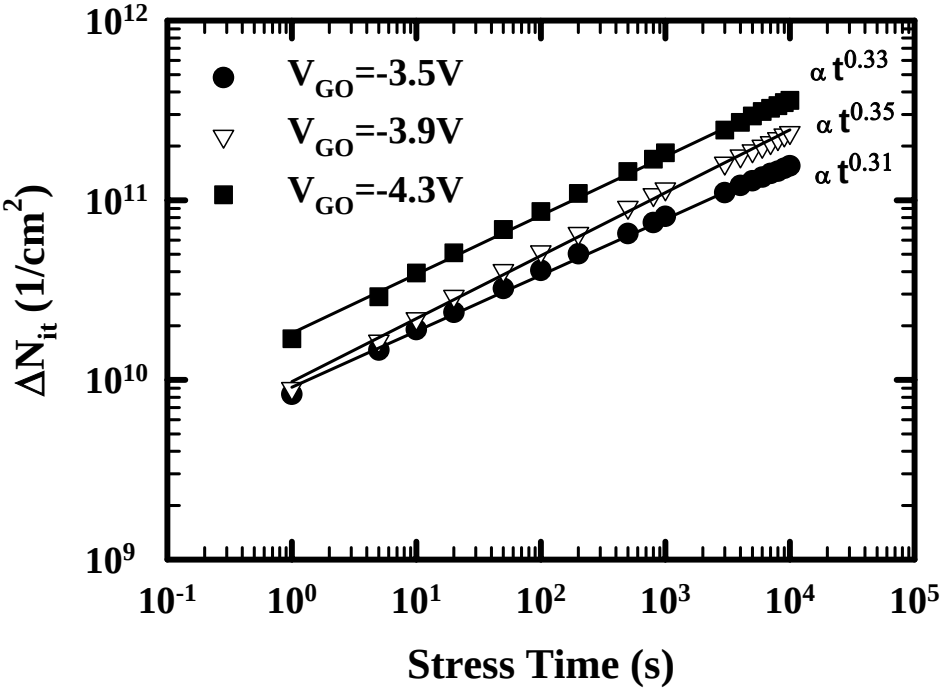


(b)

Fig. 4.5 (a) Threshold voltage shift, and (b) Interface trap density increase of the control sample at 25°C with different V_G stresses (W/L= 10μm/0.55μm).

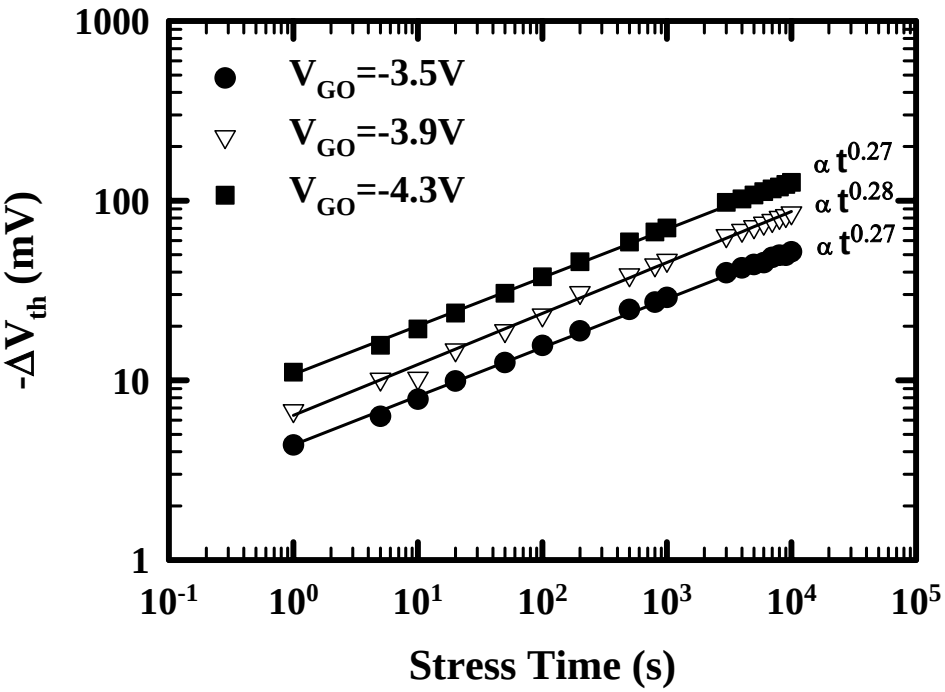


(a)

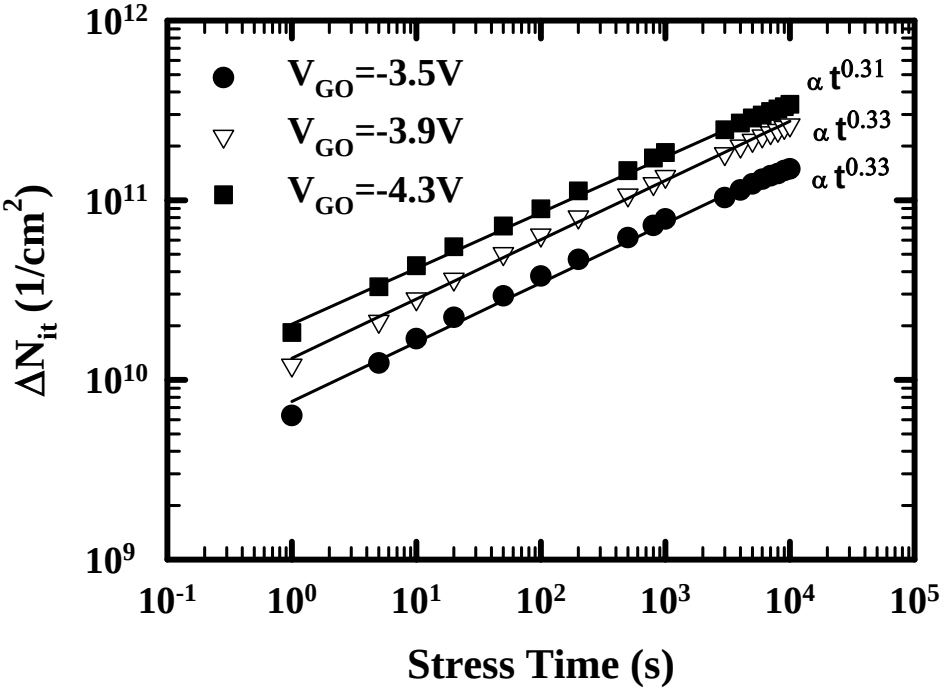


(b)

Fig. 4.6 (a) Threshold voltage shift, and (b) Interface trap density increase of the device with SiN-capping 100nm sample at 25°C with different V_G stresses. (W/L= 10μm/0.55μm)

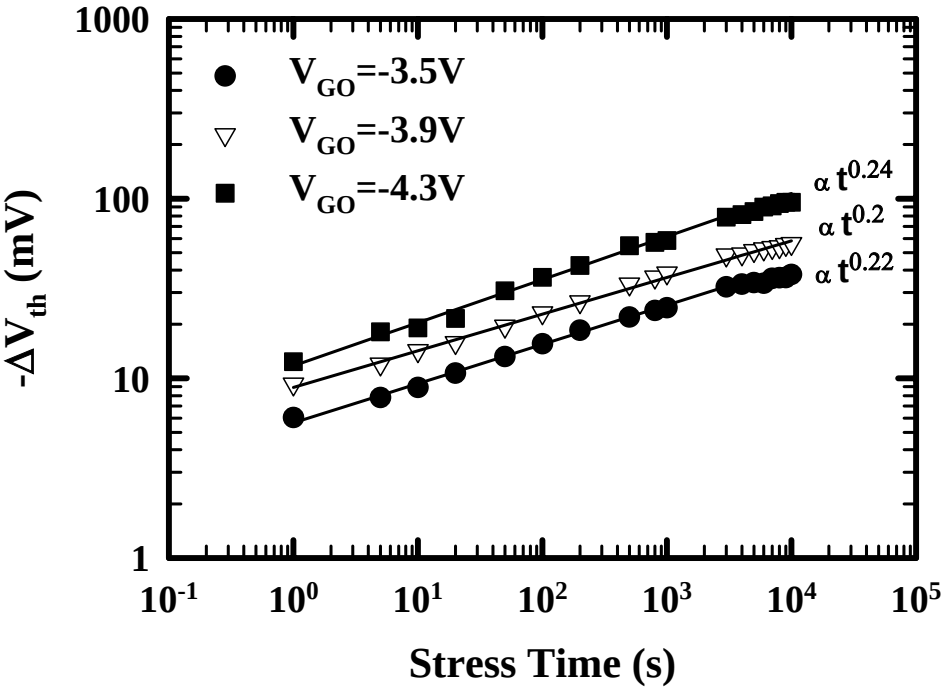


(a)

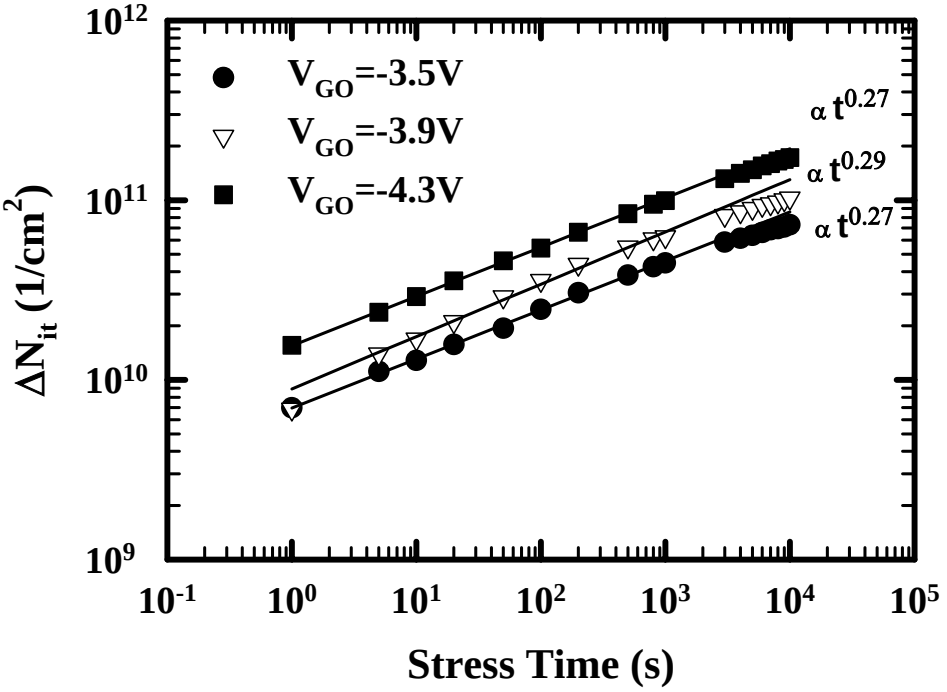


(b)

Fig. 4.7 (a) Threshold voltage shift, and (b) Interface trap density increase of the device with 300nm SiN-capping at 25°C with different V_G stresses. (W/L= 10μm/0.55μm)

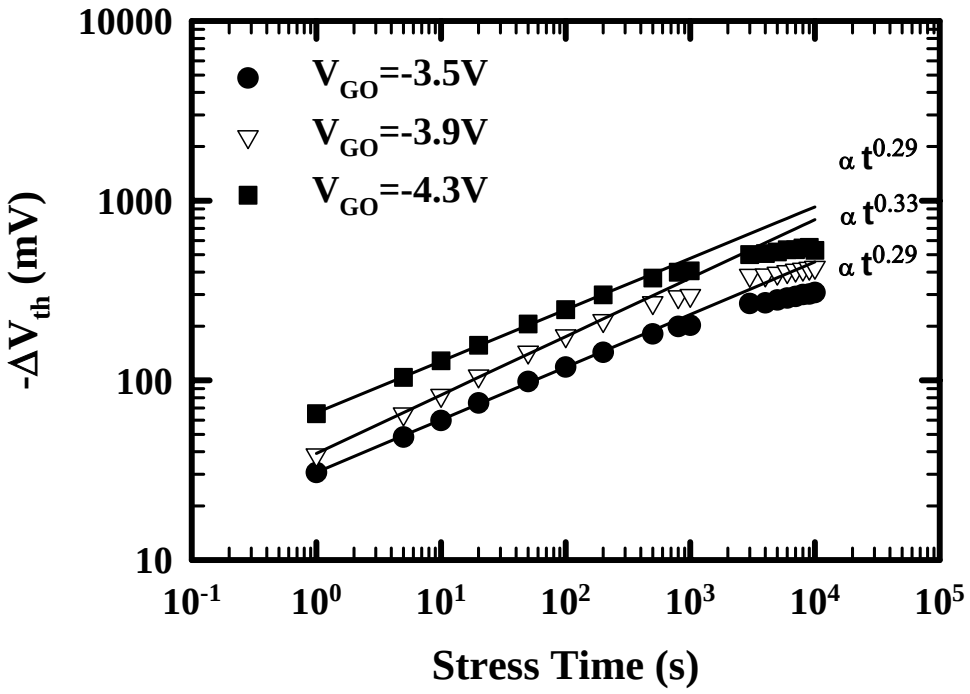


(a)

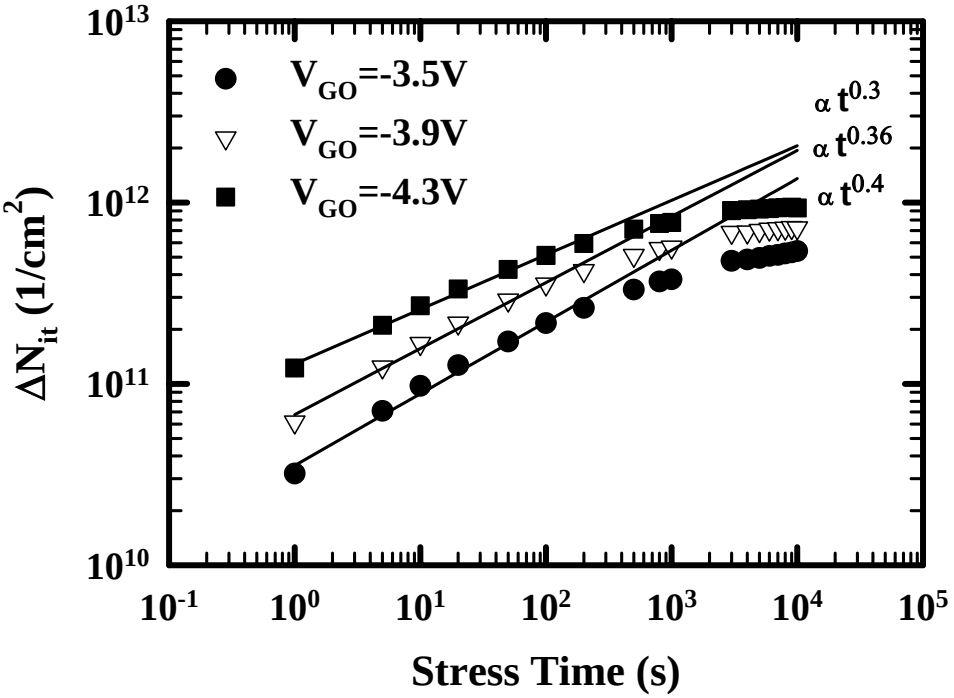


(b)

Fig. 4.8 (a) Threshold voltage shift,and (b) Interface trap density increaseof the control sample at 125°C with different V_G stresses. (W/L= 10μm/0.55μm)

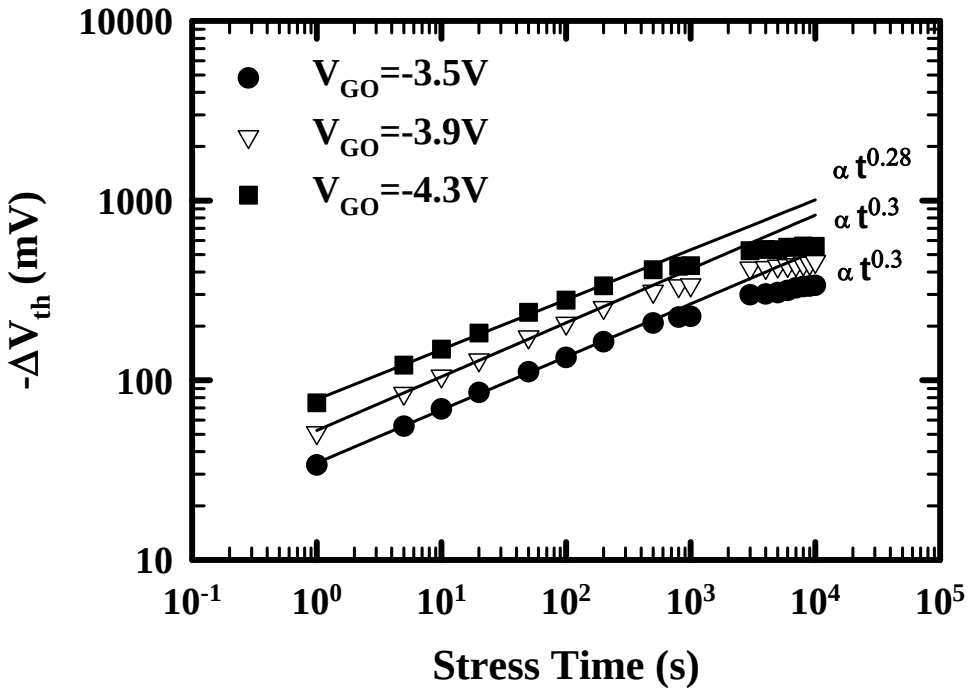


(a)

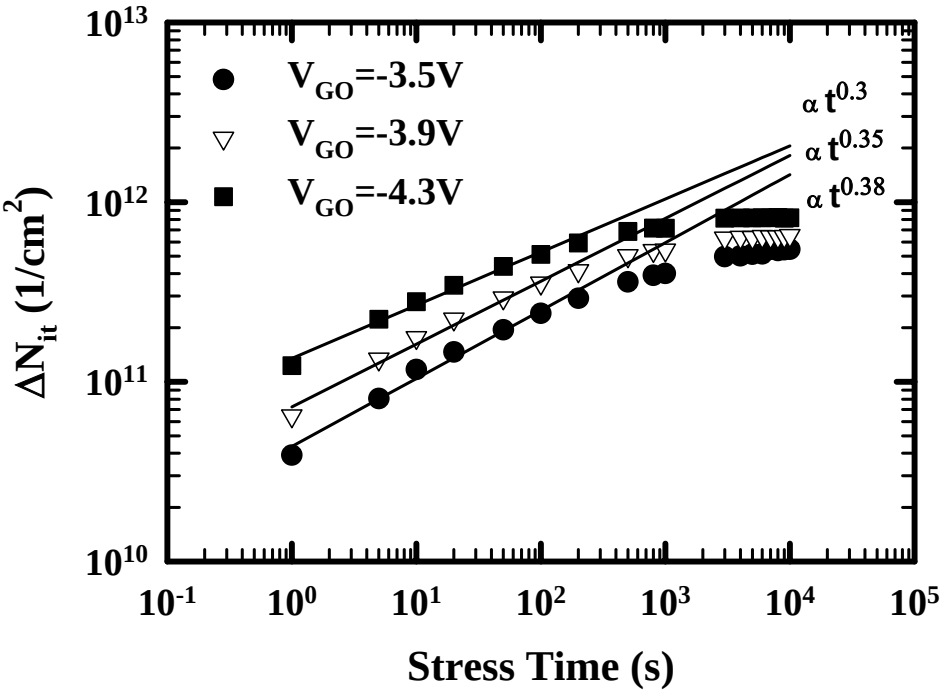


(b)

Fig. 4.9 (a) Threshold voltage shift, and (b) Interface trap density increase of the device with 100nm SiN-capping at 125°C with different V_G stresses. (W/L= 10μm/0.55μm)



(a)



(b)

Fig. 4.10 (a) Threshold voltage shift, and (b) Interface trap density increase of the device with SiN-capping 300nm sample at 125°C with different V_G stresses. (W/L=10μm/0.55μm)

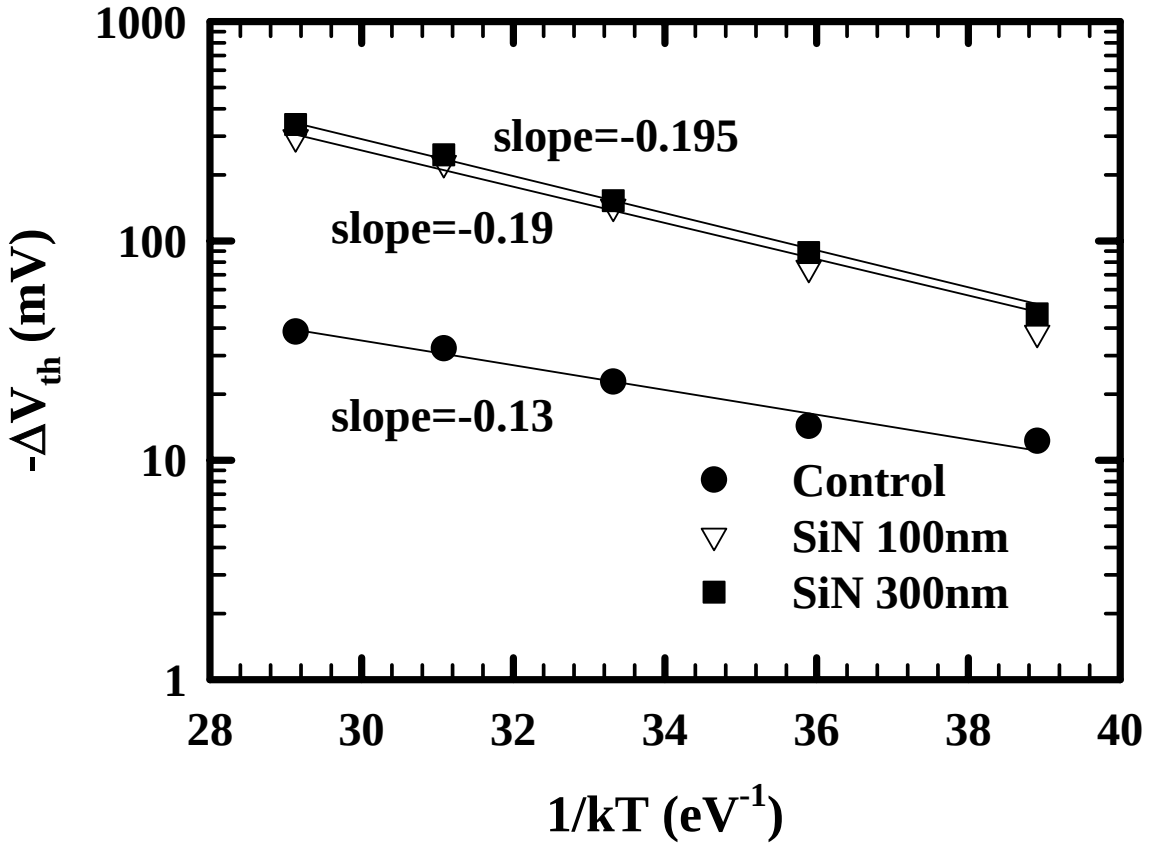
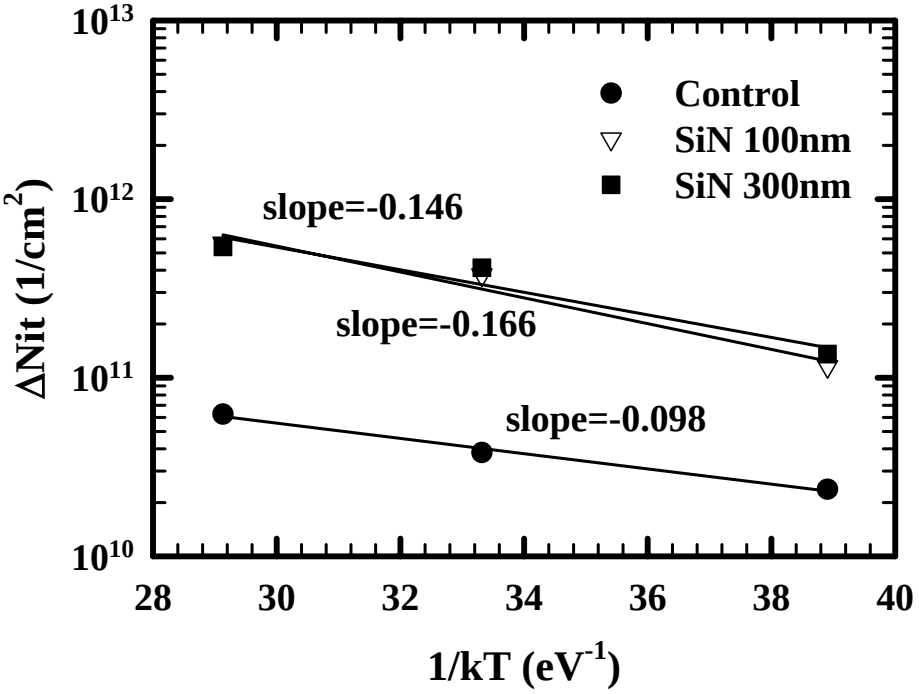
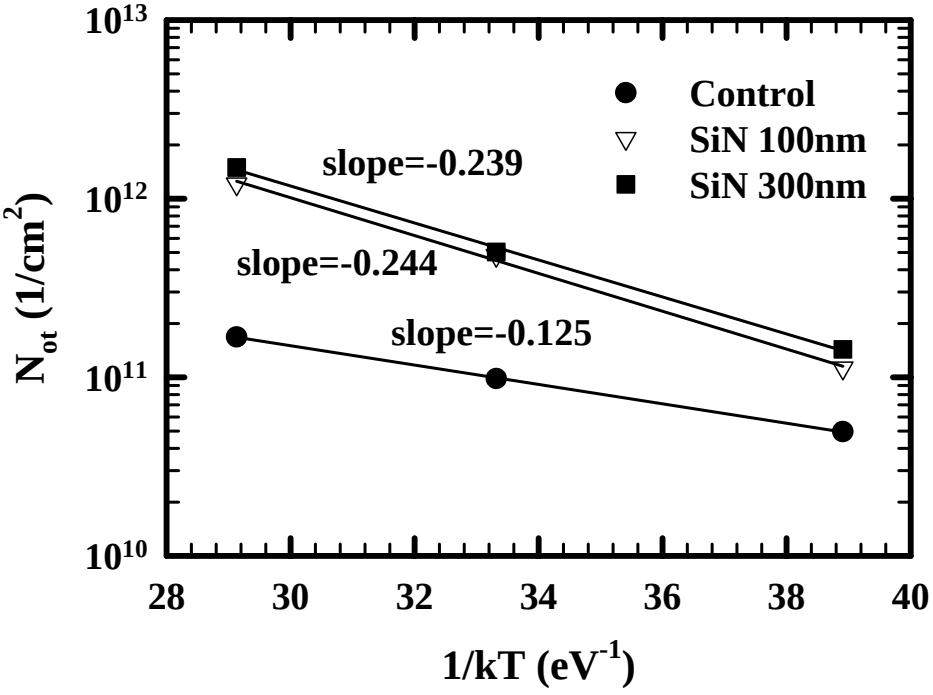


Fig. 4.11 Threshold voltage shift dependence on temperature with different capping layers, estimated by V_{GO} = –3.9V, 1000s stress.

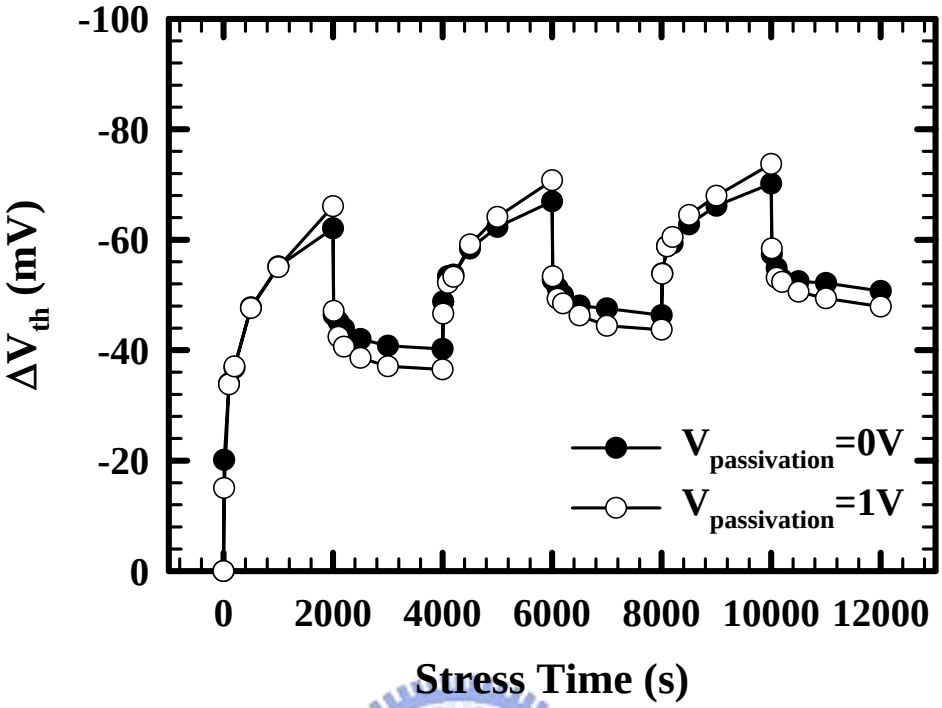


(a)

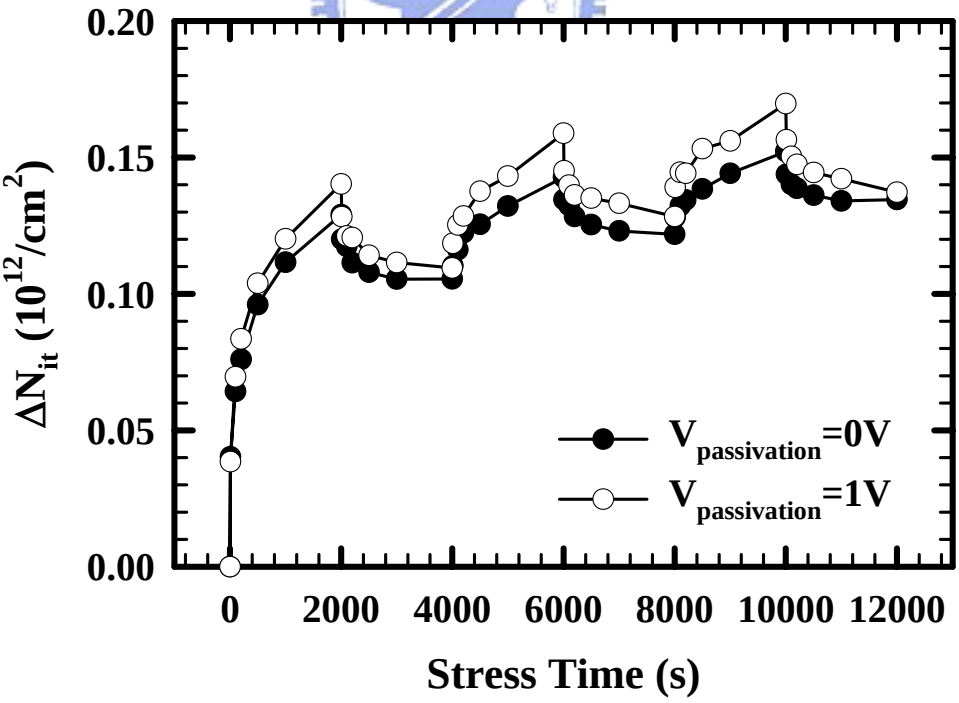


(b)

Fig. 4.12 (a) Interface trap density, and (b) Oxide trap density change dependence on temperature with different capping layers, estimated by V_{GO} = –3.9V, 1000s stress.

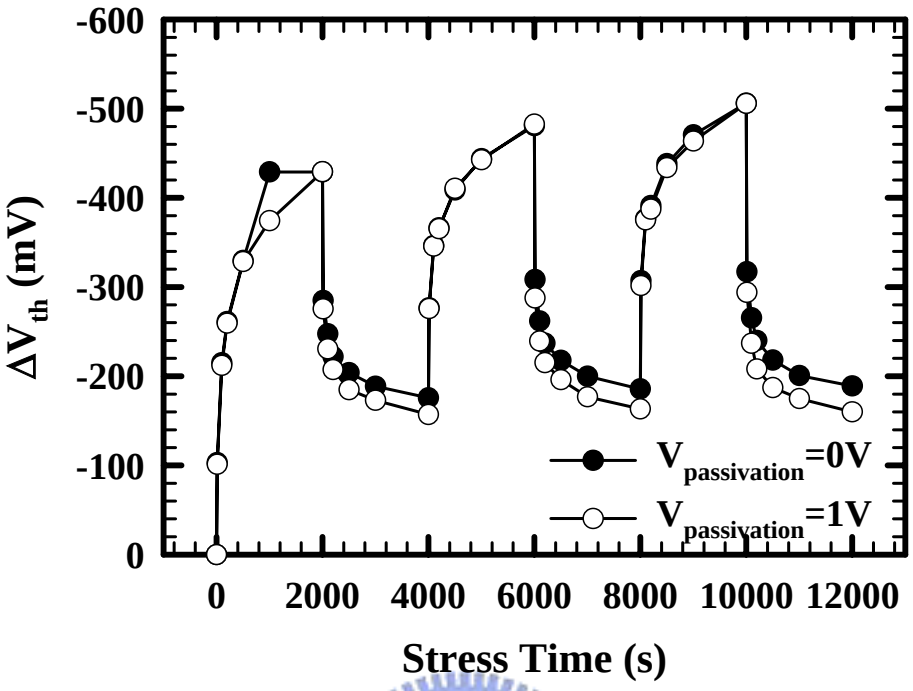


(a)

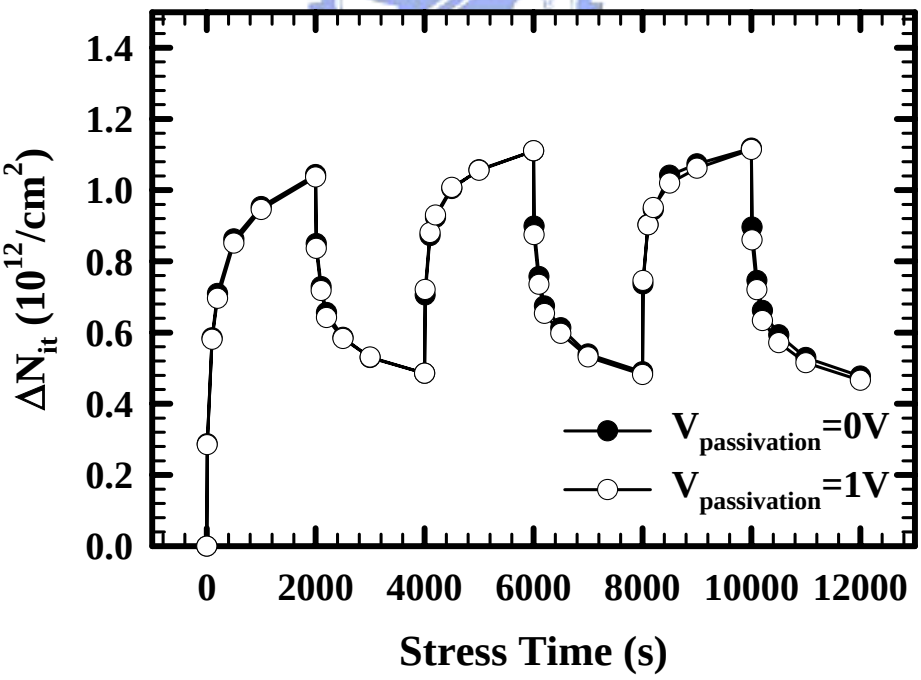


(b)

Fig. 4.13 (a) Threshold voltage shift, and (b) Interface trap density change of the control sample during V_{GO} = –4V and different passivation stresses at 125°C. (W/L= 10μm/0.75μm)

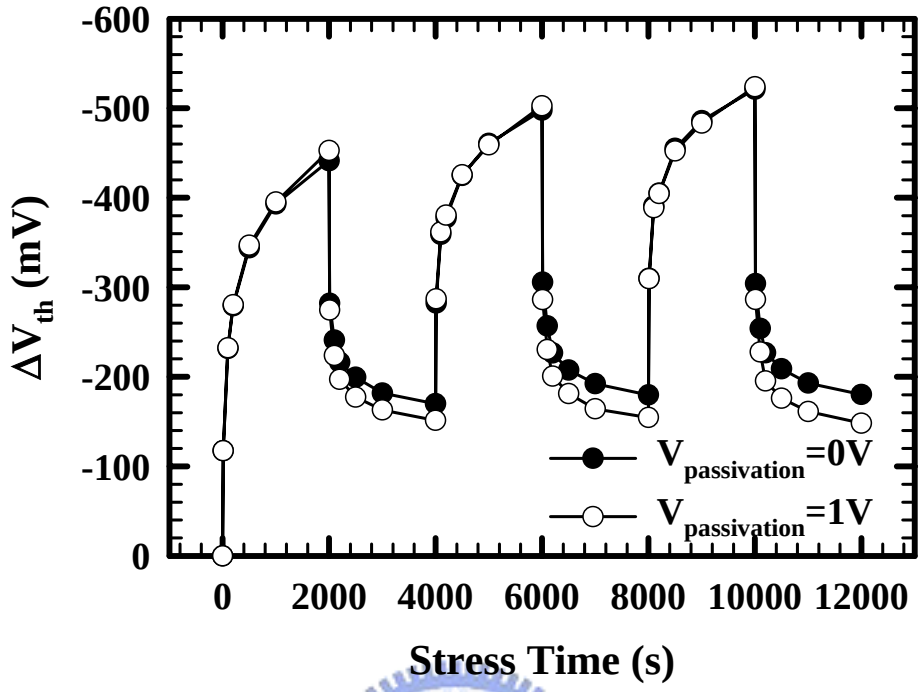


(a)

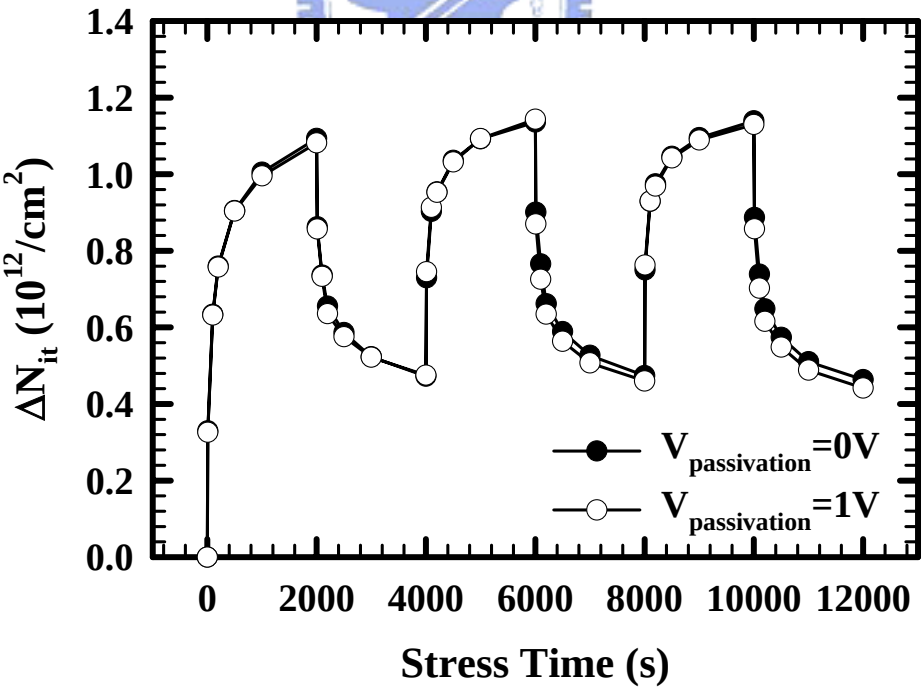


(b)

Fig. 4.14 (a) Threshold voltage shift, and (b) Interface trap density change of the device with 100nm SiN-capping 1ayer during V_{GO} = –4V and different passivation stresses at 125°C. (W/L= 10μm/0.75μm)

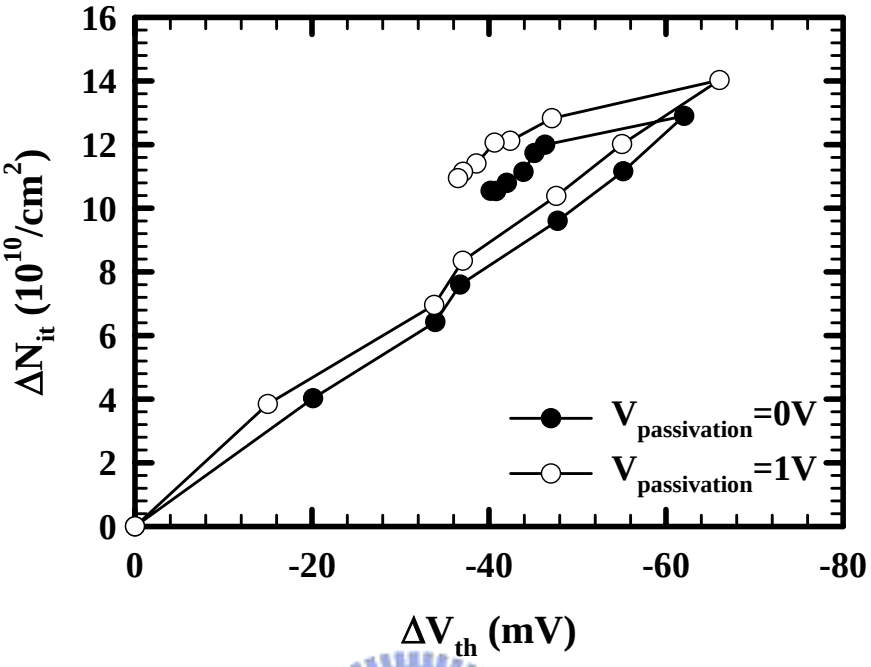


(a)

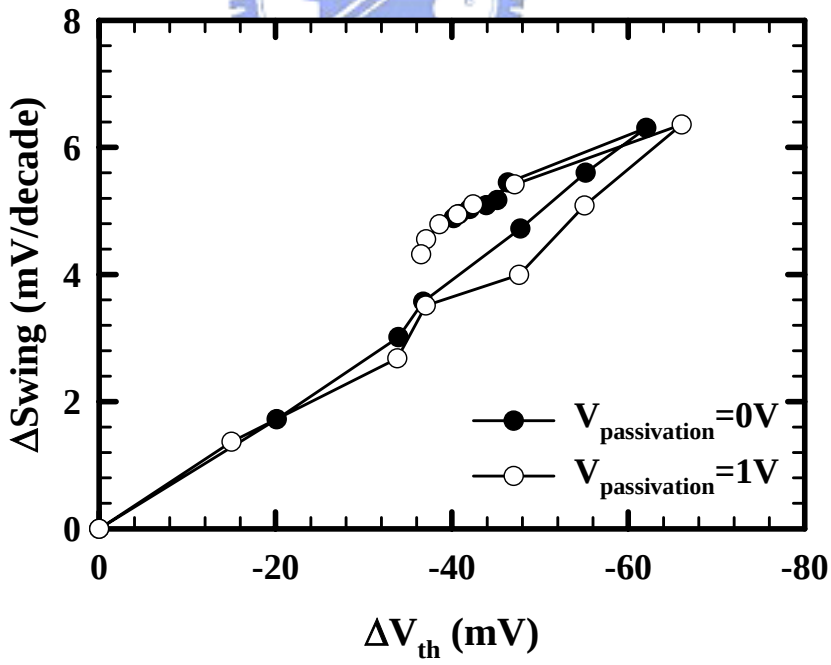


(b)

Fig. 4.15 (a) Threshold voltage shift, and (b) Interface trap density change of the device with 300nm SiN-capping layer during V_{GO} = –4V and different passivation stresses at 125°C. (W/L= 10μm/0.75μm)

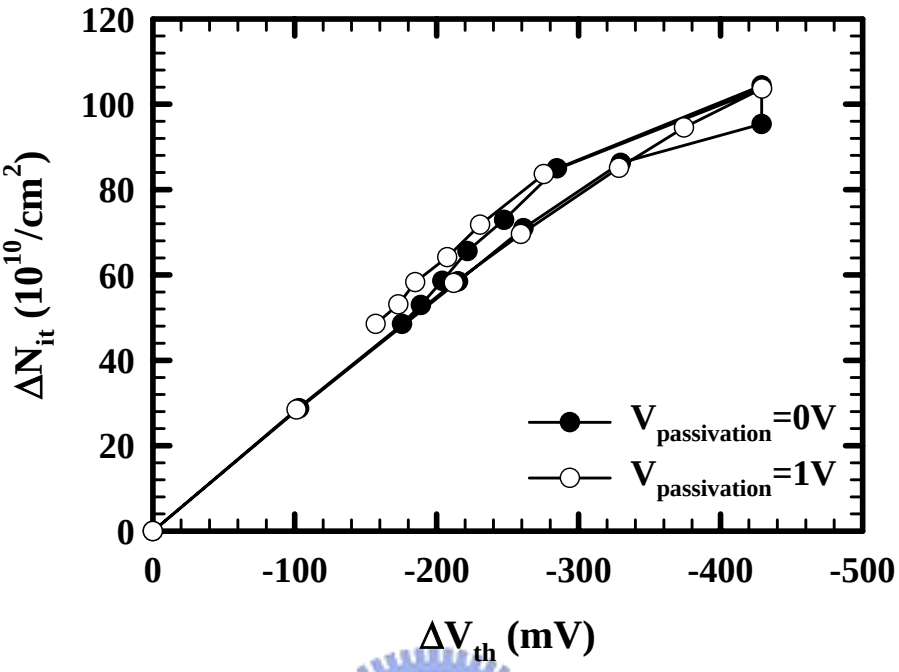


(a)

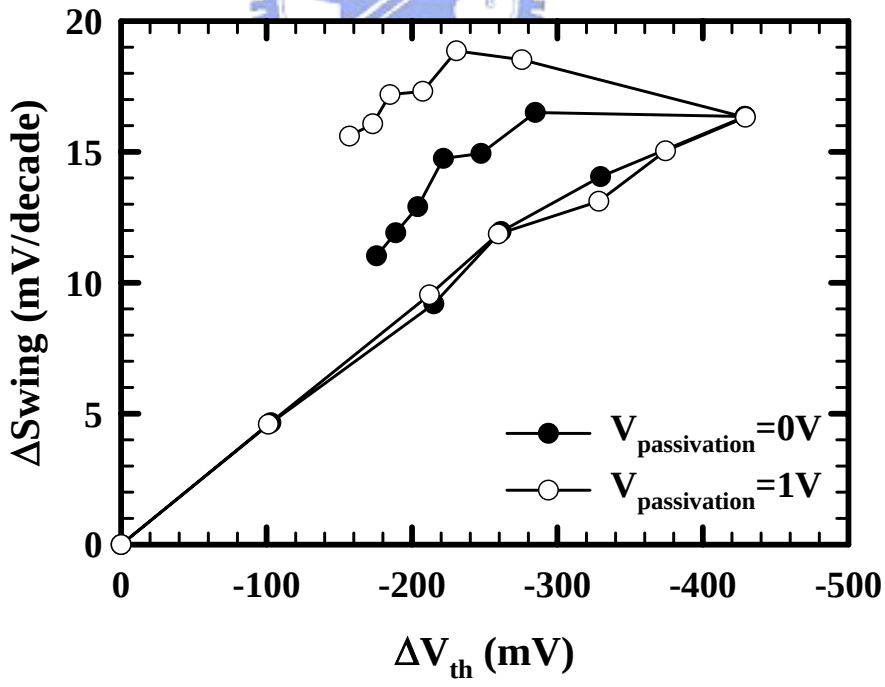


(b)

Fig. 4.16 (a) Interface trap density change, and (b) Subthreshold swing shift dependence on threshold voltage shift of the control sample, during V_{GO}= –4V and different passivation stresses at 125°C. (W/L= 10μm/0.75μm)

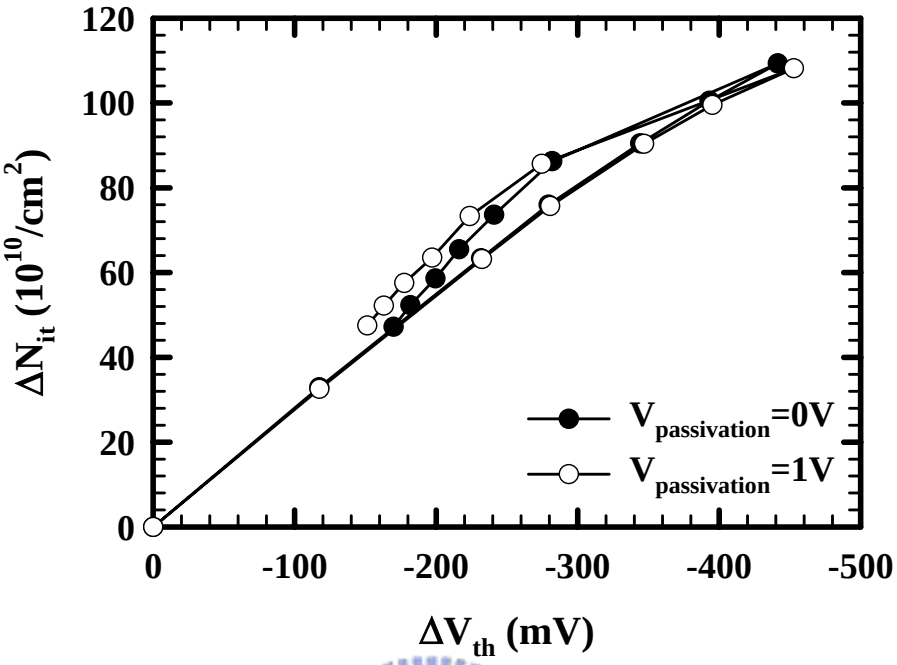


(a)

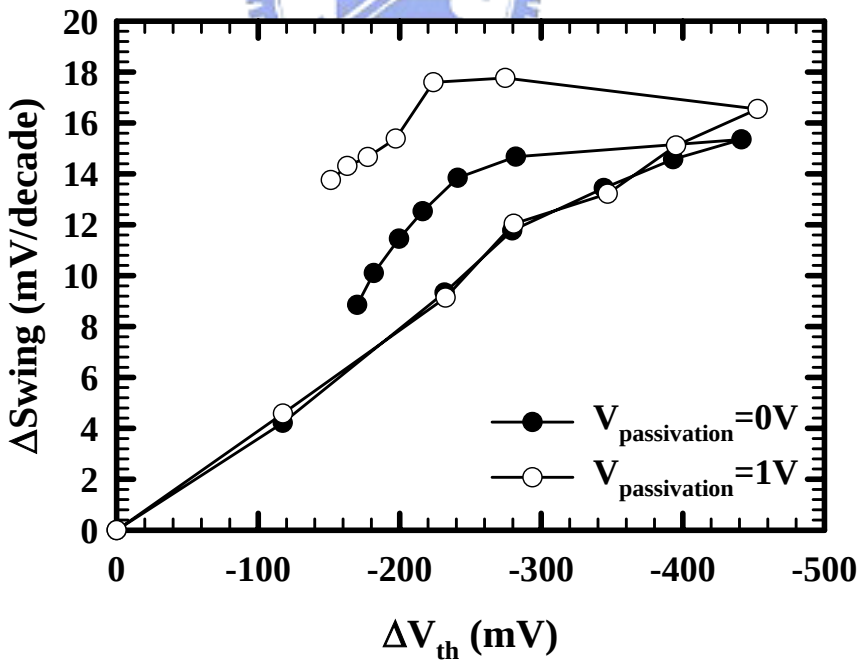


(b)

Fig. 4.17 (a) Interface trap density change, and (b) Subthreshold swing shift dependence on threshold voltage shift of the device with 100nm SiN-capping layer, during V_{GO}= –4V and different passivation stresses at 125°C. (W/L= 10μm/0.75μm)

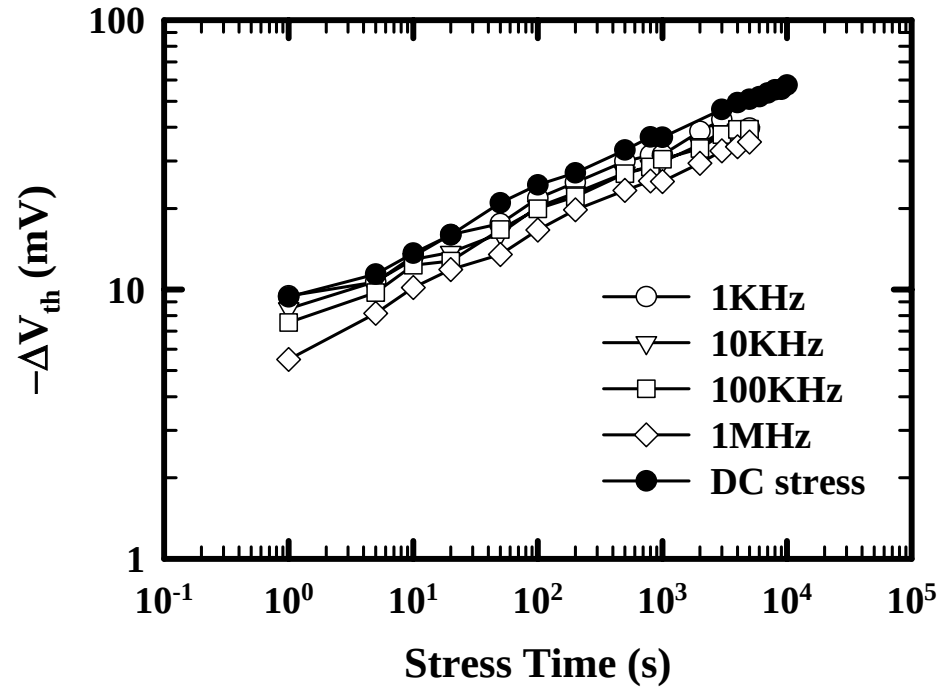


(a)

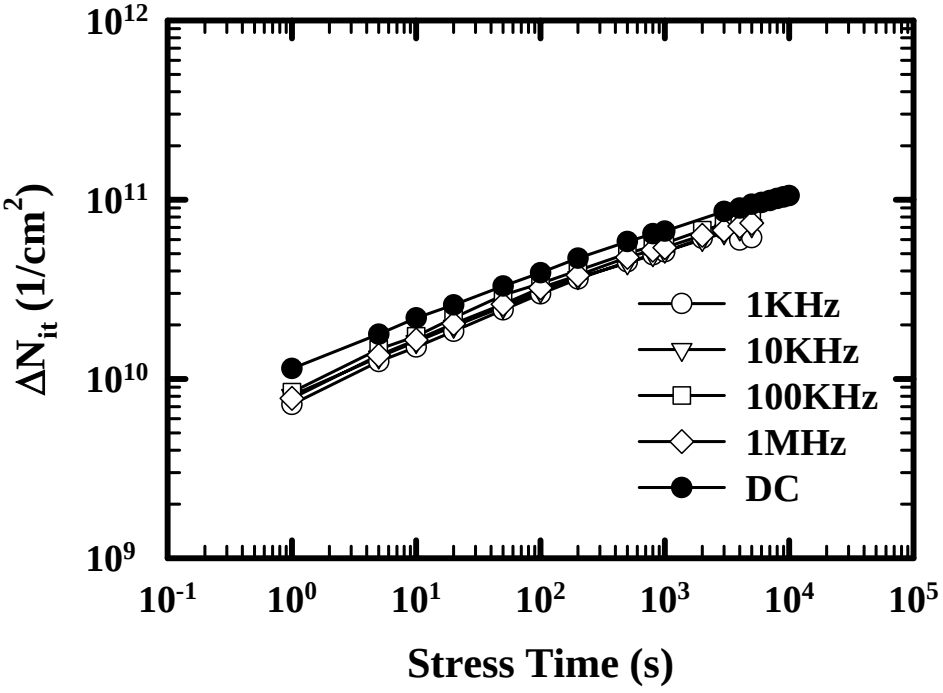


(b)

Fig. 4.18 (a) Interface trap density change, and (b) Subthreshold swing shift dependence on threshold voltage shift of the device with 300nm SiN-capping layer, during V_{GO}= –4V and different passivation stresses at 125°C. (W/L= 10μm/0.75μm)

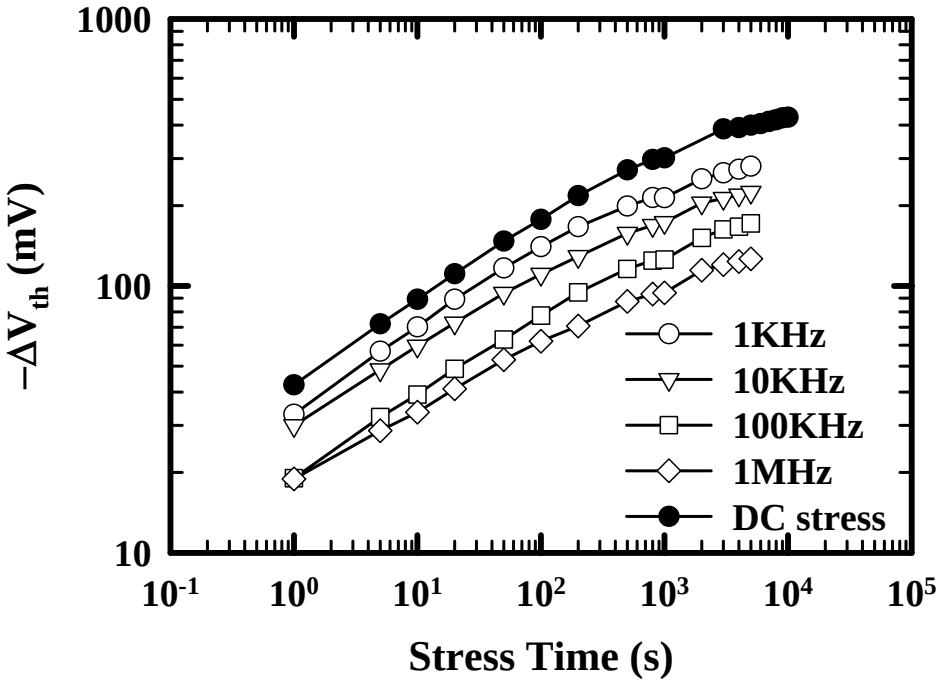


(a)

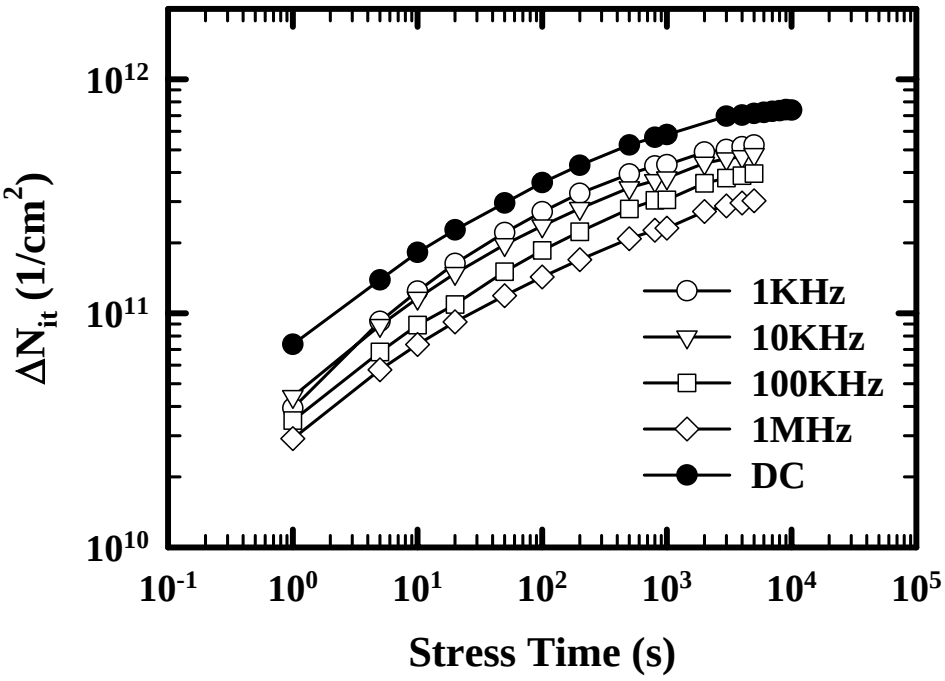


(b)

Fig. 4.19 (a) Threshold voltage shift, and (b) Interface trap density change of the control sample during different frequency AC stresses (V_{GO}= -3.9V) at 125°C. (W/L= 10μm/0.65μm)

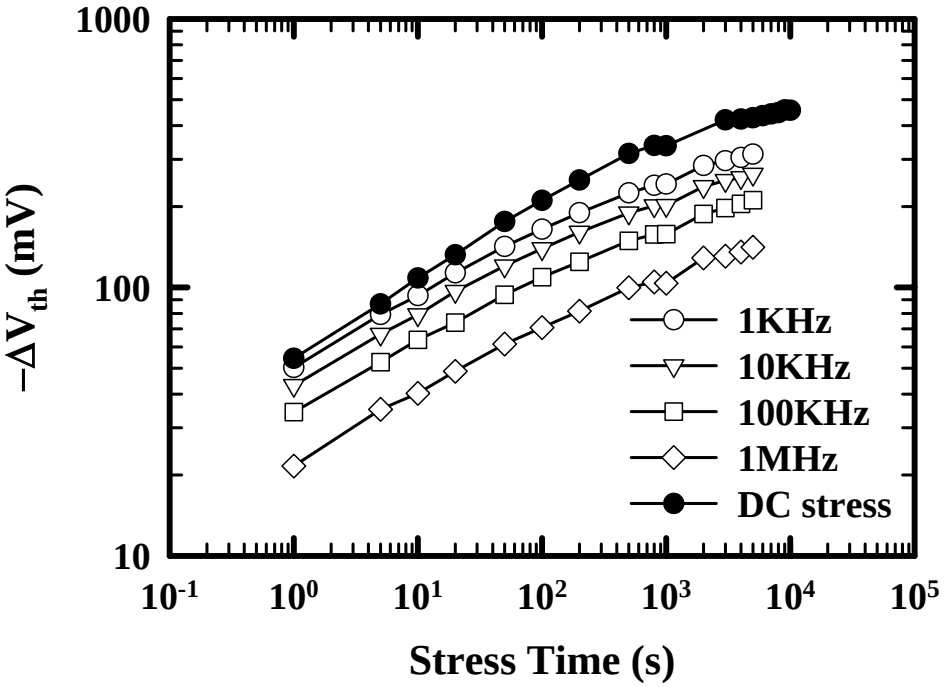


(a)

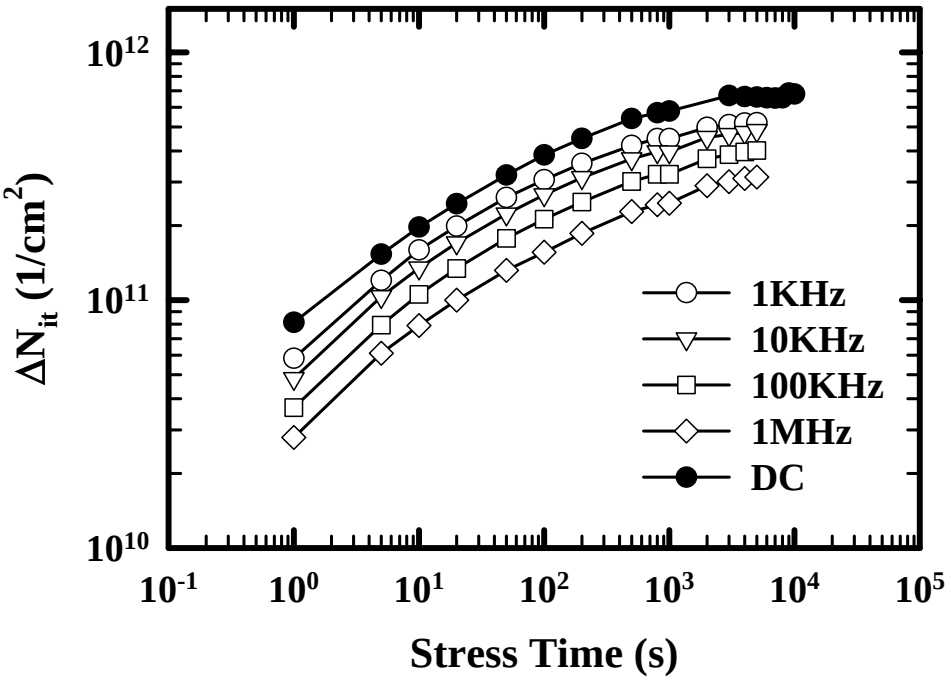


(b)

Fig. 4.20 (a) Threshold voltage shift, and (b) Interface trap density change of the device with 100nm SiN-capping layer, during different frequency AC stresses, V_{GO}= -3.9V at 125°C. (W/L= 10μm/0.65μm)

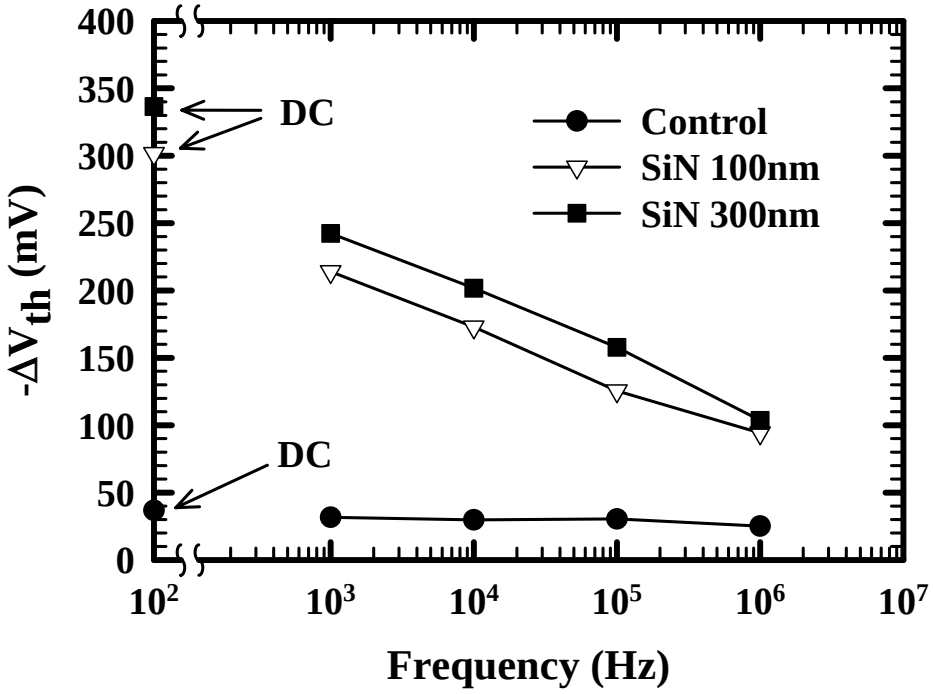


(a)

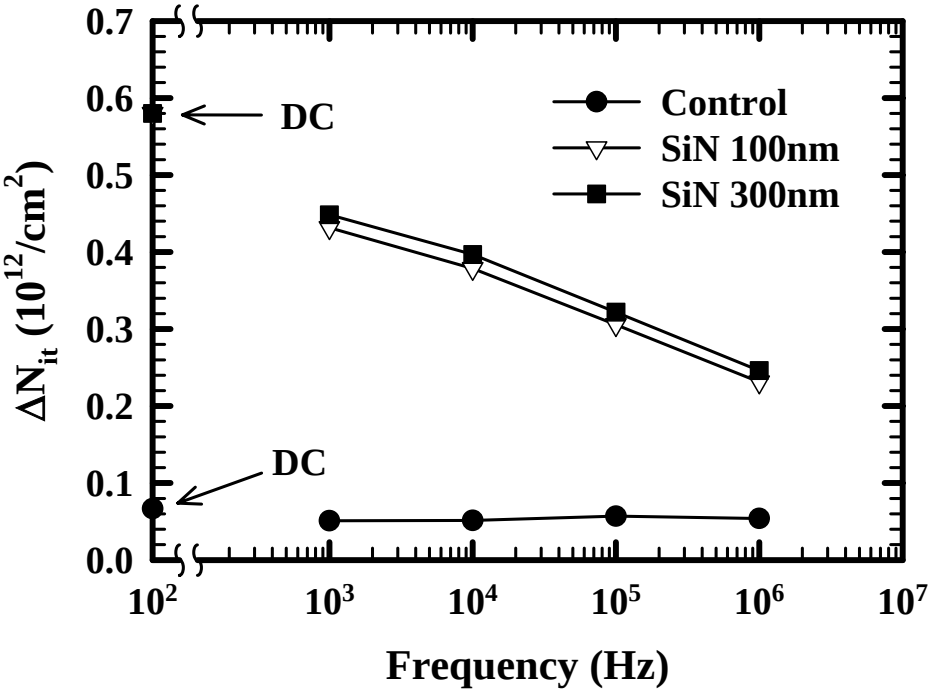


(b)

Fig. 4.21 (a) Threshold voltage shift, and (b) Interface trap density change of the device with 300nm SiN-capping layer, during different frequency AC stresses V_{GO}= -3.9V at 125°C. (W/L= 10μm/0.65μm)



(a)



(b)

Fig. 4.22 (a) Threshold voltage shift, and (b) Interface trap density change as a function of frequency for devices with different capping layers, after V_{GO} = -3.9V 1000sec stress at 125°C. (W/L= 10μm/0.65μm).

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論文題目：具有複晶矽鍺閘極與局部形變通道之 P 型金氧半場效電晶體元件製作與分析

Fabrication and Characterization of PMOSFETs with Poly-SiGe gate and Locally Strained Channel