國　立　交　通　大　學

電子工程學系　　電子研究所碩士班

碩　士　論　文

具有加厚源/汲極與薄通道之新穎低溫複晶矽薄膜電晶體之製作與特性研究

The Novel Structure of Low-Temperature Polycrystalline Silicon Thin-Film Transistors with Thick S/D and Thin Channel

研 究 生 ： 謝 孟 帆

指導教授 ： 張 國 明　博士

桂 正 楣　博士

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研 究 生：謝孟帆　　Student： Mon-Fan Hsieh

指導教授：張國明 博士　　Advisor： Dr. Kow-Ming Chang

桂正楣 博士　　Dr. Cheng-May Kwei

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摘要

本篇論文中，我們將探討和比較所製作的新穎結構，此新穎結構具有加厚的汲/源極和一個薄通道，因加厚的汲/源極和薄通道帶來的效應，我們可以增大導通狀態時的電流以及降低漏電流，進而改善我們的開/關電流的比值至 10^7，且更可以抑制扭節現象 (kink effect) 的產生，而不需要在製程中多出一道額外的光罩。在我們的研究中，將新結構與傳統結構相比，開/關電流比在汲極電壓爲 5V 時，將會從 $6*10^6$ 增加到 $3.5*10^7$。此新穎結構的各種尺寸也具備不錯的對稱性。此外我們還探討了閘極下方與汲/源極重疊處對元件特性的影響，我們認爲此區較小會獲得較佳之電性。

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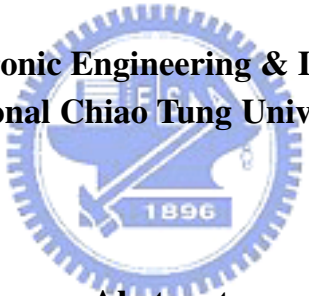
Student : Mon-Fan Hsieh **Advisor: Dr. Kow-Ming Chang**
Dr. Cheng-May Kwei

Department of Electronic Engineering & Institute of Electronics
National Chiao Tung University



Abstract

In this thesis, the characteristics of the novel structure of poly-Si TFTs with thick S/D and thin channel have been investigated and compared. With the thick S/D and thin channel, we can not only decrease the off-state current but also increase the on-state current. Therefore, we succeed to achieve the on/off ratio about 7 orders and substantially suppress the kink effect without an extra mask. In our study, the on/off ratio is rose from $6*10^6$ to $3.5*10^7$ for V_{ds} = 5V, W/L = 50 μm/10 μm. We also have a great symmetry for four device sizes of our novel structure of LTPS TFTs. In our experiment, we also investigated the influence of different gate-overlap region, we have shown the smaller gate-overlap region would be more better.

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謝謝交大奈米中心與國科會 NDL 提供了完整的機台讓我可以順利地完成我的論文，也謝謝黃月美女士等技術員給予我大力幫忙。

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Table captions

Table. Major electrical parameters of the LTPS TFTs with thick S/D and thin channel. The On/Off current ratio is measured at V_{gs} = 5V. The field-effect mobility(μ_{fe}) is measured in the linear region at a V_{ds} of 0.1V. The threshold voltage is defined at a normalized drain current of (100nA)*(W/L) at V_{gs} = 5V; W/L = 50μm/20μm

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Chapter 1

Introduction

1.1 An overview of Low Temperature Polycrystalline Silicon (LTPS) TFTs

In recent years, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been widely studied because of their potential applications in peripheral driving circuits in AMLCDs, AMOLEDs [1], high density SRAMs [2][3], linear image sensors [4], nonvolatile memories [5], thermal printer heads [6], photodetector amplifier [7] etc. Most importance of all, the poly-Si TFTs is the most promising pixel switching controller in AMLCDs.

In the past, amorphous silicon thin-film transistors (a-Si:H TFTs) are mainly used for active-matrix addressed LCDs [8]. However, to be compared with poly-Si TFTs, they have extremely low field-effect mobility (typically below 1cm^2/V sec). Poly-Si TFTs have better characteristics than amorphous silicon thin-film transistors, including higher mobility, lower photocurrent and better reliability [9]. Most important advantage of poly-Si TFTs is for their use on the peripheral driving circuit in large-area active matrix liquid crystal displays (AMLCDs). Therefore, we can achieve the goal to system on panel (SOP).

Recrystallization technology is an important process for fabricating low temperature poly-Si TFTs because the performance of poly-Si TFTs is strongly influenced by grain size, grain boundary and intragranular defects [10]. To obtain bigger grains, better performance, lower process temperature and lower cost, we have studied some recrystallization technology such as: solid-phase crystallization (SPC) [11], eximer laser annealing (ELA) [12]-[14], metal-induced lateral crystallization

(MILC) [15]-[17], rapid thermal annealing (RTA) [18], and microwave crystallization [19] etc. In my thesis, the poly-Si TFTs were crystallized by SPC methods.

Recently, many device architectures which are different from the conventional self-aligned source/drain structure have been studied to enhance TFT performance and reliability, such as offset gate [20][21], gate-overlapped LDD [22]-[24], lightly doped drain (LDD) [25]-[26], multi-channel structure [27]. In the following sections, we will discuss some useful device architectures and make a simply description of the reason that they enhance LTPS TFTs' parameters such as on/off current ratio, subthreshold swing and field-effect mobility[28].

1.2 Several Novel High Performance Structures for LTPS TFTs

In general, poly-Si TFTs have two different structures: top-gate coplanar structure and bottom-gate structure. The top-gate TFTs have mainly used in AMLCD applications because their self-aligned source/drain regions provide low parasitic capacitances and is suitable for device scaling down. On the other hand, although bottom-gate TFTs have better interface, higher plasma hydrogenation rate, higher circuit density and improved topography [29][30] than top-gate TFTs, they have lower current and need extra process steps for backside exposure and difficult fabrication.

The dominant leakage current mechanism in poly-Si TFTs is the field emission via grain boundary traps by a high electric field near the drain [31]. Therefore, reducing the lateral electric field near the drain junction is required. Today, many device structures have been proposed to improve poly-Si TFTs performance. For example, the lateral electric field can be reduced by using a lightly doped drain (LDD) structure [25][26]. However, LDD structure indeed reduced the electric field but also introduces high source/drain series resistance which limits the on-state current.

Besides, an extra mask in LDD structures is a major problem. Thus, how to reduce off-state current without degrade on-state current too much is a trade-off.

Super-thin channel, for example 200Å, poly-Si TFTs are reported to have higher current drive compared to their thicker film counterparts [32] [33]. However, thin-film devices experience a high electric field at the channel/drain junction region when the device is operated in the saturation region. It exhibited a high electric field due to two-dimensional effect arises from the reduced junction depth compared to thicker film devices [34] [35]. This increase in lateral electric field causes anomalous leakage current at zero and negative gate bias regime and is a serious problem in poly-Si TFT [36][37]. Further more, this high electric field is the major cause of impact ionization at the channel/drain junction region, which results in the accumulation of holes in the floating body of the device [38][39]. This hole accumulation causes a profound kink effect in the I-V characteristics of thin-film devices, which in turn deteriorates the output characteristics and reduces the gain of the transistors [40]. In addition, the kink effect also causes the avalanche induced short channel effect which places a limitation on scaling down of the device size. Thus, the kink effect is a serious problem in poly-Si TFTs for analogue circuit application in large area microelectronics [41]. Recently, a study on the influence of lateral electric field on the anomalous leakage current and kink effect of poly-Si TFT has been reported [42]. It was found that the high lateral electric field at the channel/drain junction can be effectively reduced by use of a thick drain but thin channel structure. In my thesis, I will use a different fabrication to realize a novel structure with a thick S/D and a thin channel.

1.3 Reliability Issues in LTPS TFTs

Under the long-term operation, to raise the stability of device characteristics is more indispensable. As a result, the reliability of LTPS TFTs must be taken into

consideration when they are applied to advanced circuitry such as data-driver in AMLCDs or driving elements in AMOLEDs. The special processes used in the fabrication of LTPS TFTs and nature properties of crystallized poly-Si channel make the reliability issues in LTPS TFTs different from those in the conventional MOSFETs.

We usually deposit the gate oxide film by CVD method at low temperature. To be compared with high-temperature thermal grown oxide which is used in MOSFETs, it always exhibits poor physical and electrical quality, such as high gate leakage current, low breakdown voltage, and low density.

The surface roughness of poly-Si film will enhance the local electrical field near the interface between gate oxide and channel, which will also degrade the reliability of TFT under high gate bias operation.

The hot carrier effects have been widely investigated in MOSFETs. Meanwhile, it is also another important reliability issue in LTPS TFTs.

1.4 motivations

Poly-Si TFTs are mainly used for pixel switching controller in AMLCDs, so increasing on/off ratio is an important target of our study. In order to improve on/off ratio, we try to decrease the off-state current and increase the on-state current. In other studies, we know that thickened source and drain can help reduce the lateral electric field near the drain junction and then reduce the off-state current. Therefore, we combine thick S/D and thin channel to obtain better characteristic. In the fabrication process, I also omit a step of depositing an amorphous-Si film to lower the cost. Furthermore, we don't need an additional mask to define a raised source and drain.

1.5 Thesis Organization

In chapter 1, a brief overview of LTPS TFT technology and related applications were introduced.

In chapter 2, the fabrication process flow of the novel TFT device, experimental recipes, and device parameter extraction methods will be described. We also show the SEM image of our novel structure.

In chapter 3, we will show the electrical property of the novel poly-Si TFT device, includes transfer characterization, output characterization, the symmetry, and different ovelap-length LTPS TFTs.

Finally, conclusions and future work as well as suggestion for further research are given in chapter 4.

Chapter 2

Experimental of Low-Temperature Poly-Si TFTs with thin channel and thick S/D

2.1 The Fabrication Process flow of Low-temperature Poly-Si TFTs

The poly-Si TFTs were fabricated on 4-inch-diameter p-type silicon wafer. Fig.2-1 shows the process flow of unhydrogenation poly-Si TFTs. The 120 nm undoped amorphous silicon (a-Si) films were initially deposited on 500 nm thermally oxidized silicon (100) wafers by low-temperature chemical vapor deposition (LPCVD) system with silane (SiH_4) gas at 550°C. The deposition pressure was 100mtorr and the silane flow rate was 40 sccm.

After the lithography step, we used poly-RIE system to etch the α-Si film. We left 400Å-α-Si for the channel, then the solid phase crystallization (SPC) process was carried out with 600°C, 24 hours. A 40 nm-thick TEOS oxide film was deposited at 350°C to serve as the gate dielectric by PECVD. Then, a 300 nm-thick poly-Si was deposited by LPCVD at 620 °C with SiH_4 for the gate electrode. Gate areas were patterned and S/D region were over-etched about 40 nm. Then the regions of source, drain, and gate electrode were doped by a self-aligned 5E15 ions/cm^2 phosphorus implantation with a He-diluted PH_3 gas, at 50Kev of acceleration voltage. The dopants were activated at 600°C in N_2 ambient for 24 hours. Next, a 450 nm oxide was deposited by PECVD at 350°C as a passivation layer, and contact lithography was carried out. After opening contact holes, a 650 nm Al was deposited by evaporation and the metal layer was patterned. Finally, the samples were sintered at 400°C for 30 minutes in N_2 gas ambient.

In Fig.2-2, we also fabricated conventional poly-Si TFTs to compare with our novel structure in the same run.

The detailed fabrication process flows are listed as follow.

1. (100) orientation Si wafer
2. initial cleaning
3. thermal wet oxidation at 1050°C to grow 500nm thermal SiO_2 in furnace
4. 120nm a-Si was deposited by LPCVD at 550°C in SiH_4 gas
5. Mask#1: define S/D
6. 80nm α-Si dry etch by Poly-RIE system , to leave 40nm to be channel
7. SPC was carried out with 600°C, 24hrs
8. RCA cleaning
9. 40nm gate dielectric deposition by PECVD at 350°C
10. 300nm poly-Si was deposited by LPCVD at 620°C in SiH_4 gas
11. Mask#2: Define gate regions
12. Poly-Si dry etch by Poly-RIE system, S/D need to be over-etched 40nm
13. Ion implantation: P^{31}, 50Kev, 5e15 ions/cm^2
14. Dopant activation in N_2 ambient at 600°C for 24hrs in furnace
15. 450nm oxide was deposited by PECVD as passivation layer
16. Mask#3: Open contact holes
17. 650nm Al thermal evaporation
18. Mask#4: Al pattern defined
19. Etching Al and removing photoresist
20. Al sintering at 400°C in N_2 ambient for 30 minutes

2.2 The design of the Poly-Si TFTs with thick S/D and thin channel

The top-view of the proposed structure of poly-Si TFTs is shown in Fig.2-3. In the Fig.2-3, we can clearly see the symbol such as gate length, gate width, contact hole, overlap region etc. and easily find the difference between conventional TFTs and proposed structures of TFTs, and the overlap region will be discussed in the thesis.

Fig.2-4 shows the A—A' cross-section from Fig.2-3, this part is like to the fabrication process figure.

Fig.2-5 shows the B—B' cross-section from Fig.2-3, it was difference for proposed and conventional ones. The gate mask width of the proposed structure (W') is larger than that of the conventional sample. Notice that, the active region would be formed under the whole of the gate region.

Fig.2-6 shows the I_{sub} in our novel structure of TFTs.

2.3 Methods of Device Parameter Extraction

Many methods have been proposed to extract the characteristic parameter of poly-Si TFT. In this section, the methods of parameter extraction used in this research are described.

2.3.1 Determination of Threshold Voltage (V_{th})

The threshold voltage V_{th} is an important MOSFET parameter required for the channel length-width and series resistance measurement. However, V_{th} is a voltage that is not uniquely defined. Various definitions exist and the reason for this can be

found in the I_D-V_{GS} curves. One of the most common threshold voltage measurement techniques is the linear extrapolation method with the drain current measured as a function of gate voltage at a low drain voltage of typically 50-100 mV to ensure operation in the linear MOSFET region [43]. But the drain current is not zero below threshold and approaches zero only asymptotically. Hence the I_D verus V_{GS} curve is extrapolated to I_D=0, and the threshold voltage is determined from the extrapolated or intercept gate voltage V_{GSi} by

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \qquad \text{(Eq. 2.1)}$$

Equation (2.1) is strictly only valid for negligible series resistance. Fortunately series resistance is usually negligible at the low drain currents where threshold voltage measurement is made. The I_D-V_{GS} curve deviate from a straight line at gate voltage below V_{th} due to subthreshold currents and above V_{th} due to series resistance and mobility degradation effects. It is common practice to find the point of maximum slope on the I_D-V_{GS} curve by maximum in the transconductace fit a straight line to the I_D-V_{GS} curve at that point and extrapolate to I_D=0.

2.3.2 Determination of Subthreshold Swing

Subthreshold swing S.S (V/dec) is a typical parameter to describe the control ability of gate toward channel. That is the turn on/off speed of a device. It is defined as the amount of gate voltage requires increase/decrease drain current by one order of magnitude.

The subthreshold swing should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to short channel effect such as charge sharing, avalanche multiplication, and

punchthrough effect. The subthreshold swing is also related to gate voltage due to undesirable and inevitable factors such as serial resistance and interface state.

In my thesis, the subthreshold swing is defined as one-third of the gate voltage required to decrease the threshold current by three orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to threshold voltage.

2.3.3 Determination of Field Effect Mobility (μ_{FE})

Usually, μ_{FE} is extracted from the maximum value of transconductance ($\mathbf{g}_m$) at low drain bias (V_{DS}=1V). The drain current in linear region ($V_{DS} < V_{GS}-V_{th}$) can be approximated as the following equation:

$$I_{DS} = \mu_{FE} C_{ox} (\frac{W}{L})[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^{2}] \qquad \text{(Eq. 2.2)}$$

Where W and L are width and length, respectively. C_{ox} is the gate oxide capacitance. Thus, g_m is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} C_{ox} (\frac{W}{L}) V_{DS} \qquad \text{(Eq. 2.3)}$$

Therefore,

$$\mu_{FE} = \frac{L}{C_{ox} W V_{DS}} g_{m(\max)}\Big|_{V_{DS}\to 0} \qquad \text{(Eq. 2.4)}$$

2.3.4 Determination of On/Off Current Ratio

On/Off current ratio is one of the most important parameters of poly-Si TFTs

Since a good performance means not only large On current but also small Off (leakage) current. The leakage current mechanism in poly-Si TFTs is not like it in MOSFET. In MOSFET, the channel is composed of single crystalline and the leakage current is due to the tunneling of minority carrier from drain region to accumulation layer located in channel layer region. However, in poly-Si TFTs, the channel is composed of poly crystalline. A large amount of trap densities in grain structure attribute a lot of defect state in energy band gap to enhance the tunneling effect. Therefore, the leakage current due to the tunneling effect is much larger in poly-Si TFTs than in single crystalline devices. When the voltage drops between gate voltage and drain voltage increase, the band gap width decrease and the tunneling effect becomes much more severe. Normally we can find this effect in typical poly-Si TFT I_D-V_G characteristics where the magnitude of leakage current will reach a minimum and then increase as the gate voltage decrease/increase for n/p-channel TFTs.

There are a lot of ways to specify the On and Off current. In my thesis, take n-channel poly-Si TFTs for examples, the On current and Off current is defined as the drain current when gate voltage equal to 15V and drain voltage is 1 V(linear operation mode). The Off current is specified as the minimum leakage current in linear operation mode for usual cases.

$$\frac{I_{ON}}{I_{OFF}} = \frac{Maximum\ \ current\ \ of\ \ I_{DS}-V_{GS}\ \ plot\ \ at\ \ V_{DS}=1V}{Minimum\ \ current\ \ of\ \ I_{DS}-V_{GS}\ \ plot\ \ at\ \ V_{DS}=1V} \qquad \text{(Eq. 2.5)}$$

2.4 The introduction of SEM and the device picture

2.4.1 Scanning Electron Microscope (SEM) System

The operation of the SEM consists of applying a voltage between a conductive sample and filament, resulting in electron emission from the filament to the sample. This occurs in a vacuum environment ranging from 10^{-4} to 10^{-10} Torr. The electrons are guided to the sample by a series of electromagnetic lenses in the electron column. A schematic of a typical SEM is show if Fig.2-5. The resolution and depth of field of the image are determined by the beam current and the final spot size, which are adjusted with one or more condenser lenses and the final, probe-forming objective lenses. The lenses are also used to shape the beam to minimize the effects of spherical aberration, chromatic aberration, diffraction, and astigmatism.

The electrons interact with the sample within a few nanometers to several microns of the surface, depending on beam parameters and sample type. Electrons are emitted from the sample primarily as either backscattered electrons or secondary electrons. Secondary electrons are the most common signal used for investigations of surface morphology. They are produced as a result of interactions between the beam electrons and weakly bound electrons in the conduction band of the sample. Some energy from the beam electrons is transferred to the conduction band electrons in the sample, providing enough energy for their escape from the sample surface as secondary electrons. Secondary electrons are low energy electrons (<50eV), so only those formed within the first few nanometers of the sample surface have enough energy to escape and be detected. High energy beam electrons which are scattered back out of the sample (backscattered electrons) can also form secondary electrons when they leave the surface. Since these electrons travel farther into the sample than the secondary electrons, they can emerge from the sample at a much larger distance away from the impact of the incident beam which makes their spatial distribution larger. Once these electrons escape from the sample surface, they are typically detected by an Everhart-Thornley scintillator-photomultiplier detector. The SEM

image formed is the result of the intensity of the secondary electron emission from the sample at each *x,y* data point during the rastering of the electron beam across the surface.

2.4.2. Scanning Electron Microscope (SEM) analysis

Fig.2-7 shows the novel structure of a poly-Si TFT, we realized the structure with thick S/D and thin channel. We could clearly see the raised overlap-region, gate oxide, passivation layer, thermal oxide and the silicon substrate.

Chapter 3

The Electrical Property of LTPS TFTs with thick S/D and thin channel

In this chapter, we will discuss the device performance and reliability of our novel structure of poly-Si TFTs, and also compare with the conventional TFTs. We measured the thickness of the films by n&k analyzer, and the I-V characteristics of poly-Si TFTs by HP4156 semiconductor parameter analyzer.

3.1 The Characterization of Low-Temperature Poly-Si TFTs with thick S/D and thin channel compared with the conventional TFT's

Fig.3-1~Fig.3-4 show the proposed structure's I_{ds}-V_{gs} transfer characteristics. The symbols L, W, T_{ox}, and T_{si} represent the gate length, gate width, gate-oxide thickness, and channel poly-Si thickness, respectively, and the measured effective mobility (μ_{eff}), subthreshold swing (S), and threshold voltage (V_t) of a device are listed in Table. For example, the subthreshold swing, and the effective mobility of the device (L=20 μm, W=50 μm) is 1.1 V/dec, 13.1 cm^2/V-S), respectively. From the Figures and tables, we can know the preliminary performance of our proposed structure.

Fig.3-5~Fig.3-6 show the measured current-voltage (I_d-V_d) characteristics of the proposed structure of poly-Si TFT and the conventional ones. The proposed structure has a good performance, and don't have obvious kink effect when being applied for high voltage. (~50V), to be compared with conventional TFTs. On the side, the conventional TFTs have a kink point at V_{ds} = 13V for W/L = 50 μm/20 μm, and a kink

point at V_{ds} = 20V for W/L = 10 μm/10 μm. The reason which alleviates the kink effect is mentioned before, the proposed structure has a thick S/D to reduced the lateral electric field near drain junction, so in relation with alleviating the kink effect when applied high voltage.

Fig.3-7~Fig.3-10 show the proposed structure and conventional TFTs' I_{ds}-V_{gs} transfer characteristics. We have fabricated two different thickness of channel of conventional TFTs. Fig.2-2 shows the conventional structure of poly-Si TFT. Conventional-A TFT is for 400Å-thick channel, and convention-B TFT is for 1200Å-thick channel, and the conventional fabrication process's condition is always like the proposed structures. Compared with conventional-A TFT, the proposed structure have a slightly higher on-state current and a much lower off-state current. In some studies, it is well known that the dominant leakage current mechanism in poly-Si TFTs is the field emission via grain boundary traps by a high electric field near the drain side, and it is believed that the thick drain region would have lower the lateral electric field near drain junction [45][46][47]. Therefore, in our proposed structure, an 800A-thick S/D and a thinner channel-400A were formed; the lateral electric field near the drain junction would be reduced. So, the off-state current would be decreased. In addition, we would see the top-view of proposed structure of poly-Si TFTs in Fig.2-6. As shown in figure 2-6, the active area width (W') of the proposed structure is longer than that of the conventional TFT (W). Therefore, the proposed structure has another path for current flowing than the conventional one; we called the extra current as I_{sub}. So, the fact that the current of the proposed structure is higher than that of the conventional one is expected. Furthermore, we consider the I_{sub} have a significant influence of our novel structure, especially at smaller size such as W/L = 10 μm/10 μm, 10 μm /20 μm etc. We will further discuss about this section later. The other reason for increased on-state current is the good contact of S/D. Because of the

thick S/D, we obtain a lower S/D resistance, and it indeed increases the on-state current.

Compared with conventional-B TFT, the on-state current and off-state current of proposed structure are both substantially improved. The channel thickness and source/drain region thickness of the conventional-B TFT are the same. It is because that the thick channel is used to obtain the lower on-state current and higher off-state current [48].

We have measured the current on/off ratio (maximum on-state current/ minimum off-state current), subthreshold swing (S), and threshold voltage (V_{th}), both the proposed and the conventional structures, listed at Table.

Fig.3-11 shows the I_d-V_{gs} transfer characteristics of the proposed structure of poly-Si TFTs of different widths such as W/L = 10 μm /10 μm and W/L = 50 μm /10 μm, and Fig.3-12 is the conventional one for different widths. From these figures, we can obtain that the on-state current of the proposed structure is increasing about 4.84 times from W = 10 μm to W = 50 μm, and the on-state current of the conventional TFT is increasing about 9.96 times from W = 10 μm to W = 50 μm. It indicated that the increasing rate of conventional TFTs is higher than the proposed ones as increasing the width length. It would be expected when we consider the existence of I_{sub}. The effect of increasing on-state current for I_{sub} will be alleviated when the width length is higher. It is because that, at the higher width length such as W = 50 μm, the channel carriers were mainly transferred in main channel. Therefore, the influence of I_{sub} is not noticeable.

3.2 The symmetry of the Low Temperature Poly-Si TFTs with thick S/D and thin channel

The bidirectional transfer characteristics of a proposed structure of TFT with the source and drain reversed are shown in Fig.3-13. The different sizes of the proposed structure are shown in Fig.3-14~Fig.3-16, respectively. When we measured the reverse mode of proposed structures, we changed the source and drain by each other, this would let us know the symmetry of the proposed structure as well as the device performance variation. From Fig.3-14~Fig.3-16, we would see the perfect symmetry at different size such as W/L = 50 μm /10 μm, W/L = 10 μm /20 μm, W/L = 50 μm /20 μm, but in Fig.3-13, we found the off-state current of the reverse mode is slightly higher than that of the forward mode. We believed it is the misalignment resulted from the lithography step affected the off-state current. In the gate mask step, we would have a misalignment error about 0.5~1 μm, it resulted in different overlap-length regions. As we know, the longer overlap-length region would have more traps in the film, and this effect is more remarkable at high negative voltage.

3.3 The Characterization of different overlap-length of LTPS TFTs with thick S/D and thin channel

Fig.3-17~Fig.3-20 show the different overlap-length of the proposed structure. The overlap-length of L1, L2, L3 for W/L = 50 μm/10 μm is 1.0 μm, 1.2 μm, 1.5 μm, respectively, and it is the same for W/L = 10 μm/10 μm. And the overlap-length of L1, L2, L3 for W/L = 50 μm/20 μm is 1.5 μm, 2.0 μm, 2.5 μm, respectively, and it is the same for W/L = 10 μm/20 μm. From Fig.3-17~Fig.3-20, we can see that the smaller

overlap-length would have better performance in all cases.

The proposed structure has a disadvantage that there were more traps in the gate-overlap region, to be compared with conventional TFTs, and it is well known that the traps would reduce the on-state current. Therefore, we could expect that the on-state current of the shortest gate-overlap length structure would be the highest.

When device was applied at negative high voltage, the leakage mechanism is dominant by traps in the inversion layer, and there were more traps in the larger gate-overlap region. Therefore, the off-state current of the longer gate-overlap length would be higher.

Fig.3-21 shows the current on/off ratio of different gate-overlap length TFTs. It has a remarkable trend that the shorter overlap-length TFTs has better current on/off ratio. The similar result could be seen in Fig.3-22, the off-state current is lower when the gate-overlap length is shorter.

Chapter 4
Conclusions and Future works

4.1 Conclusions

In this thesis, we have introduced a novel structure of poly-Si TFT with thick S/D and thin channel, it can help us obtain better performance such as current on/off ratio, higher mobility, and also suppress the kink effect, to be compared with conventional TFTs. In the fabrication process, we omit a step of depositing amorphous-Si, and don't need an extra mask to define source and drain. In order to prevent the misalignment in the lithography steps and over-etched the channel, we design a gate-overlap region. In this thesis, we also showed that the smaller gate-overlap region will have better performance. In our measurement, our structure also has great symmetry.

Therefore, the novel structure of thick S/D and thin channel exhibits significantly superior electrical characteristics to the conventional poly-Si TFTs. Hence, the proposed high performance Poly-Si TFTs are promising for the application of integrated circuits on LCD panel.

4.2 Future Works

We have proposed a low-temperature Poly-Si TFTs with thick S/D and thin channel to improve conventional low-temperature Poly-Si TFTs performance. However, in order to further improve device electrical characteristics and apply to glass substrates, there will be still some works worth of being investigated.

In our experiment, we design an overlap-region to prevent the channel broken when we define the gate. However, the overlap-region would affect the device performance. It is expected that in some advanced laboratories the overlap-region will be reduced to the minimum, and the performance won't be affected remarkable. We also try to combine the LDD structure into our proposed structure to obtain good electric characteristic and it will be realized soon.

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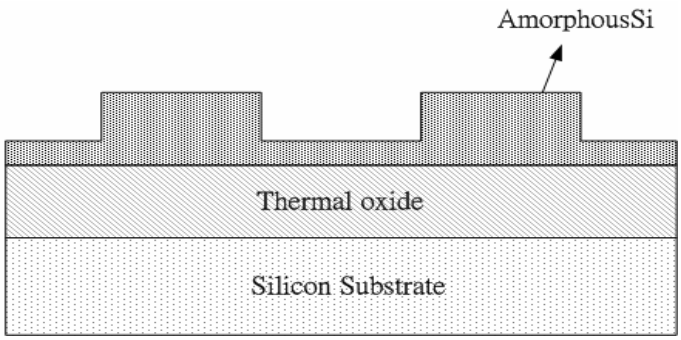
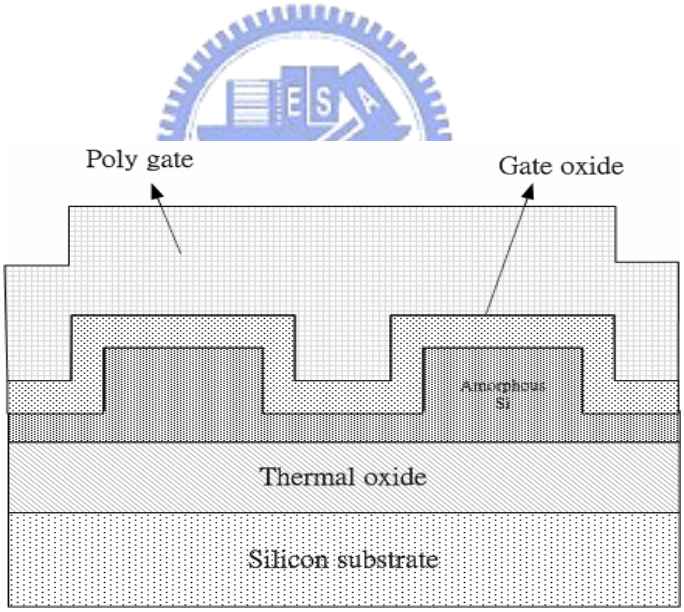
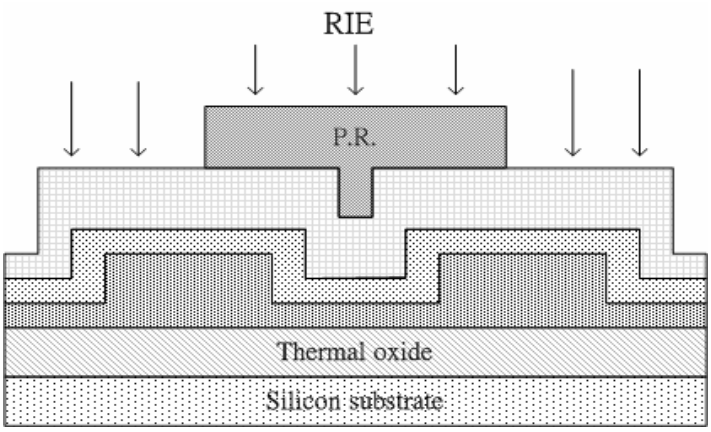


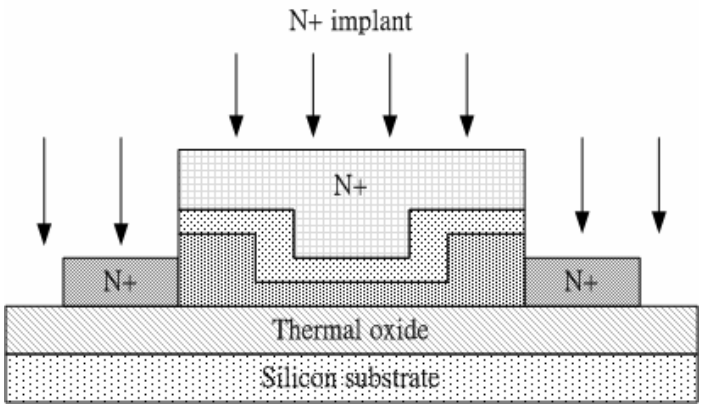
(a) LPCVD a-Si, define active layer, recrystallization



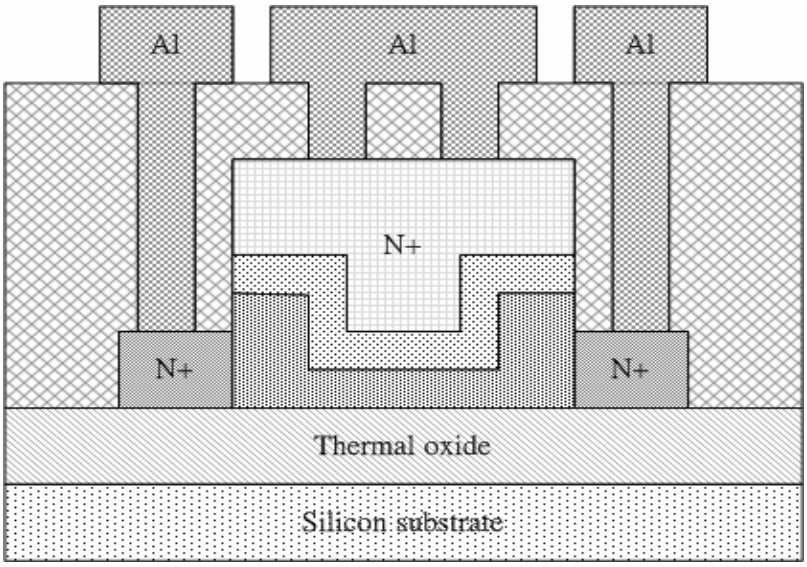
(b) Deposit SiO2 dielectric by PECVD and poly gate by LPCVD



(c) define poly-Si gate



(d) ion implantation (self-align) and dopant activation



(e) deposit PECVD TEOS oxide as passivation layer, and define contact holes and Al electrode

Fig. 2-1 Process flow of fabricating LTPS n-channel poly-Si TFTs with thick S/D and thin channel

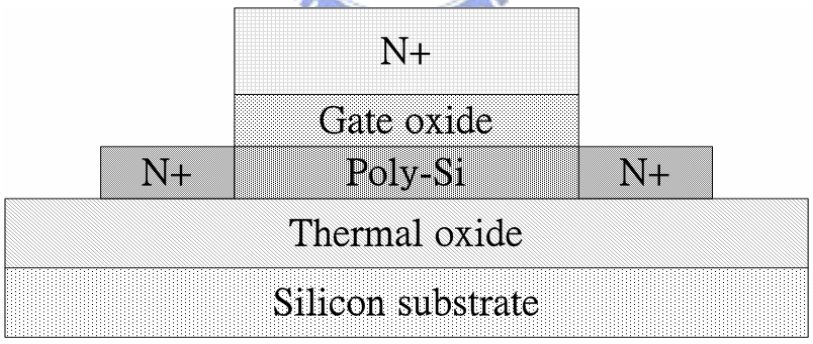


Fig. 2-2 The conventional TFT

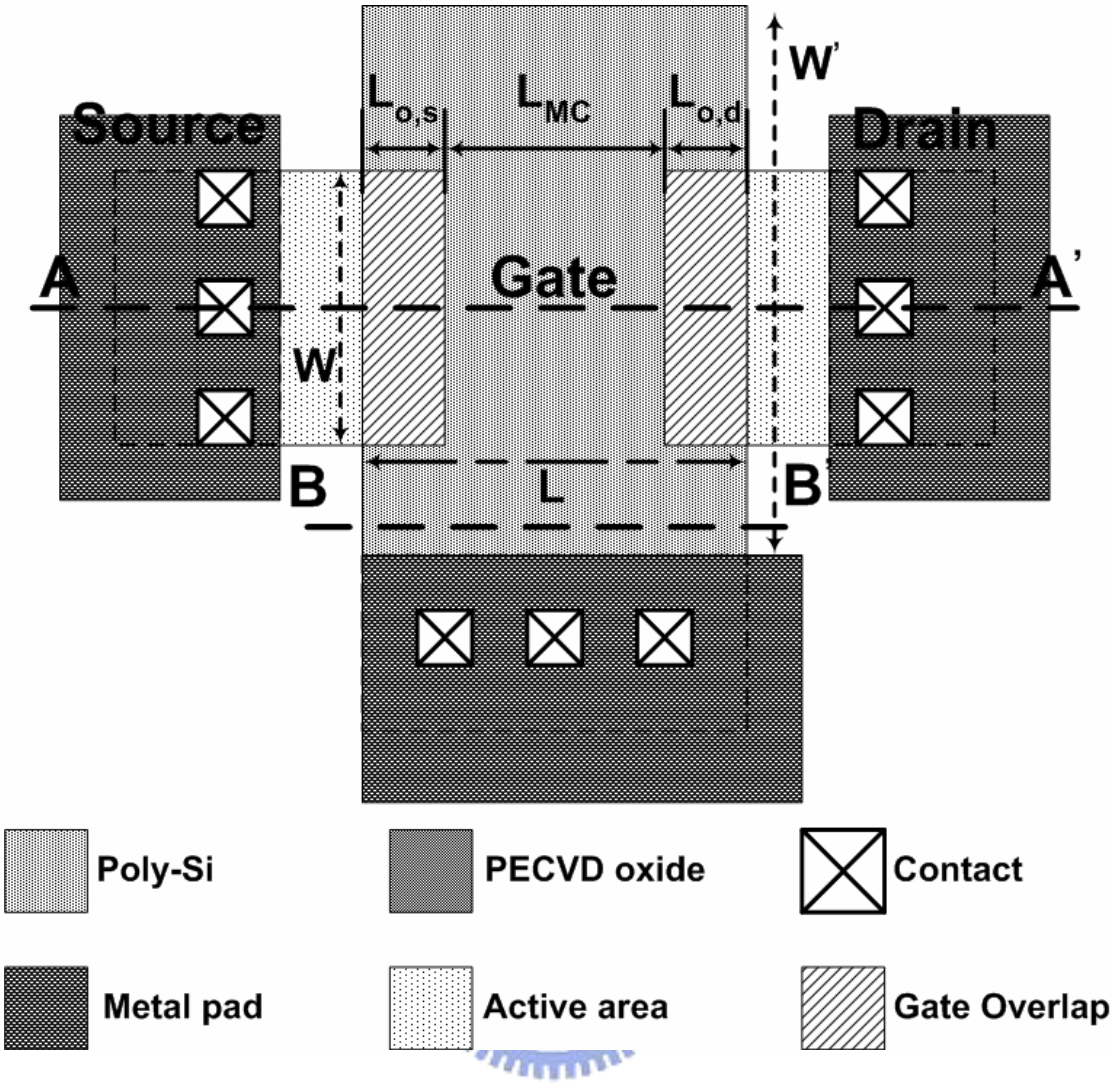


Fig.2-3 The top-view of the proposed structure.

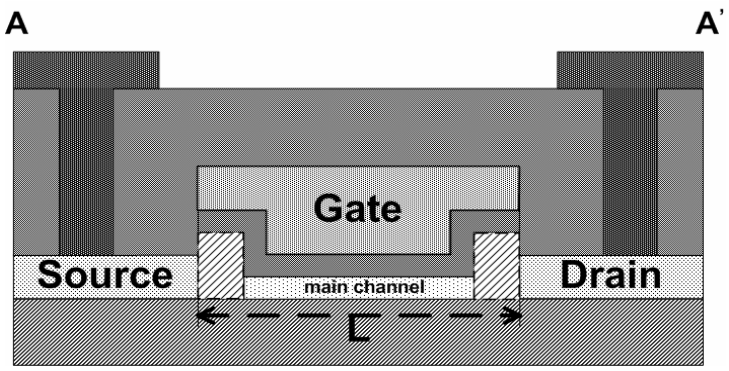


Fig.2-4 The A--A' cross-section of the Fig.2-3.

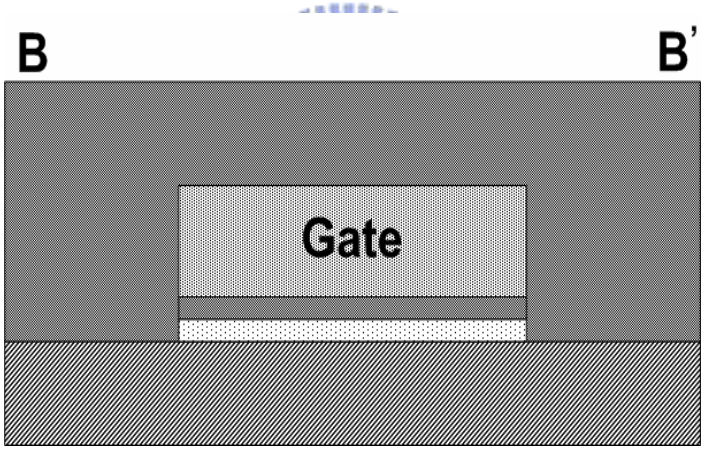


Fig.2-5 The B—B' cross-section of the Fig.2-3.

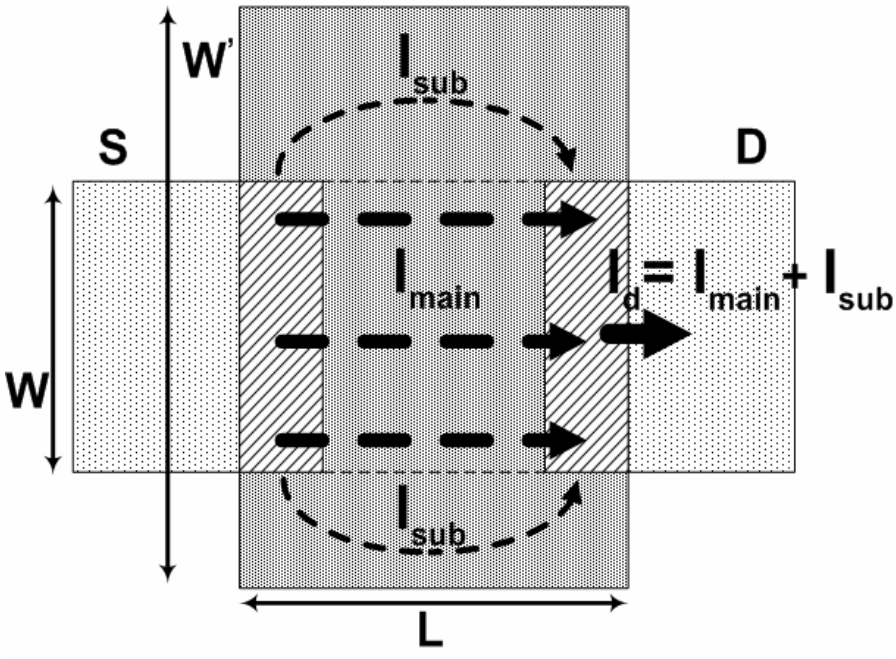


Fig.2-6 the current flows of the proposed structure.

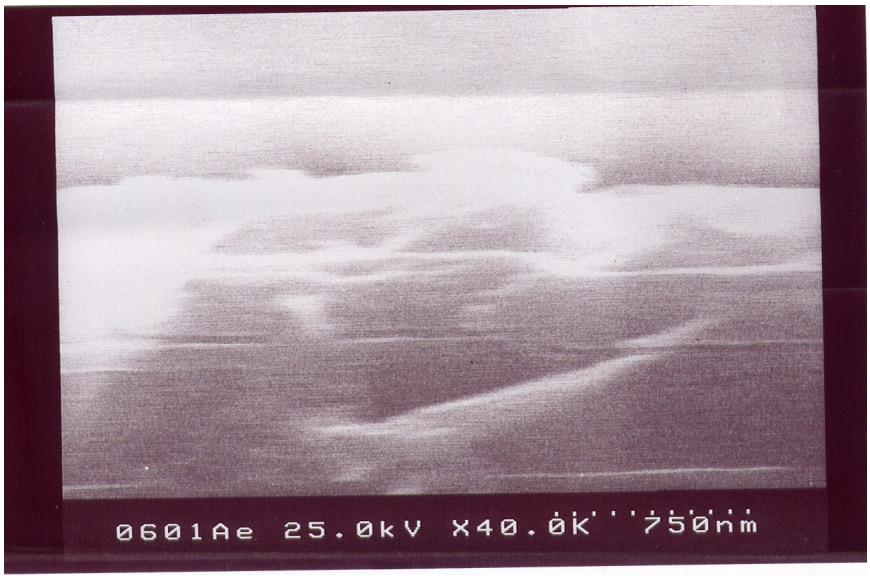


Fig.2-7(a) The SEM image of the proposed structure

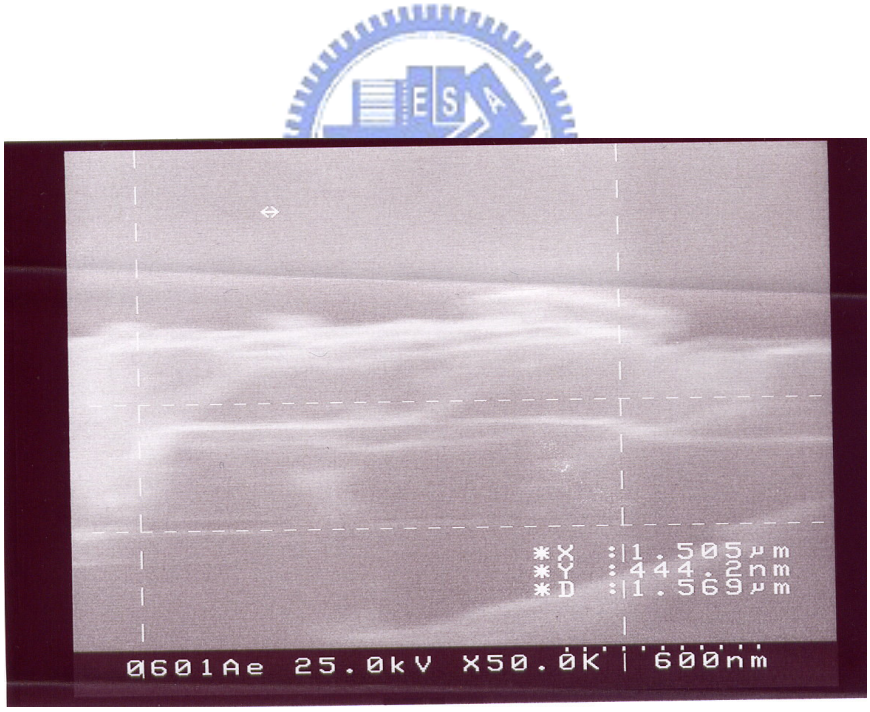


Fig.2-7(b) The SEM image of the proposed structure

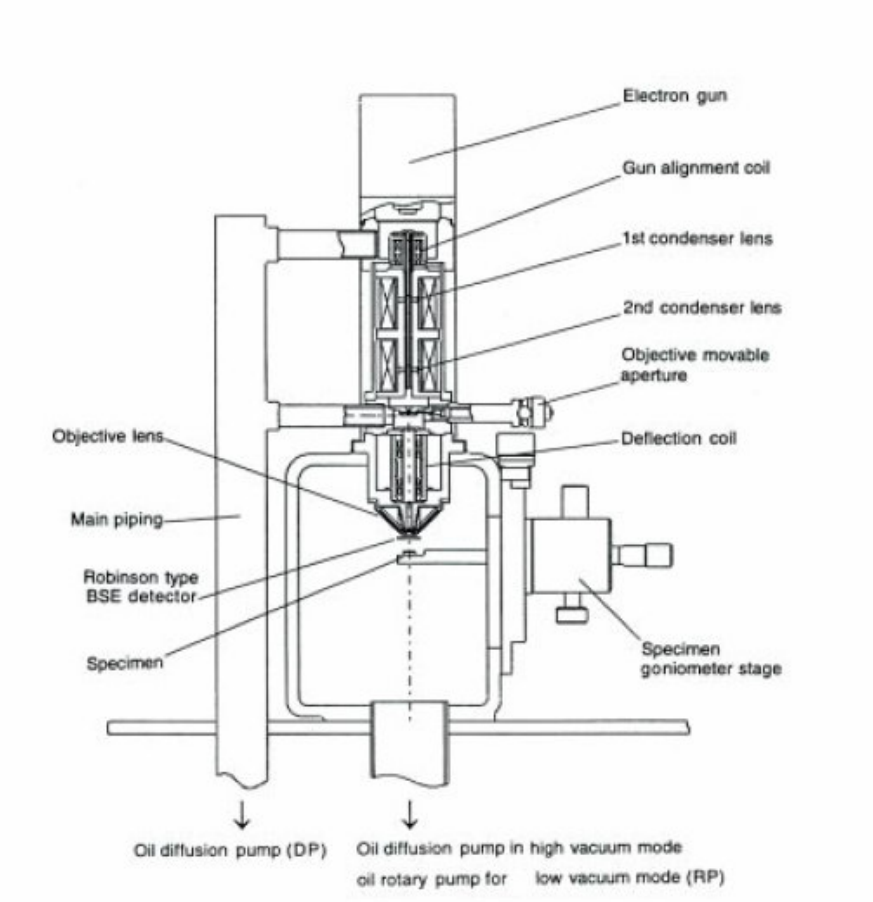


Fig.2-8 Schematic of the primary components of a typical SEM.

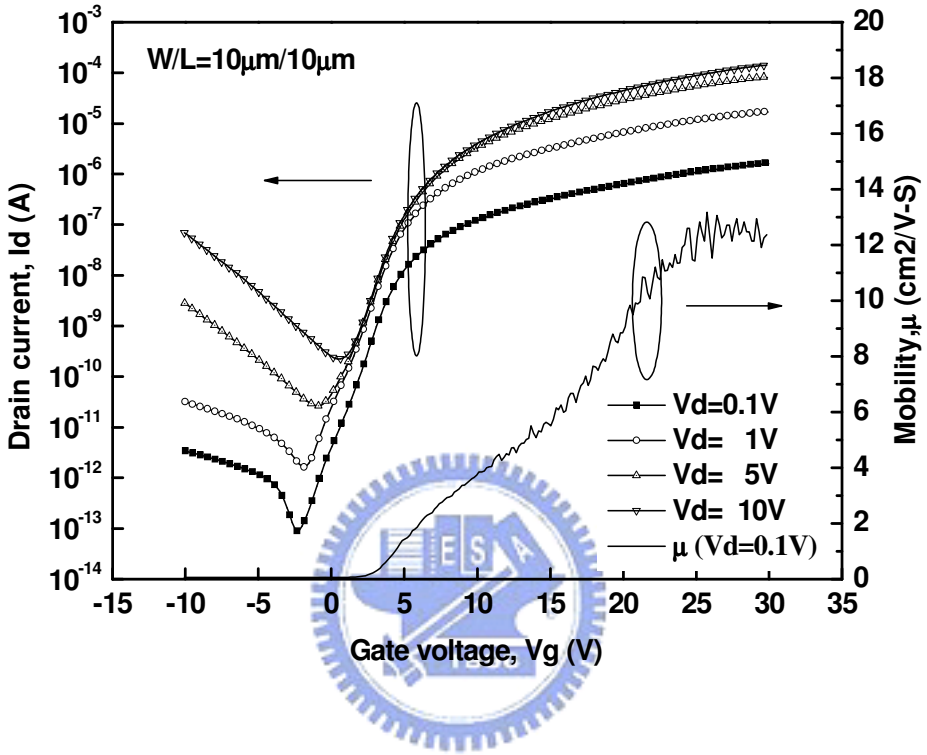


Fig.3-1 I_d-V_g transfer characteristics and the effect mobility of the proposed structure of LTPS TFT; W/L = 10 μm/10 μm.

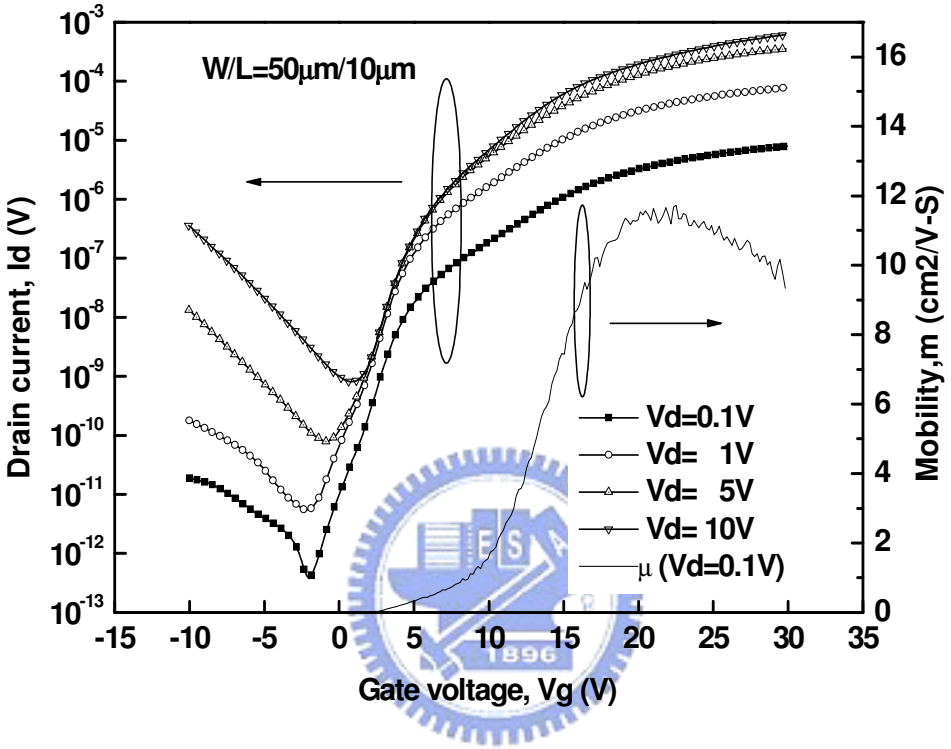


Fig.3-2 I_d-V_g transfer characteristics and the effect mobility of the proposed structure of LTPS TFT; W/L = 50 μm/10 μm.

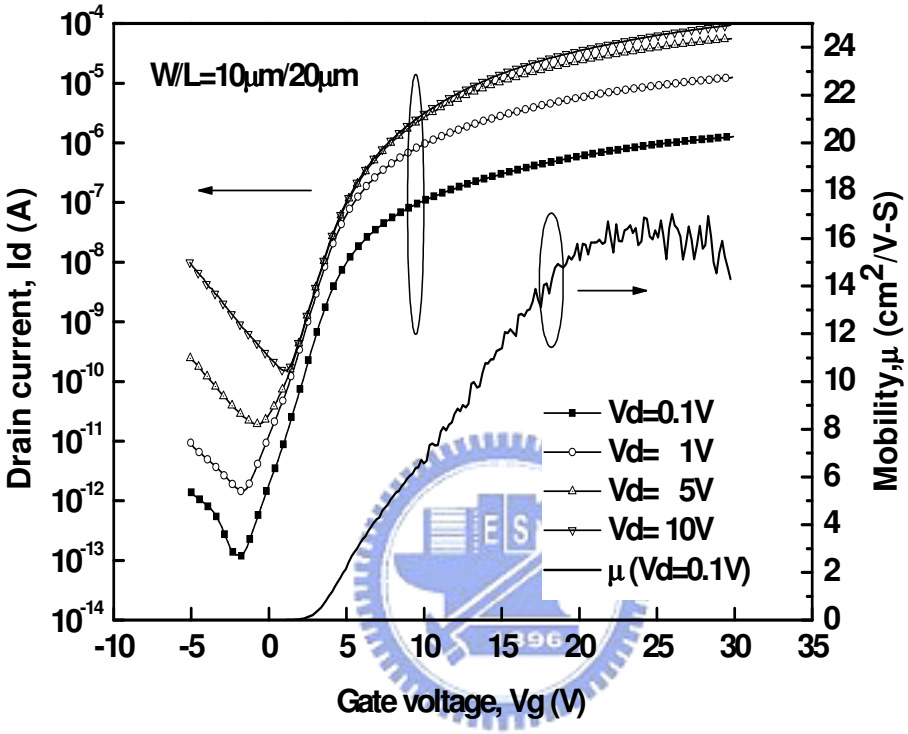


Fig.3-3 I_d-V_g transfer characteristics and the effect mobility of the proposed structure of LTPS TFT; W/L = 10 μm/20 μm.

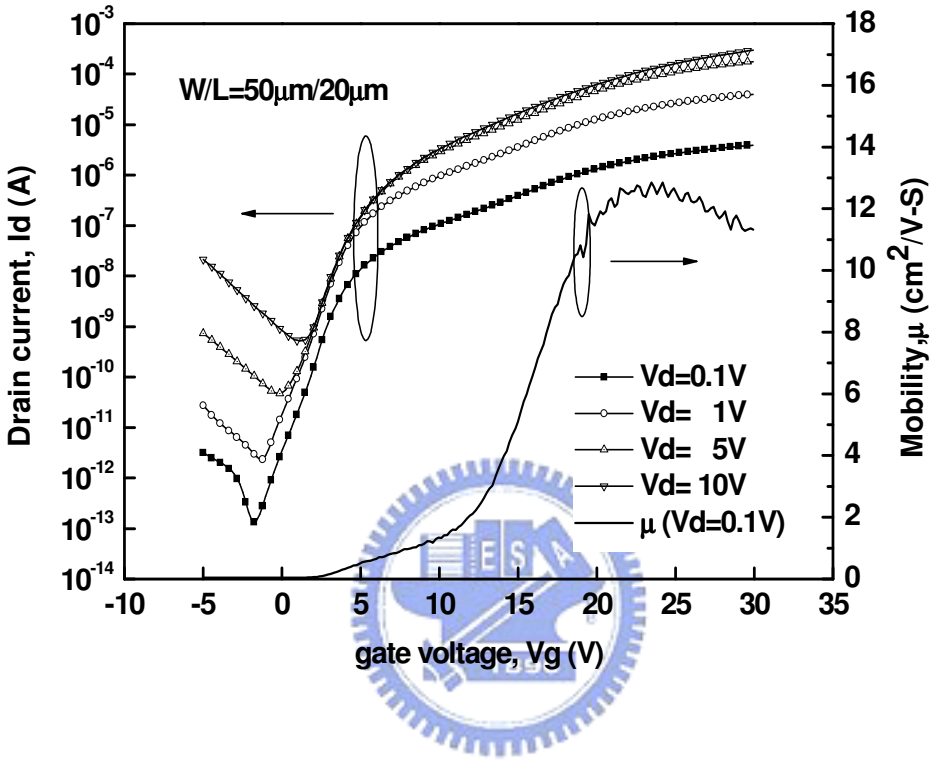


Fig.3-4 I_d-V_g transfer characteristics and the effect mobility of the proposed structure of LTPS TFT; W/L = 50 μm/20 μm.

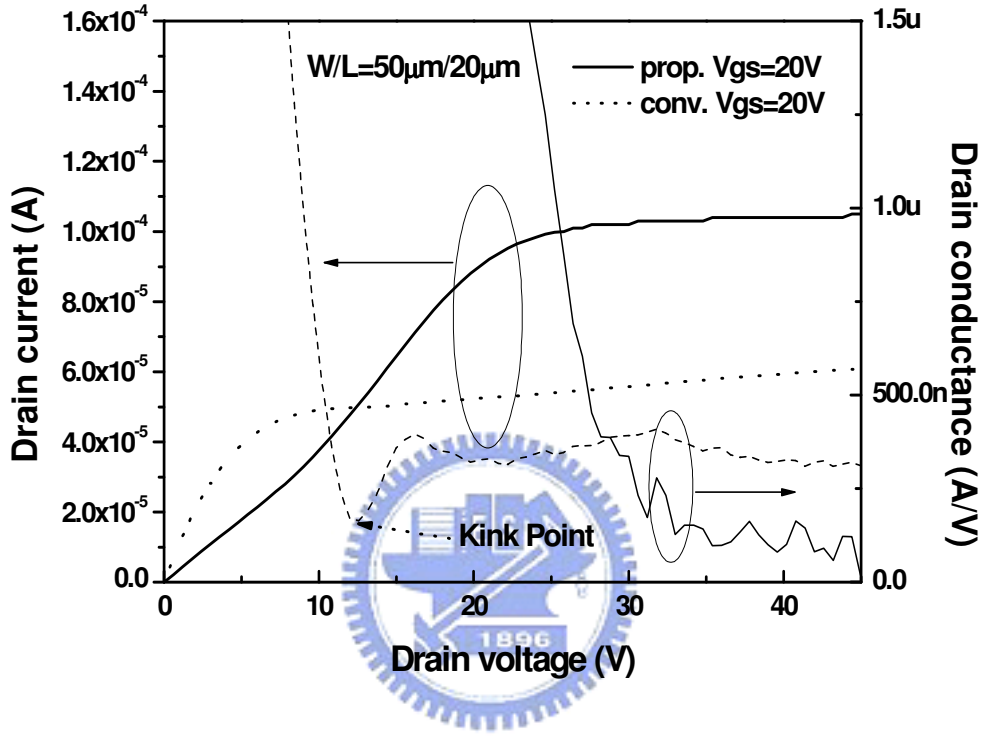


Fig.3-5 I_d-V_d output characteristics of proposed structure and conventional structure of TFTs; W/L = 50 μm/20 μm.

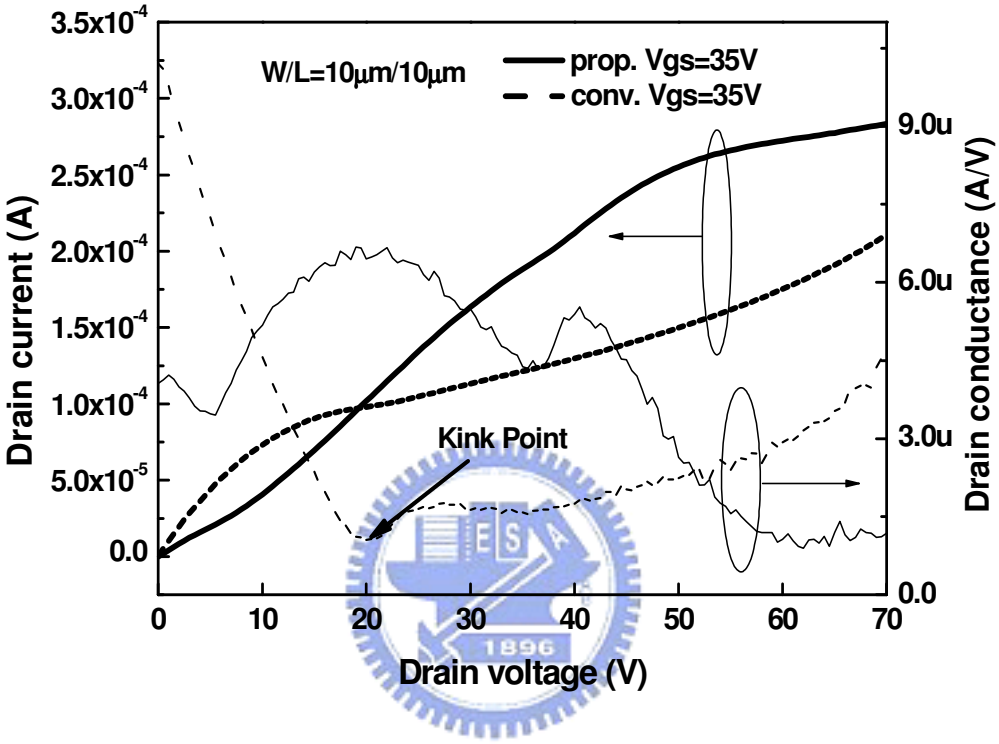


Fig.3-6 I_d-V_d output characteristics of proposed structure and conventional structure of TFTs; W/L = 10 μm/10 μm.

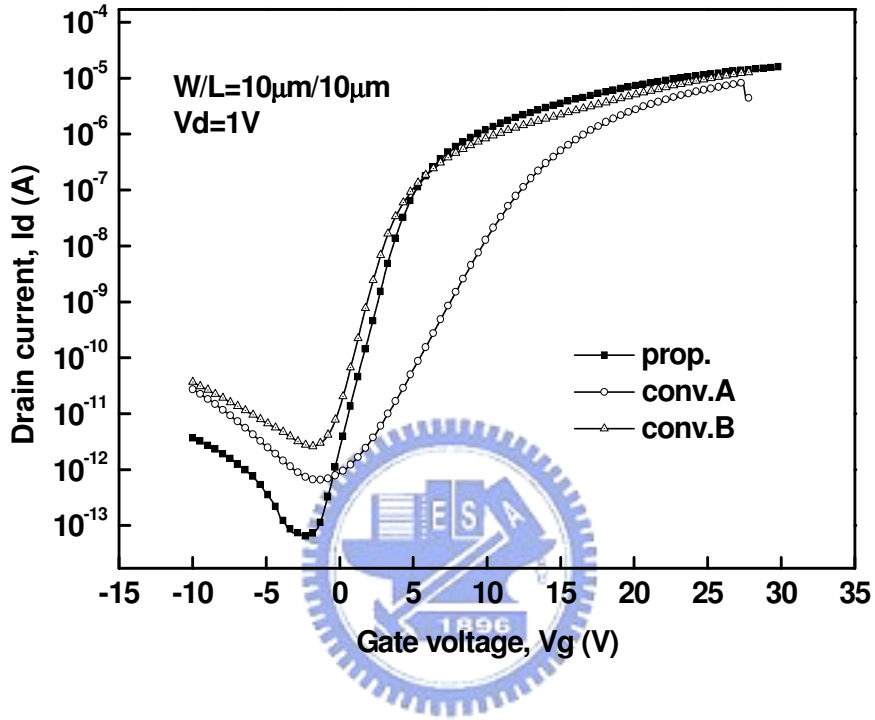


Fig.3-7 I_d-V_g transfer characteristics of proposed structure and the conventional-A , B of LTPS TFTs; W/L = 10 μm/10 μm.

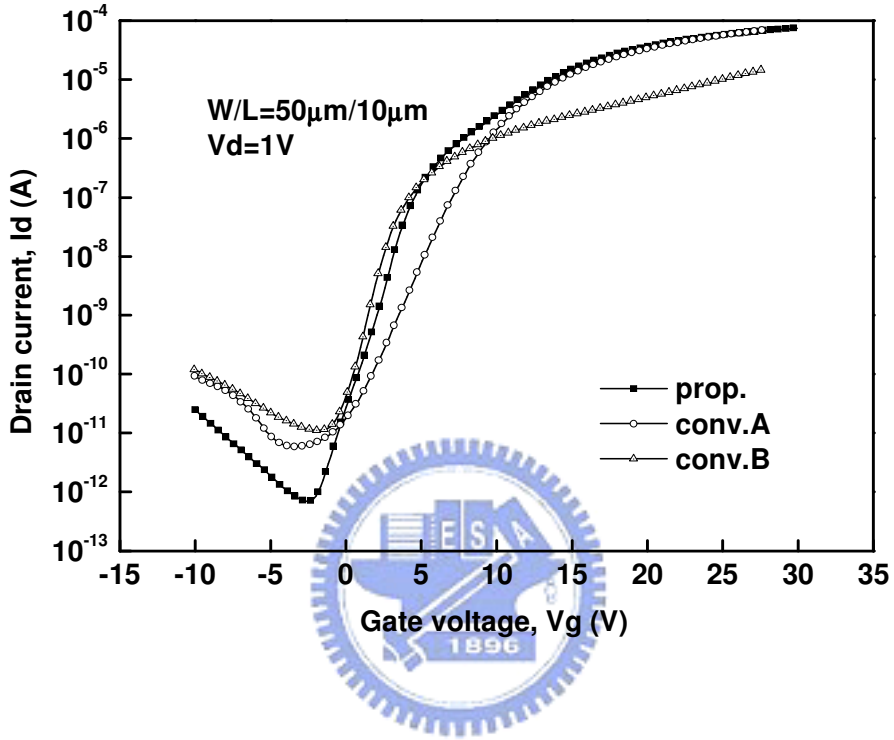


Fig.3-8 I_d-V_g transfer characteristics of proposed structure and the conventional-A , B of LTPS TFTs; W/L = 50 μm/10 μm.

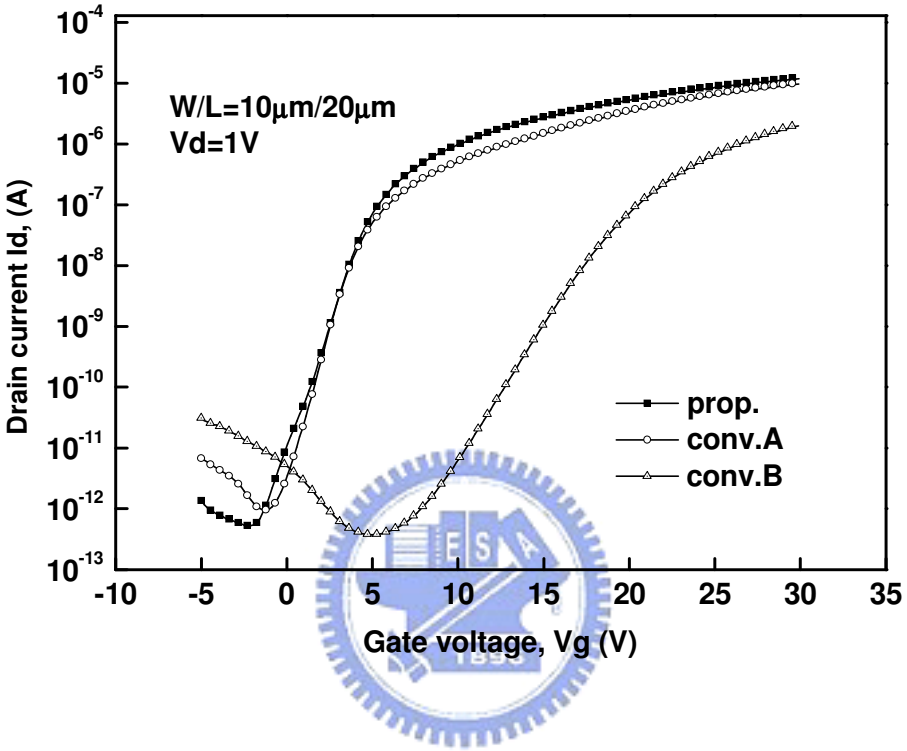


Fig.3-9 I_d-V_g transfer characteristics of proposed structure and the conventional-A , B of LTPS TFTs; W/L = 10 μm/20 μm.

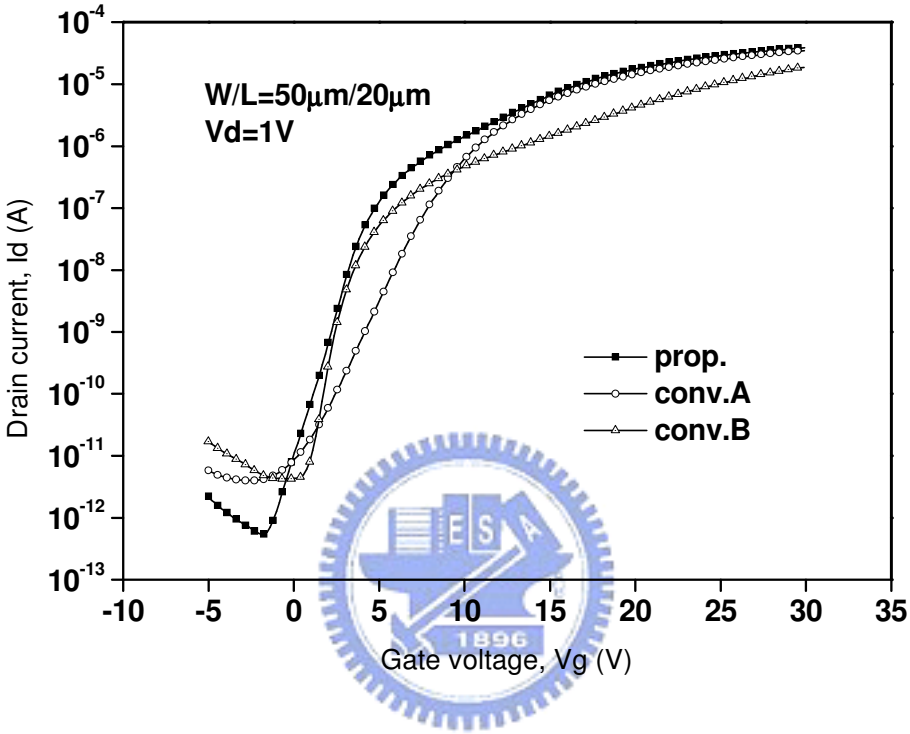


Fig.3-10 I_d-V_g transfer characteristics of proposed structure and the conventional-A , B of LTPS TFTs; W/L = 50 μm/20 μm

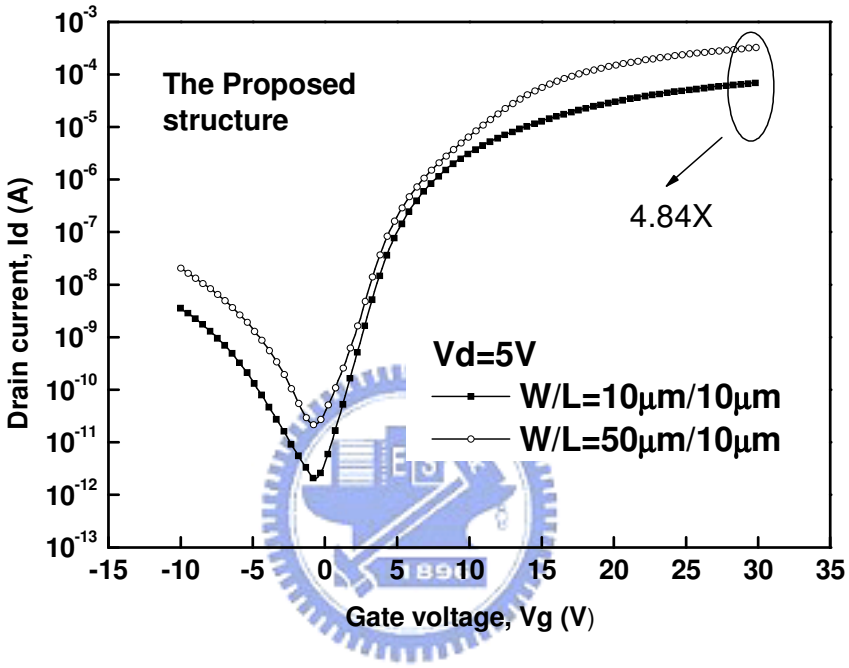


Fig.3-11 The increasing rate of on-state current of the different width of the proposed LTPS TFTs.

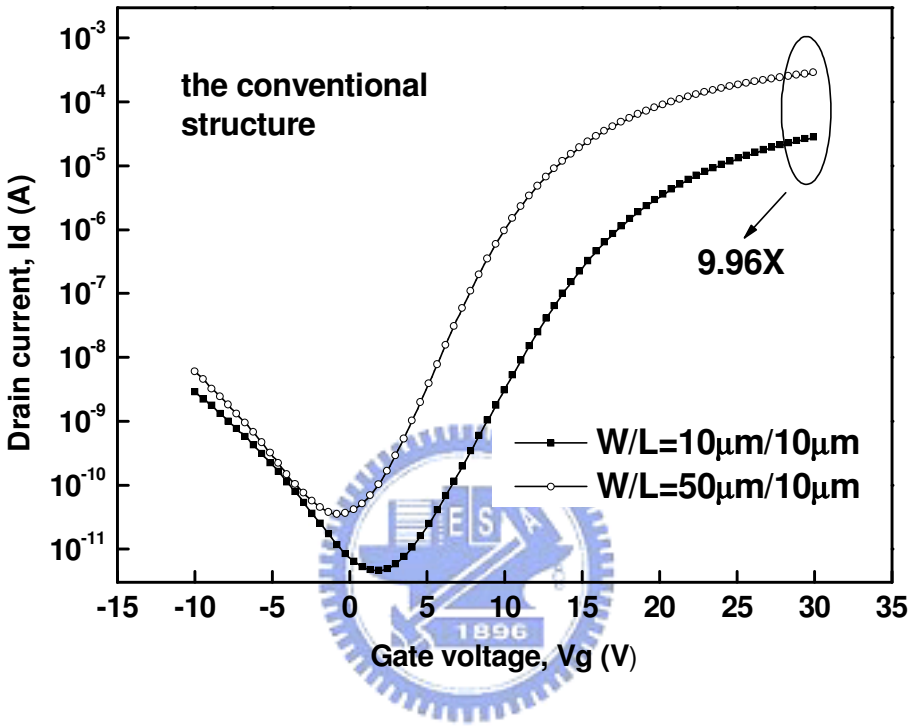


Fig.3-12 The increasing rate of on-state current of the different width of the conventional TFTs.

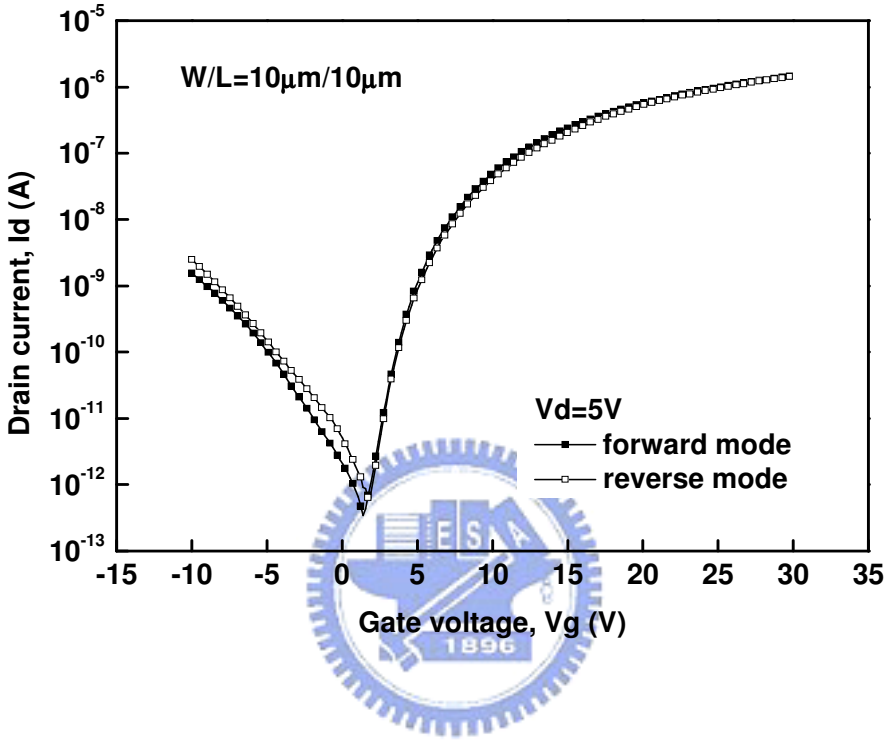


Fig.3-13 The symmetry of the proposed structure of LTPS TFTs; W/L = 10 μm/10 μm.

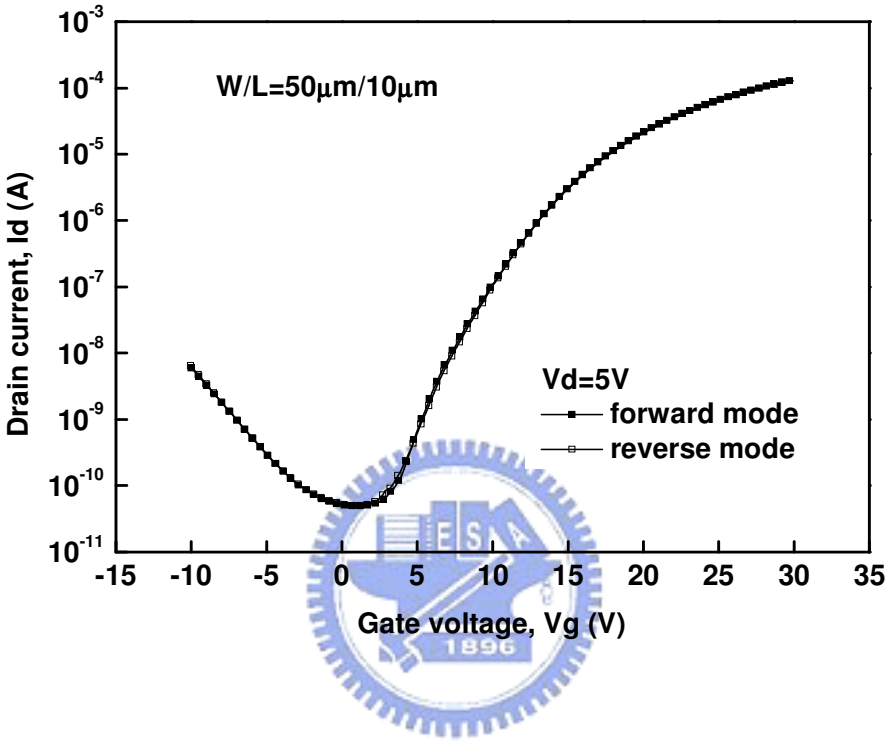


Fig.3-14 The symmetry of the proposed structure of LTPS TFTs; W/L = 50 μm/10 μm.

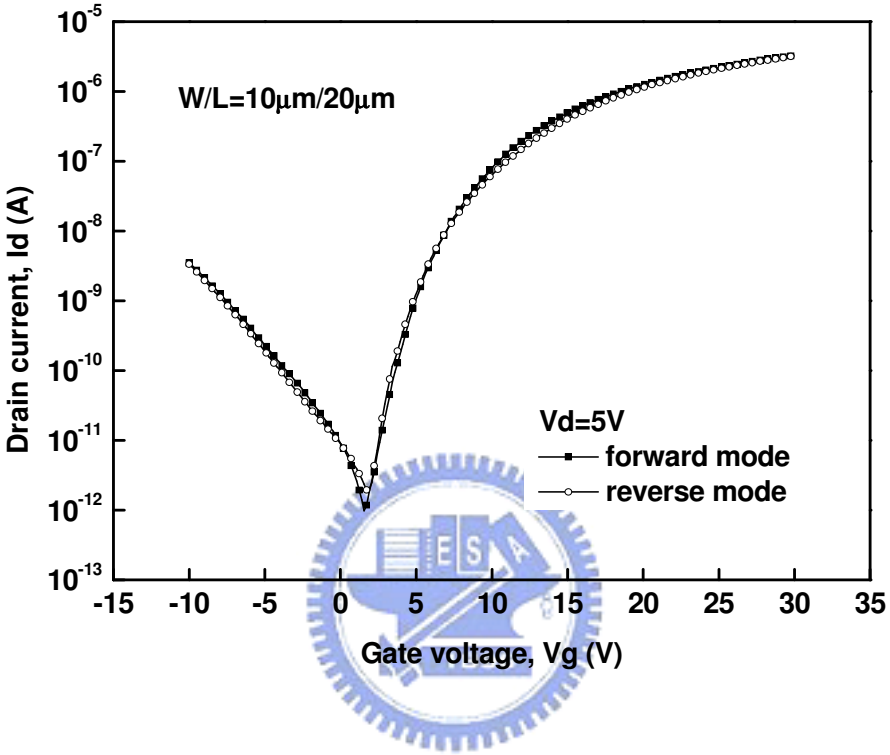


Fig.3-15 The symmetry of the proposed structure of LTPS TFTs; W/L = 10 μm/20 μm.

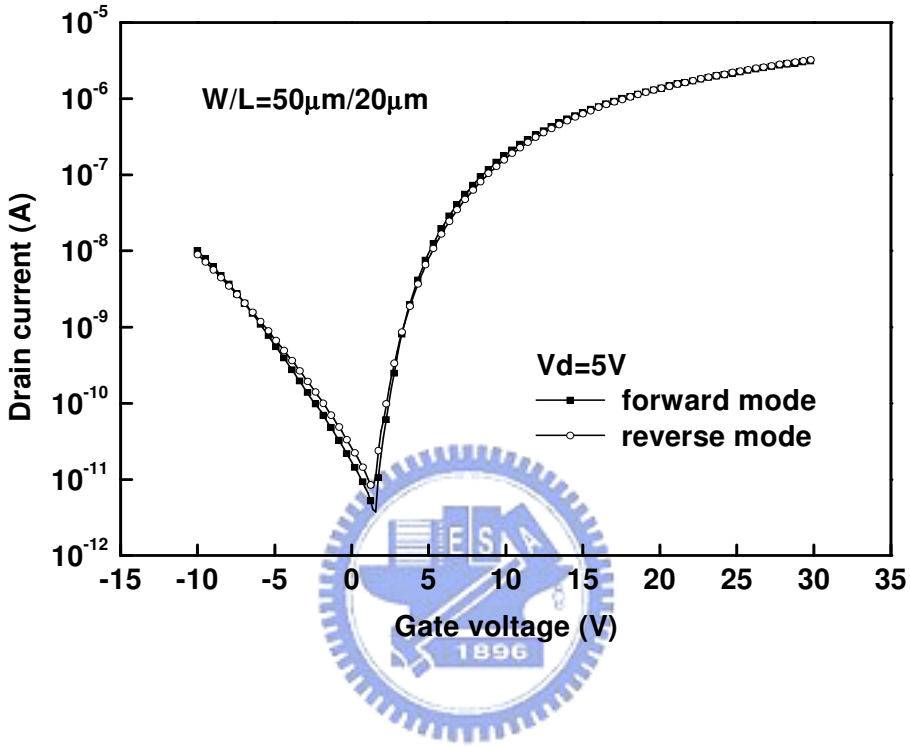


Fig.3-16 The symmetry of the proposed structure of LTPS TFTs; W/L = 50 μm/20 μm.

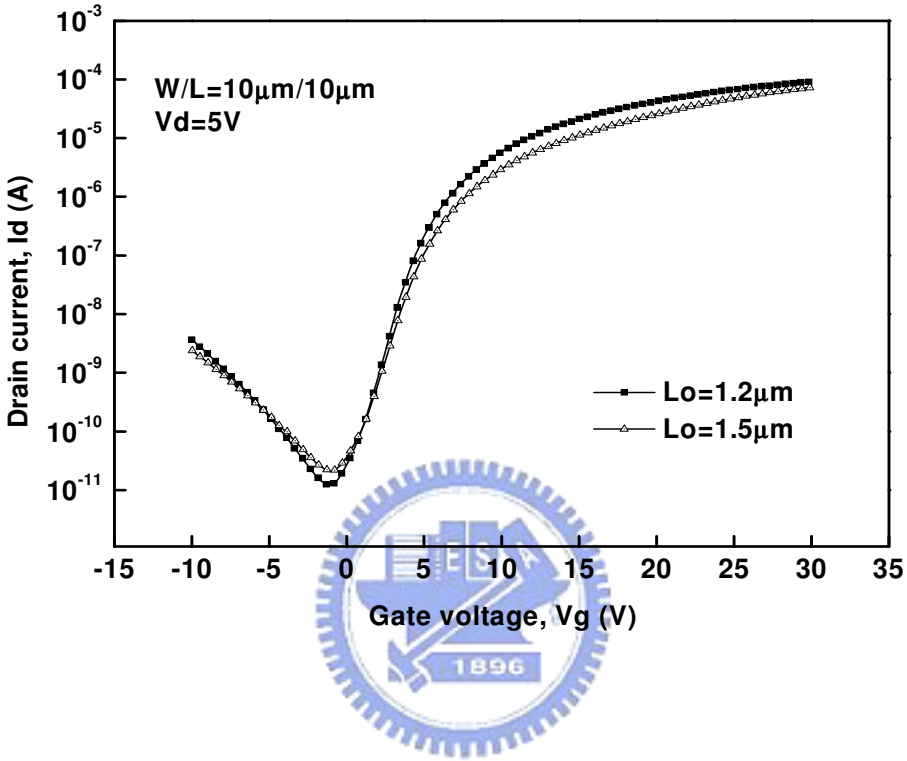


Fig.3-17 I_d-V_g transfer characteristics of the different gate-overlap length of the proposed structure of LTPS TFTs; W/L = 10 μm/10 μm.

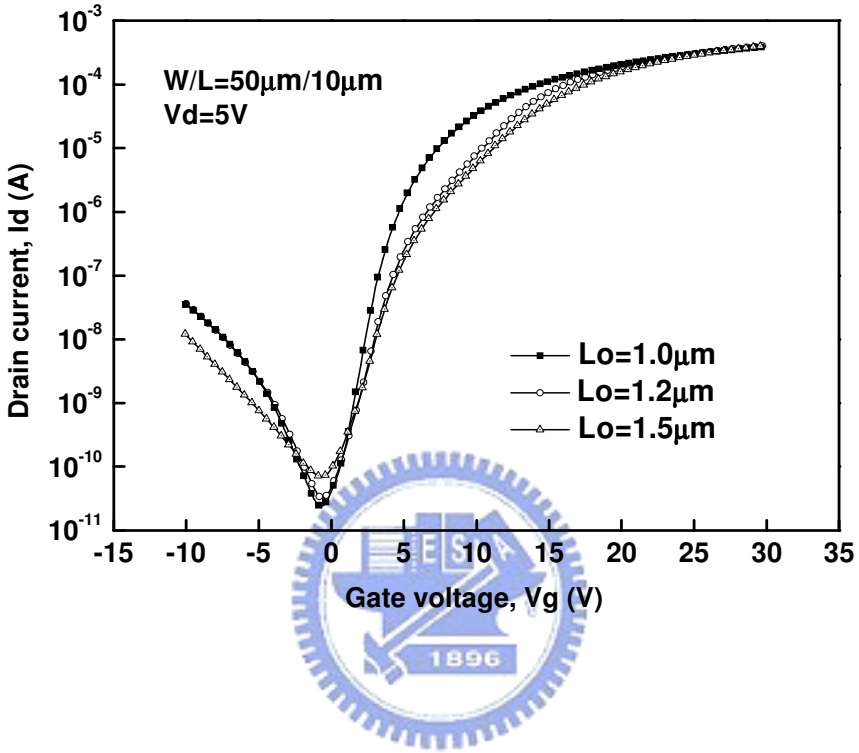


Fig.3-18 I_d-V_g transfer characteristics of the different gate-overlap length of the proposed structure of LTPS TFTs; W/L = 50 μm/10 μm.

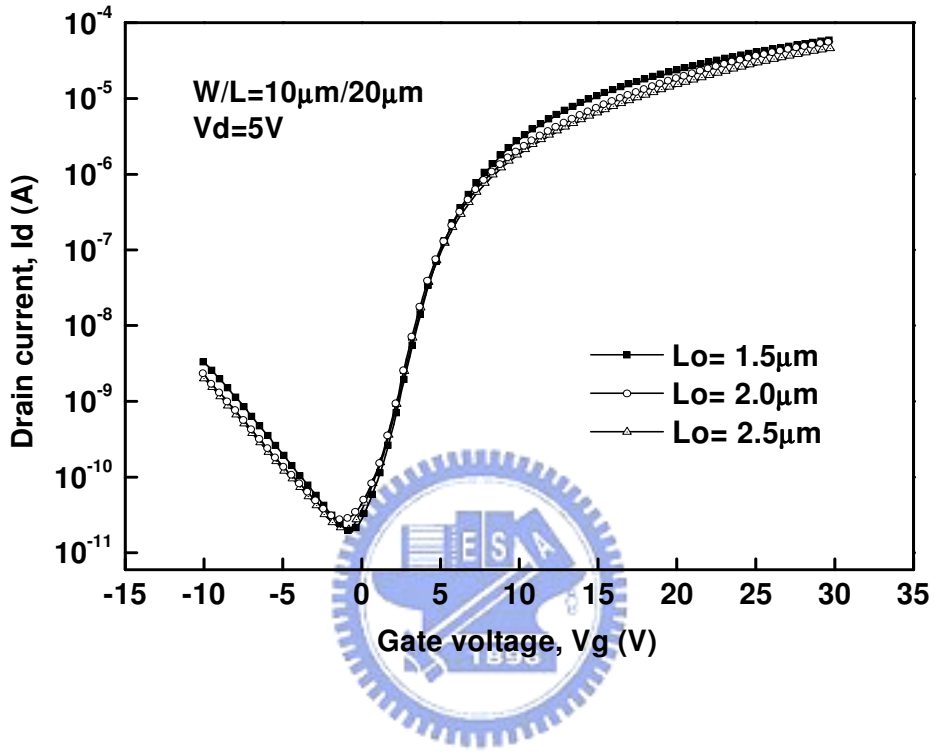


Fig.3-19 I_d-V_g transfer characteristics of the different gate-overlap length of the proposed structure of LTPS TFTs; W/L = 10 μm/20 μm.

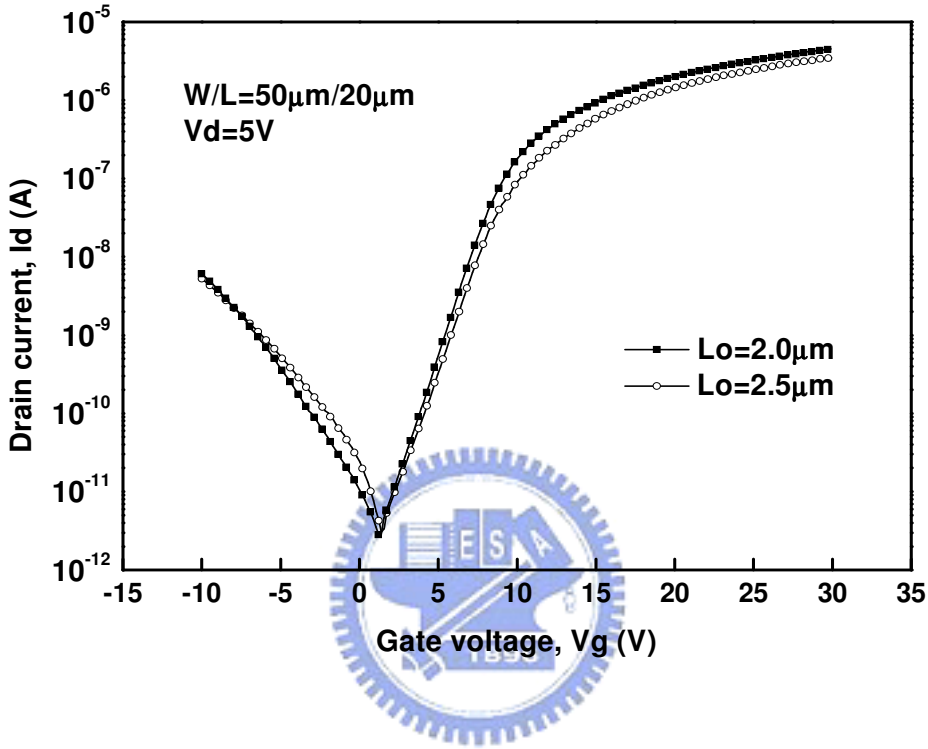


Fig.3-20 I_d-V_g transfer characteristics of the different gate-overlap length of the proposed structure of LTPS TFTs; W/L = 50 μm/20 μm

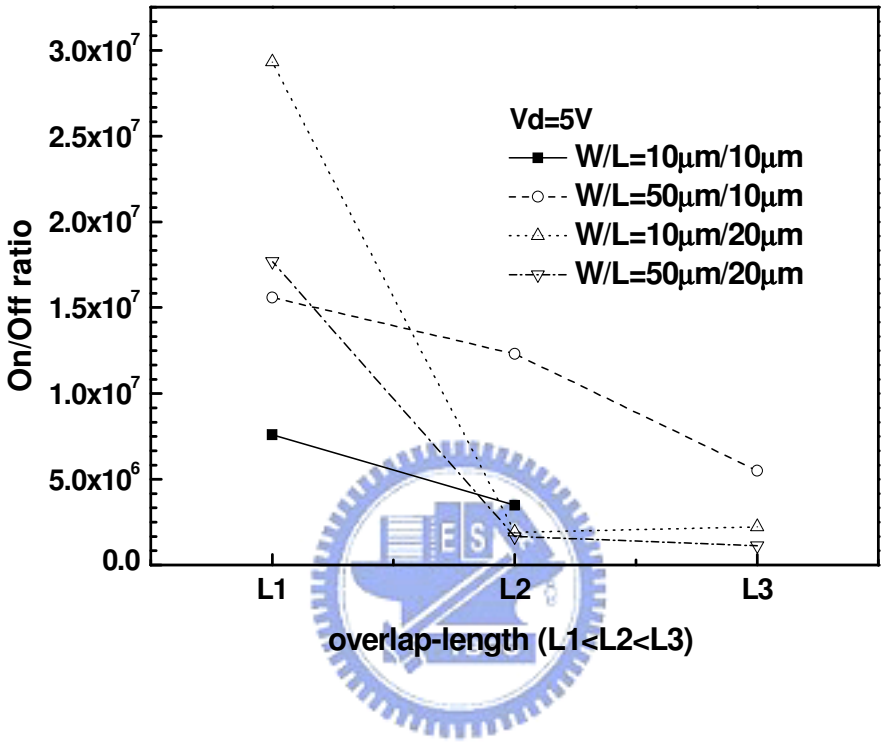


Fig.3-21 The relation between on/off ratio and overlap-length.

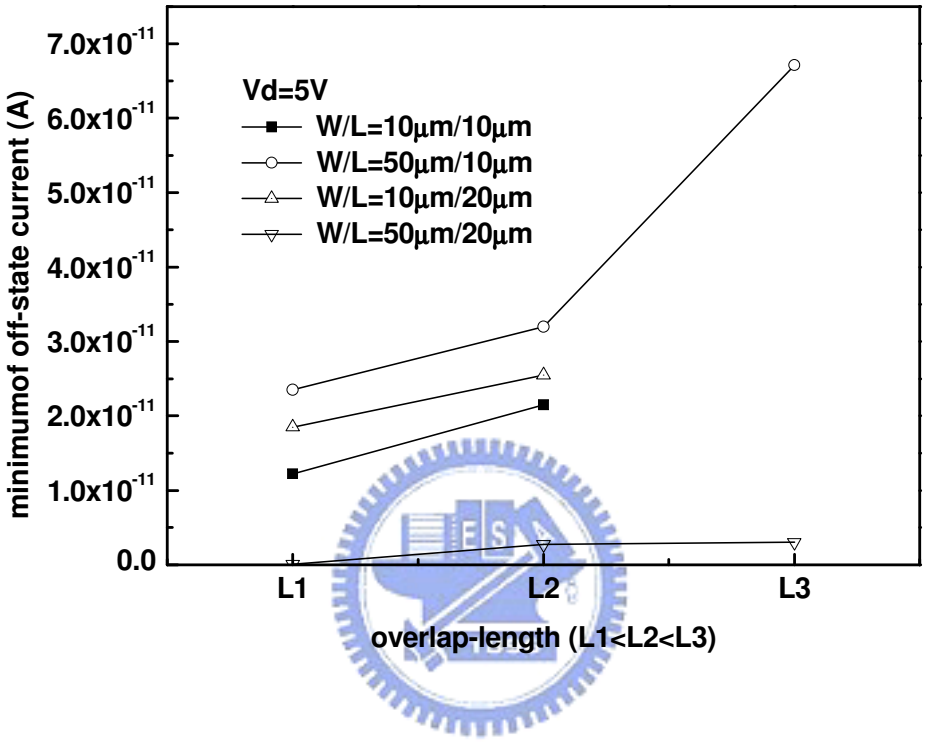


Fig.3-22 The relation between off-state current and overlap-length.

簡歷

姓　　名：謝孟帆

性　　別：男

出生日期：民國 70 年 7 月 25 日

出 生 地：台灣省台北市

住　　址：台北市士林區士東路 89 巷 16 弄 11 號 1 樓

學　　歷：台北市國立師大附中(民國 85 年 9 月~88 年 6 月)

國立成功大學物理學系(民國 88 年 9 月~92 年 6 月)

國立交通大學電子工程所碩士班(民國 92 年 9 月~94 年 6 月)

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