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碩 士 論 文

高壓元件 LDMOS 之特性分析
與 SPCIE 模型建立

Characterization and SPICE Modeling of High Voltage LDMOS

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摘要

隨著半導體產業的發展，高功率元件經常被應用在許多電力電子方面。LDMOS(平面二次擴散之金氧半場效電晶體)通常在高壓積體電路中作為驅動元件，這可歸功於它的平面結構。由於缺少內建的高壓元件模型，因此功率元件的模擬通常是利用子電路（sub-circuit）的模擬方法。本論文我們將利用子電路的方式提出一套可以模擬 LDMOS 的方法。

首先，我們將探討 LDMOS 與 MESDRIFT（比 LDMOS 多一個接觸點佈值）的特性；其中包括準飽和、衝擊離子化的機制以及 LDMOS 與 MESDRIFT 的特性比較。藉由元件模擬軟體 TCAD 的使用，我們可以更瞭解元件內部操作原理與過程。接著，LDMOS 完整的模型翠取流程將會被討論；其中包含了利用各種測試結構翠取出來的 MOS 模型以及藉由數值分析的 Vk 公式推導之 R_D 電阻模型。最後，LDMOS 產生的自我熱效應（Self-Heating Effect）將會藉由 TCAD 模擬來探討元件內部溫度分佈情況，為了更進一步的瞭解 SHE，我們建立一套微秒暫態量測電路（micro-second transient measurement circuit），藉著此電路的輔助，我們將得以觀測脈衝長短與功率大小相依的熱造成的電流下降程度議題，並提出兩套簡單模型來描素 SHE 的行為。

根據我們的研究，可以歸納出以下結果：KPC 的元件與 LDMOS 的特性最

為相近，因此利用 Vk 的概念，可被選來作為模擬的測試結構；利用反算的電阻 R_D 可以來彌補在高汲極與高閘極電壓狀況下，模擬與量測不準的情形；SHE 是受施加於元件的脈衝長短與功率大小所影響（脈衝愈長，功率愈大，則 SHE 就愈明顯）；最後，考慮準飽和效應的 LDMOS SPICE 模型將會在本論文中完成。

Characterization and SPICE Modeling of High Voltage LDMOS

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Abstract.

Power metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely applied to power electronics owing to great semiconductor industry. LDMOS (lateral Double-Diffused MOSFET) is usually the driver component in high voltage integrated circuits, thanks to its planar structure. Because of the lack of suitable built-in HV model, the sub-circuit modeling is usually used for the simulation of the power devices. In this thesis, we propose a method to modeling LDMOS by sub-circuit method.

First, we engage in the characteristics of LDMOS and MESDRIFT devices which have an extra contact implant comparing to LDMOS, including the quasi-saturation, impact ionization mechanism and the comparison between LDMOS and MESDRIFT device. We can make it clearer that the operation principle and process inside LDMOS while device is under

operation. Then, macro model extraction flow of LDMOS including MOS model which can be extracted from various test structures and R_D model which can be modeled through Vk formula derivation in numerical method will be discussed. Finally, self-heating effect will be investigated by TCAD simulation for temperature profile and by pulsed-gate experiment for the influence of heat which is dependent on pulse width and power. Two simple models are also proposed to describe the behavior of SHE.

According to our study, we can conclude that: KPC device has the best match to LDMOS, so it is chosen to modeling LDMOS with the concept of intrinsic drain voltage, Vk; using reverse calculated R_D can modify the mismatch between simulation and measurement of LDMOS at high drain and gate bias; SHE is affected by pulse width and the power applied to device (the longer pulse width, the larger power, and then the more serious SHE); finally, SPCIE model of LDMOS considering quasi-saturation is completed.

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本論文得以完成，必須要感謝許多人。首先要感謝汪大暉教授的指導與鼓勵，他的銳利目光總是趕在眾人之前就先看到未來的趨勢，他紮實且深入的研究訓練，使我面對未來的挑戰更有信心；接著要感謝莊紹勳教授、劉致為教授及謝定華經理在百忙之中抽空來做我口試委員，讓我能夠順利畢業。

論文研究上感謝鄭志昌學長一年多來無私的教誨，細心與耐心的教導，使我很容易對實驗上手，並有效率學習到新的知識及觀念。另外，David 學長的嚴謹治學與小兔學長的實事求是，令我受用無窮。

成長，就是尋找自己的旅程。感謝曾經一同走過的許多學長，及參與研究的同學。首先感謝陳旻政、吳俊威學長在研究生活中的鼓勵與指導；感謝王銘德及游建文學長，有你們的陪伴，在嚴肅的學問鑽研中增添輕鬆愉悅的氣氛。學識上的傾囊相授與人生經驗的交流由衷地感謝智維、煥淇、晉豪、又仁、冠德、益輝、靖泓、書仁及道宏的陪伴，一起走過精彩的兩年；還要感謝學弟妹們，包括杜大姊、機八強、唐大肥及薛小喵在嘻鬧中陪我渡過快樂的時光。

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Contents

Figure Captions

Chapter 1

Introduction

The scaling of Complementary Metal-Oxide-Semiconductor (CMOS) technologies has forced the continuous reduction of the power supply voltages in modern Integrated Circuits (IC). Although hot-carrier effects due to high electric field can be improved by lowering power supply voltages, devices implemented by these low-voltage CMOS technologies cannot meet the requirement of system applications where high-voltage capabilities are needed.

Ever since power MOSFET was first introduced in the 1970's [1], the technology of power devices has made impressive progress. The development of power MOSFET provided a direct link between integrated circuits and power devices. Lateral double-diffused metal-oxide-semiconductor (LDMOS) field-effect-transistor is one of the widely used power MOSFETs in high-voltage applications. It has the advantages of high performance and process compatibility to CMOS technologies and is easy to integrate with other devices [2], [3], [4]. This allows the development of high-voltage integrated circuits (HVIC's) based on LDMOS transistors. Consequently, we will study the characteristics of LDMOS by simulations and characterization.

There are two board groups of the applications on power device as shown in Fig. 1.1. The first category requires relatively low breakdown voltage (less than 100 volts) but requires high current handling capability, such as automotive electronics and switch mode power supplies. The double-diffused MOSFETs (DMOS), the main object of this study, are also included in this group. The second group lies along trajectory of increasing breakdown voltage and current handling capability, such as display drivers and motor control drivers.

Despite the increasing importance of power devices, there is a lack of simple yet accurate SPICE HV MOS model for advanced HV IC simulation. Nevertheless, we

propose a SPICE sub-circuit method which consists of one MOSFET and one variable resistance for the simulation of power MOSFET's I-V characteristics. Many researches and studies were dedicated to model HV DMOS taking into account the specific physics and phenomena associated to the extended drain region architecture, such as the quasi-saturation mechanisms [5], [6]. Over the last 5 years, some critical reports on modeling LDMOS by sub-circuit method are summarized in Table 1.1. There are two kinds of components JFET and resistance added to MOS to model HV LDMOS. For JFET, its model can only meet the operation regime: Vg < 5 V; Vd < 20, but for resistance, its model can meet the operation regime: Vg<12V; Vd <100V. Hence, we choose variable resistance to model LDMOS in our sub-circuit method.

This thesis is organized as follows: Chapter1 is introduction. Chapter2 provides a description of LDMOS used in our work and introduces various test structures called MESDRIFT devices which are designed for modeling LDMOS. We compare the characteristics between MESDRIFT devices and LDMOS and select the best one to model LDMOS. Chapter3 shows the overall extraction flow in detail and make some improvements to get more accurate LDMOS model. Then, simple models to describe self-heating effect of LDMOS are introduced in Chapter4. Finally, we will make a brief conclusion.

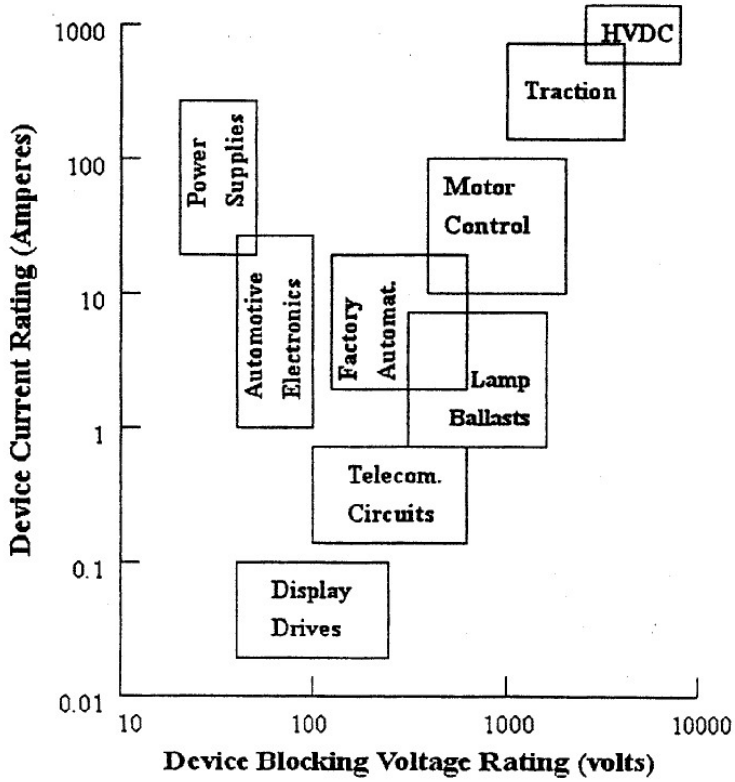


Fig. 1.1 Applications for power devices in relation to their voltage and current ratings [7].

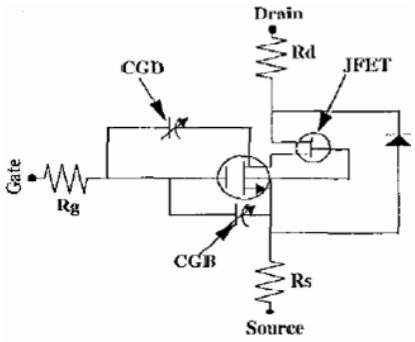
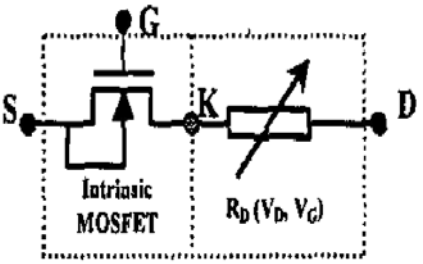
Model	Vg	Vd	paper
With JFET 	<5V	<20V	E. C. Griffith et. al, IEEE ICMTS 2000
With Resistance 	<12V	<100V	C. Anghel et.al, IEEE CAS 2003 N. Hefyene et.al, IEEE SISPAD 2002 C. Anghel et.al, IEEE CAS 2001
			IST project 2000~2002

Table. 1.1 Comparison between different components in sub-circuit model.

Chapter 2
Characterization of LDMOS and MESDRIFT

2.1 Introduction

In this chapter, the characteristics of LDMOS including the quasi-saturation effect and impact ionization are presented and impact ionization mechanism will be discussed by simulation. For modeling purpose, we also layout various test structures called "MESDRIFT" which have an extra contact implant in drift region and we will introduce them in this chapter. First, a schematic view of LDMOS is provided and its basic I-V curves are illustrated. Then, simulation results about impact ionization are illustrated. Finally, planar layout and cross section views of MESDRIFT devices are demonstrated and the comparison between MESDRIFT and LDMOS will be shown to find out the best match one for modeling.

2.2 Basic Structure and I-V Curve Discussions of LDMOS

2.2.1 LDMOS Basic Structure

The cross section of N-LDMOS studied in our work is shown in Fig. 2.1. The whole device is inside a lightly epitaxial layer. The extended drain region under the field oxide (FOX) consists of an n^- drift region and an n-well for on-state resistance control. The double diffused n^+/P-Body region consists of source and channel, a threshold voltage adjustment layer should be used to avoid a laterally varying doping concentration in the channel region. In order to measure source substrate current respectively for advanced reliability analysis, source and substrate are separated. The existence of n-well is not only to control the on-resistance, but also to increase breakdown voltage [8], [9]. It is because the n-well lowers the high electric field near the n^+ drain diffusion. The field plates (the portions of the poly-gate that cross over the field oxide) can increase the breakdown voltage because of reducing field

crowding at the edge of depletion layer under the poly-gate.

Some important dimensions of LDMOS transistor are outlined, which are the effective channel length L_g, the additional length of the gate poly overlap gate extension length, and the drift region length L_D. The P-Body concentration and n^- epitaxial layer concentration are also important parameters.

2.2.2 Basic I-V Curve Discussions

The LDMOS devices studied in our work have the following feature; threshold voltage V_t=1.67V, gate oxide thickness t_{ox}≈1000Å, field oxide thickness t_{FOX}≈3500Å, channel length L_g=3μm, and device width W=20μm with device operation region: Vg=0 ~ 40V, Vd=0 ~ 40V. The measured I-V curves at low gate voltage are shown in Fig 2.2. The current path is described as follows. During on-state, electrons flow from the N^+ source into the channel formed in P-body region under the gate oxide, and continue to flow through the N-epi drift region and N-well to the N^+ drain. Obviously, the resistance from channel to drain terminal is lager than that from channel to source terminal. This is an asymmetric HV MOS device with respect to source/drain resistance. From Fig. 2.2, we can see that at low gate voltage, impact ionization current is obvious, so we take some device simulations to find out the changes inside the device by examining the location of maximum impact ionization generation rate (IIG). Before that, Fig. 2.3(a) and (b) revel the simulated current flowlines in linear region and saturation regions. It is observed that in linear region, the current path is along the Si-SiO2 interface within the gate extension region. This differs from the saturation condition where the current path is far below the Si-SiO2 interface. This is because the voltage under the Si-SiO2 interface is still large in saturation region. In contrast, the voltage under the Si-SiO2 interface in linear region is small.

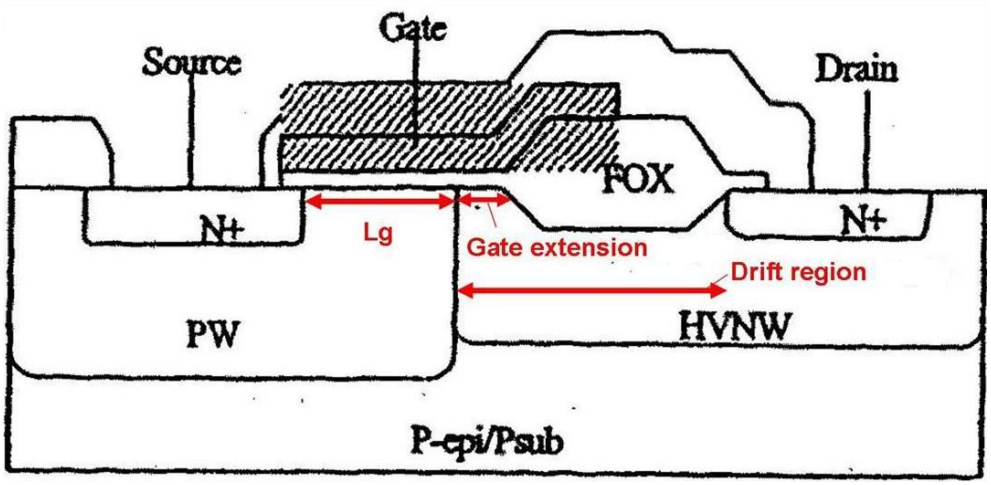


Fig. 2.1 Schematic cross section of NLDMOS device used in our study. (Width=2μm, Lg=3μm)

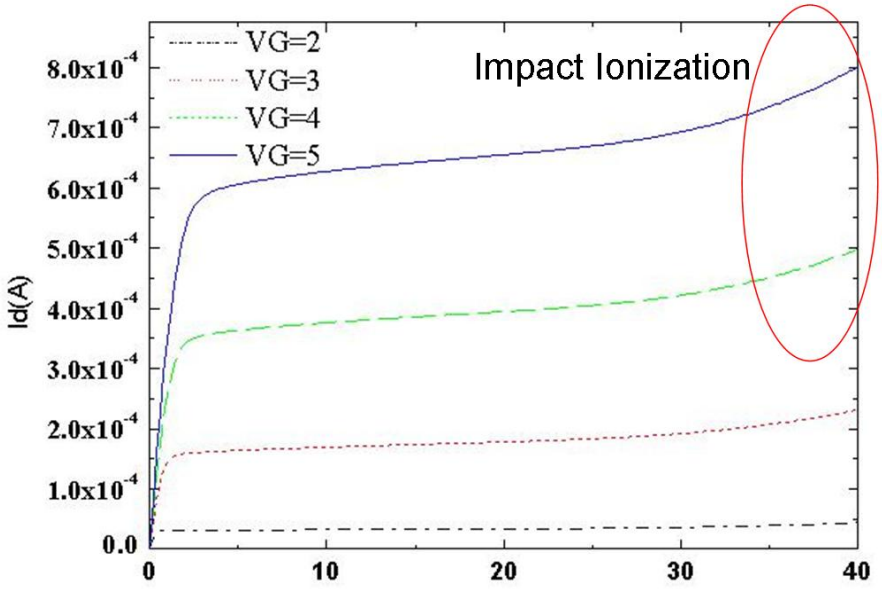


Fig. 2.2 Measured IdVd characteristics at low gate bias of NLDMOS.

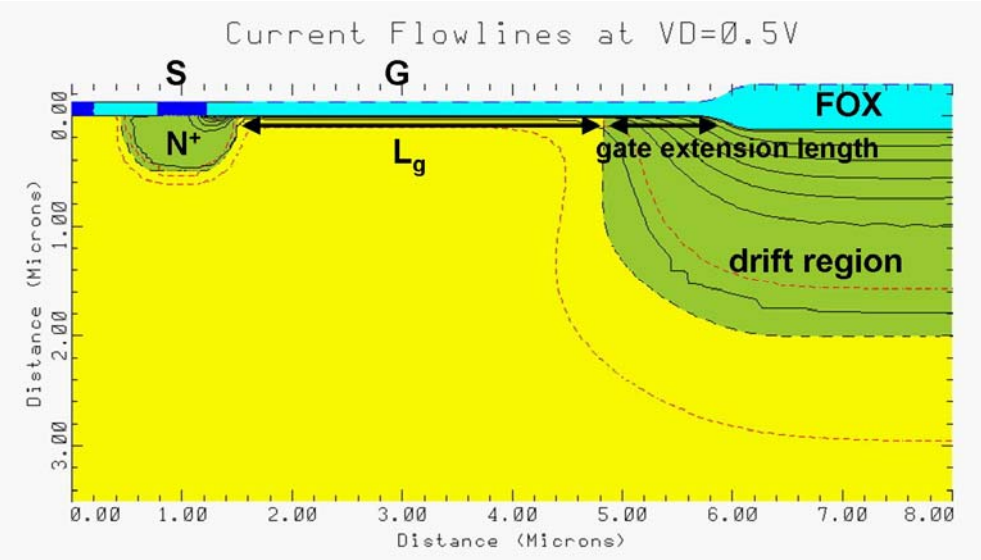


Fig. 2.3(a) Simulation of current flowlines for LDMOS operating in the linear region. Current flows near the surface in the gate.

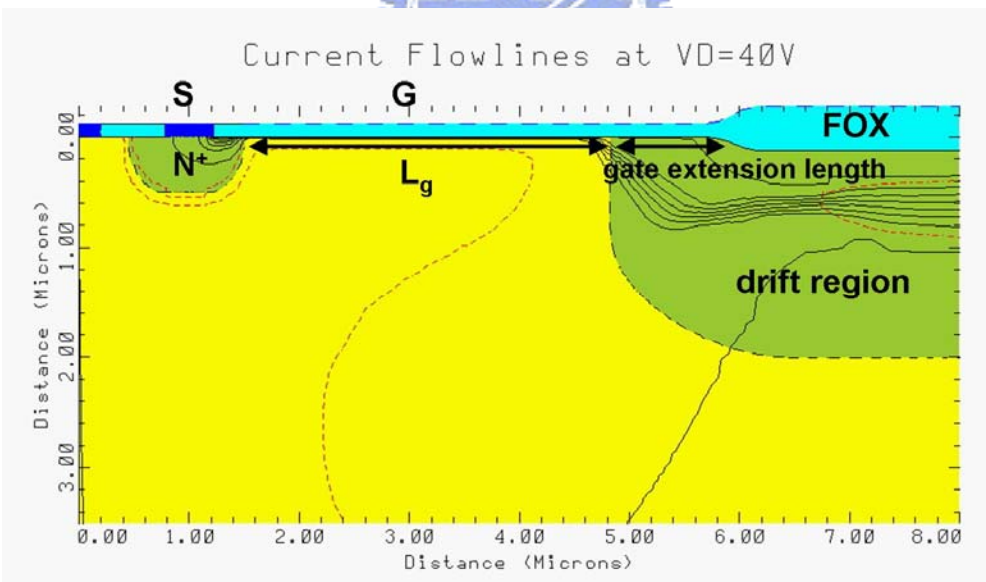


Fig. 2.3(b) Simulation of current flowlines for LDMOS operating in the saturation region. Current flows near the surface in the gate.

2.2.2-1 Vd dependence of the maximum impact ionization rate

Several researchers have indicated three different regions within the LDMOS where significant hot-carrier generation can occur [10], [11]. From Fig 2.4(a), we have found that when the drain bias is small, the peak electric field is located in the channel near the source side gate edge. The physical reason for the source peak can be attributed to the gate edge effect [12], [13].

The "gate edge effect" occurs because the variation of vertical band bending generates high lateral electric field. The gate edge effect may occur at two positions: the gate edge near the source side and the gate edge near the drift region side (bird's beak). In the former case, high Vg will lead to gate edge effect. In the latter one, low Vg will cause gate edge effect more seriously. The high electric field near the source side gate edge or the bird's beak is the result of gate edge effect.

When drain bias reaches saturation, the channel is pinched-off producing large electric field near the P-Body-epitaxial junction as shown in Fig. 2.4(b). After Id is saturated, almost all the further increase in Vds drops in the drain series resistance region and does not affect the lateral electric field in the channel, but the field in the drift region increase almost linearly with Vds [14]. Hence, for sufficiently high drain bias, the IIG is located in the drift region, as can be seen in Fig 2.4(c).

2.2.2-2 Vg dependence of the maximum impact ionization rate

In the preceding section, we discuss the Vd dependence of the maximum IIG location. Nevertheless, the Vg dependence of IIG has already a major concern in reliability issue [15]. By using device simulation, the correlation between Vg and IIG is explored.

Fig 2.5 illustrates the simulated results. When Vg increases from 10V to 40V, the location of maximum IIG moves to the right side gradually. This is due to the current flowlines we discuss previously. As gate voltage increases, the current path is close to the Si-SiO2 interface in the gate extension region, and then begins to spread

out near the bird's beak.

Although the peak electric field is located in the silicon bulk, the critical position we are more concerned about is the IIG value near the bird's beak where electrons will be trapped easily [16]. As Vg increases, the IIG near the bird's beak is enhanced expect for Vg=10V. The gate edge effect, as we mentioned above, accounting for this exception. This result is in correspondence with the experimental data.

2.2.3 Quasi-saturation effect

In this section, we introduce a unique phenomenon in LDMOS called "quasi-saturation effect" or "early-saturation effect" which appears at sufficiently high gate voltages. This effect limits the maximum current at high gate voltage [17], [18]. On measuring the DC characteristics in our LDMOS transistors, it is noticed that the drain current is limited at high gate voltage as illustrated in Fig. 2.6. Conventional MOS circuit models are incapable of modeling this effect [19]. This quasi-saturation effect is because of the existence of the drift region. The drain current tends to be saturated not because of the pinch-off of the channel at the drain end, rather because of the velocity saturation in the drift region for carriers from the channel. Thus, the drift region can be modeled as a JFET [20], [21]. Other researches also model the quasi-saturation effect by adding a nonlinear resistance controlled by drain current through the drift region [22]. In our study, we use nonlinear resistance controlled by drain and gate voltage to model drift region and the macro model overall extraction flow of LDMOS will be discussed in Chapter 3.

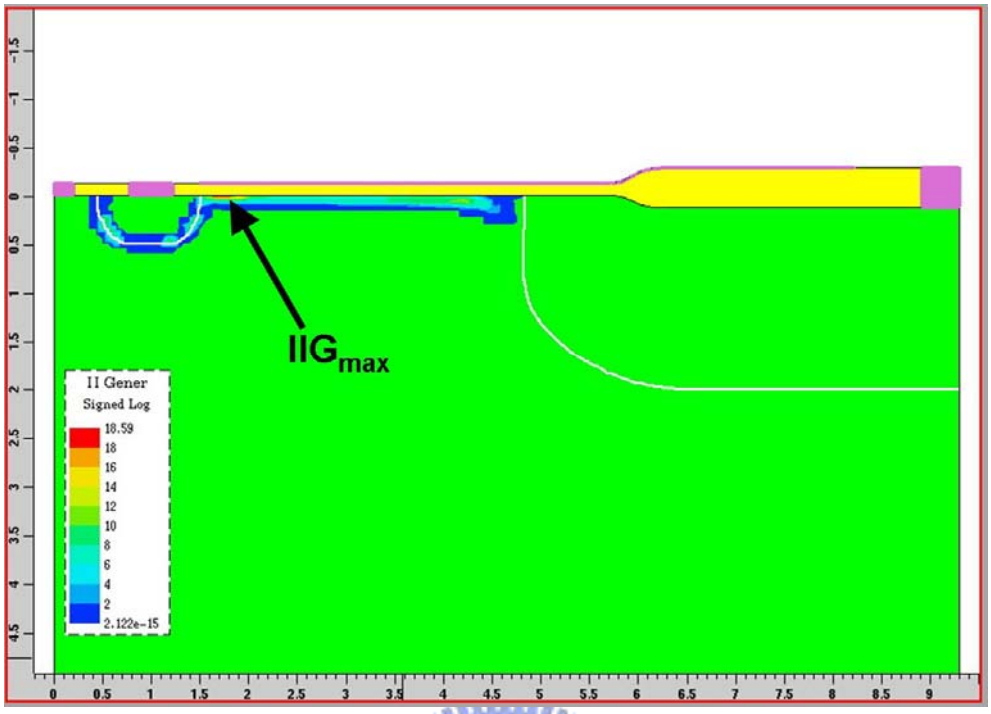


Fig. 2.4(a) The location of maximum impact ionization rate (IIG) at Vd=0.5V, Vg=10V.

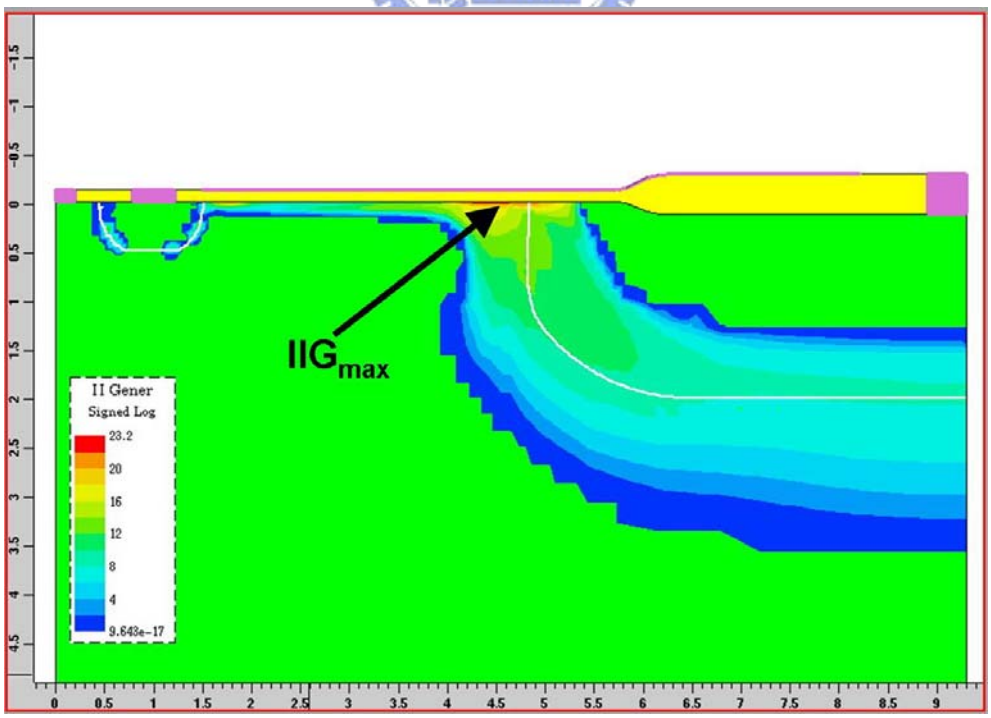


Fig. 2.4(b) The location of maximum impact ionization rate (IIG) at Vd=10V, Vg=10V.

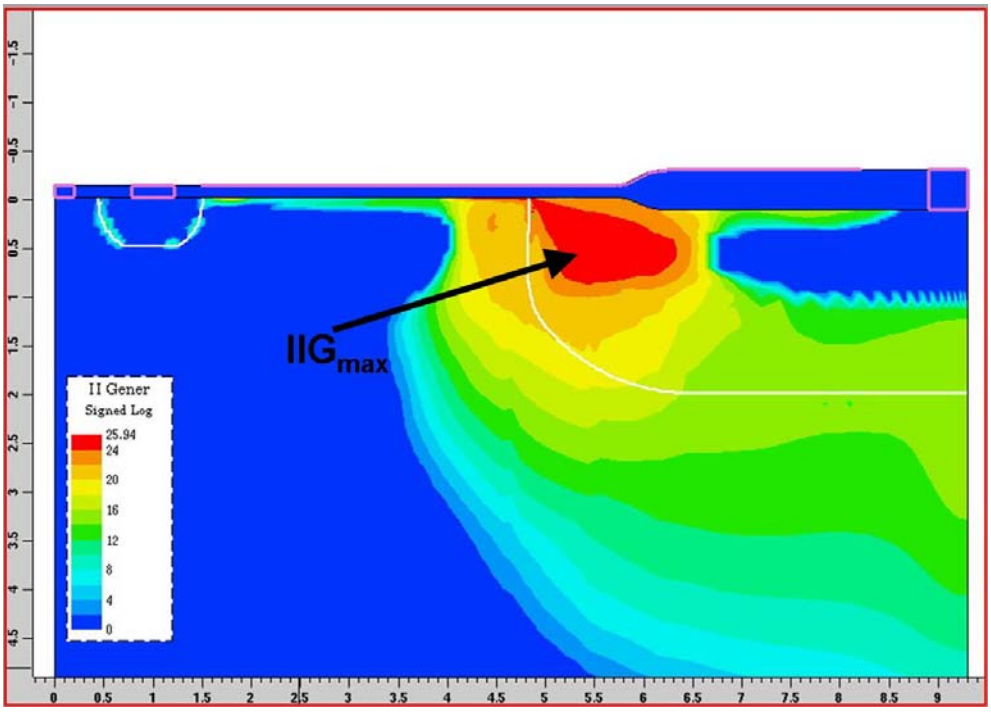
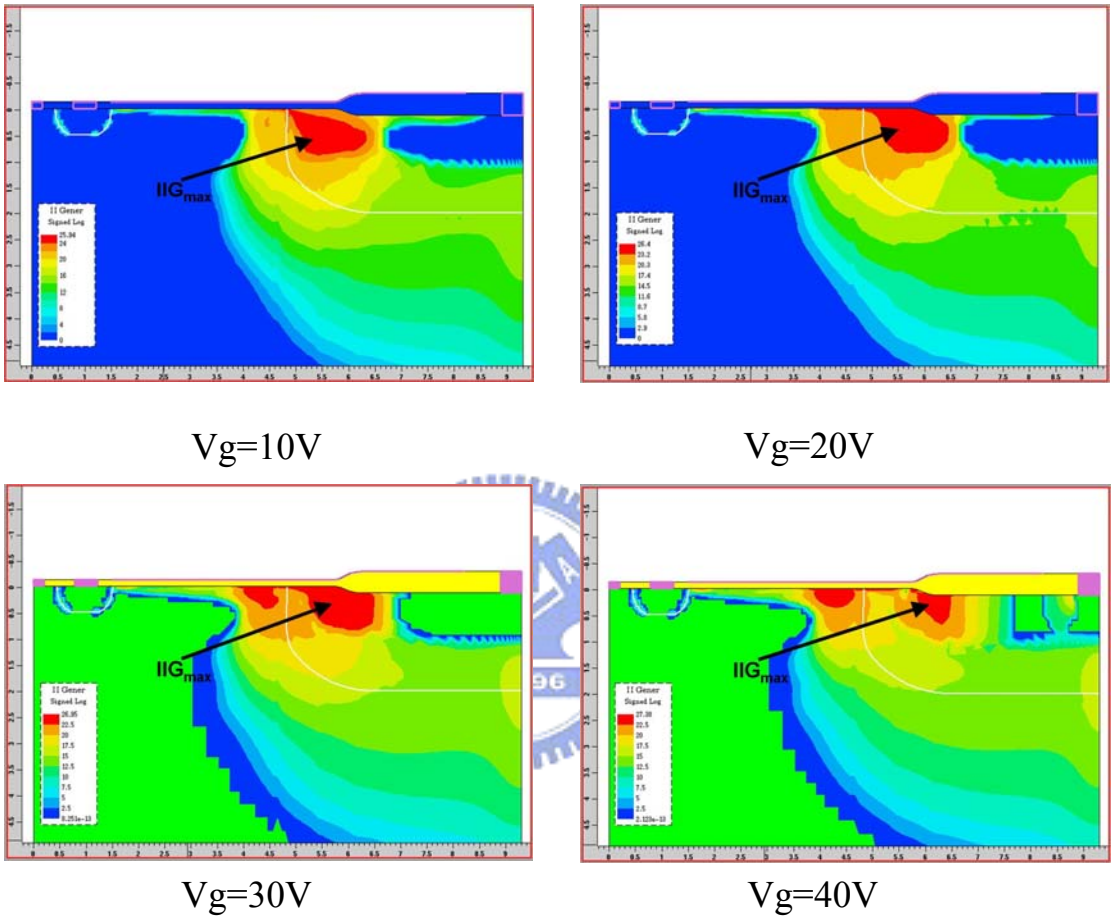


Fig. 2.4(c) The location of maximum impact ionization rate (IIG) at Vd=40V, Vg=10V.



Vg=10V Vg=20V

Vg=30V Vg=40V

Fig. 2.5 The location of maximum impact ionization rate moves toward the bird's beak when Vg is elevated.

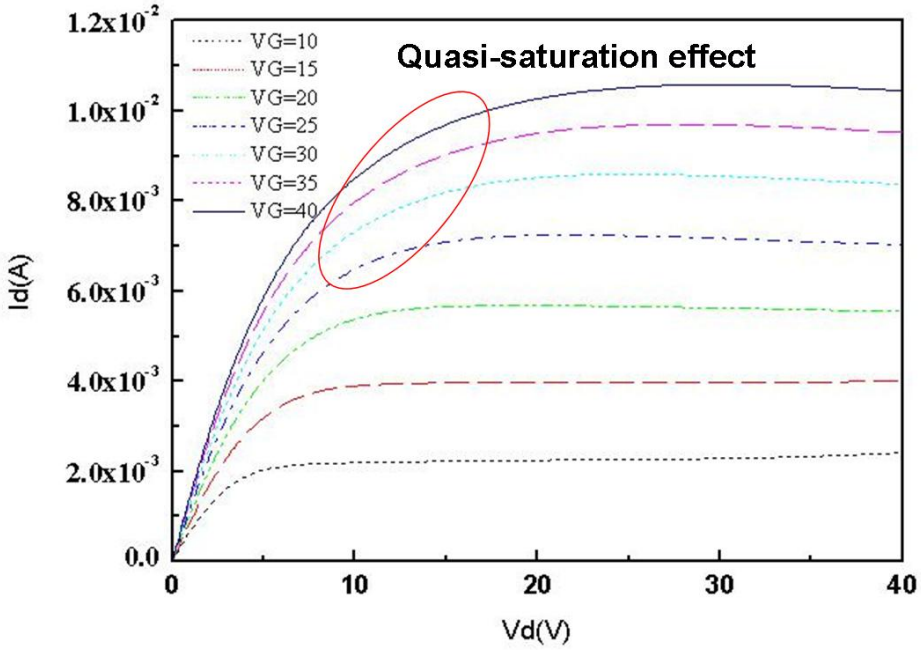


Fig. 2.6 Measured I-V characteristics of NLDMOS with quasi-saturation effect.

2.3 Structure and I-V Discussions of MESDRIFT Device [23], [24]

In this section, MESDRIFT devices which compared to LDMOS device have an extra contact implant in gate extension region are introduced. In our study, there are four kinds of structures about MESDRIFT devices including KL, KP, KPC and KPF. These four kinds of devices are all design to get intrinsic MOS and drift resistance data because with them modeling LDMOS can be easier. LDMOS devices have some unique effects like quasi-saturation effect, so we can not model it by a single built-in SPICE MOS model. Hence, we use MESDRIFT devices to get information inside LDMOS which includes the channel region and drift region while device is under operation. Detail extraction flow of modeling LDMOS by the use of MESDRIFT will be discussed in chapter3. Cross section, planar layout and I-V curves of KL, KP, KPC and KPF devices are presented as following.

2.3.1 KL Device

KL device cross section is shown as Fig. 2.7(a) and its planar layout picture is shown as Fig. 2.7(b). As mentioned above, MESDRIFT device has an extra contact implant in gate extension region. For KL device, the contact implant is along with the device width, so there is a ”line” implant in the middle of gate extension region like source and drain, and that is the reason we call such a device “KL” MESDRIFT device. The line implant affects the I-V characteristics of KL device much different from those of LDMOS device as shown in Fig. 2.7(c). Compared to LDMOS, KL devices have serious impact ionization occurs at high drain bias and low gate bias region. Hence, the currents of KL device are much larger than LDMOS device.

2.3.2 KP Device

KP devices also have an N^+ implant in gate extension region. The implant is a point implant which locates at the middle of gate extension region. KP device cross section is shown in Fig. 2.8(a) which is the same with KL device and its planar layout

is shown in Fig. 2.8(b) which shows the contact implant is the middle of device width. I-V comparison between KP and LDMOS device are shown in Fig. 2.8(c). From Fig. 2.8(c), we know that KP device is similar to LDMOS device on DC measuring, but the K implant still makes some influence on I-V characteristics. At low gate voltage and high drain voltage region, the current of KP device is a little higher than that of LDMOS while at high gate voltage region, I-V characteristics have a good match with those of LDMOS.

2.3.3 KPC Device

Like KP device, KPC device also has an N^+ implant in gate extension region, but the implant locates at the channel end (the interface between P-body and N^- drift region). KPC device cross section is shown in Fig. 2.8(a) and its planar layout is shown in Fig. 2.8(b). I-V comparison between KPC and LDMOS device are shown in Fig. 2.8(c). From Fig. 2.8(c), we can see that KPC device is very similar to LDMOS device on DC measuring, because the point implant near channel does not change the LDMOS structure too much. So we choose KPC device for our modeling of LDMOS and this will be discussed in chapter 3.

2.3.4 KPF Device

Like KP device, KPF device has a N^+ implant in gate extension region with the location at the right side of gate extension region which is close to bird's beak. Cross section of KPF device is shown in Fig. 2.9(a) and its planar layout is shown in Fig. 2.9(b). I-V comparison between KPF and LDMOS device is shown in Fig. 2.9(c). From Fig. 2.9(c), we can see that KPF device is also similar to LDMOS device on DC measuring, but the point implant does not easy to control due to the FOX, so its I-V curves are different from those of LDMOS just shown as Fig. 2.9(c).

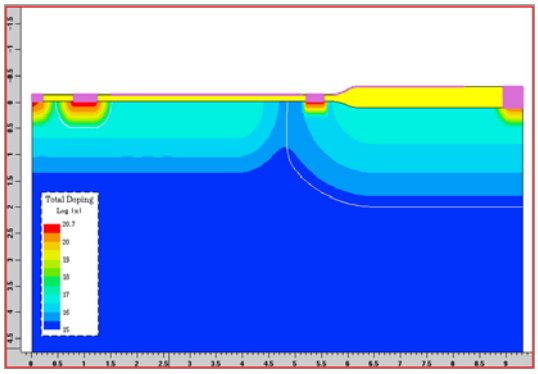


Fig. 2.7(a) Cross section of KL MESDRIFT device.

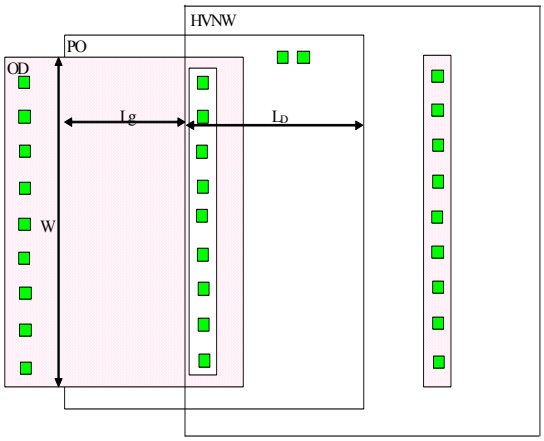


Fig. 2.7(b) Planar layout of KL MESDRIFT device.

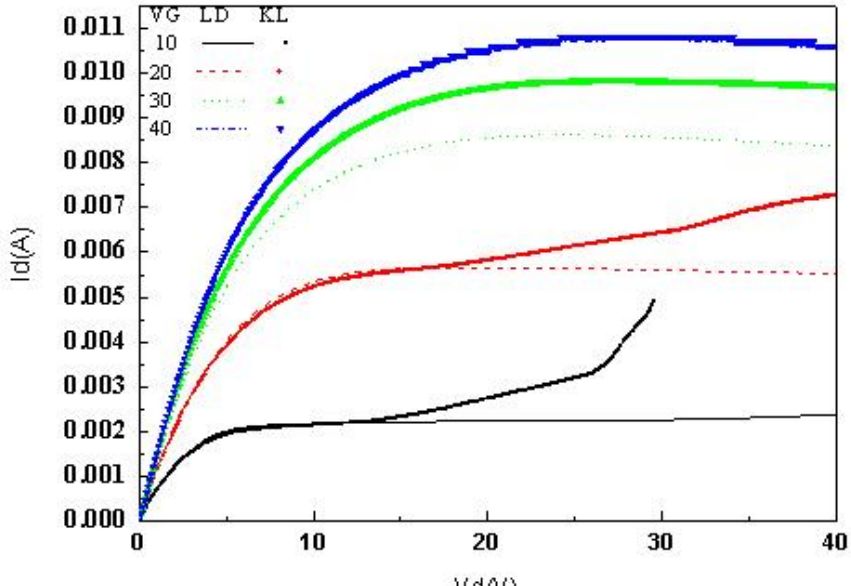


Fig. 2.7(c) I-V comparison between KL and LDMOS device.

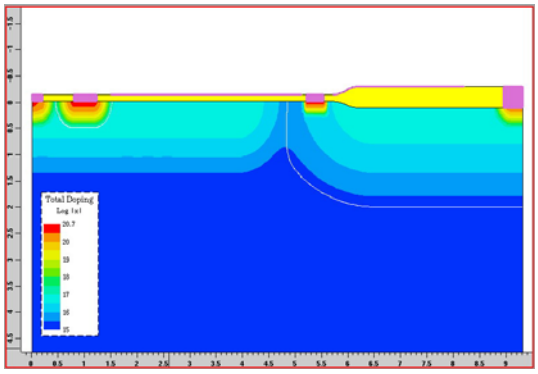


Fig. 2.8(a) Cross section of KP MESDRIFT device.

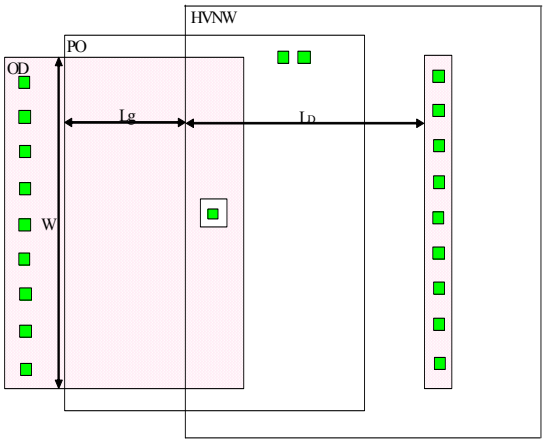


Fig. 2.8(b) Planar layout of KP MESDRIFT device.

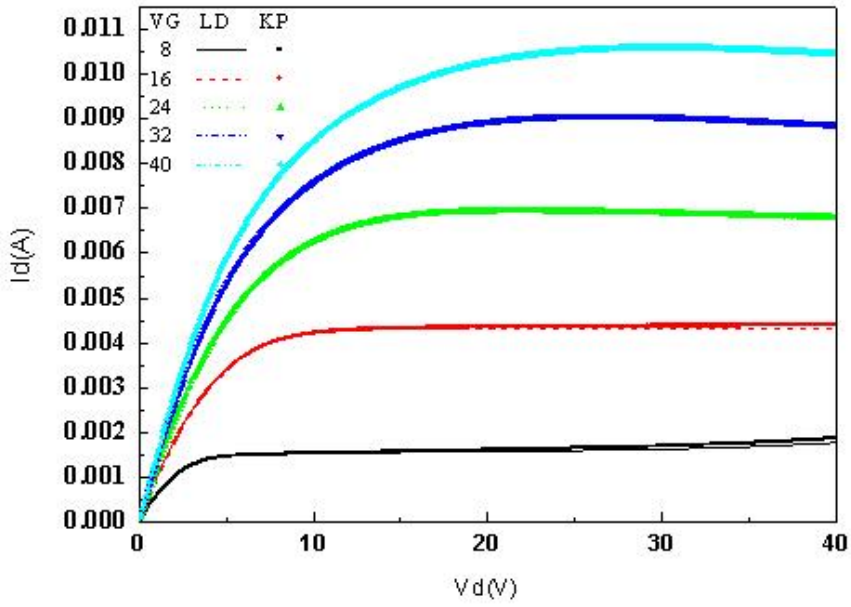


Fig. 2.8(c) I-V comparison between KP and LDMOS device.

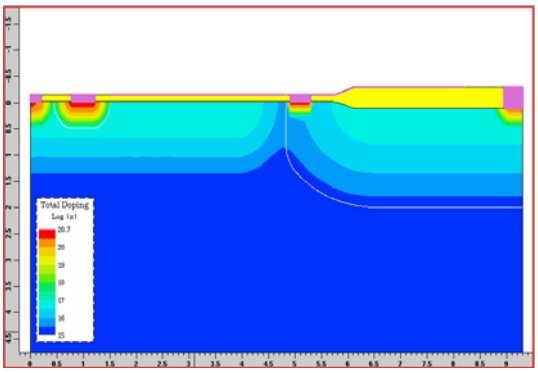


Fig. 2.9(a) Cross section of KPC MESDRIFT device.

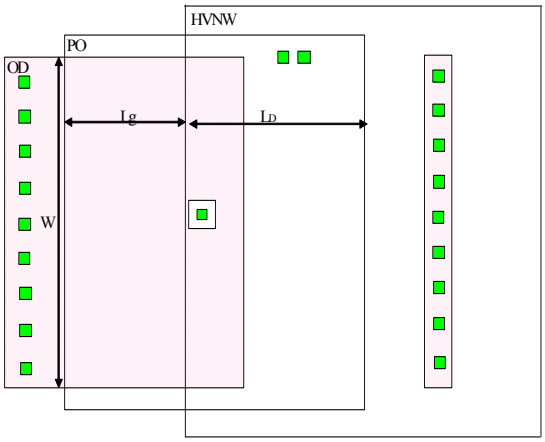


Fig. 2.9(b) Planar layout of KPC MESDRIFT device.

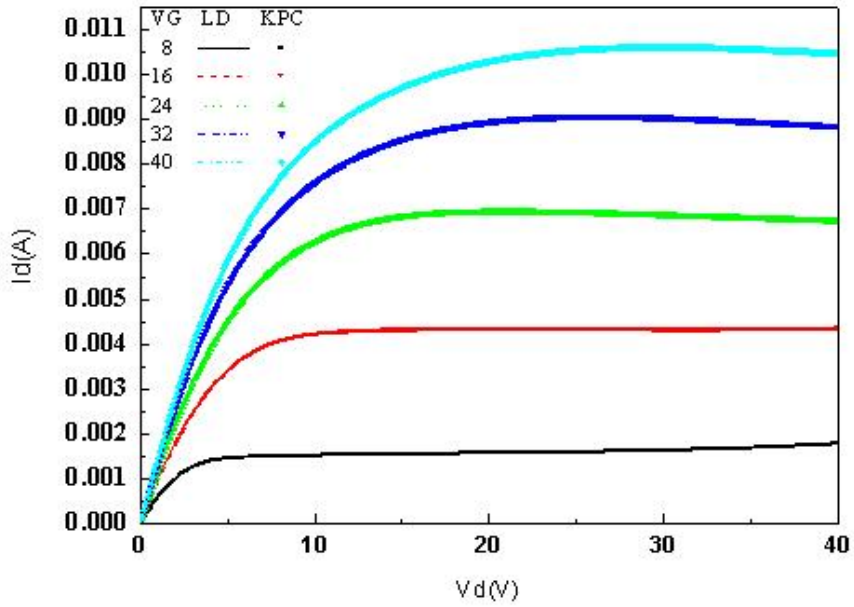


Fig. 2.9(c) I-V comparison between KPC and LDMOS device.

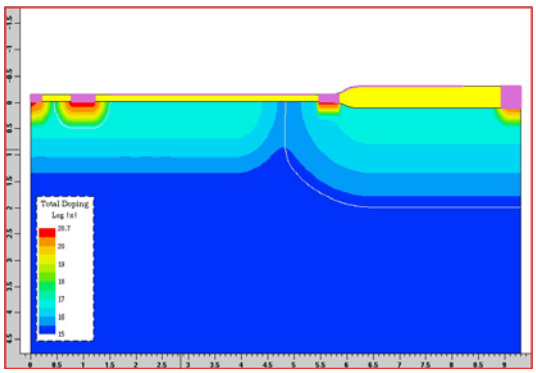


Fig. 2.10(a) Cross section of KPF MESDRIFT device.

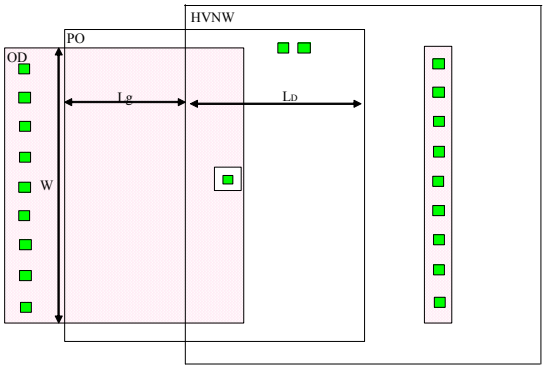


Fig. 2.10(b) Planar layout of KPF MESDRIFT device.

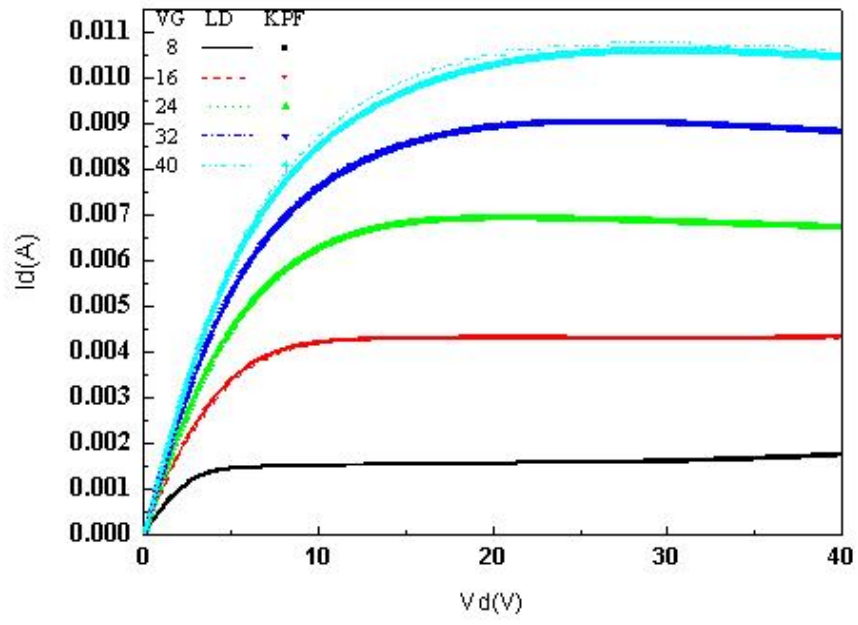


Fig. 2.10(c) I-V comparison between KPF and LDMOS device.

Chapter 3
Extraction Flow of Intrinsic MOSFET and Drain Resistance

3.1 Introduction

An overall macro model extraction flow of LDMOS is illustrated step by step in this chapter. First, we show our strategy for modeling LDMOS by sub-circuit method which includes one intrinsic MOS model and one bias dependent resistance. Then, we find out the intrinsic MOS model from KPC device which is the best match to LDMOS. To find R_D model, we calculate R_D data from KPC measurement. In order to get more correct R_D data, we use reverse calculated R_D data to adjust macro model for fitting LDMOS. To simply R_D model, we derive Vk formula to reduce R_D model parameters. For more convenient and faster MOS model extraction, we use KL device to get intrinsic MOS data. Finally, simulation and measurement data of MOS, R_D and macro model of various method combinations are presented and discussed.

3.2 Strategy and Initial Extraction

3.2.1 Sub-circuit method

The built-in MOSFET models in BSIM3v3 are more attuned to the modeling of low-voltage lateral type MOSFETs such as might be encountered in integrated circuits than to the modeling of high-voltage power MOSFETs. These built-in models are not capable of simulating some features of power MOSFET, such as drain-gate capacitance, body-drain diode, pinch effect between cells, and quasi-saturation effect, which are essential to the determination of the device response. In the absence of a suitable built-in model, power MOSFETs are usually simulated by combining the existing built-in MOSFET model with some extra resistance resistive elements such that the combination is able to give a more faithful representation of the

power MOSFETs. In our study, we separate LDMOS into a MOSFET and a drift region which could be simulated by a bias-dependent resistance on drain and gate voltage, so acceptable accuracy for the simulation of HV MOS devices can be obtained by sub-circuit method and the illustration of our concept is shown in Fig. 3.1(a). For ideal case, intrinsic MOS data and R_D data can be obtained directly from MESDRIFT device by sensing K potential while measuring MESDRIFT device. Then, we can easily extract MOS model and R_D model by the processed data measured from MESDRIFT device. Macro model extraction flow is shown in Fig. 3.1(b). In next Section, we show the detail MOS model extraction and the comparison result between measured data and MOS model. Section 3.2.2 shows the detail R_D extraction and the comparison result between measured data and R_D model. Section 3.2.3 shows the initial macro model result compared to the measured IV cures of LDMOS.

3.2.2 MOS model from KPC

From section 2.3, we know that the I-V characteristics of KPC device have the best match with those of LDMOS, so we choose KPC device to get MOS data and R_D data for initial extraction. For MOS data, according to BSIM manual, the following device characteristics must be measured: (1)Ids vs. Vgs at Vds=0.1 volt (deep linear region); (2)Ids vs. Vds at different gate bias (Vgs) for getting a SPICE MOS model. In other words, IkVk and IkVg data are necessary and these data can be obtained by sensing K potential while measuring the IV of KPC device. Fig. 3.2 shows the intrinsic MOS I-V including IkVk and IkVg. Because Vk step is not constant (Vk step does not equal to 0.1V), so we use interpolation to get constant step data. Fig. 3.3 shows the I-V curves after constant step normalization. With these data, we can find out one intrinsic MOS model by using BSIMPro software. The initial extracted BSIM3 MOS parameters are shown in Appendix A. (The BSIM3 parameters are listed in the H-SPICE script.) Fig. 3.4 shows the comparison between intrinsic MOS model and the measured IkVk.

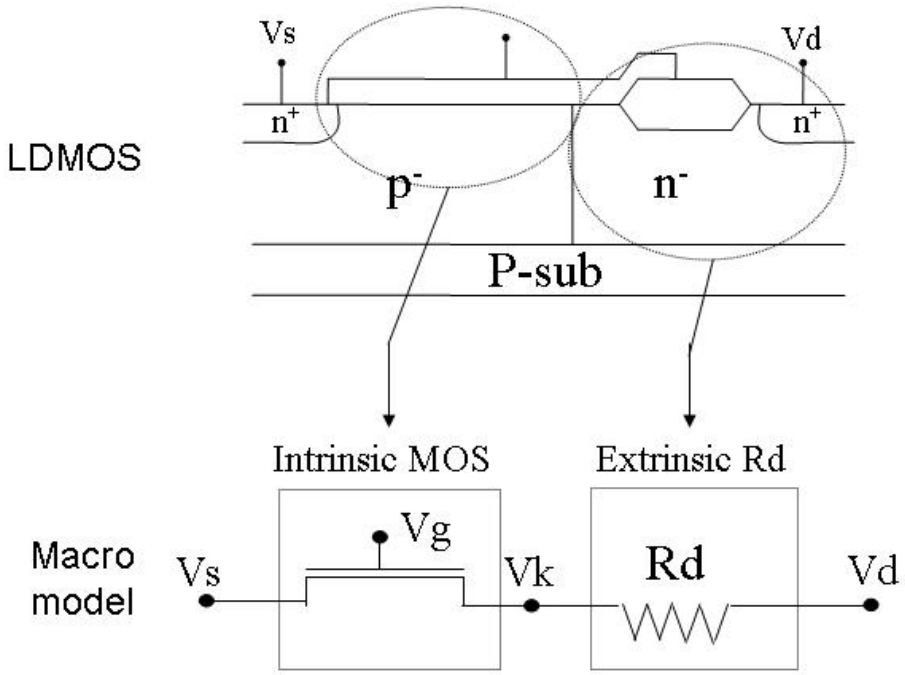


Fig. 3.1(a) Illustration of sub-circuit model concept.

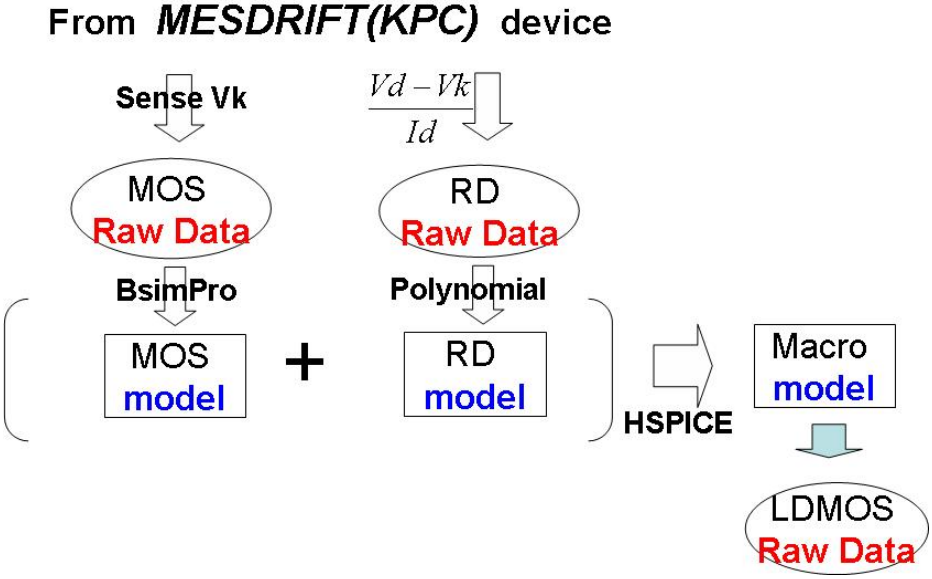


Fig. 3.1(b) Macro model extraction flow from KPC device.

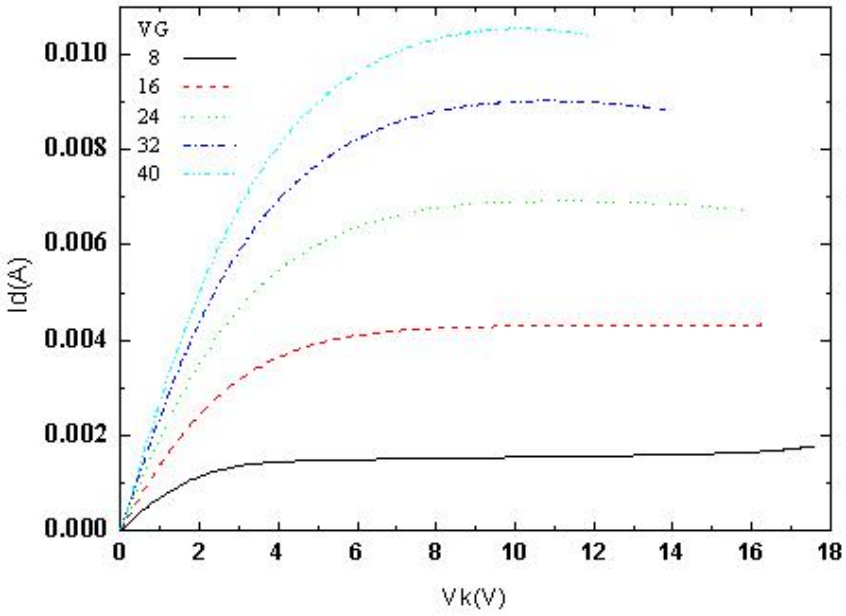


Fig. 3.2 MOS I-V obtained from KPC device.

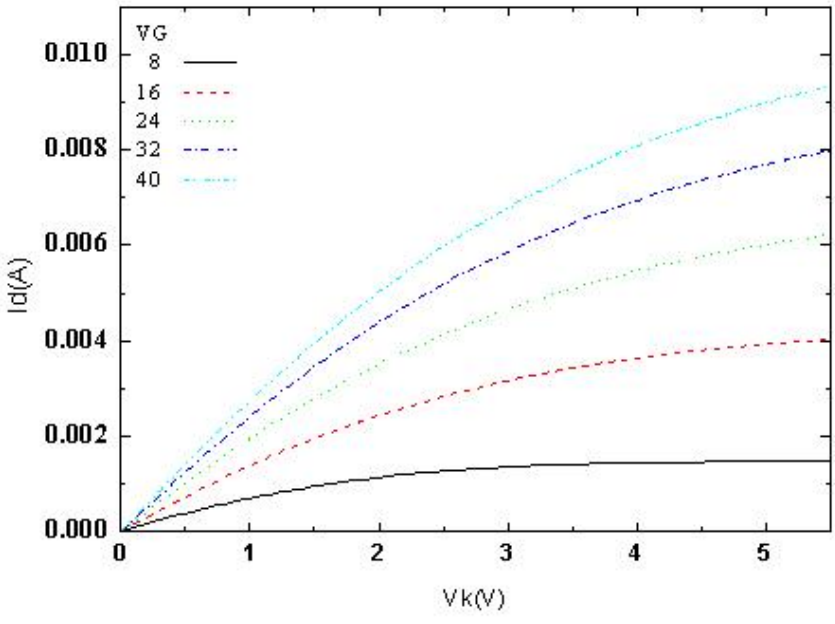


Fig. 3.3 MOS I-V after constant step normalization.

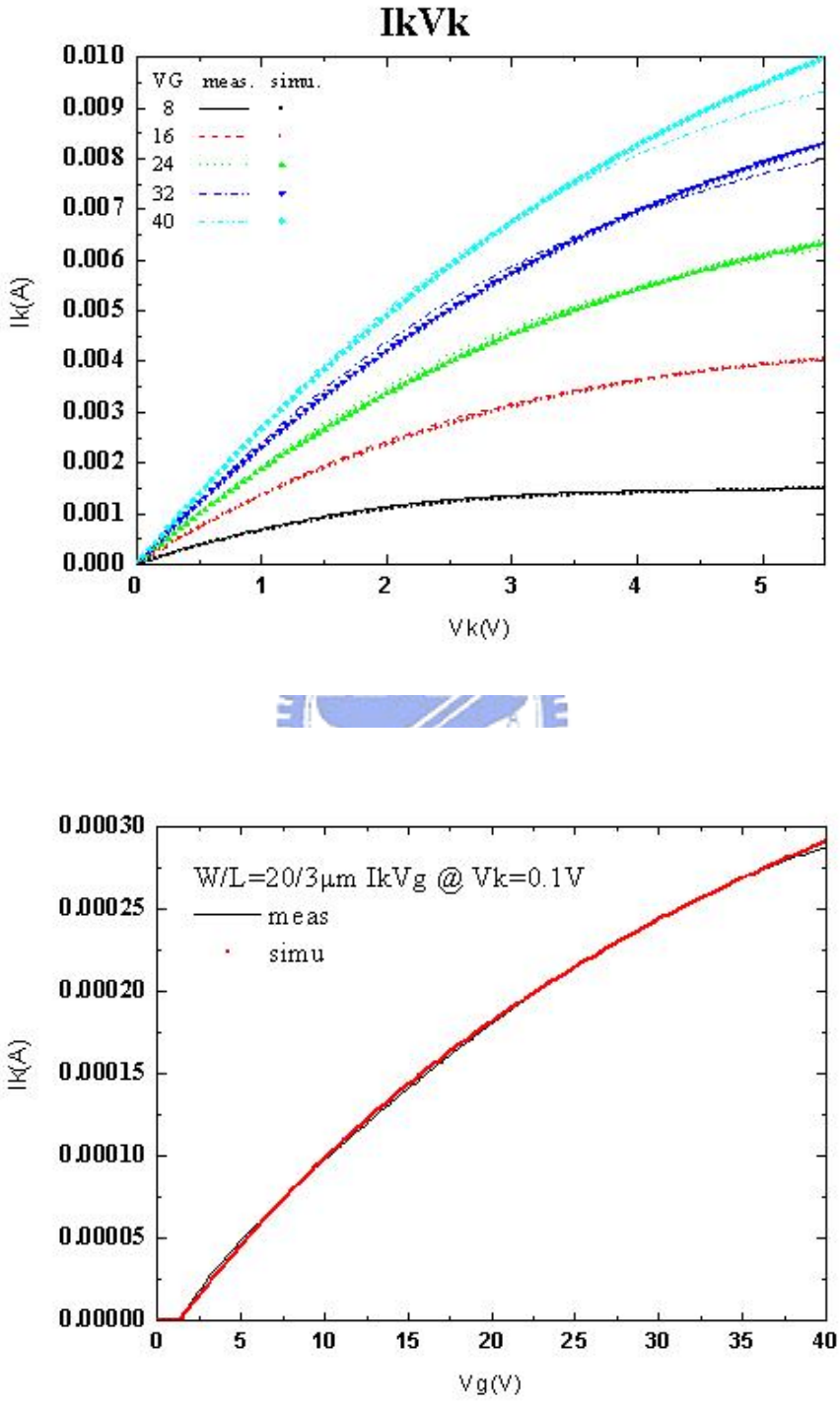


Fig. 3.4 Comparison between MOS model and measured data from KPC device.

3.2.3 R_D model from KPC

Since we have Id, Vg, Vd and Vk data, we can calculate drift resistance with the following equation:

$$Rd = \frac{Vd - Vk}{Id} \tag{3.1}$$

The calculated drift resistance versus Vd at different Vg is shown in Fig. 3.5. It can be seen that the drift resistance (R_D) increases with drain voltage (Vd) and decreases with gate bias (Vg). This can be explained by the concept of intrinsic drain voltage (Vk) that Vk increases with Vd but will tend to reach a saturated small value as Vd keep increasing for the entire bias domain [25]. The fact that the increasing rate of voltage drop across the drift region is lager than that of drain current makes the increase of drift resistance (R_D) with increasing drain voltage (R_D). Besides, Vk also increases with gate bias (Vg) because Vg raise the surface potential [25], making R_D decreasing with Vg. For initial extraction, we choose polynomial function to fit R_D. We make R_D in the following form:

$$R_D = (\alpha_1 + \alpha_2 V_d + \alpha_3 V_d^2 + \alpha_4 V_d^3) \cdot (\beta_1 + \beta_2 V_g + \beta_3 V_g^2 + \beta_4 V_g^3) \tag{3.2}$$

where α_1, α_2, α_3, α_4, β_1, β_2, β_3, and β_4 are model parameters. By using the drift resistance Rd (at a given Vg and Vd) calculated above, we are able to determine these parameters using least square fitting method. We can see that a very good fit is obtained at high Vg, but under small gate bias some discrepancy between the measured and simulated data can be seen as shown in Fig. 3.5. This may be caused by not well enough R_D function form. Combine MOS model and R_D model obtained above, we get a macro model of LDMOS. Fig. 3.6 shows the comparison between macro model simulation I-V and measured I-V. We can see that I-V curves match well at linear region but there is a large difference at saturation region. The discrepancy at saturation region may probably be caused by MOS model error at high Vd and no good enough R_D function. The calculated R_D at low Vg may be incorrect at low Vg because of the contact implant influence. For IdVg cure, we can see oscillation in macro model. Consequently, we need to do some modification in this method. In next

section, we will demonstrate how to improve this method.

3.3 Modified R_D Model

3.3.1 Reverse calculated Rd data

Because we still can't find out one set of intrinsic MOS model parameters to fit these data which have been eliminated the quasi-saturation effect by measuring KPC device, we adjust calculated R_D for macro model to fit LDMOS data. The concept picture is shown in Fig. 3.7. Once we get intrinsic MOS model from KPC measurement, we can use LDMOS I-V to reverse calculate R_D data. Fig. 3.8(a) shows reverse calculated Vk characteristics. At high Vg , reverse calculated R_D corresponds to the measured one from KPC device, but at low Vg reverse calculated R_D is larger than measured one. This results from the reducing R_D at low Vg because of the contact implant. With these data, we can find out R_D model parameters by least square fitting method. Fig. 3.9 shows the comparison between modified R_D model which is in polynomial form and reverse calculated R_D data. We can see that there is a very good match over the all range. Then, we combine MOS model and modified R_D model, so we get our modified macro model. Fig. 3.10 shows the result which is a very good fitting with a mean error of less than 5%.

3.3.2 Vk derivation for simplifying R_D

In order to improve R_D model and to eliminate the oscillation in IdVg at low drain bias, we attempt to derive R_D formula with Vk concept. From equation (3-1), we know that once we get Vk function, we obtain R_D formula. The overall extraction flow with reverse calculated Vk concept is shown as Fig 3.11. From Fig 3.8(a), we see that Vk versus Vd curves at different gate bias and we find that Vk tend to saturate as Vd reach certain value. The point of Vk saturation indicates that depletion region increasing with Vd bias covers K implant region, so Vk potential keeps in the same value. Therefore, we assume Vk have the following function form:

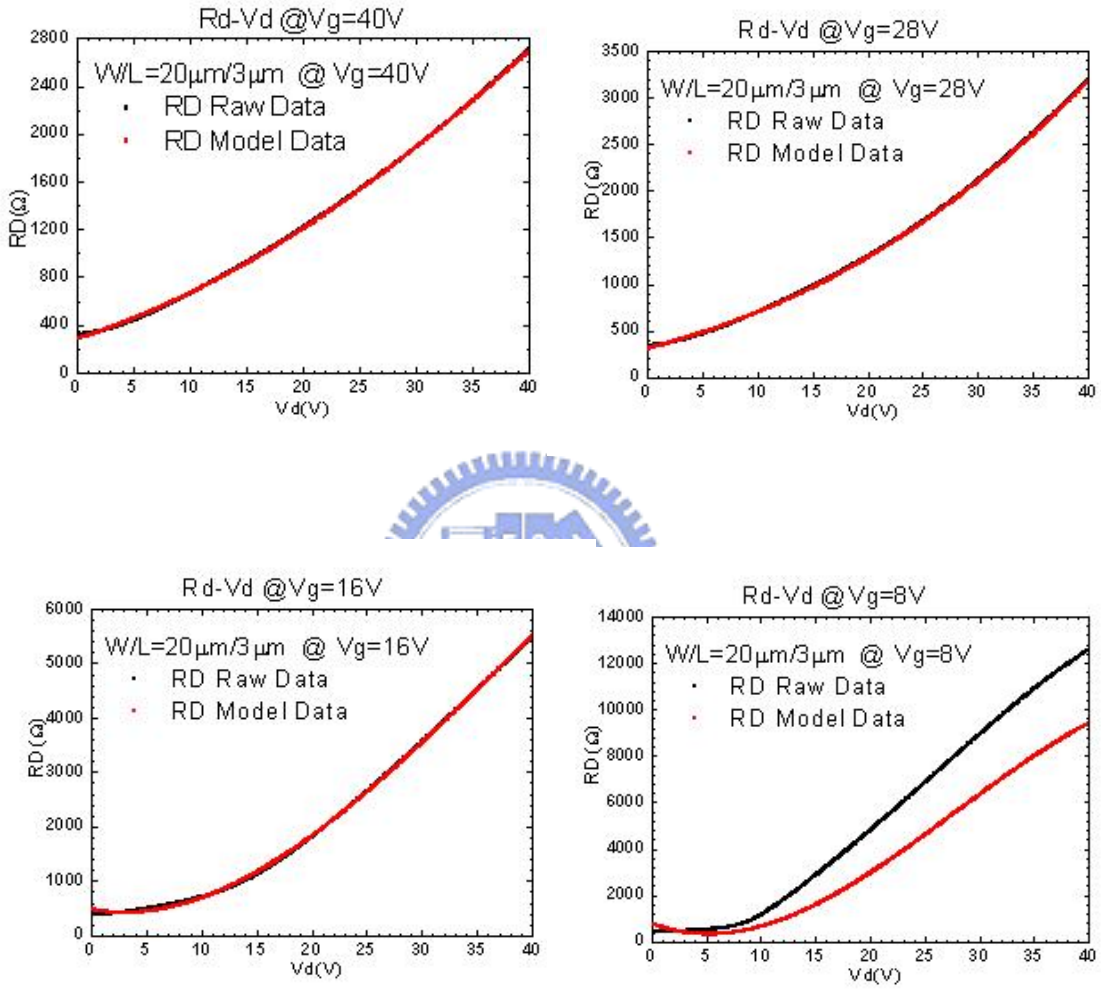


Fig. 3.5 Comparison between Rd model (polynomial function form) and measured Rd from KPC device by equation (3-1)

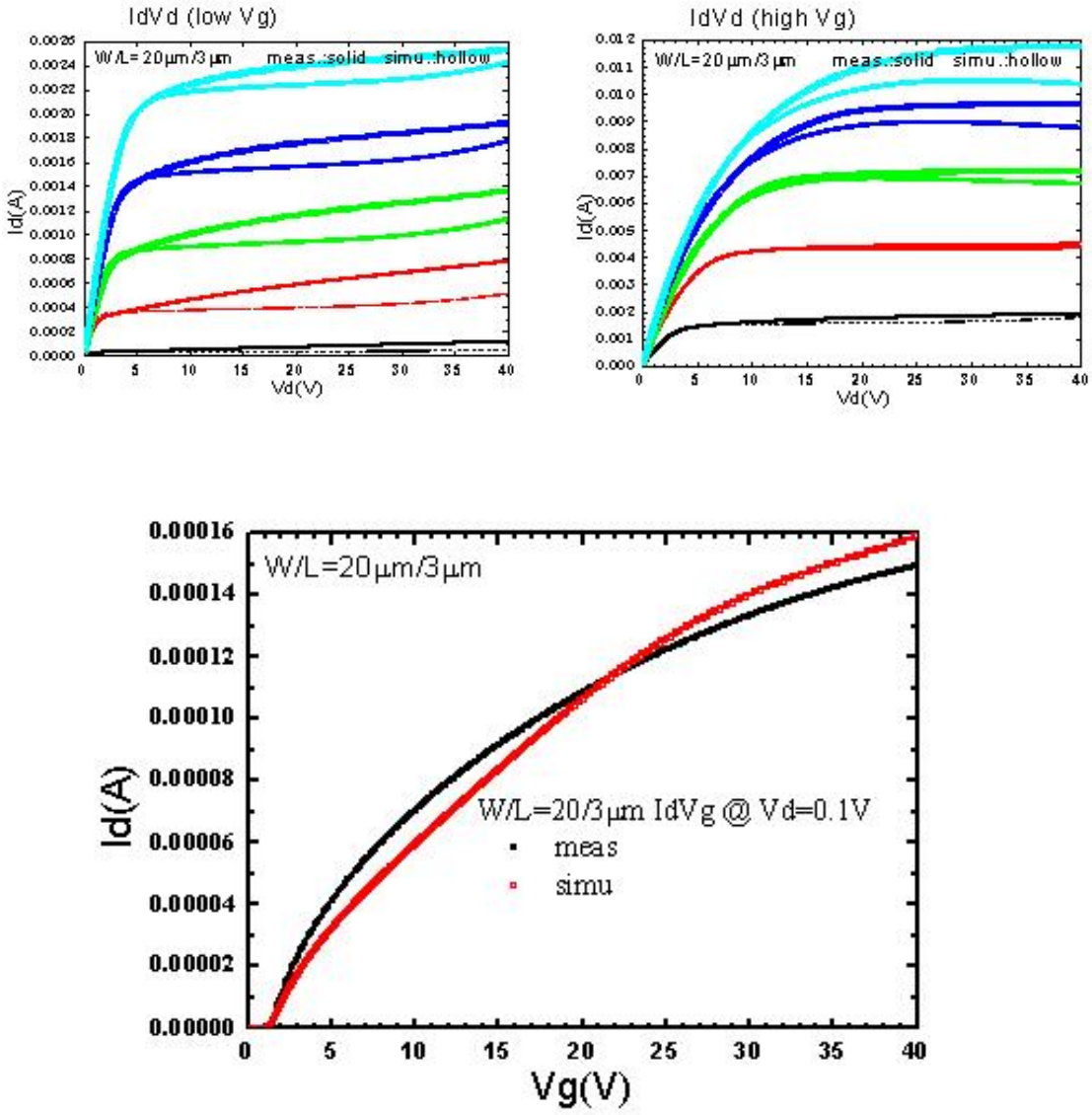


Fig. 3.6 Comparison result between initial macro model and measured I-V of LDMOS

$$V_K = \alpha \cdot \tanh(\frac{slope}{\alpha} \cdot V_d) \quad \textbf{(3.3)}$$

Such a function form has a shape like Fig 3.8(a). Parameters α and slope in equation (3.3) are function of Vg and we define **α** as the saturation Vk values and **slope** as the slopes of Vk versus Vd curves in linear region. Because Vk has more complicated mechanism on gate bias than drain bias, we use numerical method to deal with such a problem. We make that:

$$\alpha = \alpha_1 \cdot \mathrm{VG}^{\alpha_2} \quad \textbf{(3.4)}$$

$$slope = \mathrm{s}_1 + \mathrm{s}_2 \cdot \exp(\mathrm{s}_3 \cdot \mathrm{VG}) \quad \textbf{(3.5)}$$

From Fig. 3.8(b) and (c) we can find α and slope values use and we can also determine these parameters α_1, α_2, S_1, S_2, and S_3 by statistical regression. Finally, we have Vk in following form:

$$V_K = (\alpha_1 \cdot \mathrm{VG}^{\alpha_2}) \cdot \tanh\{\frac{[\mathrm{s}_1 + \mathrm{s}_2 \cdot \exp(\mathrm{s}_3 \cdot \mathrm{VG})]}{(\alpha_1 \cdot \mathrm{VG}^{\alpha_2})} \cdot V_d\} \quad \textbf{(3.6)}$$

Hence, R_D is in the form:

$$Rd = \frac{V_d - (\alpha_1 \cdot \mathrm{VG}^{\alpha_2}) \cdot \tanh\{\frac{[\mathrm{s}_1 + \mathrm{s}_2 \cdot \exp(\mathrm{s}_3 \cdot \mathrm{VG})]}{(\alpha_1 \cdot \mathrm{VG}^{\alpha_2})} \cdot V_d\}}{I_D(MOS)} \quad \textbf{(3.7)}$$

where I_D(MOS) means the MOS current at given Vd and Vg. Table. 3.1 shows the extracted parameters values of Vk formula and Fig. 3.12 shows the comparison between simulation of Vk formula and reverse calculated Vk data. Fig. 3.13 shows the comparison between macro model using tanh function and LDMOS measurement data. The results present excellent match with a mean error of less than 2%.

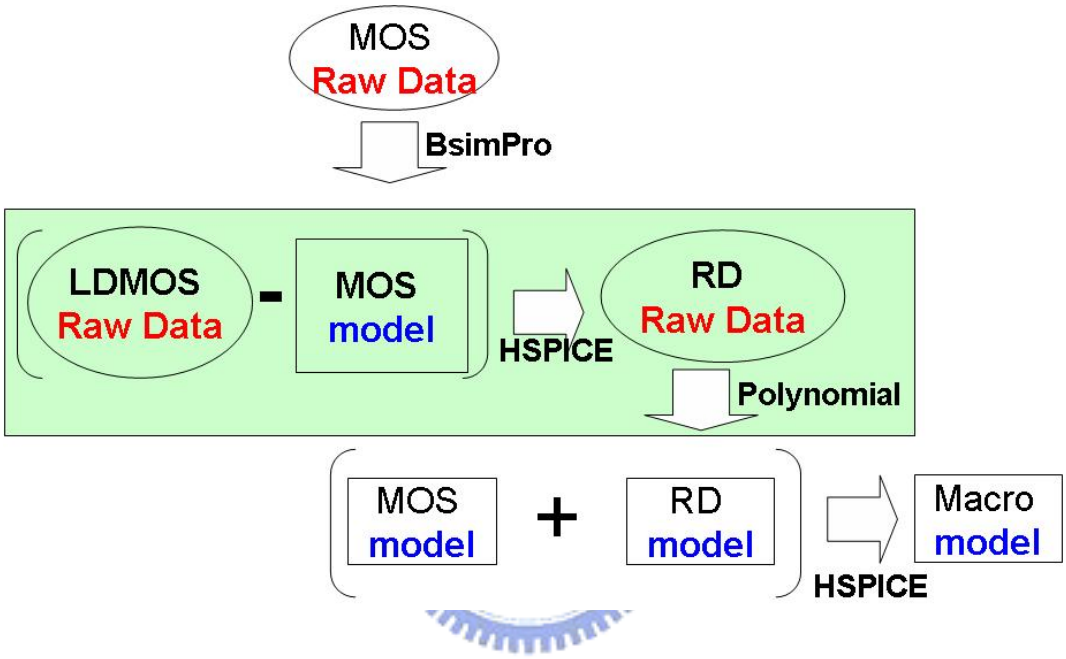
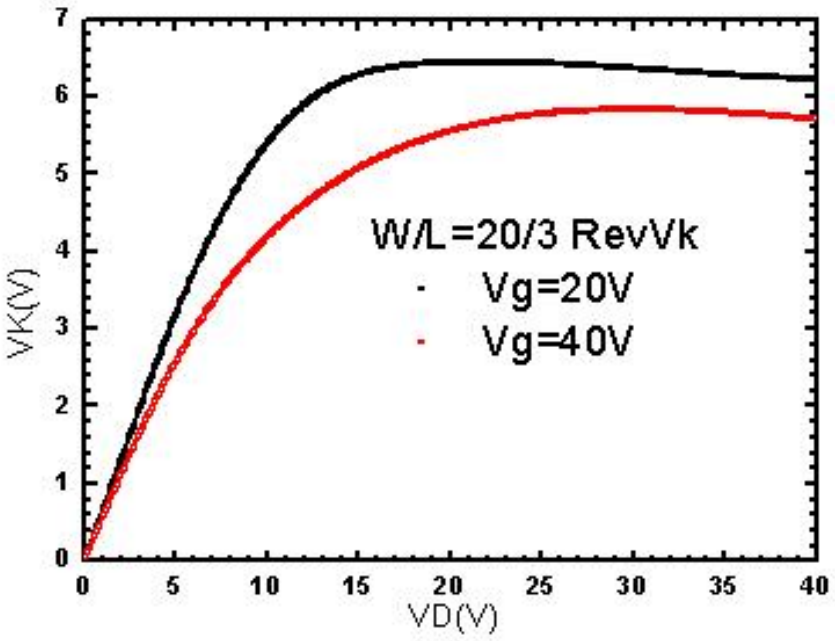
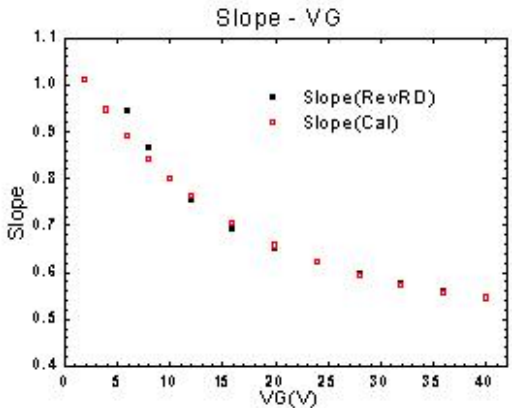


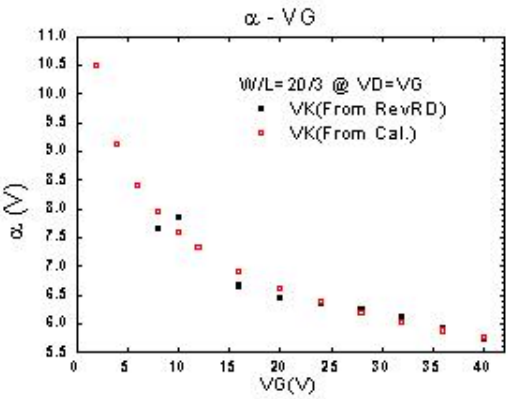
Fig. 3.7 Reverse calculated Rd overall extraction of macro model.



(a)



(b)



(c)

Fig. 3.8 Reverse calculated VK characteristics.

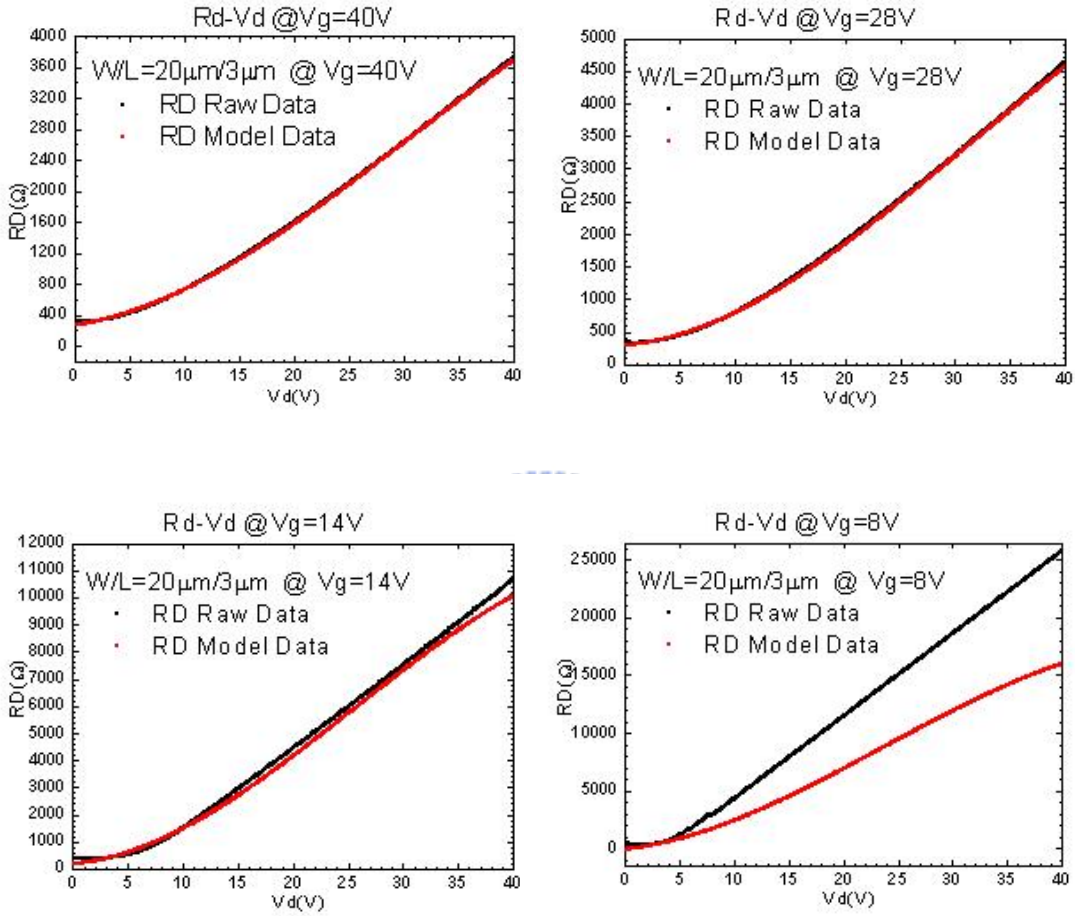


Fig. 3.9 Comparison between modified Rd model (polynomial function form) and reverse calculated Rd data.

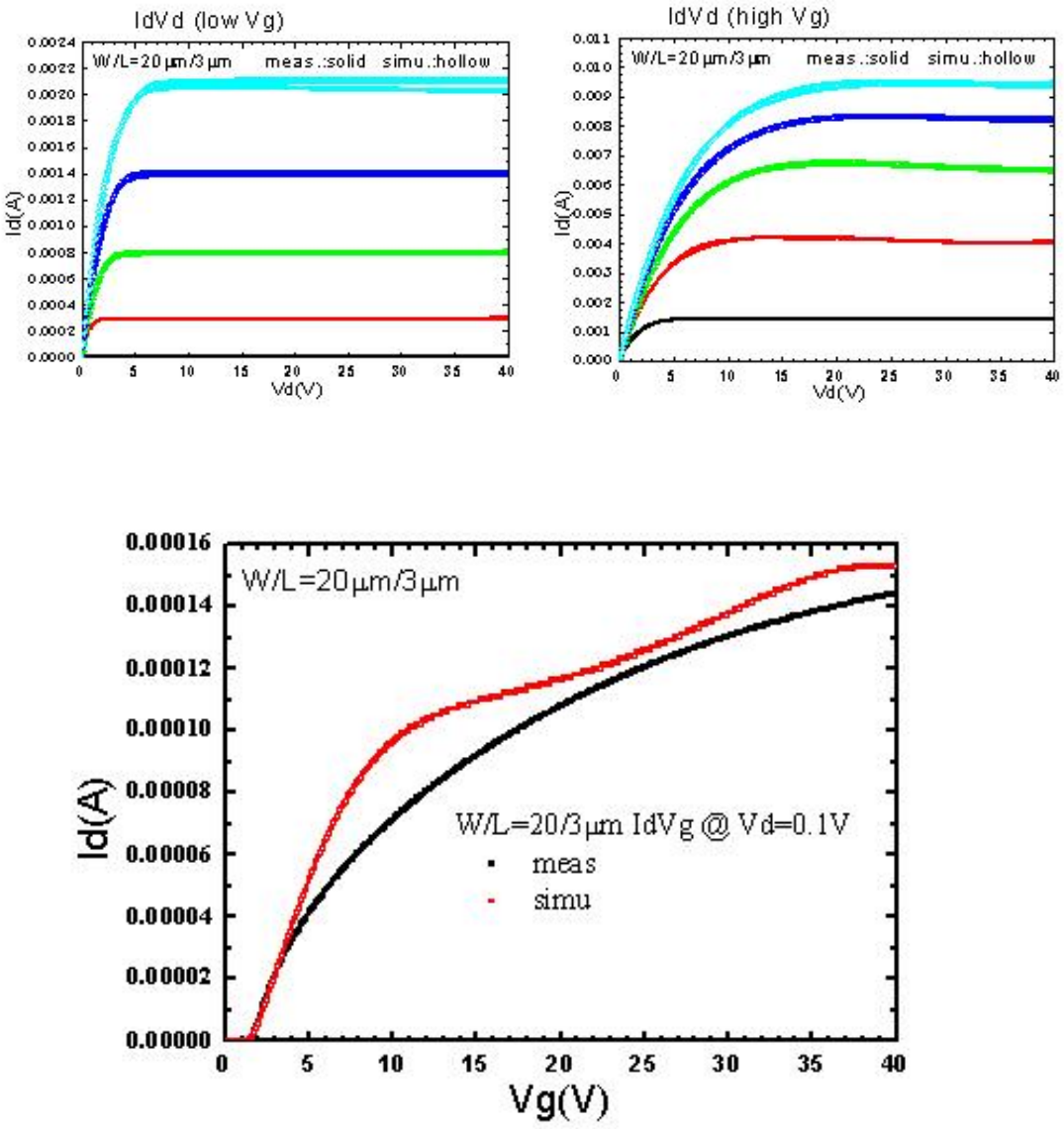


Fig. 3.10 Comparison between modified macro model (with polynomial Rd) and measured I-V of LDMOS.

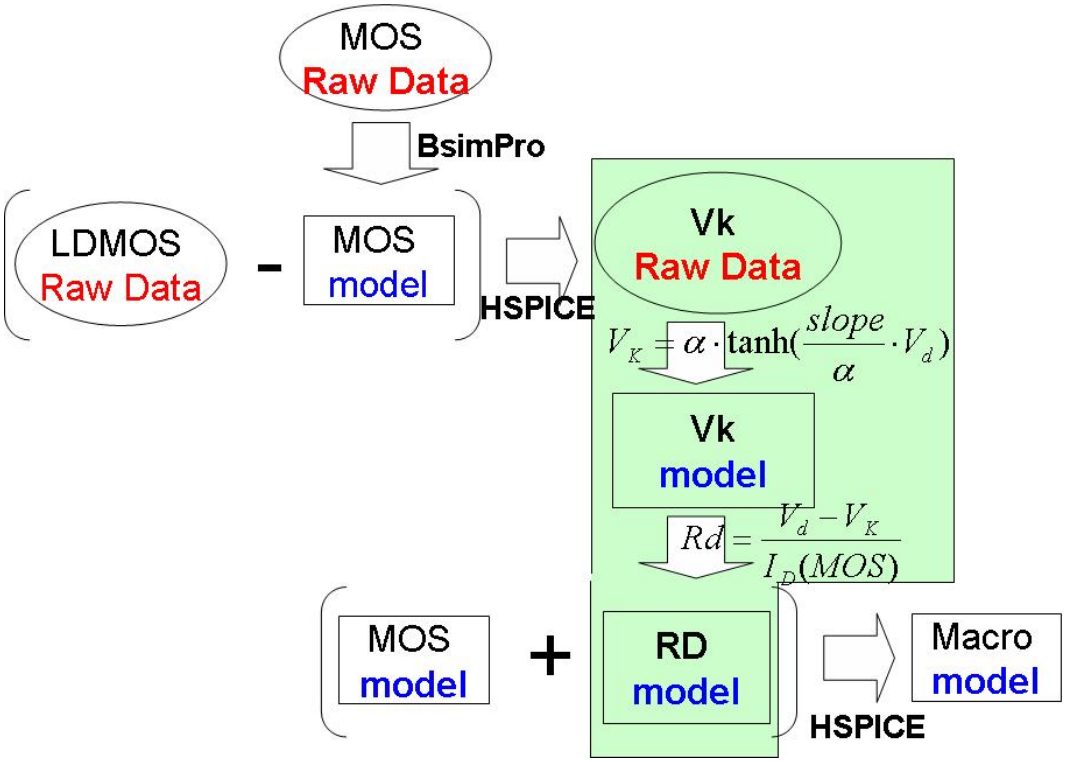


Fig. 3.11 Reverse calculated VK model concept overall extraction flow of macro model.

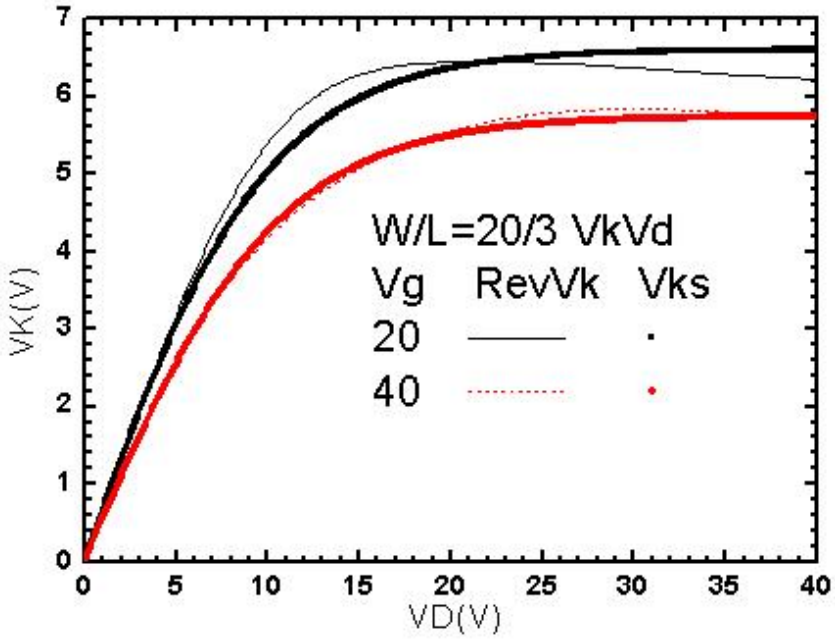


Fig. 3.12 Comparison between Vk formulas (tanh function form) and reverse calculated Vk data.

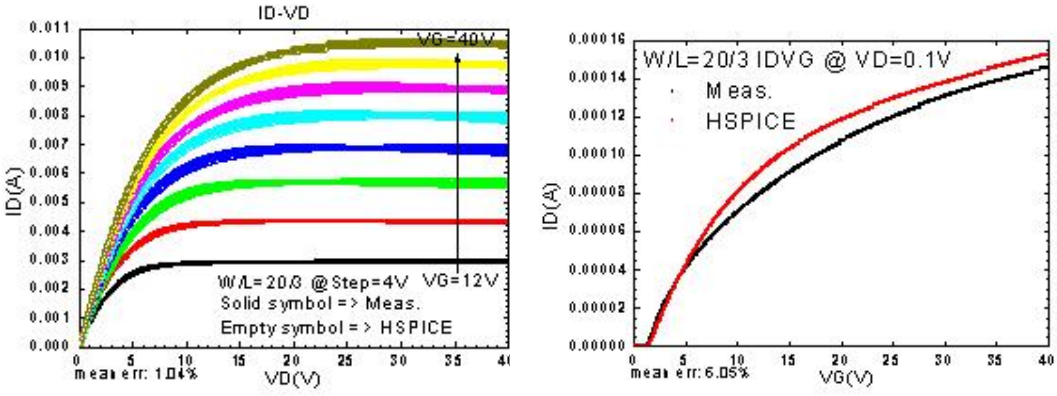


Fig. 3.13 Comparison between modified macro model (with tanh Rd) and measured I-V of LDMOS.

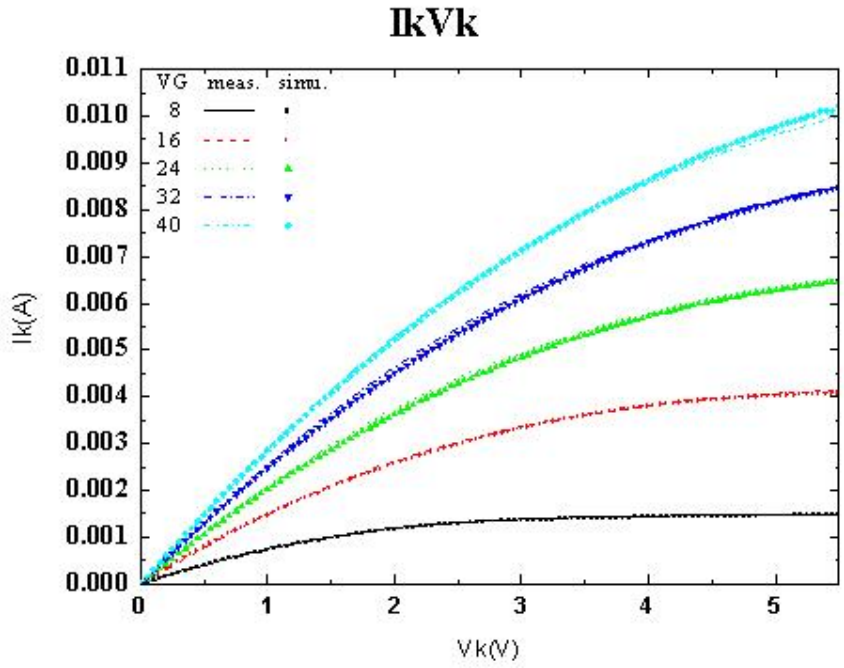
3.4 Modified MOS Model from KL Device

3.4.1 MOS model by KL device

Section 3.2 and section 3.2 present an overall extraction flow of LDMOS by using KPC device. But it's time-consuming for MOS model extraction because of the constant step normalization, so we propose another method to get MOS data by using KL device. Because the K contact area of KPC device is too small so that we can't directly apply voltage to K contact. Hence, we use KL device because the K contact of KL device has large enough contact area to sustain voltage. Then we can directly apply voltage to the K contact and measure K contact current which indicates that IkVk and IkVg data can be directly measured by using KL device. Now it becomes easier to get MOS data and we can use extractor software to get MOS model. Fig. 3.14 shows the comparison between MOS model and measured data extracted from KL device. It has a good match.

3.4.2 Reverse calculated R_D model and macro model by KL device

After MOS model is obtained, we can use the method mentioned in section 3.3.1 and 3.3.2 to get R_D model. Fig. 3.15 shows Vk formula comparison results. We can see that at high gate bias a very good match is obtained, but at low gate bias some discrepancy between the measured and simulation of R_D and Vk occur. This may be caused by the instability of contact line implant. Combine MOS model and R_D model obtained above and then we get a macro model. The final results are shown as Fig. 3.16.



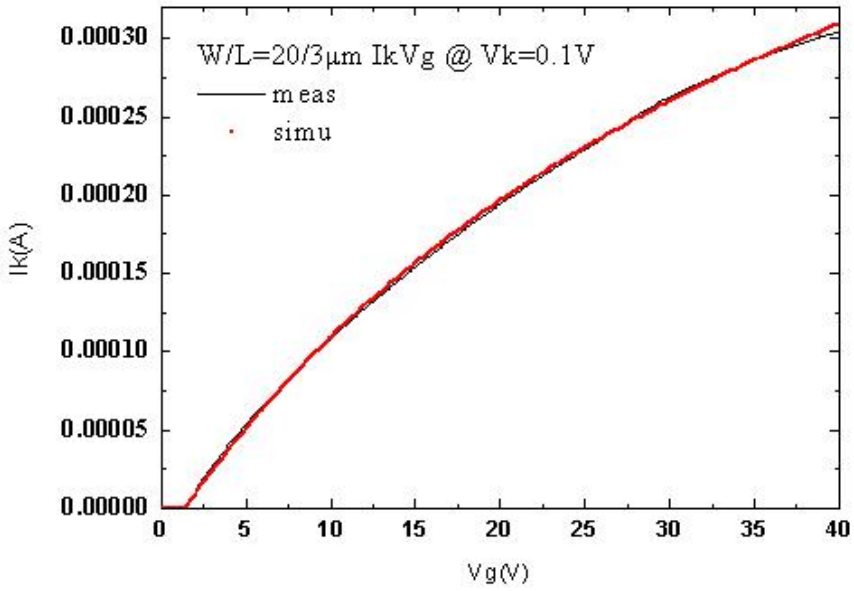


Fig. 3.14 Comparison between MOS model and measured data from KL device.

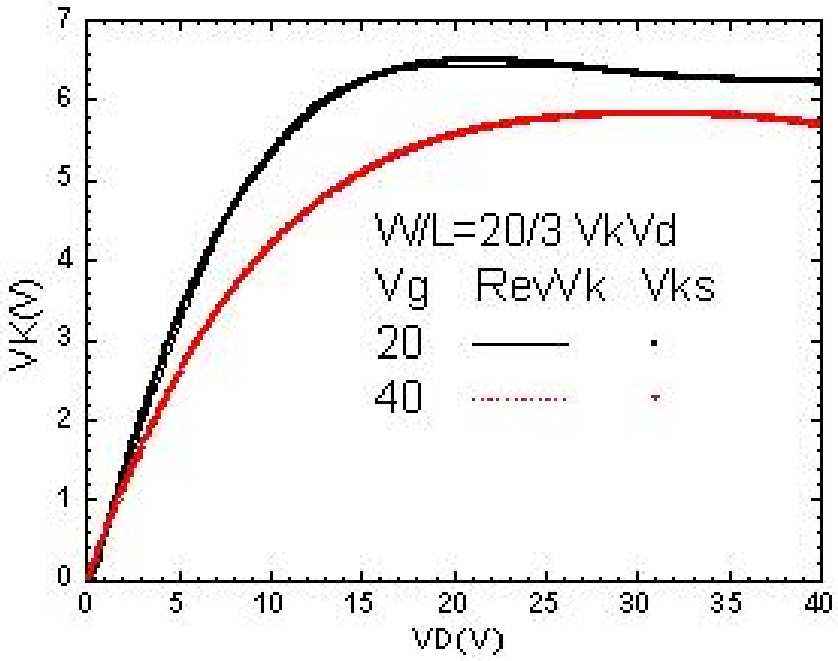


Fig. 3.15 Comparison between calculated Vk (with tanh function form) and reverse calculated Vk data.

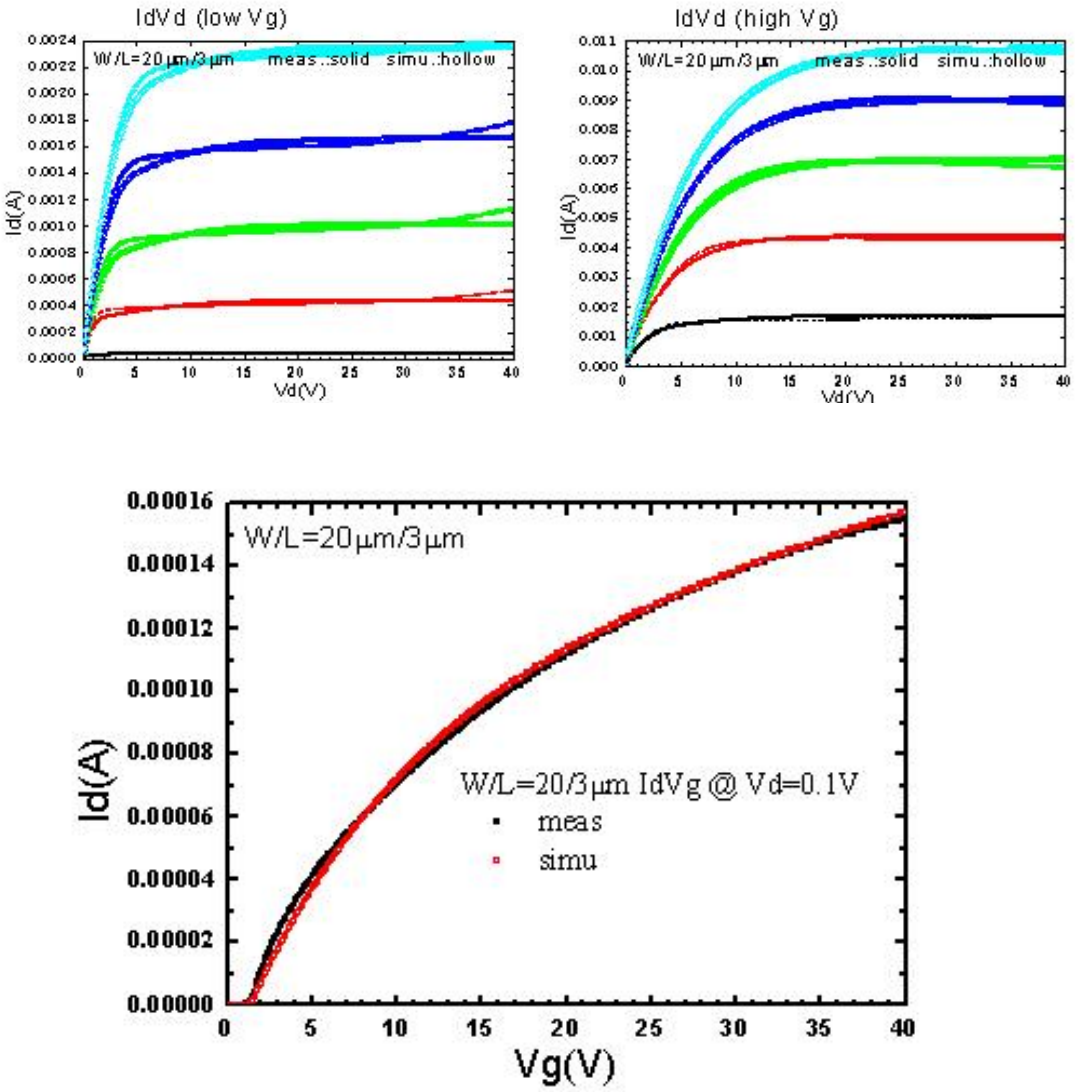


Fig. 3.16 Comparison between modified macro model (with tanh Rd) and measured I-V of LDMOS.

Chapter 4

Self-Heating Effect of LDMOS

4.1 Introduction

This chapter reports on the self-heating effect (SHE) [26] characterization of LDMOS and a simple pulsed-gate experiment is proposed and the influence of pulse duration are analyzed. SHE results in a reduction of the drain current and the well-know negative output conductance effect [27]. Some other interesting reports on SHE characterization and its modeling originate from the SOI MOS devices where this effect is particularly critical. Despite these efforts, there is a lack of simple yet efficient model to describe the SHE. The aim of our work is to investigate the impact of SHE and propose simple models to illustrate the behavior of SHE in LDMOS.

4.2 Simulation of temperature profile

Temperature profiles inside LDMOS devices arising from self-heating are simulated using TCAD simulator shown as Fig. 4.1. Fairly uniform temperature profiles were found in devices with uniformly doped drift region, which is consistent with the power dissipation profile inside the device [28]. The heat generated inside device while operation does not easily disperse due to the field plate, so at FOX (field oxide) region it has high temperature. Near bird's beak it has the highest temperature because of the current crowding. Fig. 4.1 also shows that the higher gate bias gets the higher temperature. It is because the higher gate bias gets the more current and power. Hence more heat is generated inside device which contributes to higher temperature.

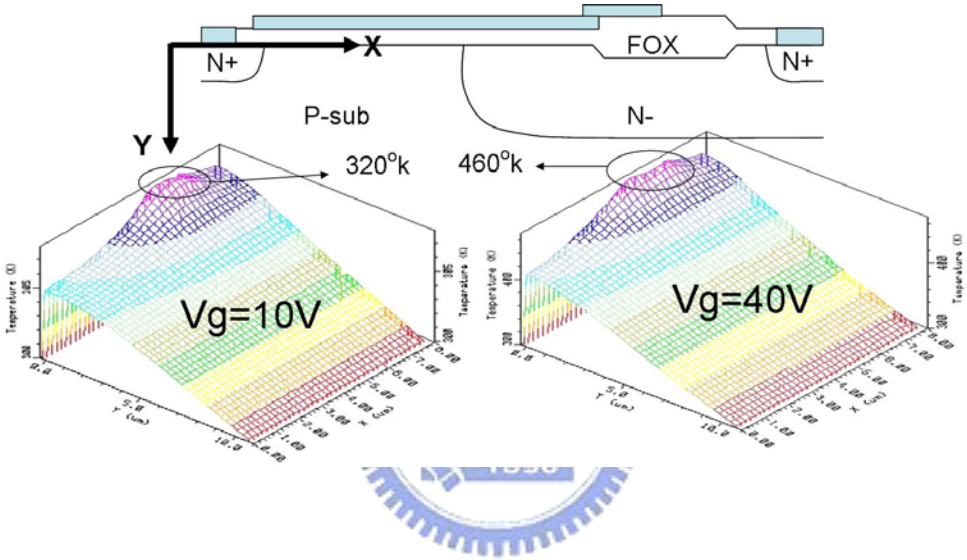


Fig. 4.1 Simulation of temperature profile inside LDMOS.

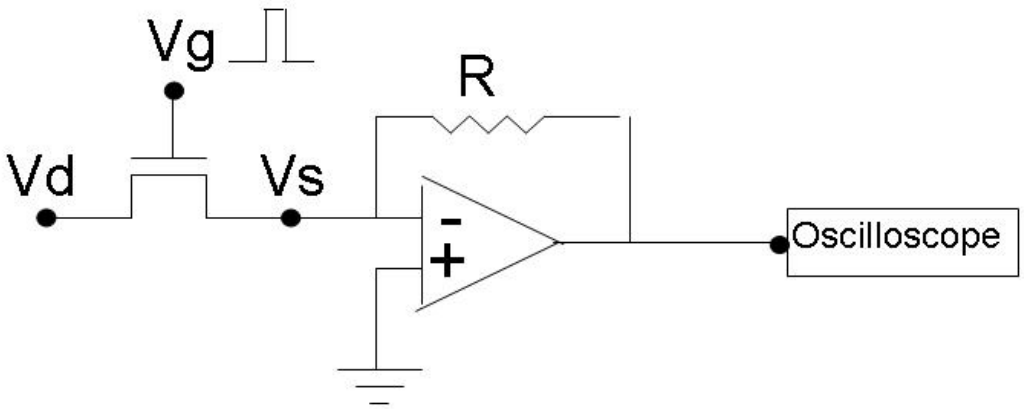
4.3 Measurement Set-up and Experiment Result

Various pulsed measurements aimed to access the HV and SOI MOSFET characteristics without SHE have been reported in previous works [27]. In general, such measurement set-up requires a dedicated and expensive configuration since this can not be achieved with semiconductor parameter analyzers (where integration time exceeds 80μs and much faster pulses are requested to avoid SHE). Herewith, we have used a simple yet efficient test configuration able to measure the characteristics of the HV devices without SHE (Fig. 4.2) and investigate SHE as function of the pulse duration and the power. A pulse generator is used to turn on and off the transistor by applying a square signal on the gate. The drain is biased by a high voltage generator. One OP amplifier and resistor are used in parallel. The minus input of OP amplifier is connected to the source of the transistor while the plus input is ground to make sure the source of the transistor virtual ground. A digital memory oscilloscope that triggers the signal applied on the gate is used for monitoring the voltage variations on the output of the OP amplifier.

The proposed measurement setup relies on the on-off transitions of the HV transistor. The oscilloscope triggers the rising edge of the gate signal (the driving signal), while the output of the OP amplifier is synchronously monitored on the other channel. The output voltage is recorded as function of time by the oscilloscope. A typical response of the transistor is presented in Fig. 4.3. The .drain current is simply calculated by:

$$Id = \frac{-Vo}{R} \qquad \textbf{(4.1)}$$

We can see that drain current decreases with the increasing of pulse width. Because the longer the channel turns on, the more heat it generates, mobility hence is affected due to the high temperature. Such a result leads to the decreasing of drain current. Fig. 4.4 shows the IdVd comparison measured between by pulse generator and by HP4155C. When the gate bias is higher, then the SHE gets more serious because of the more heat generated. For different width and length, we find that SHE



Vg : pulse (HP8114)　　Vd : constant bias (HP4155C)

Fig. 4.2　Measurement set-up of pulse mode to investigate SHE.

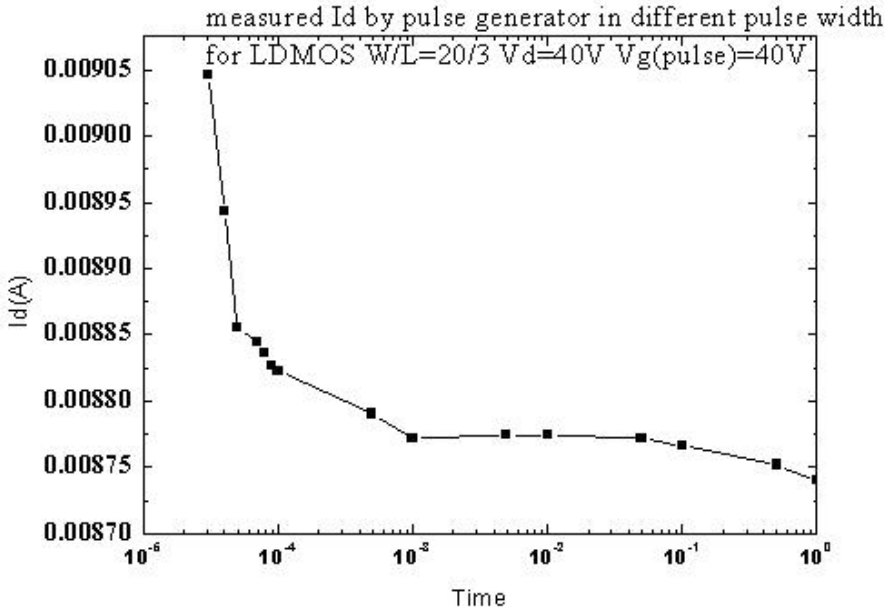


Fig. 4.3 Measured Id by pulse mode for different pulse width at VG=40V and VD=40V.

is the most serious on device which has the shortest length and widest width as shown in Fig. 4.5. This results from the high current density.

4.4 Simple Time Model and Simple Power Model

In order to derive simple models to describe the SHE, we investigate the drain current degradation as measurement time (heating time) on Vd dependence and on Vg dependence as shown in Fig. 4.6(a), Fig. 4.7(a) in linear scale and Fig. 4.6(b), Fig. 4.7(b) in log scale, and we can find that Id degradation has the trend:

$$y = \gamma \cdot x + \beta \tag{4.2}$$

$$y = \ln\left(\frac{\Delta Id}{Id_{10ms}}\right) \tag{4.3}$$

$$x = \ln(t) \tag{4.4}$$

where γ means the slope and β means the intercept. Therefore, we have the following result:

$$Id(t) = Id_{10ms} \cdot [1 + e^{\beta} \cdot t^{\gamma}] \tag{4.5}$$

where Id_{10m} means the measured drain current for 10 ms pulse width. Fig. 4.8 shows the comparison between the model derived above and the measured data and Table. 4.1 shows the values of model parameters.

For power model, we investigate the drain current degradation dependence on power. Fig. 4.9 shows the power dependence of SHE. We know that SHE is directly dependent on the power dissipated by the device [29], [30], and the more the power dissipated the SHE gets more serious. From Fig. 4.9 we find it the following form:

$$\frac{\Delta Id}{Id_{100ms}} = \theta \cdot P_D \tag{4.6}$$

$$Id_{2\mu s} = Id_{100ms} \cdot [1 + \theta \cdot Id_{100ms} \cdot Vd] \tag{4.7}$$

where θ=0.1275 and Id_{100m} means the measured drain current for 100 ms pulse width. Fig. 4.10 shows the comparison between simple power model and the measured data. From Fig. 4.8 and Fig. 4.10, we have excellent match with the measurement data. With these models, we can predict the values without SHE for advanced investigation.

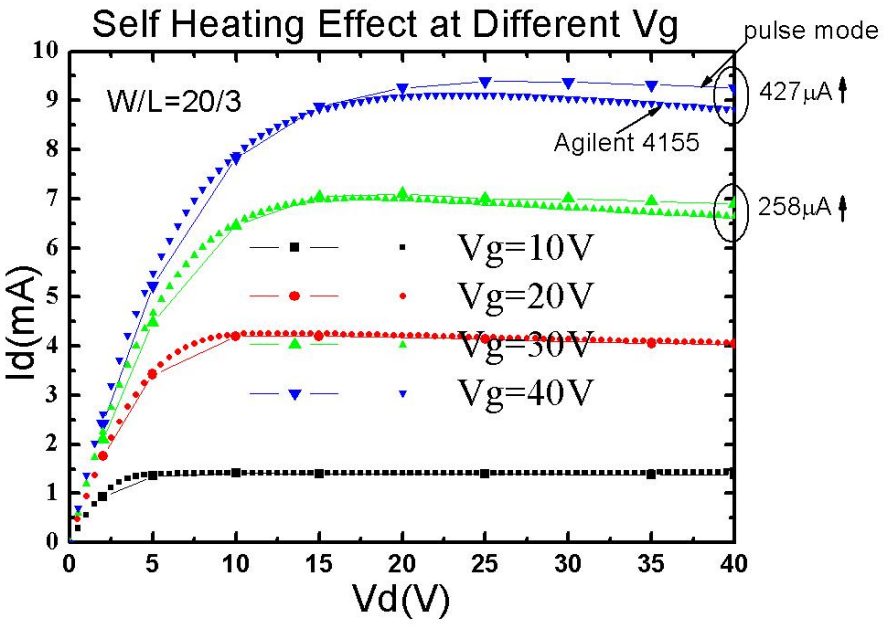


Fig. 4.4 Comparison of IDVD measured between by pulse mode and HP4155 for different VG and VD.

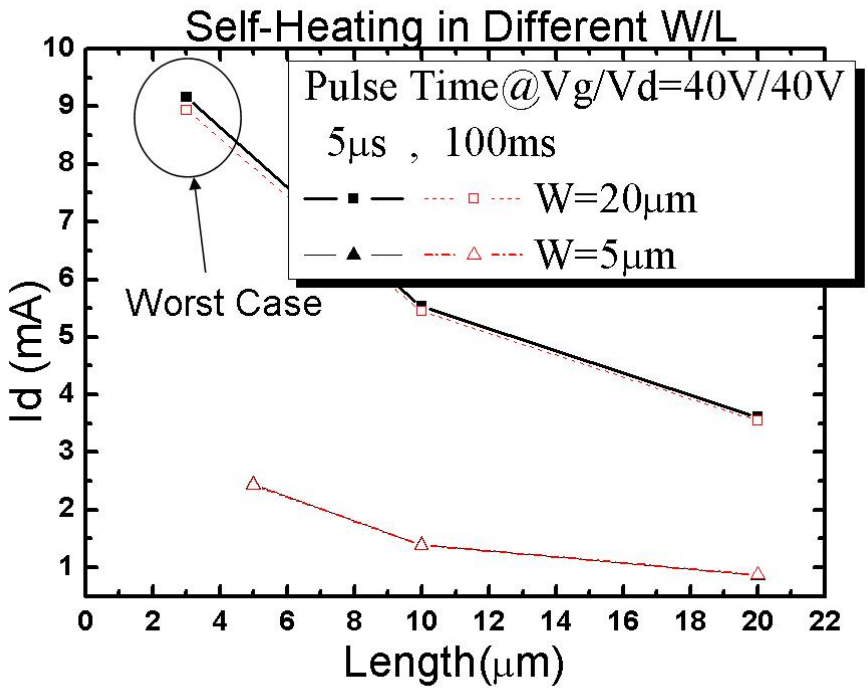


Fig. 4.5 SHE comparison on different width and length @ Vg/Vd=40V/40V.

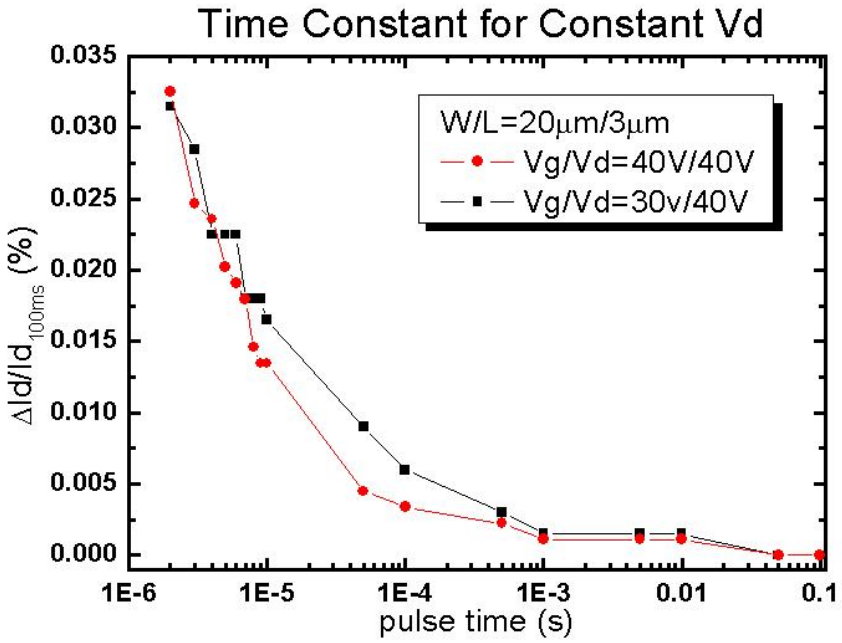


Fig. 4.6(a) Id degradation in linear scale vs. measurement time (heating time) at constant Vd.

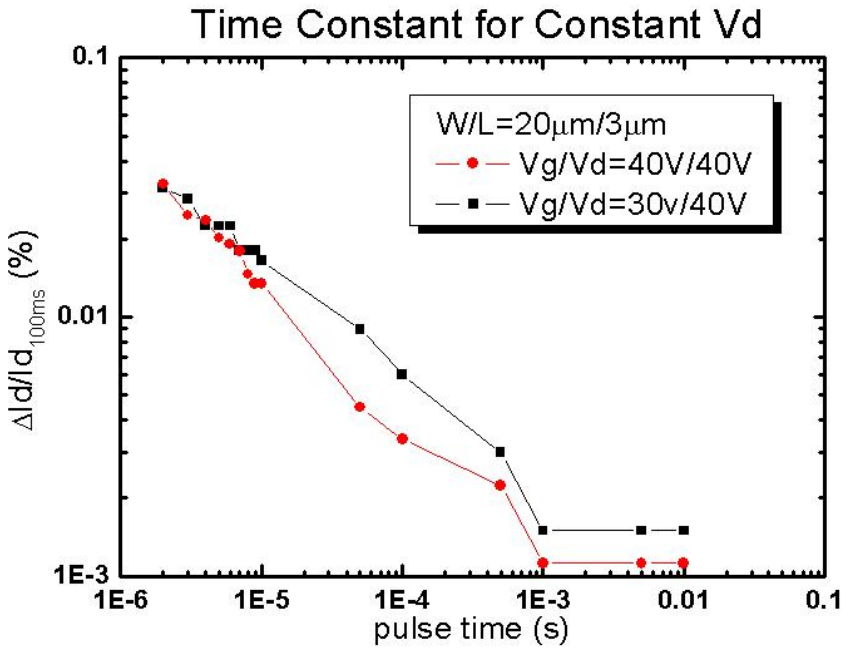


Fig. 4.6(b) Id degradation in log scale vs. measurement time (heating time) at constant Vd.

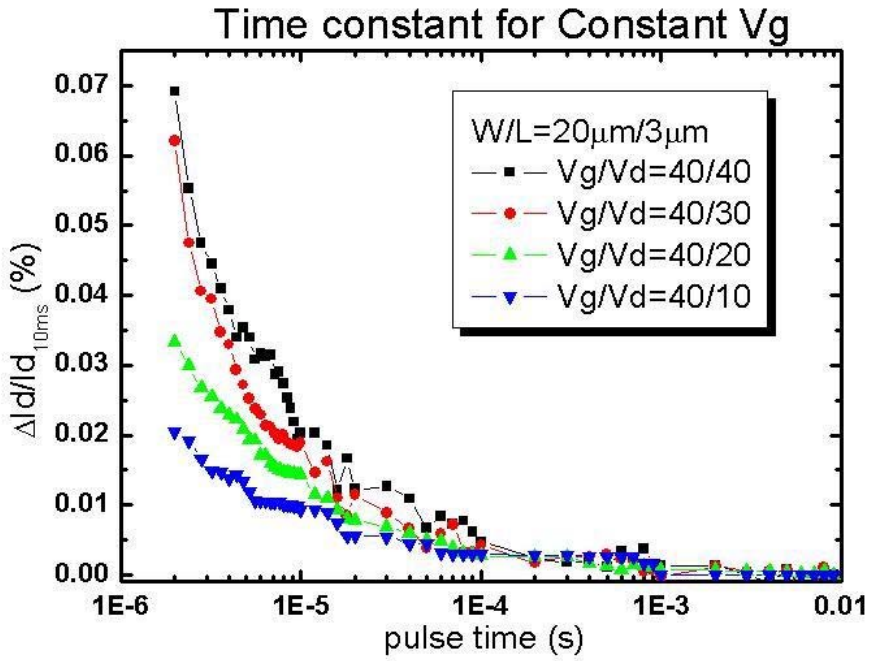


Fig. 4.7(a) Id degradation in linear scale vs. measurement time (heating time) at constant Vg.

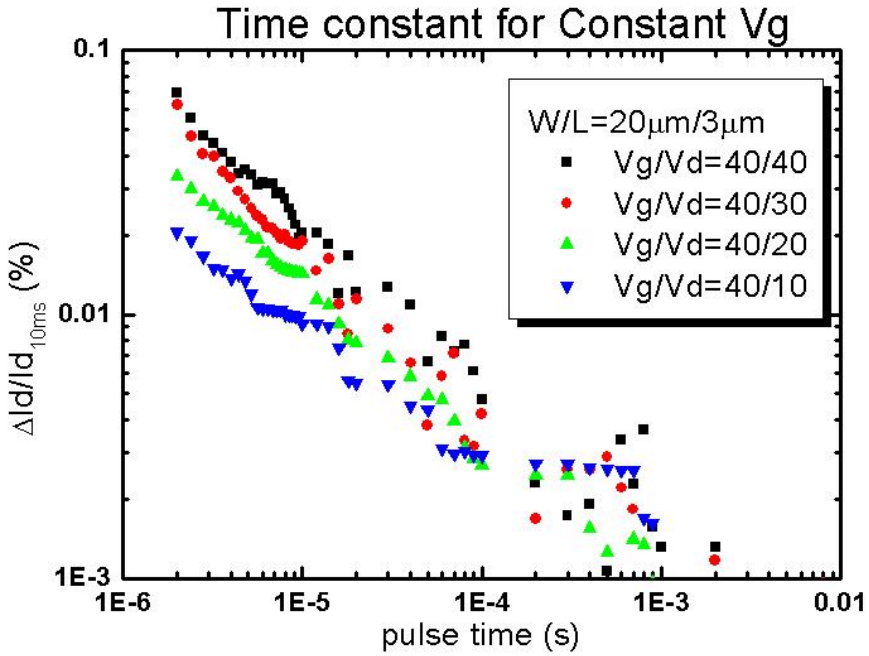


Fig. 4.7(b) Id degradation in log scale vs. measurement time (heating time) at constant Vg.

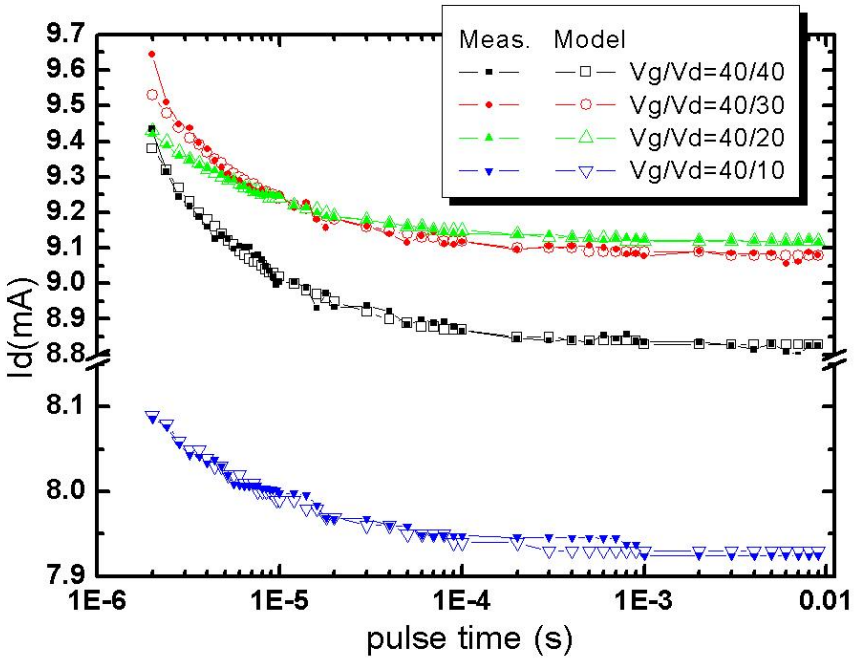


Fig. 4.8 Comparison between simple time model and the measured data.

Vg/Vd	γ	b
40/40	-0.613	-10.861
40/30	-0.5894	-10.861
40/20	-0.5649	-10.861
40/10	-0.5333	-10.861

Table. 4.1 Simple time model parameters used above.

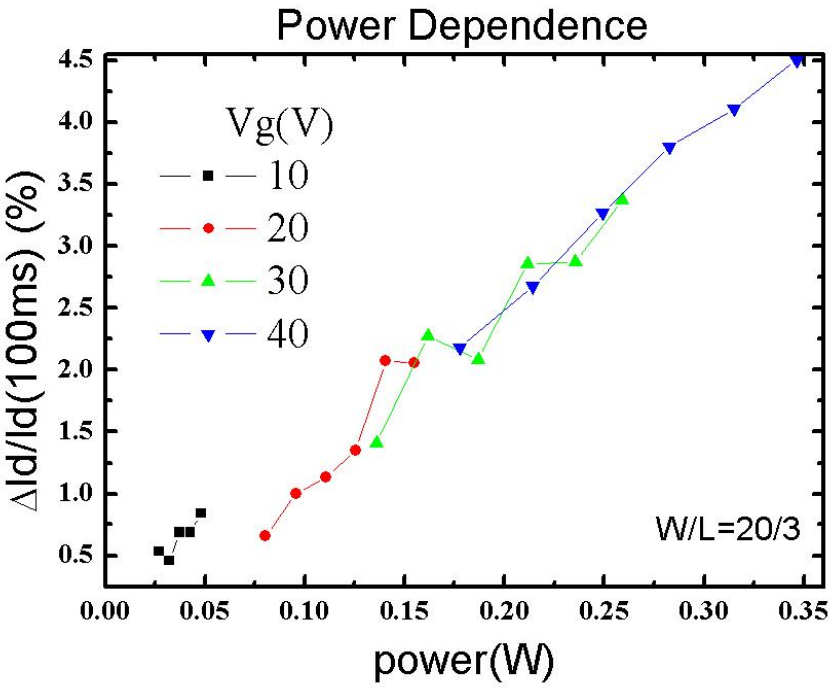


Fig. 4.9 Power Dependence for Different Vg.

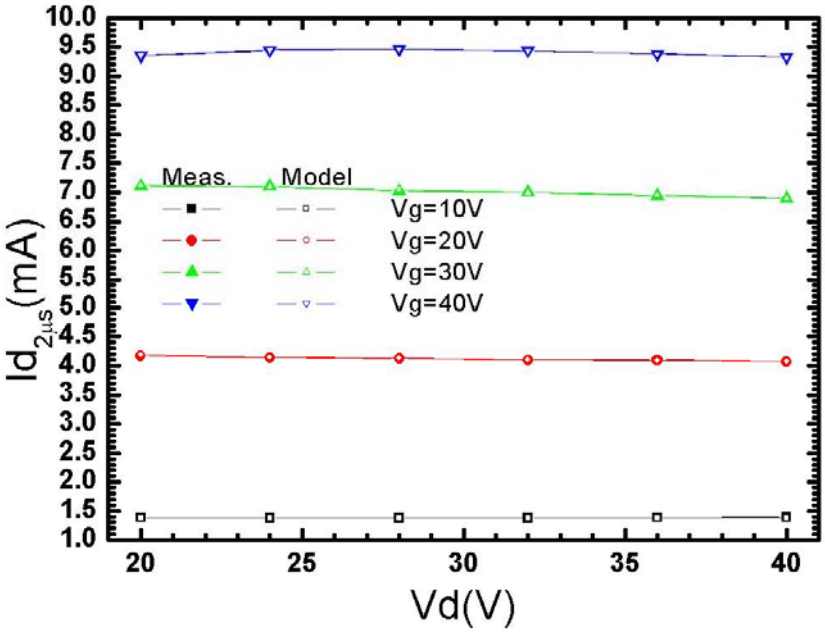


Fig. 4.10 Comparison between simple power model and the measured data.

Chapter 5
Conclusion and Future Work

According to all the investigation, we can get some conclusion. In chapter2, lateral double diffused MOSFET (LDMOS) has been characterized including quasi-saturation effect and the current flowlines and the impact ionization location by TCAD 2D simulation. Various test structures of MESDRIFT devices are also discussed with respect to the I-V characteristics influence by different contact implant location and implant area. Here, we propose two ways to find MOS model from KPC and KL devices, respectively. KPC device has the best match I-V characteristics to LDMOS while KL device has the advantage to extract MOS data easily.

In chapter3, LDMOS macro model overall extraction flow is presented in detail. Such a model is developed by adding a voltage controlled resistance to a standard BSIM3 MOSFET model. In order to reduce mismatch of macro model at high gate bias due to the contact implant, we use reverse calculated R_D to modify the error. For more physical R_D model, we derive Vk formula to reduce R_D model parameter numbers. For time-saving purpose, we use KL device to extract MOS model. Combining MOS model and R_D model, we have a macro model and such a macro model can exactly describe the I-V characteristics of LDMOS with a mean error of less than 2%.

An investigation of Self-heating effect (SHE) in LDMOS based on pulsed measurements is discussed in chapter4. It has been shown that pulse width and power are important parameters to define free-SHE measurements conditions. Two simple models are proposed and validated to describe the behavior of SHE in LDMOS.

For more complete macro mode, different geometry must be used for the extraction of the BSIM3 parameters, e.g. one large size device and two sets of smaller-sized devices should be taken into account. This will significant improve the

accuracy of parameter extraction but it will raise the difficulty in the meantime. Besides, SHE should also be taken into account in macro model.

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Appendix A The intrinsic MOS model parameters extracted from KPC device.

.MODEL N NMOS (				level	= 49
+lmin	= 1e-006	lmax	= 1e-006	wmin	= 1e-006
+wmax	= 1e-006	version	= 3.2	mobmod	= 1
+capmod	= 3	nqsmod	= 0	binunit	= 1
+stimod	= 0	paramchk	= 0	binflag	= 0
+vfbflag	= 0	hspver	= 2000.2	lref	= 1e 020
+wref	= 1e 020	tref	= 25	xl	= 0
+xw	= 0	lmlt	= 1	wmlt	= 1
+ld	= 0	llc	= 0	lwc	= 0
+lwlc	= 0	wlc	= 0	wwc	= 0
+wwlc	= 0	tox	= 1.22e-007	toxm	= 1.22e-007
+wint	= 0	lint	= 0	hdif	= 0
+ldif	= 0	ll	= 0	wl	= 0
+lln	= 1	wln	= 1	lw	= 0
+ww	= 0	lwn	= 1	wwn	= 1
+lwl	= 0	wwl	= 0	cgbo	= 0
+xpart	= 1	vth0	= 1.2945087	k1	= 0.53
+k2	= -0.0186	k3	= 0	k3b	= 0
+nlx	= 0	dvt0	= 0	dvt1	= 0
+dvt2	= 0	dvt0w	= 0	dvt1w	= 0
+dvt2w	= 0	nch	= 1.67e 016	voff	= -0.10794781
+nfactor	= 1	cdsc	= 0	cdscb	= 0
+cdscd	= 0	cit	= 0	u0	= 0.066779793
+ua	= 1.6476433e-009	ub	= 5.0552204e-019	uc	= 1.05e-010
+ngate	= 0	xj	= 1.7e-006	w0	= 0
+prwg	= 0	prwb	= 0	wr	= 1
+rdsw	= 50	a0	= 0.5	ags	= -0.76648995

+a1	= 0	a2	= 1	b0	= 0
+b1	= 0	vsat	= 158800	keta	= -0.047
+dwg	= 0	dwb	= 0	alpha0	= 0
+beta0	= 30	pclm	= 4.7180775e-012	pdiblc1	= 0.4326837
+pdiblc2	= 0.53719751	pdiblcb	= 0	drout	= 0
+pvag	= 0.063358652	pscbe1	= 4.24e 008	pscbe2	= 0
+delta	= 0.01	eta0	= 0	etab	= 0
+dsub	= 0	elm	= 5	alpha1	= 0
+clc	= 1e-007	cle	= 0.6	ckappa	= 0.6
+cgdl	= 0	cgsl	= 0	vfbcv	= -1
+acde	= 1	moin	= 15	noff	= 1
+voffcv	= 0	kt1	= 0	kt1l	= 0
+kt2	= 0.022	ute	= -1.5	ua1	= 4.31e-009
+ub1	= -7.61e-018	uc1	= -5.6e-011	prt	= 0
+at	= 33000	noimod	= 1	noia	= 1e 020
+noib	= 50000	noic	= -1.4e-012	em	= 41000000
+af	= 1	ef	= 1	kf	= 0
+gdsnoi	= 1	rsh	= 0	js	= 0.0001
+jsw	= 0	cj	= 0.0005	mj	= 0.5
+cjsw	= 5e-010	mjsw	= 0.33	pb	= 1
+rd	= 0	rdc	= 0	rs	= 0
+rsc	= 0	xti	= 0	acm	= 12
+calcacm	= 0	nj	= 1	pbsw	= 0.8
+ptc	= 0	tt	= 0	ijth	= 0.1
+tcj	= 0	tcjsw	= 0	tcjswg	= 0
+tpb	= 0	tpbsw	= 0	tpbswg	= 0
+sa0	= 1e-006	sb0	= 1e-006	wlod	= 0
+kvth0	= 0	lkvth0	= 0	wkvth0	= 0
+pkvth0	= 0	llodvth	= 0	wlodvth	= 0

+stk2	= 0	lodk2	= 1	lodeta0	= 1
+ku0	= 0	lku0	= 0	wku0	= 0
+pku0	= 0	llodku0	= 0	wlodku0	= 0
+kvsat	= 0	steta0	= 0	tku0	= 0)

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碩士論文題目:

高壓元件LDMOS之特性分析與SPCIE模型建立

Characterization and SPICE Modeling of High Voltage LDMOS