國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

高介電常數材料氧化鋁之特性研究

The Integrated Investigation of High-κ Material Al_2O_3

研　究　生：陳彥廷　　Yen-Ting Chen

指 導 教 授：羅正忠 博士　　Dr. Jen-Chung Lou

中 華 民 國 九 十 四 年 六 月

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A Thesis

Submitted to Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronic Engineering

June 2005

Hsinchu, Taiwan, Republic of China

中華民國 九十四 年 六 月

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摘 要

在動態記憶體元件製程中，塹渠式的動態記憶體已被廣大應用在生產線上。然而，隨著半導體的微縮定律，目前技術所提供的儲存密度漸漸不敷使用，傳統的複晶矽/二氧化矽/矽已無法提供足夠的電荷儲存量，因此，我們改以金屬/絕緣層/金屬替代，配合高介電係數材料來替換傳統的二氧化矽，希望可以提高塹渠式的動態記憶體的電荷儲存量。

在許多高介電係數材料之中，氧化鋁是一種非常有潛力的高介電係數材料。它有足夠的介電係數(約 8～10)，以及相對高的載子能障(對電子的能障約 2.9 電子伏特，而電洞的能障約 4.3 電子伏特)，以及

良好的熱穩定性。相較於其他高介電係數材料，氧化鋁擁有較高的結晶溫度，適合應用在塹渠式的動態記憶體。

在我們的實驗過程中，我們先在矽基板上沉積氧化鋁的電容結構，探討氧化鋁沉積的最佳條件，包括沉積時的反應溫度、沉積後退火的溫度、沉積時通氧氣的時間以及流量……等等。

之後，我們在氮化鈦上，以這些最佳條件沉積氧化鋁，最後並沉積上電極氮化鈦，完成氮化鈦/氧化鋁/氮化鈦結構。我們研究氮化鈦/氧化鋁/氮化鈦結構，發現高的沉積後退火的溫度會導致大的漏電流。我們在降低漏電流方面也做了些努力。

我們在下電極氮化鈦和氧化鋁之間，沉積一層氮化鋁，完成氮化鈦/氧化鋁/氮化鋁/氮化鈦結構。發現降低漏電流的情況並不明顯。

我們又試著改變下電極氮化鈦的厚度，希望可以得到比較平整的氧化鋁及氮化鈦的接面，並抑制漏電流。發現漏電流可以更有效的被抑制，但仍然無法承受高的沉積後退火溫度處理。

我們從物性分析的結果發現，在高溫的情況之下鋁原子和鈦原子會相互擴散，這可能是氮化鈦/氧化鋁/氮化鈦結構在高溫處理後有很大的漏電流的原因。如何讓氮化鈦/氧化鋁/氮化鈦結構可承受高的沉積後退火溫度處理，也是往後重要的課題。

The Integrated Investigation of High-κ Material Al_2O_3

Student：Yen-Ting Chen Advisor：Dr. Jen-Chung Lou

Department of Electronics Engineering and Institute of Electronics

National Chiao Tung University, Hsinchu, Taiwan

Abstract

In the DRAM technology, trench DRAM has been applied in the production line for a long time. However, according to the scaling rules, the charge storage density nowadays is not enough for next generation. Conventional MIS structure (polysilicon/ SiO_2/Si) can not afford enough charge storage. Therefore, we substitute MIM structure (metal/insulator/metal) for conventional MIS structure. High-κ materials have been applied at the same time. We hope that larger charge storage in trench DRAM can be achieved.

Aluminum oxide (Al_2O_3) is one of the potential high-κ materials. It has the suitable dielectric constant (8~10), higher barrier height (2.9eV for electrons, and 4.3eV for holes), and excellent thermal stability. Compare with other high-κ materials, Al_2O_3 has higher crystallization temperature and could sustain source/drain activation annealing in the trench DRAM process.

In this thesis, we deposited Al_2O_3 on Si substrate. We discussed optimum conditions of Al_2O_3 deposition, including deposition temperature, post deposition annealing (PDA) temperature, oxygen purge time and oxygen purge flow.

Then, we deposited Al_2O_3 on TiN with these optimum conditions followed by upper electrode TiN deposition, and MIM ($TiN/Al_2O_3/TiN$) structure is formed. High leakage current is observed in MIM structure after high temperature PDA. We focused on suppressing leakage current in MIM and studied leakage mechanism as well.

We deposited AlN between below electrode TiN and Al_2O_3 ($TiN/Al_2O_3/AlN/TiN$). However, the suppression of reduce leakage current density is not obvious.

We changed thickness of below electrode TiN in order to get a smooth interface between Al_2O_3 and TiN. With thinner TiN electrode, lower leakage current can be achieved but it was still high after PDA.

From Auger analysis, we found out that Al and Ti would inter-diffuse after high temperature PDA. That might be the reason of high leakage current in MIM structure. In the future, it is an important issue of how to maintain low leakage current on MIM structure after high temperature PDA.

誌　謝

轉眼間，碩士兩年的奮鬥即將劃上句點……

我要感謝我的指導教授羅正忠博士以及國家奈米元件實驗室的簡昭欣博士。他們兩位在研究領域方面，給予我縝密、專業的指導以及協助，讓我養成應有的研究態度和正確的研究方法，這樣的態度以及方法，是我在踏出校園之後，仍然可以受用無窮的。在這邊，我要向兩位老師致上最誠摯的敬意與謝意。

此外，我要感謝實驗室的兩位學長— 永裕以及世璋學長，是你們在我遇到困難及問題時，適時提供寶貴的意見以及方向，幫助我走出實驗的低潮，讓我能夠順利地完成研究，沒有你們的幫助，這篇論文是無法順利完成的，謝謝你們！

同時，也要感謝曾經一起打拚的同學們：祐慈、雁雅、宗翰、昶維、陳偉、俊宏、柏慶、漢邠、啟哲、文廷、聰杰、伊鋒……，謝謝你們在學業上以及生活上的陪伴與砥礪，也感謝你們所提供的幫助與鼓勵。也要感謝修豪、忠樂、佳寧、致維、國信、國源、伯翰、文煜……等學弟們的協助。

最後還要感謝我的家人，感謝我的父母多年來辛苦的諄諄教誨，在背後默默的支持與鼓勵，給予我正確的人生觀以及待人接物的道理，當我面對每一項艱困的挑戰時，讓我有信心以及勇氣克服一切。我的生命，是你們的恩賜；我今日的成就，你們是幕後的推手。謝謝你們！還有我的姊姊宜欣、弟弟宜群，女朋友玉綺，謝謝你們跟我一起分享這兩年的點點滴滴，謝謝！

另外，我要感謝國家奈米元件實驗室與交大奈米中心提供良好的設

備和每一位勞苦功高的工作人員所給予的幫助，讓我能順利的完成實驗。謝謝！

這兩年回憶，是我和你們大家一起完成的故事，記錄在這本論文裡。這本論文，獻給大家。謝謝你們～

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CHAPTER 1

Introduction

1.1 Background

Silicon has been used for microelectronic for thirty years. Since the 1930s, the basic concept of the field-effect transistor (FET) has been understood. In the 1960s, the device became a practical reality. Since the late 1970s, a particular kind of FET, the metal-oxide-semiconductor field-effect transistor (MOSFET), has been extremely popular. MOS transistors can be made quite small, occupying a small silicon area on IC chip, and their manufacturing process is relatively simple, compared with bipolar junction transistor (BJT) manufacturing process. Furthermore, digital logic and memory functions can be implemented with circuits that use MOSFETs only (that is, no resistors or diodes are needed). This is the reason why most very-large-scale integrated (VLSI) circuits are made at the present time using complementary metal-oxide-semiconductor (CMOS) technology, including microprocessor and memory chips. CMOS technology has also been applied extensively in the design of analog integrated circuits and in integrated circuits that combine both analog and digital circuits. Since the 1980s, devices have been scaled such that performance doubled as the cost was cut in half every 2-5 years. This is the famous “Moore’s law”. Over the years, the industry’s demand for greater integrated circuit functionality and performance at lower cost requires an increased circuit density, which has translated

into a higher density of transistors on a wafer.

Figure 1-1 shows the expected equivalent oxide thickness (EOT) trends from the published 2003-ITRS roadmap (International Technology Roadmap for Semiconductor). It suggests that at the current rate of progress, we will need EOT of less than 2 nm by 2004, and oxy-nitrides can extend silicon dioxide (SiO_2) limitation to 2006 without massive change in production technologies. After 2006, oxy-nitrides can not meet the limit on gate leakage current density.

This rapid shrinking of the transistor feature size has focused the channel length and gate dielectric thickness to also decrease rapidly. This has been reported that the CMOS gate dielectric SiO_2 thickness can scale to a least 13 Å [1]. However, while SiO_2 thickness is less than 20-25 Å, large direct-tunneling current is inevitable. Therefore, it is necessarily for high dielectric constant material (high-κ) gate dielectrics to be studied as alternative gate dielectrics in order to suppress excessive gate leakage current and power consumption.

High-κ gate materials can maintain the same EOT with thicker physical thickness, and is therefore expected drastically reduced direct-tunneling current. From Figure 1-2, the increased physical thickness significantly reduces the probability of tunneling across the insulator, and hence, reduces the amount of off-state leakage current density [2].

The relationship between dielectrics constant and thickness is followed:

$$EOT = \frac{k_{ox} \times t_{high-k}}{k_{high-k}}$$

Although reduced leakage current density has been observed in some devices with high-κ gate dielectrics, there are still several problems to be solved, including thermal stability, interface quality between high-κ gate dielectrics and Si-substrate, mobility degradation, reliability, charge trapping, and fabrication integrity with IC technology, etc.

Many of the materials studied as potential high-κ gate dielectrics candidates have been reported such as aluminum oxide (Al_2O_3) [3], zirconium oxide (ZrO_2) [4] [5], hafnium oxide (HfO_2) [6] [7], tantalum oxide (Ta_2O_5) [8]. Table 1-1 summarizes the properties of potential high-κ candidates.

Due to the high dielectric constant, high thermal stability [9] and high band gap, Al_2O_3 is suitable to be integrated into trench DRAM process [10]. Al_2O_3 is therefore chosen in this thesis.

1.2 Motivation

In the conventional MIS structure, metal/ insulator/ Si-substrate has been used for a long period. There are many studies about high-κ on Si-substrate. Comparing with SiO_2, the most benefit for high-κ gate dielectrics is leakage current density reduction by several orders of magnitude at the same EOT. However, in device performance point of view, a suitable gate dielectric candidate should also meet the other requirements, such as high thermal stability, high carrier mobility, small oxide charges, and good stress immunity and CMOS compatible. Generally in high-κ materials, the higher κ value, the lower electron barrier height. Therefore, κ value and electron barrier height are in trade-off relationship. High-κ materials which κ value is larger than 40 may result huge gate leakage current due to extremely low electron

barrier height. Hence, κ value and electron barrier height should be taken into consideration at the same time. Al_2O_3 has suitable κ value and large electron barrier height and is therefore chosen in this thesis.

Different from semiconductor (Si-substrate), metal has more carriers and is more conductive. Therefore, MIM structure (metal /insulator /metal) can reduce contact resistance and raise storage charge comparing to MIS structure. On the other hand, in the trench DRAM process, trench capacitor is made by MIS structure (Polysilicon/ high-κ/ n-type dopant Si). As DRAM density increasing, device shrinkage and higher charge storage is inevitable. It is hard for conventional MIS structure to meet the requirements, MIM structure is expected to apply in trench DRAM process.

We are interested in this topic, and trying to apply MIM structure in trench DRAM process. Besides, we are wondering if high-κ material interacts with metal electrode. If high-κ material interacts with metal electrode, there will be an interfacial layer between high-κ material and metal electrode. That will change whole film property, such as interface roughness, interface stress, electron barrier height, and thermal stability, etc. These issues will be discussed as well.

1.3 Characteristics of Al_2O_3

Recently, Al_2O_3 has been studied as one of potential gate dielectric candidates. The dielectric constant (κ) of Al_2O_3 is about 8 ~10, higher than that of SiO_2 (κ~3.9) and Si_3N_4 (κ~7). Generally speaking, the increase of dielectric constant follows the decrease of the energy band-gap. The energy band gap of Al_2O_3 is about 8.8 eV. It is higher than other high-κ materials such as ZrO_2 (5.8eV), HfO_2 (6.0eV), and Ta_2O_5

(4.5eV). As shown in Figure 1-3, electron barrier height of Al_2O_3 is 2.9eV, higher than ZrO_2 (1.5eV) and HfO_2 (1.6eV). The sufficient electron barrier height can suppress the leakage current through gate dielectric.

Beside, after high-κ gate dielectric deposition, atomic layer do not combine very well. Therefore, high temperature annealing (PDA, post deposited annealing) is used to densify high-κ gate dielectric thin film. Many high-κ materials, such as ZrO_2, HfO_2, will crystallize during PDA process. It has been studied that Al_2O_3 exhibits remain crystallinity after 830°C anneal [11]. Al_2O_3 is expected to remain amorphous about 900°C [12] and therefore low leakage current can be achieved.

1.4 Characteristics of TiN

Titanium nitride (TiN) is extensively to be used in MOSFET technology. TiN film could be deposited by PVD (physical vapor deposition) or CVD (chemical vapor deposition) process.

In the PVD process, TiN film is deposited by sputtering Ti metal target under nitrogen ambient. In the CVD process, $TiCl_4$ and NH_3 can be employed to form TiN at 400°C ~ 700°C. The reaction equation is as follows:

$$6TiCl_4 + 8NH_3 \rightarrow 6TiN + 24\ HCl + N_2$$

Consideration of filling trench, CVD process can be extensively employed on DRAM technology due to good step coverage. On the other hand, resistivity of CVD TiN is higher due to its undensified structure. As shown in Table 1-2 [13-15], its resistivity is about 170μΩ-cm.

Table 1-3 lists Gibb's free energy of titanium (Ti) and its combination [16]. From the definition of Gibb's free energy, if ΔG° is positive, the reaction will not occur

spontaneously. For example, the forth equation in the Table, TiN is stable under H_2S gas until we provide energy 40.955 Kcal / mol. If $\Delta G°$ is negative, it means that the reaction will occur spontaneously even if thermal energy is not supplied. Besides, the larger the absolute value of $\Delta G°$ ($|\Delta G°|$, if $\Delta G° < 0$), the higher probability of equation will act. From the Table 1-3, Ti is likely to combine with oxygen rather than nitrogen. On the other hand, TiN metal oxidize under oxygen ambient, which has been studied in reference [13]. The equation of TiN oxidation is:

$$TiN + O_2 \rightarrow TiN_yO_x \rightarrow TiO_x \rightarrow Ti_nO_{2n-1} \rightarrow TiO_2 \text{ [13]}$$

Before TiO_2 formation, there are three intermediate stages of Ti-N-O combine. The first stage has the maximum activation energy barrier about 439 KJ/mol. In the other steps, the activation energy become less than that for the first step, about 251-334 KJ/mol. Form the XPS analysis [13], Ti 2p spectra indicate the formation of intermediate oxide at 573K (300°C) and a phase transition of TiO_2 from amorphous to anatase-phase occurs at the temperature above 673K (400°C).

1.5 Organization of the Thesis

There are four chapters in this thesis. Chapter 1 describes the background and motivation for the high-κ dielectrics and application of the MIM structure.

In Chapter 2, we first describe the experimental procedure and then, show the basic characteristics of Al_2O_3 gate stacks on Si substrate, including basic C-V and I-V characteristics. The Al_2O_3 thin film in this thesis is deposited by metal-organic chemical vapor deposition (MOCVD), and the optimum conditions is found, including deposition temperature, oxygen purge time, oxygen purge flow. Furthermore, we find optimum post-deposition annealing temperature and post-metal

deposition temperature.

In Chapter 3, we deposit Al_2O_3 on TiN metal with these optimum conditions which we find in Chapter 2. However, MIM structure performance is not as good as we expected. High leakage current density is fatalness of MIM structure. In order to suppress leakage current density, AlN buffer layer inserted between Al_2O_3 thin film and below TiN electrode is discussed. Besides, thinner the thickness of below TiN electrode is used as well.

Finally, in Chapter 4, the conclusions are made and the recommendation describes the topics which can be further researched.

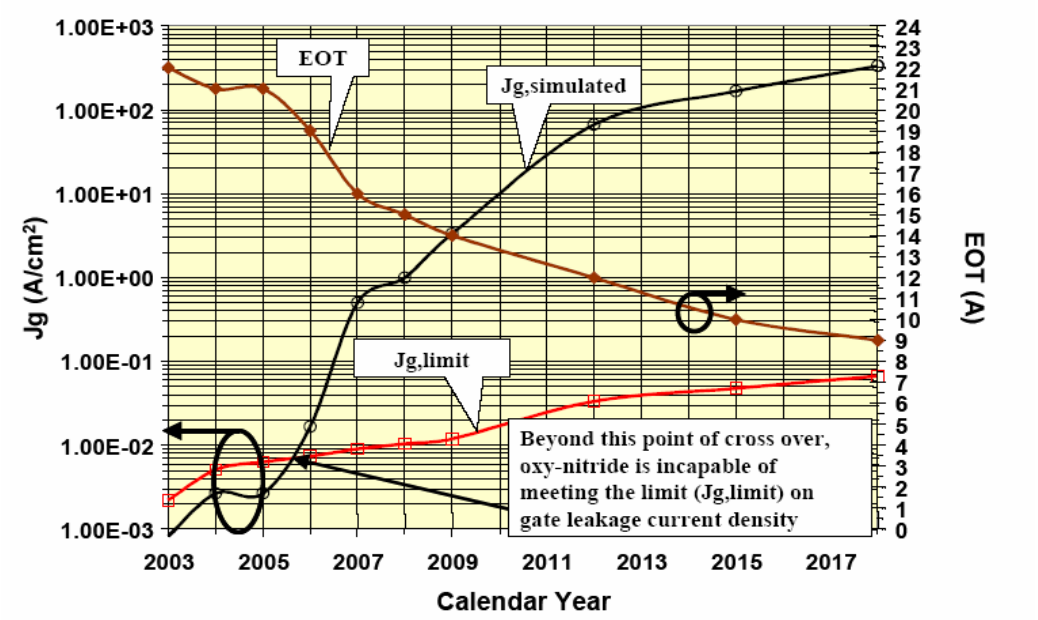


Figure 1-1 The expected equivalent oxide thickness (EOT) trends from the published 2003- ITRS roadmap.

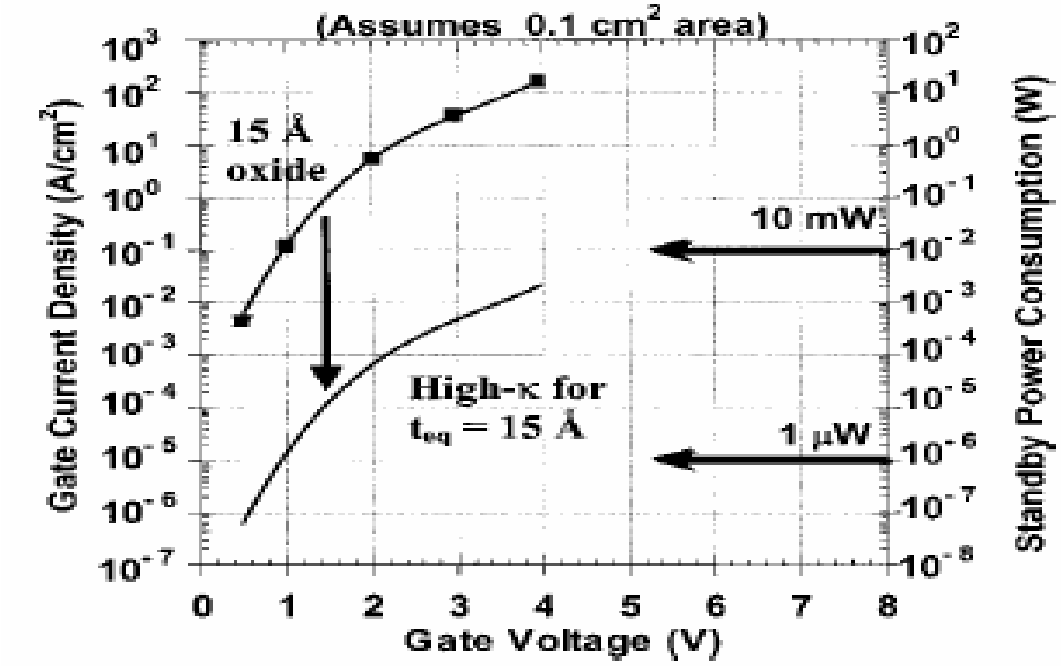


Figure 1-2 Power consumption and gate leakage current density comparing to the potential reduction in leakage current by an alternative dielectric exhibiting the same equivalent oxide thickness [1].

Material	Dielectric Constsnt(k)	Band gap Eg(eV)	△Ec(eV) to Si	Crystal Structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8	Amorphous
Ta_2O_5	26	4.5	1-1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.
HfO_2	25	5.7	1.5	Mono.,Tetrag.,Cubic
ZrO_2	25	7.8	1.4	Mono.,Tetrag.,Cubic

Table 1-1 Basic properties for many high-κ candidates [1].

Property	TiN	Ti
Structure	fcc	hcp
Density	5.4 g/cm^3	4.54 g/cm^3
Melting point	2950°C	1940°C
Thermal conductivity	30 Watt/m-K	13 Watt/m-K
Thermal expansion	9.36x10^{-6} /K	11x10^{-6} /K
Electrical resistivity	170μΩ-cm	39μΩ-cm

Table 1-2 Material properties of titanium nitride (TiN) and titanium (Ti) [14-16].

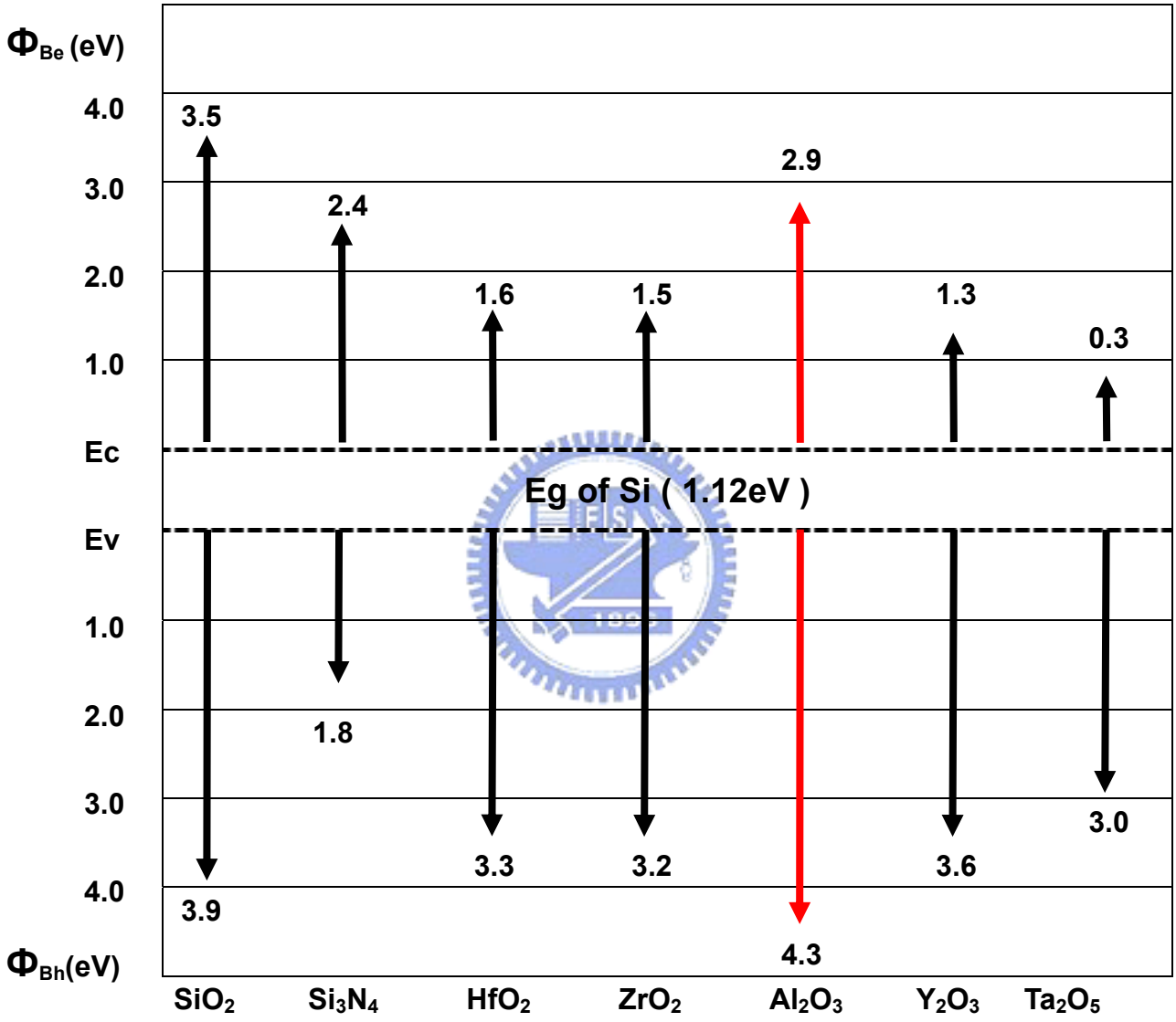


Figure 1-3 Band alignment of topical high-κ dielectrics.

Reaction	ΔG° (Kcal / mol)
$Ti\,(s) + O_2\,(g) \rightarrow TiO_2\,(s)$	-175.180
$2Ti\,(s) + N_2\,(g) \rightarrow 2TiN\,(s)$	-115.079
$2TiN\,(s) + 2O_2\,(g) \rightarrow 2TiO_2 + N_2\,(g)$	-108.960
$TiN\,(s) + 2H_2S\,(g) \rightarrow TiS_2 + 1/2N_2\,(g) + 2H_2\,(g)$	+40.955

Table 1-3 Gibb's free energy of titanium (Ti) and its combination [17].

CHAPTER 2

Characteristics of Al_2O_3 Gate Dielectrics

2.1 Introduction

While the critical dimensions (CD) of complementary metal-oxide-semiconductor (CMOS) devices are scaling down, large direct-tunneling current is inevitable due to the ultra thin gate dielectric stack. On the next generation, we substitute high-dielectric constant (high-κ) materials for conventional silicon dioxide (SiO_2). High-κ gate materials can maintain the same equivalent oxide thickness (EOT) with thicker physical thickness, and is therefore expected drastically reduced direct-tunneling current.

There are many methods to deposit high-κ gate dielectrics stack, such as physical vapor deposition (PVD) [17], atomic layer deposition chemical vapor deposition (ALCVD) [11,18-21], and metal-organic chemical vapor deposition (MOCVD) [22-24]. In the industrial production viewpoint, PVD is not an appropriate tool for high-κ film deposition due to both poor step coverage and bad uniformity. Nowadays, ALCVD and MOCVD have paid more efforts to be evaluated for high-κ dielectrics deposition in the industry. Table 2-1 is the comparison of deposition techniques which have been used. MOCVD has the advantage of superior step coverage, high deposition rate, good controllability of film composition, and excellent thickness uniformity on large dimension wafers. MOCVD system is therefore chosen to deposit

high-κ dielectrics in this thesis.

Recently, aluminum oxide (Al_2O_3) had been proved as promising candidates for the gate dielectrics of sub-0.1μm device due to their higher κ value, relatively high φ_B and superior thermal stability [22]. Due to the high dielectric constant and high thermal stability, Al_2O_3 is suitable to be integrated into trench DRAM process and is therefore chosen in this thesis.

Figure 2-1 shows the detail schematic structure of the MOCVD system. The MOCVD chamber is equipped with a turbo-molecular pump and a liquid injection system which has four independent-controlled injectors. A liquid pump is consisted of the injector and pumps the precursors through a hot nickel frit with a proper rate. The vapors are carried with a 200 sccm flow of Argon to gas distribution ring which is located at a proper distance from the substrate. On the contrary of the conventional bubbler system, the liquid injection system is with sufficient temperature window to alleviate the thermal aging of the precursor. This is because the precursor remains in liquid state at room temperature until it is pumped into the vaporizer and injected into the deposition chamber. However, the precursor should keep at long-term chemical stability in solvent and non-reactive with other precursors in solvent [25].

The components of the vaporizer, the gas ring and the connecting tube are maintained at 190°C with heating tapes and blankets, while the substrate temperature is controlled at 500°C with quartz-halogen lamps and a thermocouple. A rotating susceptor is used for uniformly heating during processing. A flow of 100 sccm N_2 is maintained throughout the deposition cycle. The base pressure of the MOCVD chamber is ~ 10^{-8} torr. The deposition pressure of the deposition is at the 5 mtorr where the gas-phase collisions are scarce.

2.2 Experimental details

In this chapter, LOCOS isolation was used to fabricate the metal-insulator-semiconductor (MIS) capacitors. The cross-sectional views and processing steps are shown in Figure 2-2. The MIS capacitors were fabricated on 6-inch (100)-oriented silicon wafer with 15~25 μΩ-cm resistivity. Prior to the growth of Al_2O_3 gate dielectrics, the native oxide was cleaned by the conventional RCA cleaning and diluted HF etching in sequence for the removal of particles and native oxides. Wafers were then processed to receive two different deposition temperatures (400°C and 450°C) by MOCVD. Aluminum precursor and oxygen gas were purged to deposited approximately 8 nm Al_2O_3 films, followed by three different RTA temperatures (800°C, 900°C, 1000°C) in N_2 ambient for 30 sec.

Subsequently, a 2000Å titanium nitride (TiN) electrode was sputtered and patterned to form gate electrodes, followed by the 450°C post metal-deposition annealing (PMA) for in N_2 ambient 30 sec. Finally, 5000Å aluminum was deposited on wafer backside with 400°C forming gas sintering for 30 min to create the backside contact.

Square or circular capacitors of different areas, ranging from 2.5×10^{-5} to 1×10^{2} cm^2, with LOCOS isolation are used to evaluate the gate oxide integrity. The physical gate oxide thickness was determined by spectroscopy ellipsometer and compared with transmission electron microscopy (TEM). The cross-section view of MIS capacitor was analyzed by transmission electron microscopy (TEM) as well. The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency capacitance-voltage (C-V) data form Hewlett-Packard (HP) 4284LCR meter under an accumulation condition with quantum mechanical correction. The tunneling leakage

current density-voltage (J-V) was measured by semiconductor parameter analyzer HP4145A. Compositions of Al_2O_3 and TiN were analyzed by X-ray photoelectron spectroscopy (XPS).

2.3 Physical and Electrical Characteristics

2.3.1 Deposition Temperature and PDA Temperature

Figure 2-3(a) reveals the capacitance-voltage (C-V) characteristics of as-deposited Al_2O_3 gate dielectrics deposited at 400°C and 450°C. The capacitance deposited at 400°C was lower than 450°C-deposited sample with similarly optical thickness, which was evidenced by ellipsometer. Since high temperature deposition would transfer high surface mobility to the deposited atomics, Al_2O_3 dielectric deposited at 450°C would expect to have higher film density than 400°C-deposited dielectric. The corresponding current density-voltage (J-V) curves were presented in Figure 2-3(b). Al_2O_3 dielectric deposited at higher temperature was beneficial to suppress leakage current than lower temperature, which was consistent with the C-V characteristics shown in Fig. 2-3(a), i.e. high deposition temperature generated higher density Al_2O_3 thin films with larger capacitance and lower leakage current than low temperature deposited high-κ dielectrics.

Atomic layer does not combine very well in the as-deposited Al_2O_3 thin film. After high temperature annealing, Al_2O_3 film is densified and shows more polarity and higher κ value [1、26]. Sequentially, PDA temperature effect is discussed. The PDA temperature effects on C-V characteristics of 400°C-deposited Al_2O_3 gate dielectrics is shown in Figure 2-4(a). Due to densification of Al_2O_3 thin film [26、27], capacitance

increases with 800°C PDA. However, while PDA temperature is up to 900°C and 1000°C, capacitance descends. This is supposed that oxygen penetration through Al_2O_3 film over 900°C [28-31] and interact with Si-substrate resulting in thicker interfacial layer, i.e. EOT increases and capacitance under accumulation decreases. The corresponding current density-voltage (J-V) curves were presented in Figure 2-4(b). Al_2O_3 thin film processed after higher PDA temperature was beneficial to suppress leakage current [28-31], which was coincident with the C-V characteristics shown in Figure 2-4(a).

Figure 2-5(a) shows C-V curves of PDA temperature effect of 450°C-deposited Al_2O_3 gate dielectrics. Capacitance of 450°C-deposited Al_2O_3 gate dielectrics decreases as PDA temperature increased. Oxygen penetration through Al_2O_3 film contribute to interfacial layer between Al_2O_3 and Si-substrate [28-31], i.e. high PDA temperature generated thick interfacial layer between Al_2O_3 thin film and Si-substrate with lower capacitance. The corresponding current density-voltage (J-V) curves were presented in Figure 2-5(b). Leakage current density decreases with PDA temperature increased, which is supposed to be suppressed by thicker interfacial layer [28、29]. Al_2O_3 thin film processed after high PDA temperature was beneficial to suppress leakage current, which was consistent with the C-V characteristics shown in Figure 2-3(a).

Figure 2-6(a) presents the EOT variation for various PDA temperatures with 400°C and 450°C deposition. EOT reduction is ascribed to densification of 400°C-deposited Al_2O_3 film with PDA 800°C [27]. Then, EOT increases because of thicker interfacial layer [28-31] when PDA temperature is above 800°C. EOT of 450°C-deposited Al_2O_3 film increases after high temperature PDA, which is cause by thicker interfacial layer between Al_2O_3 thin films and Si-substrate. Figure 2-6(b)

displays the leakage current density variation for various PDA temperatures with 400°C and 450°C deposition. Lower leakage current density is observed with PDA temperature increased both on 400°C and 450°C-deposited Al_2O_3 thin film, i.e. proper PDA can get better performance of gate leakage current density.

Table 2-2 summarizes most of the electrical characteristics under all the conditions of deposition temperature (400°C and 450°C) with PDA temperature (800°C, 900°C, and 1000°C), including EOT, gate leakage current, hysteresis, and dispersion. In the viewpoint of lowest leakage current density and hysteresis, performance of Al_2O_3 thin film processed with 400°C deposition and 900°C PDA is best, i.e. the optimum condition of deposition and PDA temperature is determined.

2.3.2 J-V Curves Measurement under Various Temperatures

Figure 2-7(a) shows J-V characteristics of as-deposited MIS capacitor measured at various temperatures from 25°C to 150°C. The dependence of leakage current density and measured temperature is observed, i.e. leakage current density increases with measurement temperature increased. The dependence is suppressed after 900°C PDA, as shown in Figure 2-7(b). Conduction mechanism is found by fitting equation described as follows. Many conduction mechanisms are fitted, including Fowler-Nordheim Tunneling [32、33] , Frenkel-Poole Emission [32、33], Trap Assisted Tunneling [34、35], and Schottky Emission [32].

In the Fowler-Nordheim Tunneling model, leakage current occurs in the high field region. High electric field across on high-κ thin film inclines band diagram and electron can tunnel more easily. The equation of leakage current density is [36]:

$$J = E^2 \exp\left[\frac{-4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E}\right] \sim V^2 \exp\left(-\frac{b}{V}\right)$$

The Fowler-Nordheim Tunneling plots were made for Jg (not shown in the thesis). In the Fowler-Nordheim Tunneling plots, Jg does not show a linearity relationship. The conduction mechanism is therefore not the Fowler-Nordheim Tunneling.

In the Frenkel-Poole Emission model, a lot of traps exist in high-κ thin film and electrons which get enough thermal energy can leap and stay in these traps temporarily and leak to substrate in the end. The equation of leakage current density is [36]:

$$J = E\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/\pi\varepsilon_I}\right)}{kT}\right] \sim V\exp\left(\frac{+2a\sqrt{V}}{T} - \frac{q\phi_B}{kT}\right)$$

The Frenkel-Poole Emission plots were made for Jg (not shown in the thesis). Jg does not show a straight line in the Frenkel-Poole Emission plots, therefore the conduction mechanism is probability not the Frenkel-Poole Emission.

In the Trap Assisted Tunneling model, it is assumed that electrons first tunnel through the SiO_x interfacial layer (direct-tunneling). Then, electrons tunnel through traps located below the conduction band of the high-κ thin film and leak to substrate finally [34]. The equation of leakage current density is [35]:

$$J = \frac{\alpha}{E_{ox}}\exp\left[\frac{-\beta}{E_{OX}}\right]$$

The Trap Assisted Tunneling model plots were made for Jg (not shown in the thesis). Jg is not a straight line in the Trap Assisted Tunneling model plots, therefore the conduction mechanism is probability not the Trap Assisted Tunneling model.

In the Schottky Emission model, the Schottky emission is generated by the

thermionic effect and is caused by the electron transport across the potential energy barrier at a metal-insulator interface. The equation of leakage current density is [36]:

$$J = A^{*}T^{2}\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_I}\right)}{kT}\right] \sim T^{2}\exp\left(\frac{+a\sqrt{V}}{T} - \frac{q\phi_B}{kT}\right)$$

The Schottky Emission model plots were made for Jg in Figure 2-8. Jg shows a clear linearity in the Schottky Emission model plots, therefore the conduction mechanism is probability the Schottky Emission model.

From the conduction mechanism fitting, we speculate that the conduction mechanism of MIS structure is Schottky Emission.

2.3.3 Transmission Electron Microscopy (TEM) Analysis

It is found that 900°C PDA can improve performance of MIS, including EOT reduction, leakage current density suppression and little dependence of leakage current density and measured temperature. The mechanism is analyzed from TEM images. As shown in Figure 2-10, thickness of Al_2O_3 thin film is recognized about 7.44 nm- 9 nm and interfacial layer is about 1.06 nm- 1.13 nm. After 900°C PDA, thickness of Al_2O_3 thin film is a little thinner about 7.06 nm- 8.21 nm and interfacial layer is about 1.81 nm-2.14 nm, as shown in Figure 2-11(b). On the other hand, the κ value of as-deposited Al_2O_3 thin film is about 7.12 and that is about 9.53 after 900°C PDA. The κ value is increased and interfacial layer is thicker after high temperature annealing. It can be understood reasonably that during high temperature annealing Al_2O_3 film is densified and thickness of interfacial layer is increasing due to oxygen penetration [28-31].

2.3.4 Oxygen Purge Conditions Optimization and Post Metal-deposition Anneal (PMA) effect

Al_2O_3 thin film is deposited by reaction of aluminum precursor and oxygen gas. Oxygen purge time and oxygen purge flow is relative to characteristics of Al_2O_3 thin film. To optimize the performance of MIS, we purge oxygen before/ after aluminum precursor purges. The detail process flow is below:

O_2 Purge -> Al_2O_3 deposition -> O_2 Purge

We are wondering how long we should purge exactly. In the first part of experiment, oxygen is purged before Al_2O_3 deposition and is skipped after Al_2O_3 deposition. The second part of experiment is contrary. List in the Table 2-3.

On the other hand, in the trench DRAM technology, trench capacitor will undergo high thermal budget while source/ drain activation annealing. To simulate industrial process, high temperature annealing after metal electrode deposition is necessarily. PMA temperature over 900°C is expected in our research. At the beginning, PMA temperature is determined at 450°C in order to get a smoother interface between upper electrode TiN and Al_2O_3 thin film.

Figure 2-11(a) shows EOT performance both with 450°C PMA and without 450°C PMA under oxygen purge 15、30、60、120 sec before Al_2O_3 deposition. Higher EOT is observed before 450°C PMA. However, EOT thickness reduces after PMA 450°C. From Figure 2-11(b), leakage current is lowest with oxygen purge 30 sec after PMA 450°C. It is found that performance of Al_2O_3 deposition is best due to lowest leakage current at the similar EOT, i.e. optimum condition of oxygen purge time before Al_2O_3 deposition is 30 sec.

Subsequently, we focus on oxygen purge time after Al_2O_3 deposition. Figure 2-12(a) displays EOT performance both with 450°C PMA and without 450°C PMA

under oxygen purge 30、70、450 sec after Al_2O_3 deposition. Before 450°C PMA, increased EOT is observed after PDA 900°C, ascribing to oxygen penetration through Al_2O_3 thin film and inducing thicker interfacial layer [28]. Similar to Figure 2-11(a), EOT decreases after PMA 450°C. On the other hand, leakage current density is lowest when oxygen purges 30 sec after PMA 450°C, as shown in Figure 2-12(b). It is found that performance of Al_2O_3 deposition is best due to lowest leakage current at the similar EOT, i.e. optimum condition of oxygen purge time after Al_2O_3 deposition is determined at 30 sec.

Finally, we focus on oxygen purge flow effect with Al_2O_3 deposition. Figure 2-13(a) shows the oxygen purge flow effect on EOT. We notice that without PMA, EOT increases slightly with oxygen flow rate increasing, causing by more oxygen penetration and thicker interfacial layer [28]. Similar to Figure 2-11(a) and Figure 2-12(a), EOT decreases after PMA 900°C. Consideration of entirely interaction of aluminum precursor and oxygen gas, oxygen purge flow must be large enough to eliminate residual aluminum atoms. However, too large oxygen purge flow induces thick interfacial layer. We therefore experiment further only on oxygen purge flow is 500 sccm and 1000 sccm. Figure 2-13(b) shows the leakage current density with Al_2O_3 thin film deposited under oxygen flow is 500 and 1000 sccm. It is observed that the leakage current density is lower when Al_2O_3 thin film deposited under 1000 sccm oxygen flow, i.e. optimum condition of oxygen purge flow during Al_2O_3 deposition is determined at 1000 sccm.

To summarize briefly, we find out optimum conditions of oxygen purge time and oxygen purge flow. The optimum process is as follows:

O_2 Purge 30 sec -> Al_2O_3 deposition -> O_2 Purge 30 sec

And oxygen purge flow is 1000 sccm.

For the time being, there is still one question in our mind, which is the mechanism of PMA effect resulting in improving MIS performance, including EOT reduction and leakage current density suppression. Subsequently, we discuss this phenomenon by TEM and XPS analyses.

2.3.5 Transmission Electron Microscopy (TEM) and X-ray Photoelectron Spectroscopy (XPS) Analyses

Figure 2-14 shows the TEM images of the sample which was processed by PMA 450°C. There is an obvious interfacial layer between upper electrode TiN and Al_2O_3 thin film about 1.25 nm, which is not seen in Figure 2-9 and Figure 2-10. From TEM images, we estimate the thickness of Al_2O_3 thin film and bottom interfacial layer is 7.94nm- 8.44nm, and 1.44nm- 2.04nm, respectively, and is not obviously changed comparing to Figure 2-10, i.e. 450°C PMA does not change the whole dielectric gate stack except the top interfacial layer between upper electrode TiN and Al_2O_3 thin film. Total dielectric gate stack is a little thicker because of top interfacial layer. However this is not coincident with electrical characteristics (EOT of total dielectric gate stack reduces after 450°C PMA). Therefore, it is necessarily to understand the composition of top interfacial layer by XPS analysis.

The XPS analyses are performed using a ULVAC-PHI PHI Quantera SXM spectrometer: the instrument employs a 180° spherical capacitor analyzer and 32 channel detectors, and a scanning monochromated (A1 anode) X-ray source. For the present study Mg Kα radiation is used, at energy 1253.6 eV, and the source is operated at 400W (15 kV and 27 mA) applied voltage and emission current, respectively. There is a 5 kV ion gun which can clean sample surface and analyze depth profile. Etching rate of ion gun is 70Å SiO_2/ min. Surface element component

analysis can reach 10 Å below the surface.

The test sample structure is Al_2O_3 80Å /CVD TiN 2000Å, without upper electrode TiN deposition. In order to expose the interface of Al_2O_3 thin film and below electrode CVD TiN, the surface of Al_2O_3 thin film is removed by Argon gas sputtering. As sputtering time increases, the composition closer to the interface of Al_2O_3 thin film and below electrode CVD TiN will be detected.

Figure 2-15 displays the survey of XPS analysis. Ti peak is detected with sputter time over 1 min, and is stronger while sputter time increased. It is ascribed to approach the bottom TiN electrode. Element of Ti、Al、O and N is detected at the same time. Figure 2-16 shows the XPS binding energy spectrum of Ti. As sputter time increased, the peak of TiN is getting strong because of closer to below TiN electrode, which is consistent with Figure 2-15. Furthermore, the peak of TiO_2 is detected as well. While sputter time increased, the peak of TiO_2 is getting obvious because of closer to interfacial layer. We therefore speculate that the interface of Al_2O_3 thin film and TiN electrode is TiO_2. From TEM analysis, there is an interfacial layer between Al_2O_3 thin film and upper electrode TiN. The samples are under 450°C PMA in N_2 ambient for 30 sec. A little bit oxygen in N_2 ambient penetrate through the upper TiN electrode and form the interfacial layer. According to XPS analyses, we recognize the interfacial layer between Al_2O_3 and TiN is TiO_2, whose κ value is above 80. Therefore, the interfacial layer between Al_2O_3 thin film and upper electrode TiN is supposed to reduce the EOT of whole dielectric gate stack with thicker optical thickness after 450°C PMA.

2.4 Summary

In this chapter, the characteristics of MOCVD-deposited Al_2O_3 thin film with two different deposition temperatures (400˚C and 450˚C) were presented. We also discussed PDA effect on Al_2O_3 thin film. We found out the optimum deposition temperature is 400˚C with PDA 900˚C according to much lower leakage current density and little hysteresis. PDA 900˚C can condense Al_2O_3 thin film and suppress leakage current density. Besides, leakage current density under high measured temperature is not obviously increasing after PDA 900˚C. Therefore, PDA is still an essential process in order to densify Al_2O_3 thin film although the EOT becomes larger inevitably. Furthermore, conduction mechanism of Al_2O_3 thin film has been studied. The conduction mechanism of Al_2O_3 thin film is Schottky Emission.

From TEM images, we confirmed the Al_2O_3 thin film deposited by MOCVD. The Al_2O_3 thin film is about 9 nm and 7.06 nm after PDA 900˚C. The κ value of as-deposited Al_2O_3 thin film is about 7.12 and is about 9.53 after 900˚C PDA. We also noticed that the interfacial layer between Al_2O_3 thin film and Si-substrate is inevitably thicker after 900˚C PDA.

Then, we studied the oxygen purge effect, including oxygen purge time before/after Al_2O_3 thin film deposition and oxygen purge flow. We found out the optimum condition of oxygen purge process is as follows:

O_2 Purge 30 sec -> Al_2O_3 deposition -> O_2 Purge 30 sec

And oxygen purge flow is 1000 sccm.

Finally, we discussed the PMA effect. From TEM image, the thickness of whole dielectric gate stack is a little thicker with an interfacial layer between upper electrode TiN and Al_2O_3 thin film after 450˚C PMA. However, the less EOT is observed in the

electrical characteristics analysis. Furthermore, from XPS analysis we inferred that the interfacial layer between electrode TiN and Al_2O_3 thin film is TiO_2. The κ value of TiO_2 is above 80 and is supposed to reduce the EOT of whole dielectric gate stack.

We have determined the optimum conditions of Al_2O_3 deposition. In the next chapter, we will deposit Al_2O_3 thin film on TiN metal electrode using these optimum conditions to form MIM structure.

Physical Vapor Deposition (PVD)	Chemical Vapor Deposition (CVD)	
	MOCVD	ALCVD
Pros: 1. Convenient for new materials screening. 2. Easy to fabricate experimental data. 3. Low cost for ownership	Pros: 1. Superior step coverage. 2. High deposition rate. 3. Good controllability of composition. 4. Uniformity of film thickness.	Pros: 1. Better thin film quality. 2. Excellent coverage and conformability.
Cons: 1. Planar, line-of-sight process, damage. 2. Not likely to be used in ULSI gate process. 3. Poor conformability, especially for high aspect ratio.	Cons: 1. Hard to deposit ultra thin films. 2. Carbon contamination.	Cons: 1. Low throughput. 2. Mechanism-related surface sensitivity. 3. Chemistry-limited final products (only binary materials are available now).

Table 2-1 Comparison of deposition techniques: Sputter, ALCVD, and MOCVD [2-9].

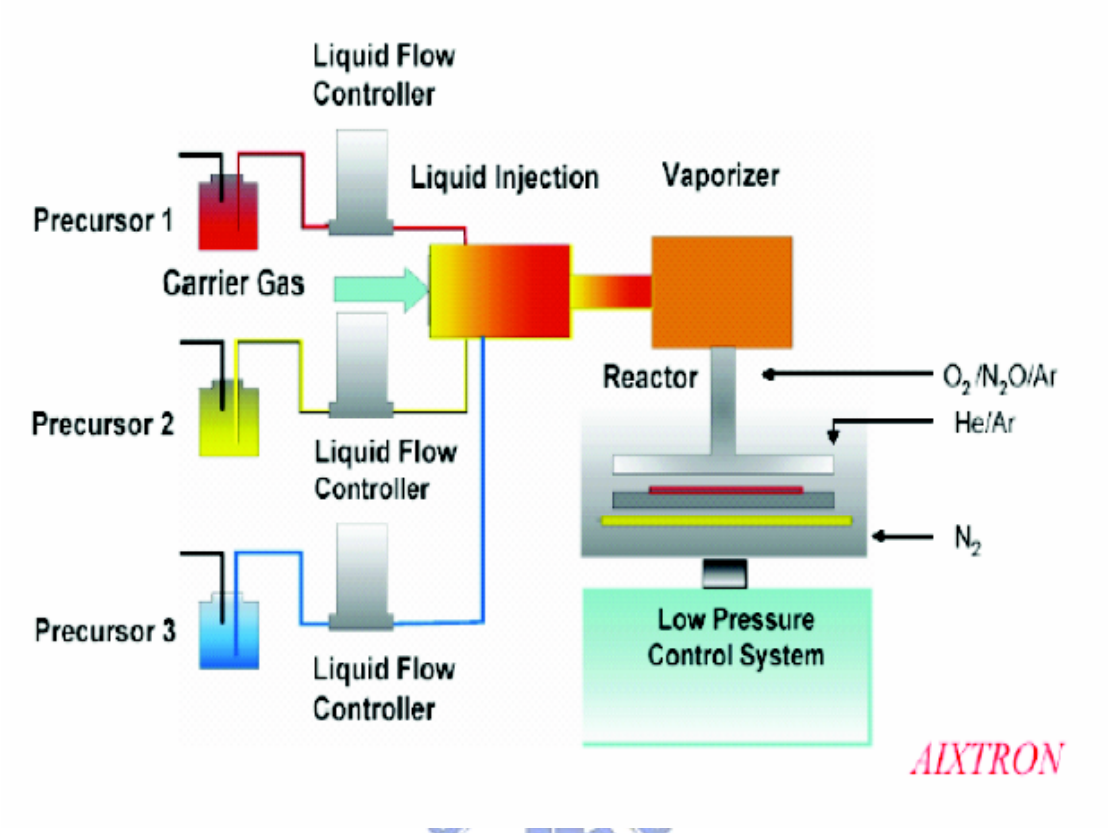
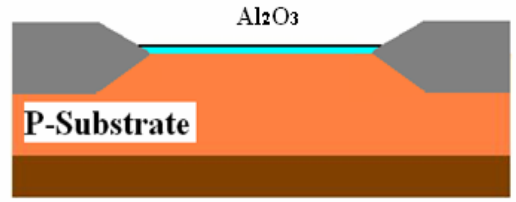


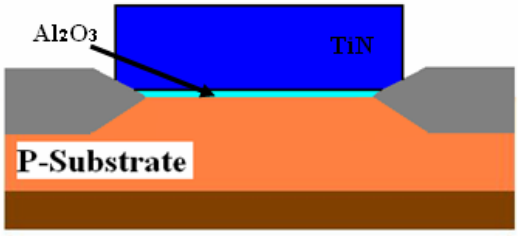
Figure 2-1 Typical MOCVD system structure.

1. LOCOS structure, RCA clean and HF dip to remove native oxide.

2. Al_2O_3 100 Å film deposited by MOCVD.
   Split condition:
   a. Deposition temperature: 400˚C, 450˚C.
   b. Oxygen purge time: O_2 before Al_2O_3 deposited: 15, 30, 60, 120 sec.
      O_2 after Al_2O_3 deposited : 30, 70, 450 sec .
   c. Oxygen flow: 300, 500, 1000, 2000 sccm.



3. Post deposit annealing, PDA: 800˚C, 900˚C, 1000˚C, N_2 30 sec.
4. TiN metal gate deposition 2000Å.
5. Post-metal deposition annealing, PMA: 450˚C, N_2 30 sec.
6. Gate definition.



7. Backside Al sputtering 5000Å.
8. 400˚C, forming gas annealing 30 min.

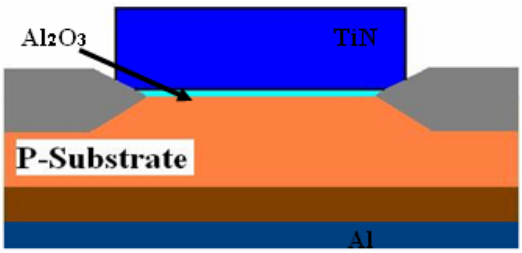
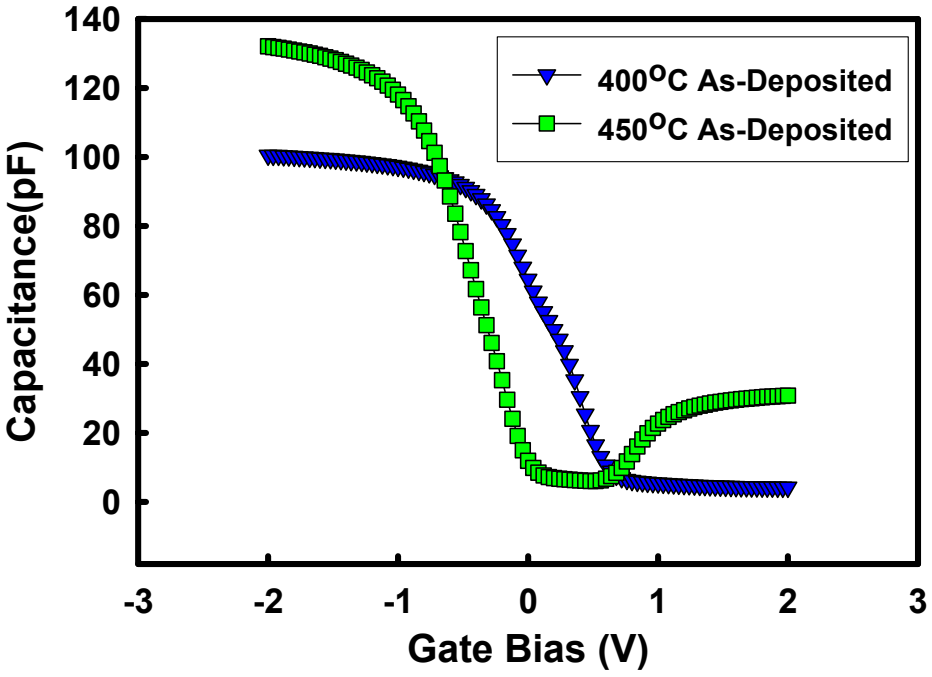
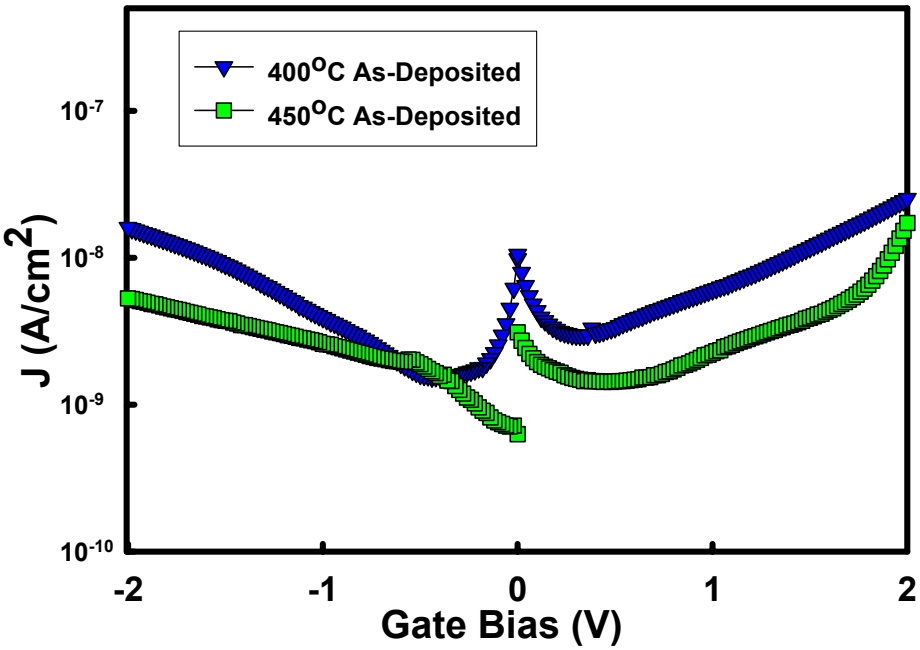


Figure 2-2 The cross-section views of MIS capacitor show LOCOS structure process flow.

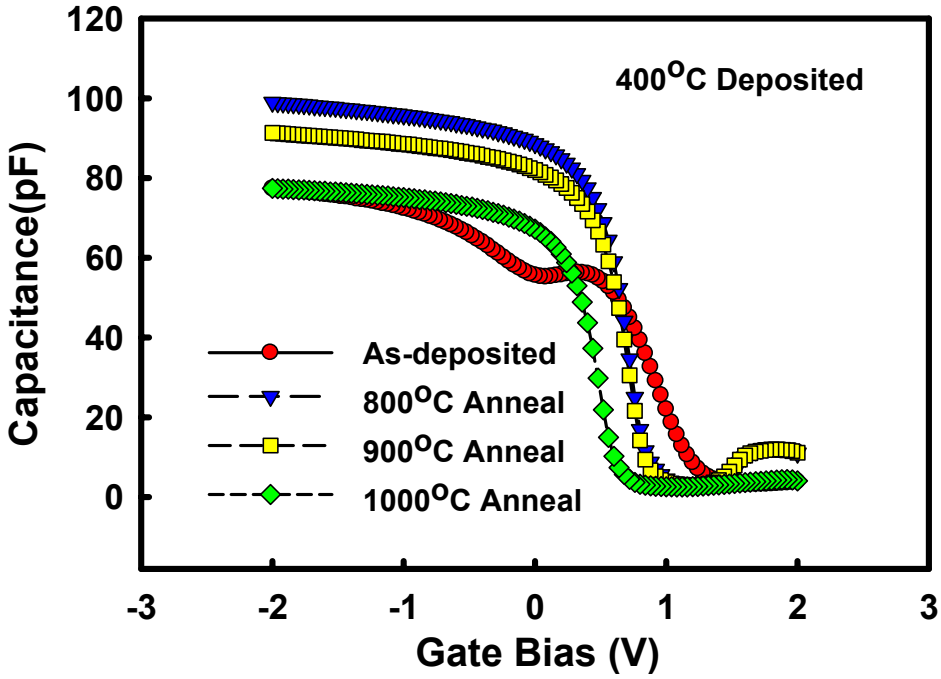


(a)

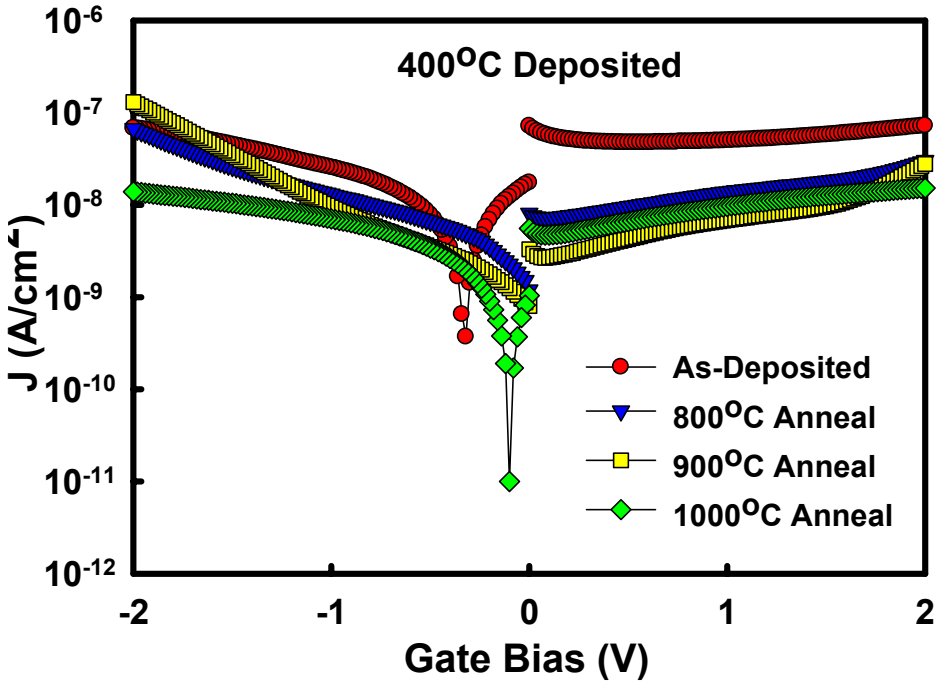


(b)

Figure 2-3 The (a) C-V and (b) leakage current characteristics of the as-deposited Al_2O_3 gate dielectrics with 400˚C and 450˚C deposition temperatures.

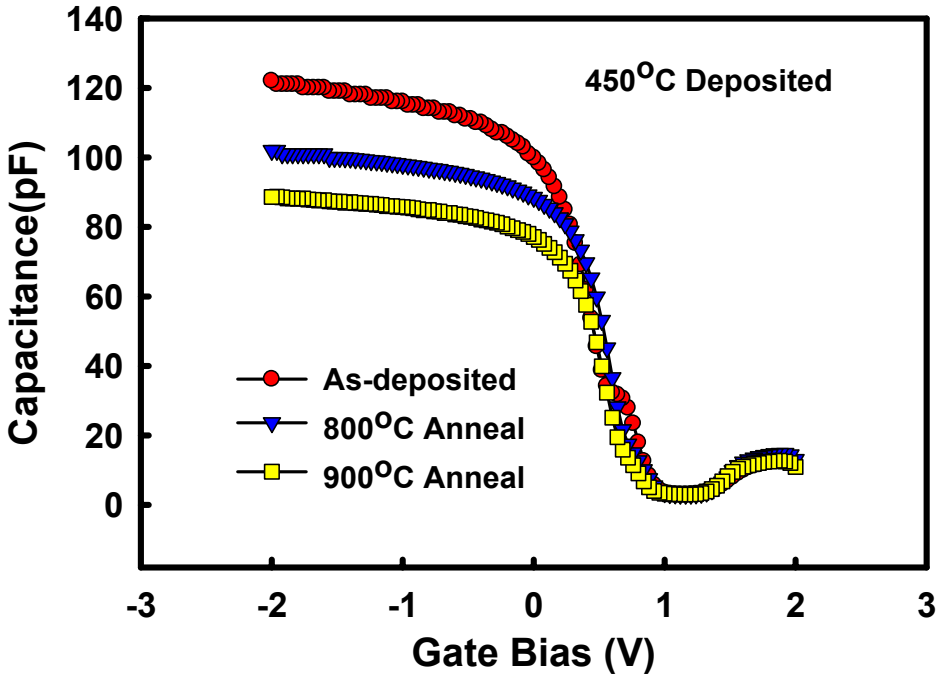


(a)

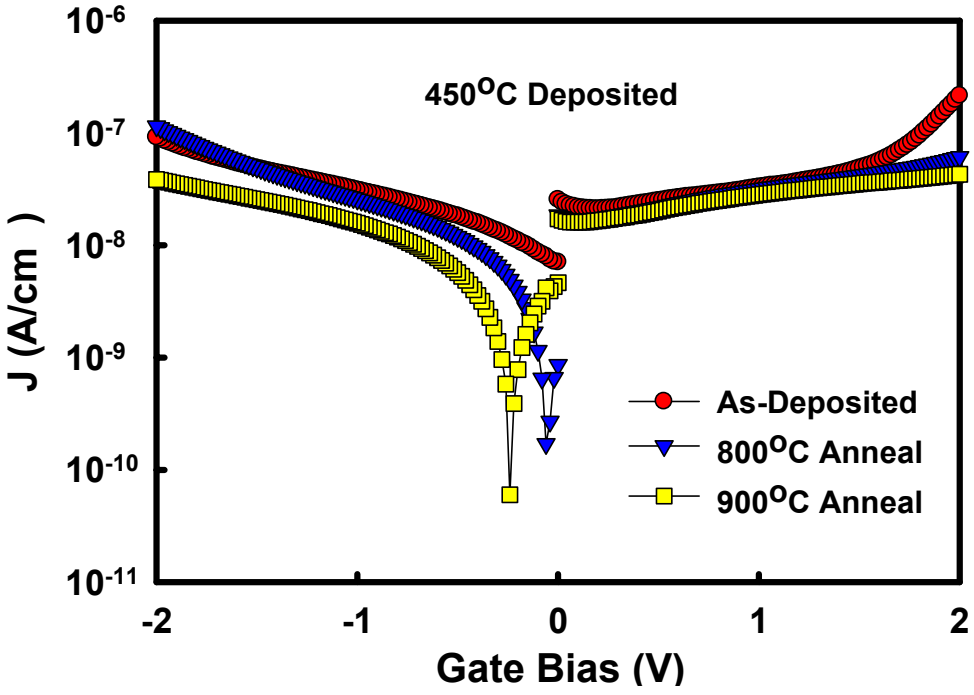


(b)

Figure 2-4 The (a) C-V and (b) leakage current characteristics of the 400˚C-deposited Al_2O_3 gate dielectrics with 800˚C, 900˚C and 1000˚C PDA.

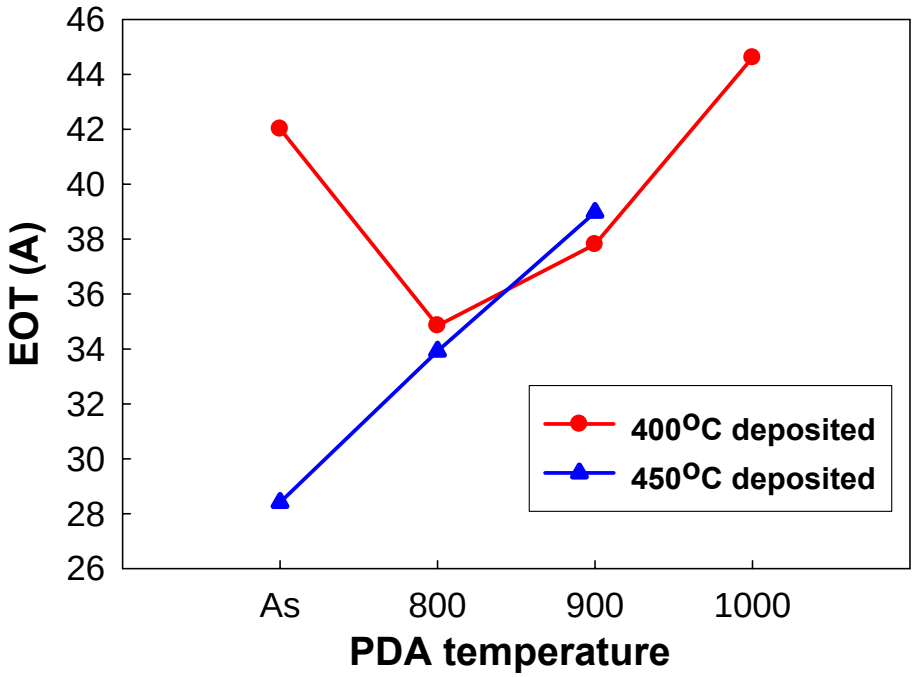


(a)

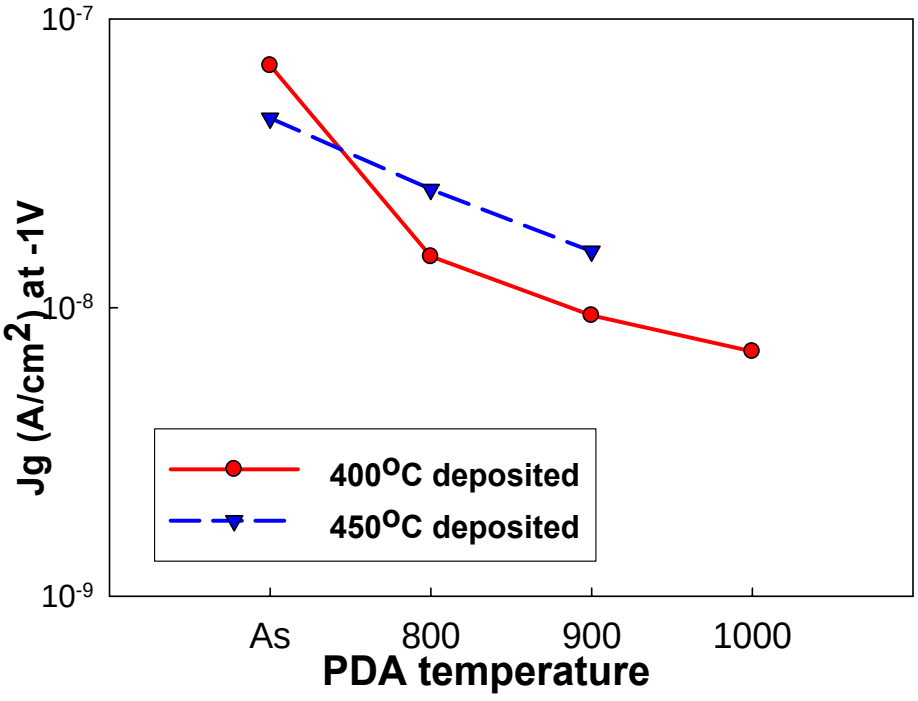


(b)

Figure 2-5 The (a) C-V and (b) leakage current characteristics of the 450°C-deposited Al_2O_3 gate dielectrics with 800°C and 900°C PDA.



(a)

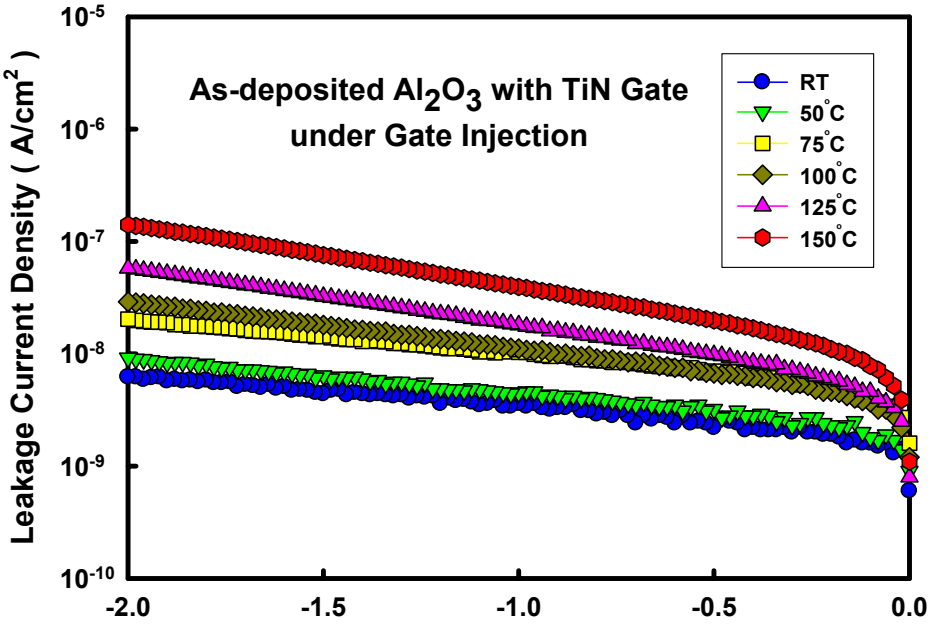


(b)

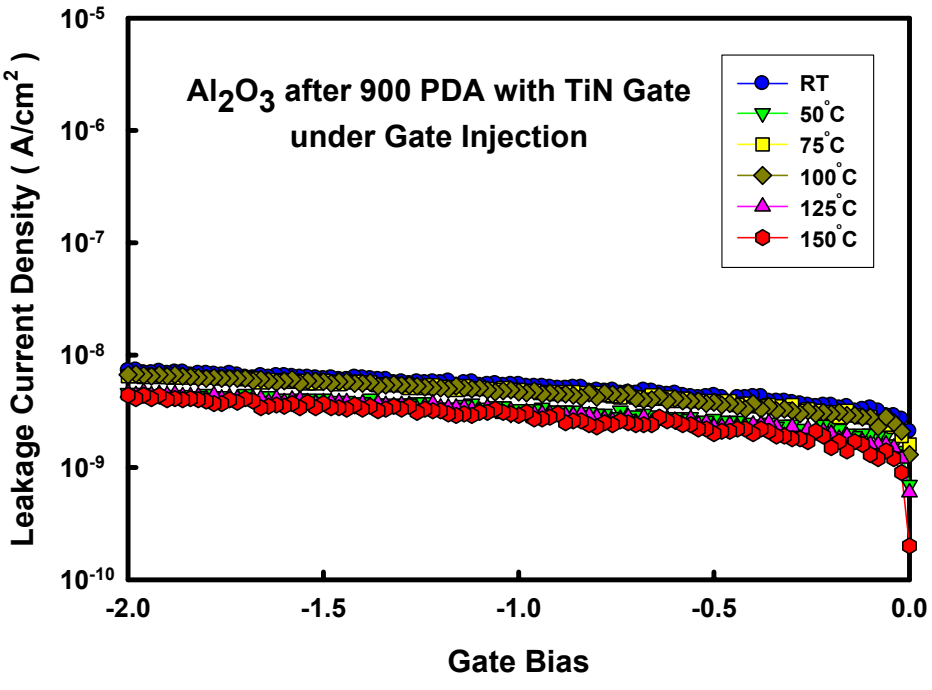
Figure 2-6 Comparison of (a) EOT and (b) leakage current characteristics as a function of PDA temperatures with 400˚C and 450˚C deposition.

	EOT @ -2V(Å)	JG @ +1V (A/cm2)	JG @ -1V (A/cm2)	Hysteresis (mV)	Dispersion 100K/10K	Dispersion 1M/10K
400-As	42.018	5.34×10^{-8}	-6.91×10^{-8}	60	98.98%	58.51%
400-800	34.858	1.58×10^{-8}	-1.51×10^{-8}	10	99.00%	63.90%
400-900	37.81	6.85×10^{-9}	-9.39×10^{-9}	10	99.02%	67.35%
400-1000	44.61	9.59×10^{-9}	-7.05×10^{-9}	10	99.61%	83.01%
450-As	28.41	4.75×10^{-8}	-4.54×10^{-8}	50	99.19%	59.19%
450-800	33.92	3.18×10^{-8}	-2.57×10^{-8}	10	99.03%	70.49%
450-900	38.97	2.82×10^{-8}	-1.57×10^{-8}	10	99.55%	76.66%

Table 2-2 Summarize most of the electrical characteristics under all the conditions of deposition temperature (400˚C and 450˚C) with PDA temperature (800˚C, 900˚C, and 1000˚C).



(a)



(b)

Figure 2-7 The J-V curves of MIS capacitor (a) without 900°C PDA (b) with 900°C PDA under various temperatures, ranging from 25°C to 150°C.

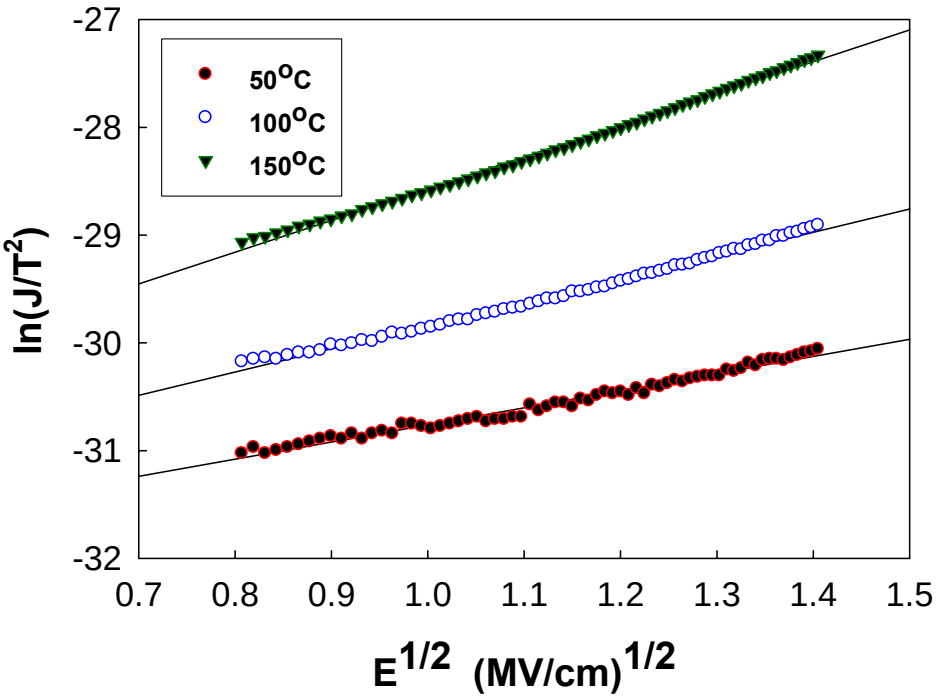


Figure 2-8 The conduction mechanism fitting with Schottky Emission.

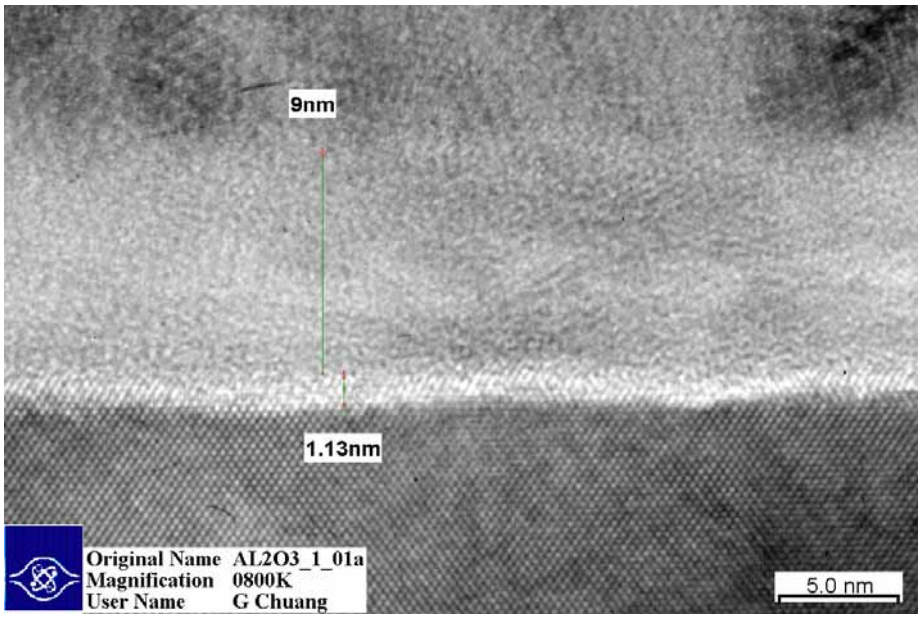


Figure 2-9 The TEM image shows the MIS (TiN/Al_2O_3/Si-substrate) structure with PDA treatment.

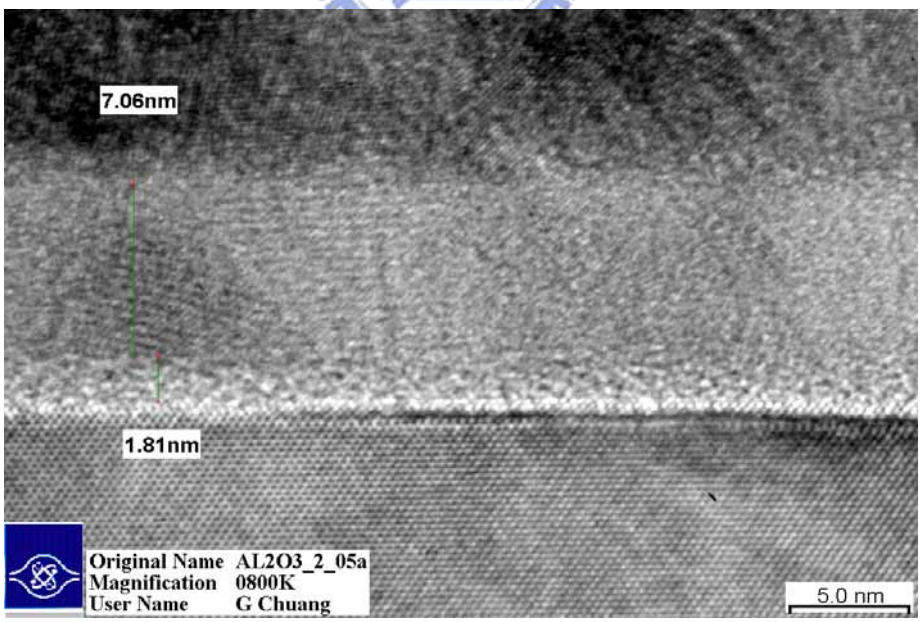
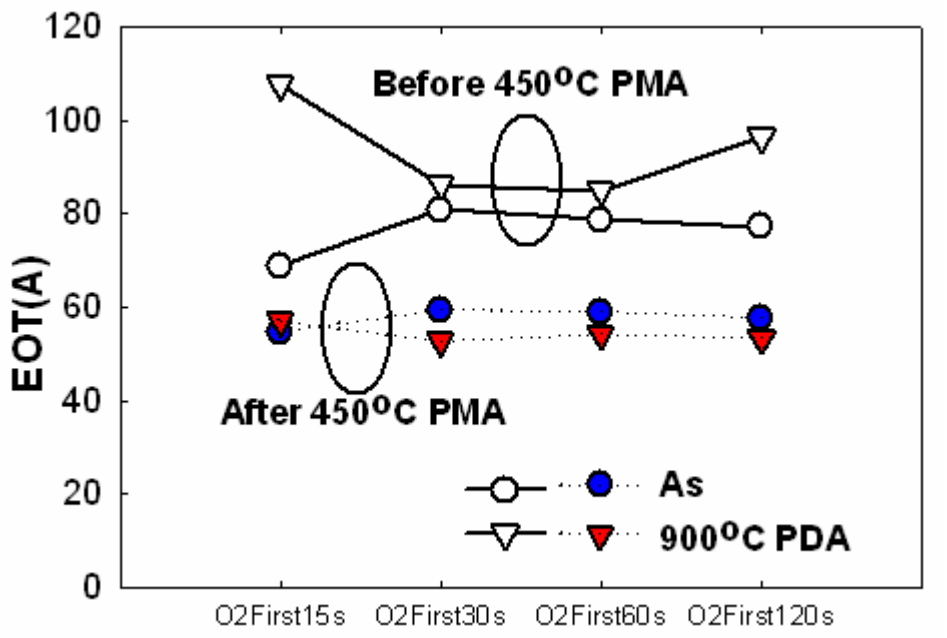


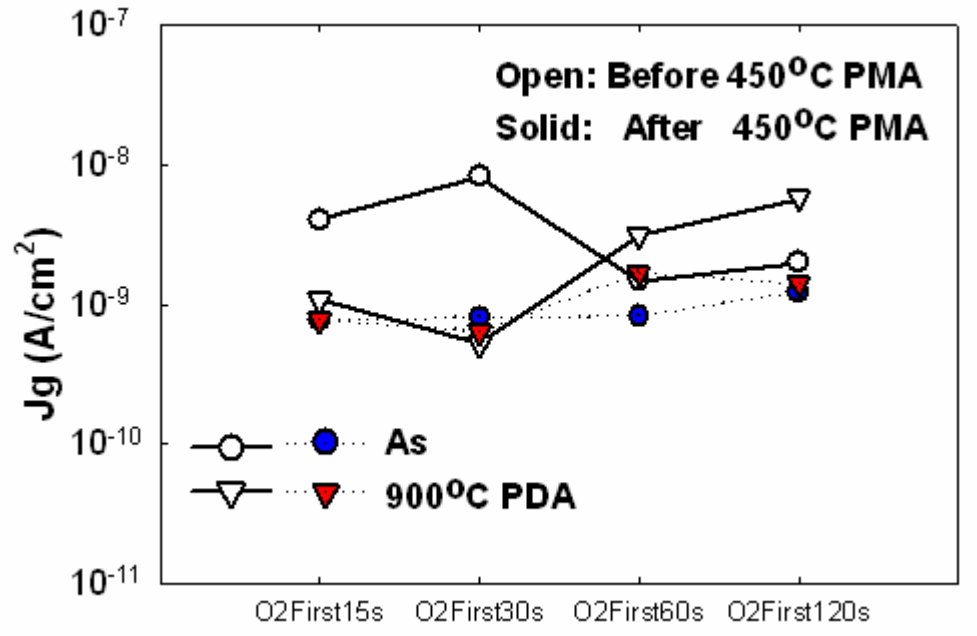
Figure 2-10 The TEM image shows the MIS (TiN/Al_2O_3/Si-substrate) structure with 900°C PDA.

O_2 first 15sec + Al_2O_3
O_2 first 30sec + Al_2O_3
O_2 first 60sec + Al_2O_3
O_2 first 120sec + Al_2O_3
Al_2O_3 + **O_2 after 30sec**
Al_2O_3 + **O_2 after 70sec**
Al_2O_3 + **O_2 after450sec**

Table 2-3 Conditions of oxygen purge time before/ after Al_2O_3 deposition.

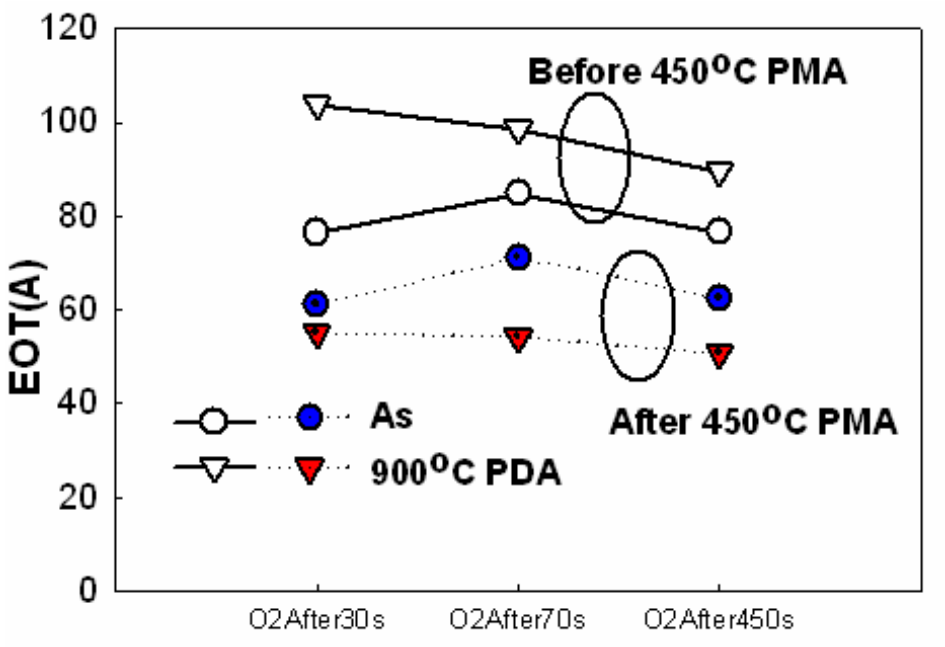


(a)

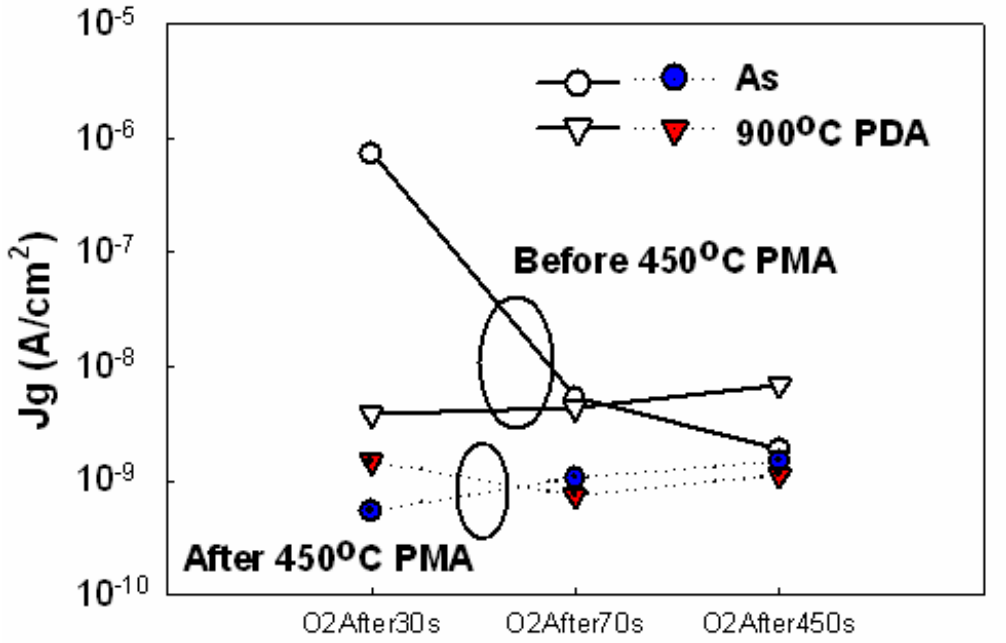


(b)

Figure 2-11 Comparison of (a) EOT and (b) leakage current characteristics as a function of oxygen purge time before Al_2O_3 deposition with and without PMA 450°C.

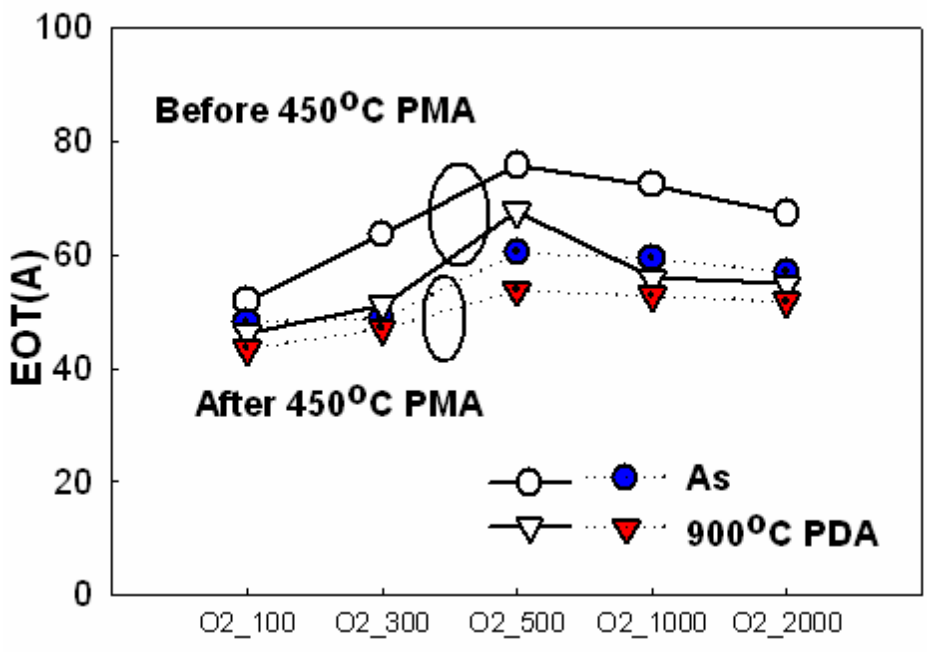


(a)

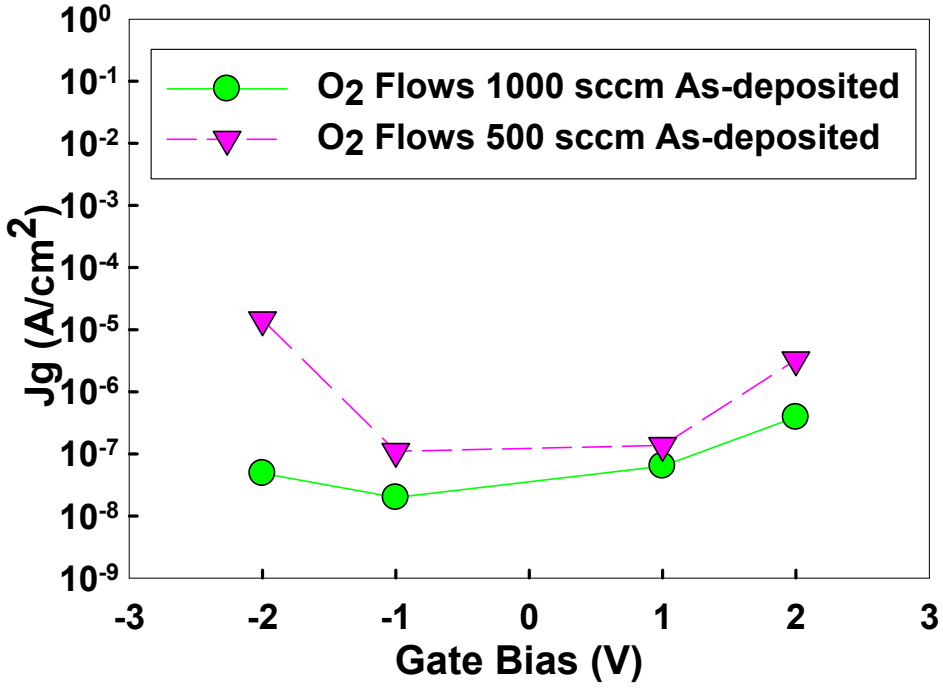


(b)

Figure 2-12 Comparison of (a) EOT and (b) leakage current characteristics as a function of oxygen purge time after Al_2O_3 deposition with and without PMA 450°C.



(a)



(b)

Figure 2-13 (a) EOT performance as a function of oxygen purge time after Al_2O_3 deposition with and without PMA 450°C and (b) leakage current characteristics while oxygen flow is 500 sccm and 1000 sccm.

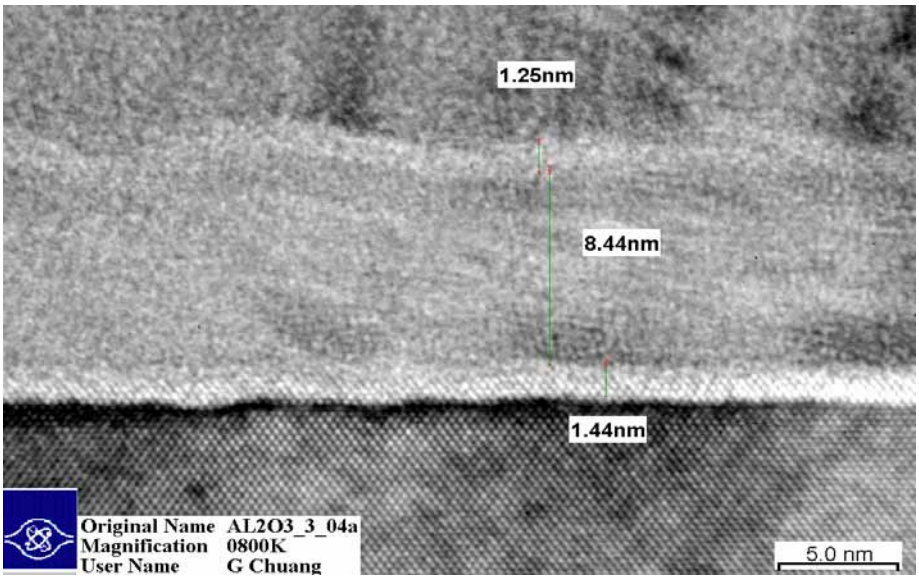


Figure 2-14 The TEM image shows the MIS (TiN/Al_2O_3/Si-substrate) structure with 900°C PDA and 450°C PMA.

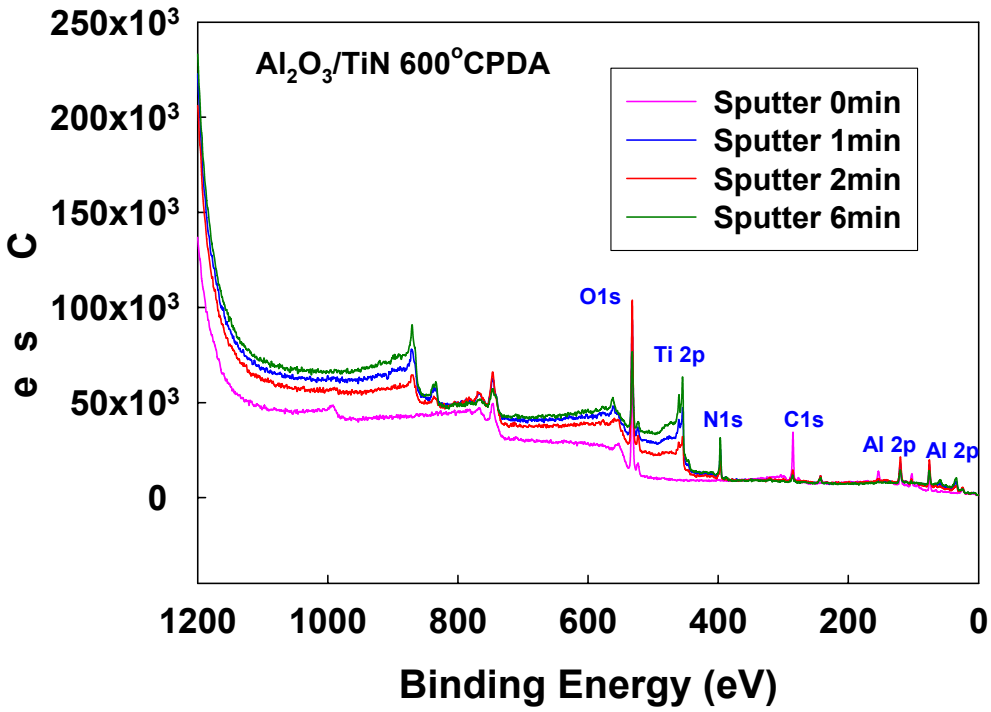


Figure 2-15 The XPS analysis shows the sample of Al_2O_3/CVD TiN structure after 600°C PDA with various sputter time 0, 1, 2, and 6 min.

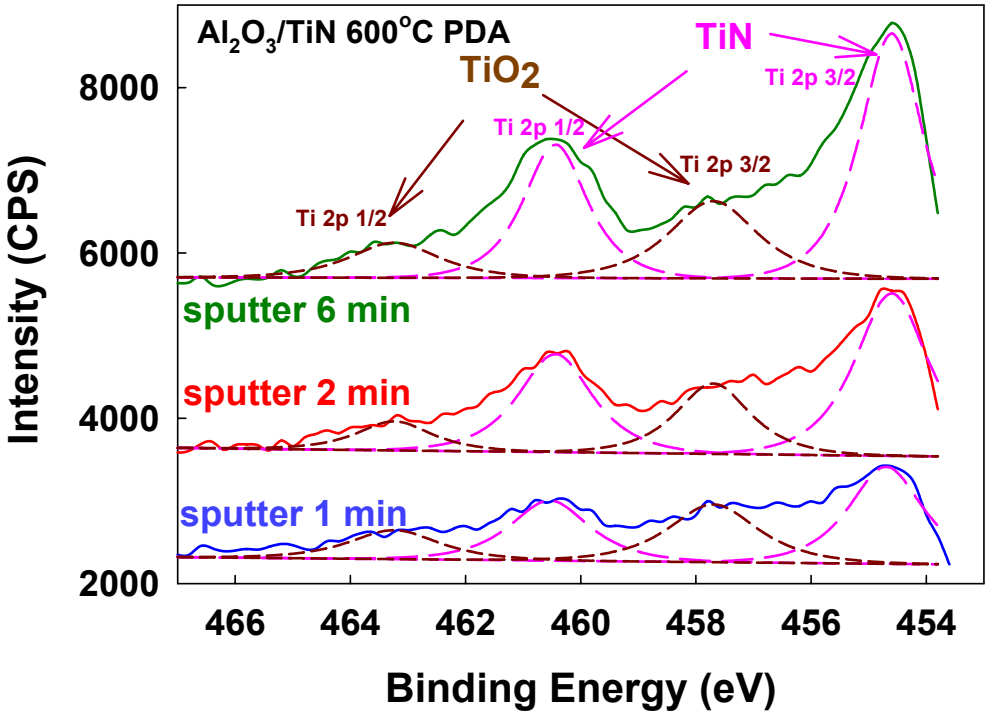


Figure 2-16 The XPS binding energy spectrum of Ti with various sputter time 0, 1, 2, and 6 min.

CHAPTER 3

Characteristics of Al_2O_3 Gate Dielectrics Deposited on TiN Metal

3.1 Introduction

Consideration of high capacitance density, the MIM capacitors (metal/insulator/metal) have been widely used in radio frequency (RF) circuit for a long time [37-39]. Comparing to conventional MIS structure, there is more carriers in metal electrode than in silicon substrate and can raise charge storage. Theoretically, we can raise charge storage in the trench DRAM technology applying the MIM structure. In this Chapter, we also use high-κ material in MIM structure (metal/ high-κ/metal).

First, we study the basic characteristics of the MIM structures. We find out that MIM structures have poor characteristics after high temperature post-deposition annealing (PDA). High leakage current density is observed after 800°C PDA. Then, we do our best to suppress leakage current and find out the leakage mechanism.

3.2 Experiment Details

In this Chapter, we deposited Al_2O_3 thin film on Titanium Nitride (TiN) to form MIM (TiN/Al_2O_3/TiN) structure. The cross-sectional views and processing steps are shown in Figure 3-1.

Consideration of adhesion of TiN on bare-Si, below electrode TiN was deposited on SiO_2 1000Å by physical vapor deposition (PVD) or chemical vapor deposition (CVD) process. Then, we deposited Al_2O_3 thin film on below TiN under the optimum conditions which were discussed in Chapter 2. The Al_2O_3 thin film of approximately 8 nm was deposited on TiN electrode. Annealing of Al_2O_3 thin film was carried out by rapid thermal annealing at three different temperatures (800°C, 900°C, 1000°C) in a N_2 ambient for 30 sec. Pattern is defined by photolithography and metal mask. In the Figure 3-1(a), 2000Å TiN upper electrode was sputtered. Then photoresist was coated on the samples and were developed after exposure, followed by TiN and Al_2O_3 removing, and then, stripping photoresist in the end. Gate electrode definition by metal mask is shown In the Figure 3-1(b) as well. After Al_2O_3 deposition, TiN gate was defined directly by metal mask and then, strip Al_2O_3.

The physical gate oxide thickness was determined by spectroscopy ellipsometer. The equivalent oxide thickness (EOT) was extracted by fitting the measured high-frequency capacitance-voltage (C-V) data from Hewlett-Packard (HP) 4284LCR meter under zero-biased. The tunneling leakage current density-voltage (J-V) was measured by semiconductor parameter analyzer HP4145A. Depth profiles of Al_2O_3 and TiN were analyzed by scanning auger nanoprobe (Auger). The micro-roughness of the TiN surface was detected by atomic force microscopy (AFM).

3.3 Basic MIM Characteristics

3.3.1 MIM ($Al/Al_2O_3/TiN$)

Figure 3-2(a) compares the C-V curves of MIM structure ($Al/Al_2O_3/TiN$) without PDA and 800°C PDA. The below TiN electrode was deposited 2000Å by PVD process. Higher capacitance is observed and dielectric constant (κ) of Al_2O_3 thin film increases from 4.86 to 6.16 with 800°C PDA. Figure 3-2(b) shows the corresponding J-V curves, leakage current density increases obviously from $10^{-8}A/cm^2$ to $10^{-5}A/cm^2$ at gate voltage -1V after 800°C PDA. It should be noted that samples with 900°C and 1000°C PDA are fail. Although high temperature annealing increases capacitance and dielectric constant, the leakage current density increases abruptly at the same time.

Figure 3-3 shows the normalized C-V curves ($\triangle C/C_o$) of MIM structure ($Al/Al_2O_3/TiN$). Voltage coefficient of capacitance (VCC) is one of the important parameters of MIM structure. It has been demonstrated that pure SiO_2 MIM structures show negative parabolic curves in C-V relationship, but high-κ MIM structures exhibit strong positive parabolic curves in C-V relationship [40]. The mechanism of nonlinearity of C-V curves is unclear. It is supposed to relate with E-field polarization, carrier injections [41], high-κ thickness [42、43], frequency [44] and leakage current [45]. Theoretically, VCC decreases with measured frequency increases [42]. It is believed that the carrier mobility becomes smaller with increasing frequency, which leads to a higher relaxation time and a smaller capacitance variation [41]. From the equation below, we calculate α and β listed in Table 3-1.

$$\frac{dC}{C_o} = \frac{C(V) - C_o}{C_o} = \alpha V^2 + \beta V$$

α and β should decrease with frequency increased, however after 800˚C PDA α value of 100KHz and 1000KHz are opposite. It is supposed that MIM structure was damaged after 800˚C PDA and could not exhibit the property of MIM structure. To explain the contradiction, more physical analyses are needed.

3.3.1.1 AFM analysis

Agglomeration in TiN metal gate during high temperature RTA has been investigated [46]. Surface roughness increases from 0.811nm (700˚C -30s) to 1.456 nm (1000˚C -10s) [46]. Figure 3-4 shows the AFM topography of TiN metal electrode with 900˚C and 1000˚C RTA. Our results also show the same phenomenon and RMS roughness of 900˚C- and 1000˚C-RTA sample is 1.027 nm and 1.040 nm, respectively comparing to as-deposited sample is 0.822nm. Due to stress relaxation and grain growth during annealing, the grain boundaries become clearly visible after high temperature RTA treatment [47]. It is found that agglomeration effect might lead to higher gate leakage current density [46] and this is consistent with high leakage current in MIM structure we discussed before.

It has been studied that there is high residual thermal stress on TiN surface after high temperature annealing [46] and thermal expansion coefficient of TiN is about 8.9×10^{-6}/˚C [48]. High thermal expansion causes volume expansion after high temperature annealing resulting in a rough interface between Al_2O_3 thin film and below TiN electrode and damage Al_2O_3 thin film as well. That might be the reasons of high leakage current density in MIM structure. In order to reduce agglomeration, we insert a buffer layer between Al_2O_3 thin film and below electrode TiN.

3.3.2 MIM ($TiN/Al_2O_3/AlN/TiN$)

3.3.2.1 Characteristics of AlN

AlN is chosen as the buffer layer between Al_2O_3 thin film and below TiN electrode. AlN is Wurtzite crystal structure [49、50]. Lattice constant of AlN is 3.111Å. AlN has a large band gap ~6.3eV [48], higher than other high-κ materials such as ZrO_2 (7.8eV), HfO_2 (5.7eV), Ta_2O_5 (4.5eV) (see Table 1-1). Dielectric constant (κ) is 8.2 [51]. As buffer layer, AlN does not lower the κ value of the whole dielectric gate stack. AlN atoms combine with each other by covalent bonds. AlN therefore has good chemical stability, and excellent thermal expansion coefficient $4\times10^{-6}/^{\circ}C$ [51], half than coefficient of expansion of TiN ($8.9\times10^{-6}/^{\circ}C$) [48]. Hence, AlN can absorb thermal expansion stress from TiN electrode and reduce stress damage on Al_2O_3 thin film during high temperature annealing.

AlN thin film was prepared by reactive sputtering of an aluminum target in gas mixture of argon and nitrogen. The aluminum target (99.999% purity) is disk-shaped with diameter of 4 inch. AlN 20Å was deposited under 2 x 10^{-6} torr.

3.3.2.2 Results and discussions

It should be reminded that the below TiN electrode of reference sample was 2000Å deposited by CVD process. From the view point of industry, the trench fill ability of CVD process is much better than PVD process. Therefore, to simulate trench DRAM process, we substituted CVD TiN for PVD TiN as below electrode. The capacitance-voltage (C-V) and leakage current density-voltage (J-V) curves of AlN inserted MIM structure ($TiN/Al_2O_3/AlN$/CVD-TiN) is shown in Figure 3-5.

Comparing to Al/Al_2O_3/PVD-TiN structure, leakage current density is much larger in TiN/Al_2O_3/CVD-TiN structure before high temperature annealing. It might be caused by residual chlorine (Cl) in CVD TiN [52].

In the CVD process, the TiN electrode was deposited by reaction of $TiCl_4$ and NH_3 gas mixture. Deposition temperature was varied from 500°C ~ 650°C. Reaction of $TiCl_4$ and NH_3 is as follows:

$$6TiCl_4 + 8NH_3 \rightarrow 6TiN + 24\ HCl + N_2$$

The residual chlorine diffuses from CVD TiN metal gate to dielectric with high temperature annealing. Out-diffused chlorine forms trap sties with defects in gate dielectrics and damages the gate dielectric reliability. Large leakage current density and poor Weibull distribution are observed in CVD TiN samples. On the other hand, chlorine out-diffusion is not observed in PVD TiN samples, hence, for PVD TiN samples, leakage current is lower and has a tight Weibull distribution [52].

Figure 3-5(a) displays the C-V curve of AlN inserted MIM structure. It should be reminded that EOT of the AlN inserted MIM structure is thicker than the reference samples and it is sensible for lower capacitance with AlN inserted MIM structure. As shown in Figure 3-5(b), leakage current density can be suppressed over than 2 orders by inserted AlN buffer layer due to thicker EOT. Even so, leakage current density increases and capacitance decreases after 600°C PDA.

It is not obviously improved of AlN buffer layer inserted between Al_2O_3 thin film and below electrode TiN. However, AlN buffer layer reduce the nonlinearity of TiN/Al_2O_3/CVD-TiN structure unexpectedly. It is demonstrated that voltage coefficient of capacitance (VCC) of MIM capacitors can be engineered and virtually zero VCC can be achieved by using stacked insulator structure of high-κ and SiO_2 dielectrics [40]. However, SiO_2 in the stacked insulator structure reduce the κ-value of

MIM structure. To avoid the reduction, we can substitute AlN for SiO_2 in other additional studies.

There has been studied that Al_2O_3 will interact with AlN [53]. As the AlN composition and reacting temperature increased, increased volume fractions of AlON phase formed, due to the enhanced reaction of Al_2O_3 and AlN [53]. It is supposed to damage Al_2O_3 composition and fail the AlN inserted MIM structure.

3.3.3 MIM (TiN/Al_2O_3/Ultra-Thin MOCVD-TiN)

Consideration of Cl out-diffusion of CVD TiN, we substitute MOCVD-TiN for CVD-TiN and lessen the thickness of below electrode TiN at the same time. It should be noted that MOCVD TiN precursors do not contain chlorine.

It has been reported that there is high residual stress on TiN metal surface under high temperature annealing, especially in thicker TiN metal [54、55]. High leakage current density is probably induced by hillocks and rough surface due to residual stress on TiN surface. The thickness of below TiN electrode we used is 2000Å. There might be large residual stress in thicker TiN electrode. Residual stress can be reduced and get a smooth interface between Al_2O_3 and TiN electrode by lessen the thickness of the below TiN electrode. Different from 2000Å, two different thicknesses of below TiN electrode: 280Å and 44Å are deposited, followed by the process of capacitance formation we used. Figure 3-6 shows the relationship between surface roughness and different thicknesses of below TiN electrode. Comparing to 2000Å TiN electrode, surface of thinner TiN electrode is smoother. RMS roughness of 280Å and 44Å is 3.43Å and 1.90Å, respectively.

The results in Figure 3-7(a) show the C-V performance of below TiN electrode 280Å. Comparing to below TiN electrode 2000Å, the capacitance of below TiN electrode 280Å is larger. It is supposed that a smoother interface is helpful in reducing the localized field and parasitical capacitance, hence, results in higher capacitance, even after 800°C PDA. It is observed that the capacitance decreases with PDA temperature increases.

Figure 3-7(b) displays the J-V curves of below TiN electrode 280Å. Comparing to below TiN electrode 2000Å, the leakage current density of below TiN electrode 280Å is much lower (about 4 orders). It can be ascribed to eliminate residual chlorine by MOCVD TiN and there are no trap sites formed by residual chlorine and dielectric defects, hence, leakage current can be suppressed. However, leakage current density increases as PDA temperature increases and is up to 10^{-1} A/cm^2 after 900°C PDA.

The C-V performance of below TiN electrode 44Å is shown in Figure 3-8(a). The capacitance of below TiN electrode 44Å before PDA is larger than that of below TiN electrode 2000Å. Similar to TiN electrode is 280Å smoother interface is helpful in reducing the localized field and parasitical capacitance and results in higher capacitance. It is also observed that the capacitance decreases with PDA temperature increases, similar to Figure 3-76(a).

Figure 3-8(b) indicates the J-V curves of below TiN electrode 44Å. Comparing to below TiN electrode 2000Å, the leakage current density of below TiN electrode 280 Å is lower (about 2 orders). It can be contributed to remove residual chlorine by MOCVD TiN and there are no trap sites formed by residual chlorine and dielectric defects, hence, leakage current can be suppressed. However, leakage current density increases as PDA temperature increases and leakage current density is up to 10^{-1} A/cm^2 after 900°C PDA.

To summarize briefly, thinner below TiN electrode deposited by MOCVD indeed improves MIM characteristics, including C-V and J-V performance before high temperature annealing. This is probably caused by residual stress reduction using thinner below TiN electrode and smoother interface between Al_2O_3 and below TiN electrode, which can reduce the localized field and parasitical capacitance. However, leakage current is still increased after high temperature annealing.

It is notable that nonlinearity of C-V curve is much serious in below TiN electrode is 44Å. The mechanism of nonlinearity of C-V curves is unclear. It has been studied that lattice anharmonic interactions can be responsible for the nonlinearity of the dielectric constant [56]. Besides, TiN might be formed incompletely when thickness is too thin and charge could not maintain with external voltage bias.

3.4 Physical analysis

Up to present, we used AlN as a buffer layer between Al_2O_3 and below electrode TiN and substituted thinner below TiN electrode. Substitution for ultra-thin TiN can improve MIM characteristics on C-V and J-V curves without PDA. However, the improvement reduces after high temperature annealing. We find out related papers which have been published and do some physical analyses.

3.4.1 XRD analysis

Generally speaking, crystalline type provides smooth paths for electron tunneling through grain boundary resulting in large leakage current. On the other hand,

amorphous type has a lot of small and irregular grains, and therefore leakage current can be suppressed. The deposited titanium nitride (TiN) films consisted of cubic TiN crystals oriented in the (111) (200) and (220) lattice planes has been investigated [57、58]. Furthermore, it has been reported that TiN films preferentially oriented in the (200) lattice plane have lower resistivitiy and many grain boundaries in comparison with (111)-oriented films [59].

Figure 3-9 displays the X-ray diffraction spectra of CVD TiN with various PDA temperatures. Deposition temperature of CVD TiN is varied from 500°C ~ 650°C. The peak (200) is found at 2Θ=42.96.

3.4.2 Al and Ti diffusion

Under high temperature annealing, it has been studied that unoxidized Al will diffuse to metal Ti [60]. On the other hand, after 650°C annealing for 45min TiN would dissociate at the interface and Ti diffuses into upper layer (Al, in the reference) [40]. Figure 3-10 shows the Auger depth profiles of Al_2O_3 250Å/TiN samples with and without 900°C PDA. Comparison of non PDA and with 900°C PDA is shown in Figure 3-11. It is observed that the intersection of TiN and O move toward TiN bulk after 900°C PDA, ascribed to increased thickness of Al_2O_3. Furthermore, after 900°C PDA the Al and O signals move toward the TiN bulk as well, indicating that the Al and O diffuse toward TiN. A lot of metal ion Ti in the Al_2O_3 thin film and incomplete structure of Al_2O_3 might lead to high leakage current and the abnormal C-V behavior. Furthermore, more physical analyses are necessarily, such as XPS, Auger, and TEM.

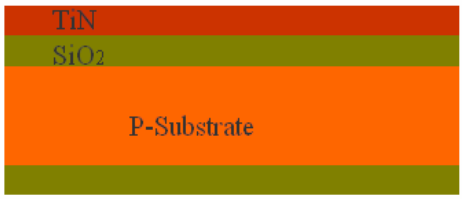
3.5 Summary

In this chapter, we studied PDA effect on MIM structure at first. We met a few questions of large leakage current density under high temperature annealing. Because of low thermal expansion, we inserted AlN buffer layer between Al_2O_3 and below TiN electrode. However, improvement was not obvious.

Secondly, consideration of chlorine out-diffusion, we substituted MOCVD TiN and change thickness of below TiN electrode. It has been studied that there is large residual stress on TiN surface after high temperature annealing. In order to reduce surface stress and get a smoother interface, we deposited two different thicknesses of TiN, 280Å and 44Å. We found out that thinner below TiN electrode indeed improves C-V and J-V performance before high temperature annealing. This is probably caused by removing residual chlorine, reduction of residual stress in thinner below TiN electrode, and smooth interface between Al_2O_3 and below TiN electrode. However, leakage current is still large after high temperature annealing.

Finally, form Auger depth profiles, we found out that TiN might react with Al_2O_3 with high thermal budget resulting in inter-diffusion of Ti and Al. Lots of metal ion Ti in the Al_2O_3 thin film and incomplete structure of Al_2O_3 might be the reason of high leakage current density.

1. CVD or PVD TiN 2000Å after wet oxidation 1000Å.

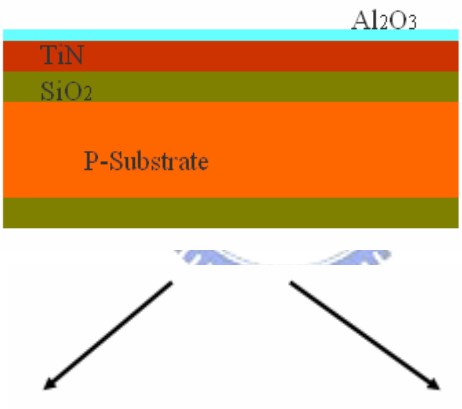


2. Al_2O_3 80Å film deposited by MOCVD.
Deposition temperature: 400˚C

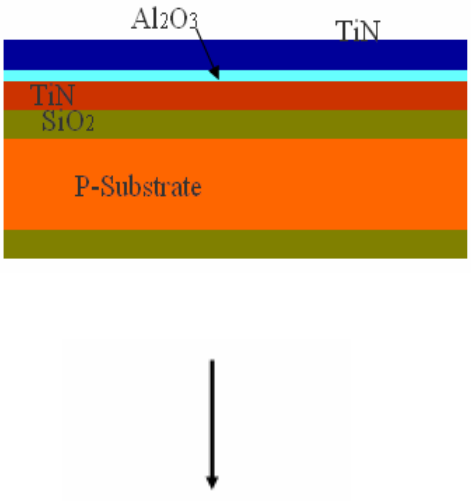
O_2 Purge 30 sec –> Al_2O_3 deposition –> O_2 Purge 30 sec

And oxygen purge flow is 1000 sccm.

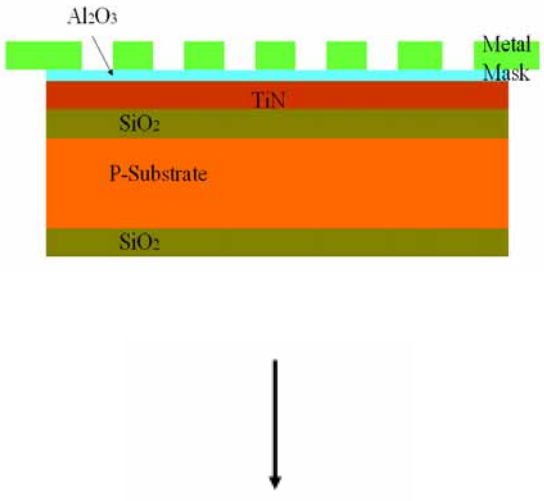
3. Post deposit annealing, PDA: 800˚C, 900˚C, 1000˚C, N_2 30 sec.



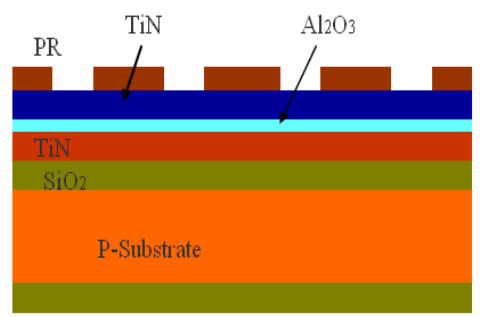
4. (a) TiN metal gate deposition 2000Å.



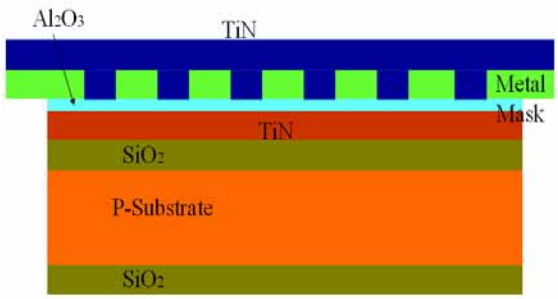
4. (b) Metal mask.



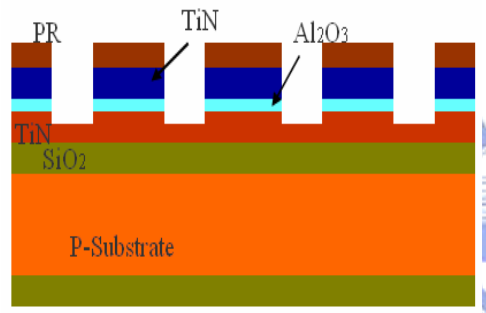
5. (a) PR coating.



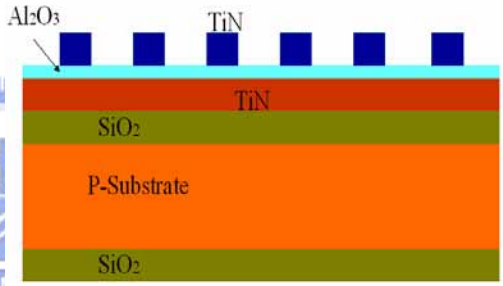
5. (b) TiN deposition 2000Å.



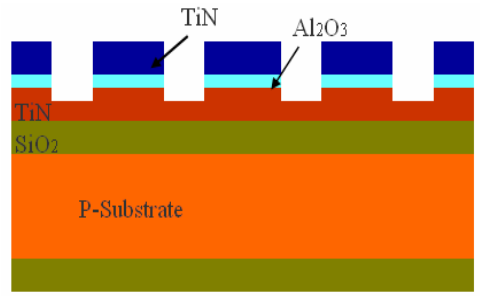
6. (a) TiN and Al_2O_3 etching.



6. (b) TiN gate patterning.



7. (a) PR removing.



7. (b) Al_2O_3 etching.

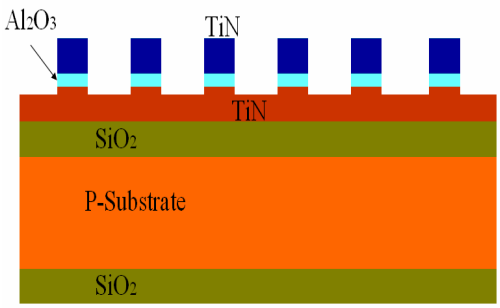
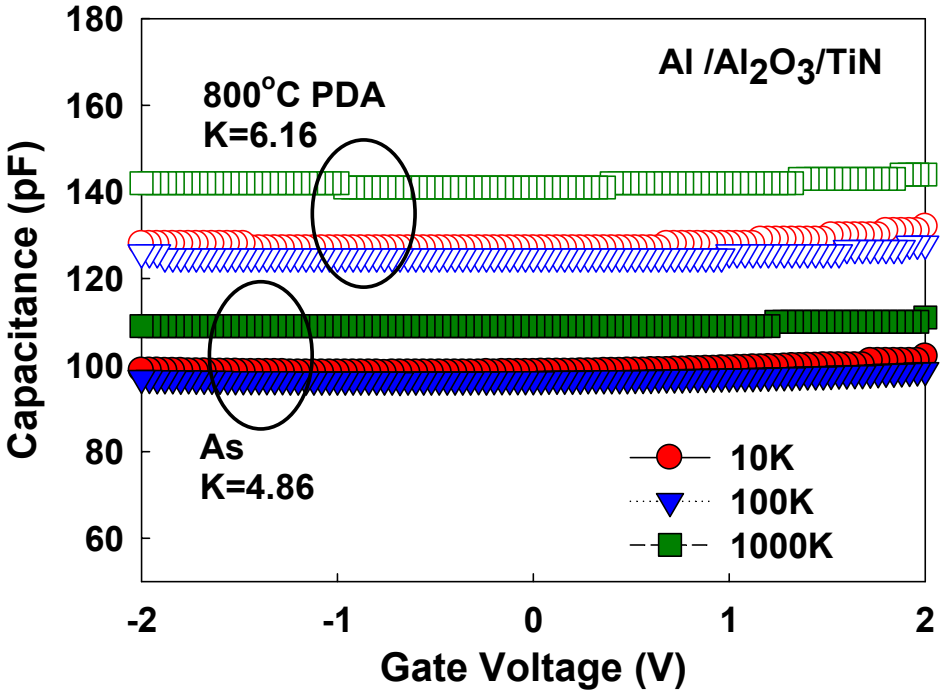
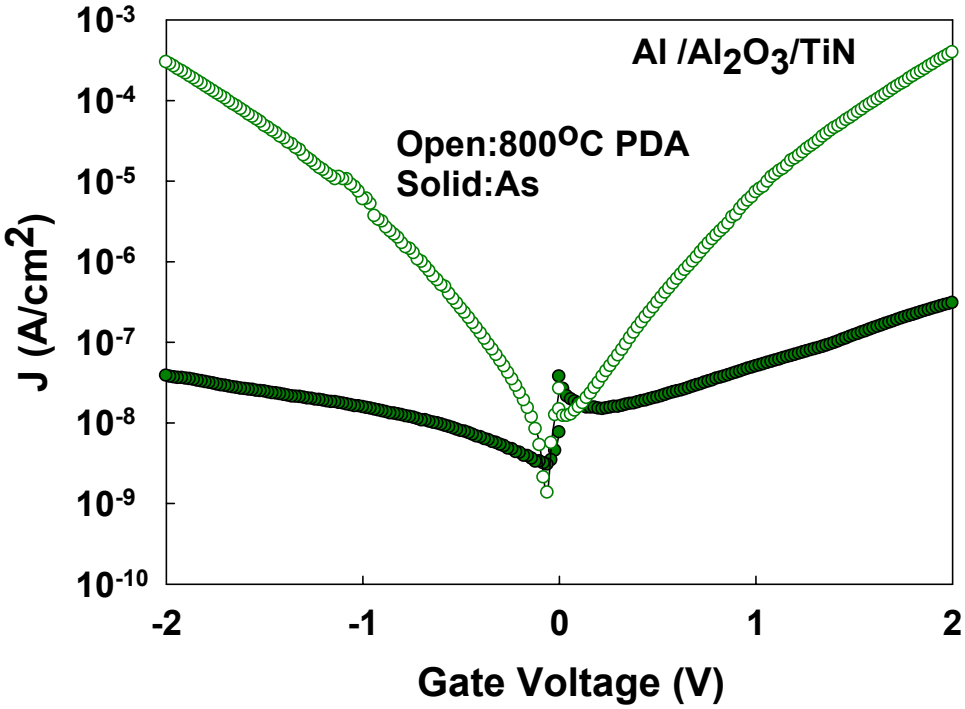


Figure 3-1 The cross-section views of capacitor show MIM structure process flow by (a) photolithography and (b) metal mask.

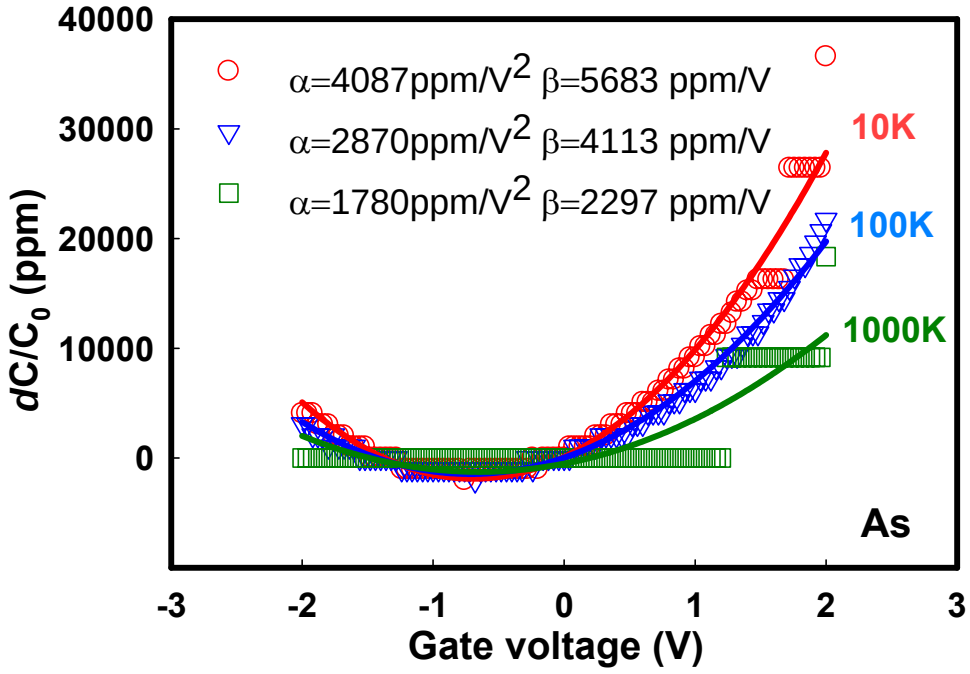


(a)

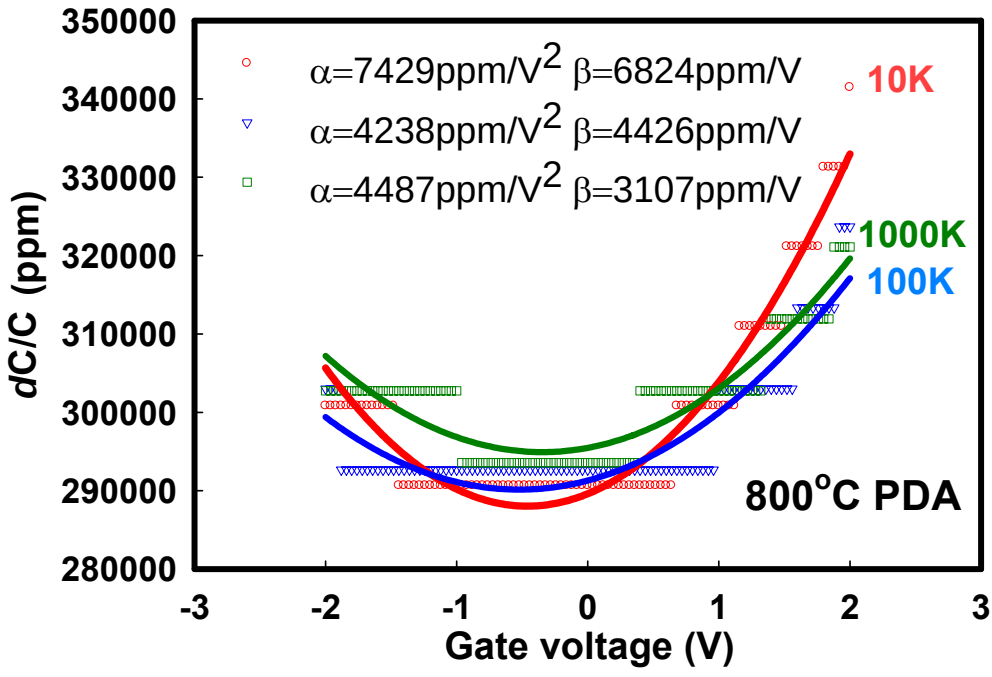


(b)

Figure 3-2 The comparison of (a) C-V and (b) J-V characteristics of MIM structure ($Al/Al_2O_3/TiN$) without PDA and 800°C PDA.



(a)

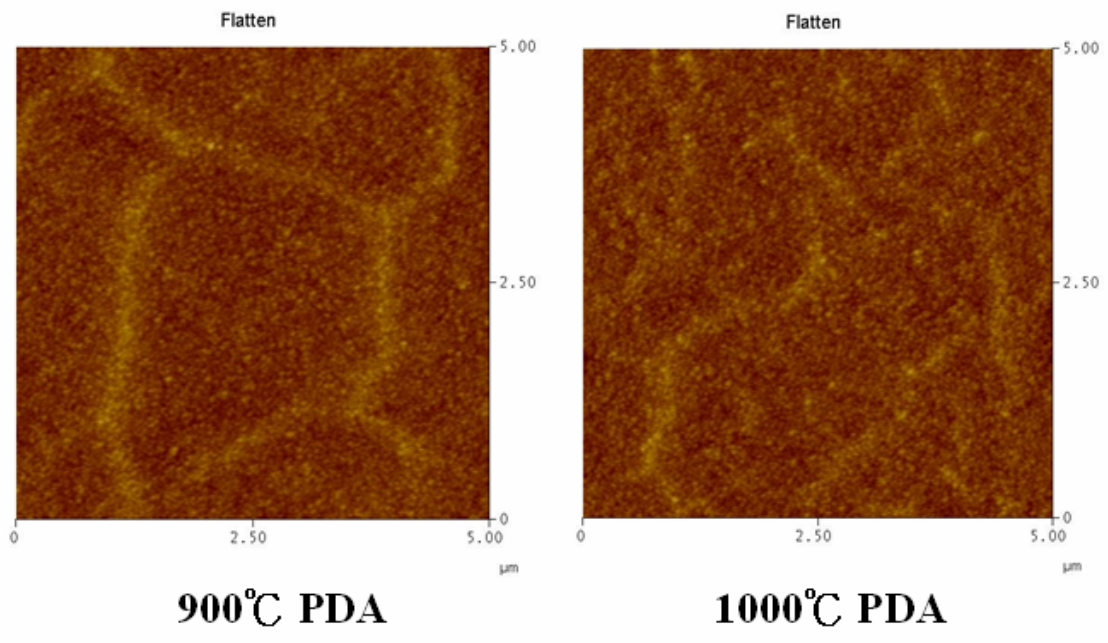


(b)

Figure 3-3 Normalized C-V curves ($\triangle C/C_o$) of MIM structure ($Al/Al_2O_3/TiN$) (a) without PDA and (b) with 800˚C PDA.

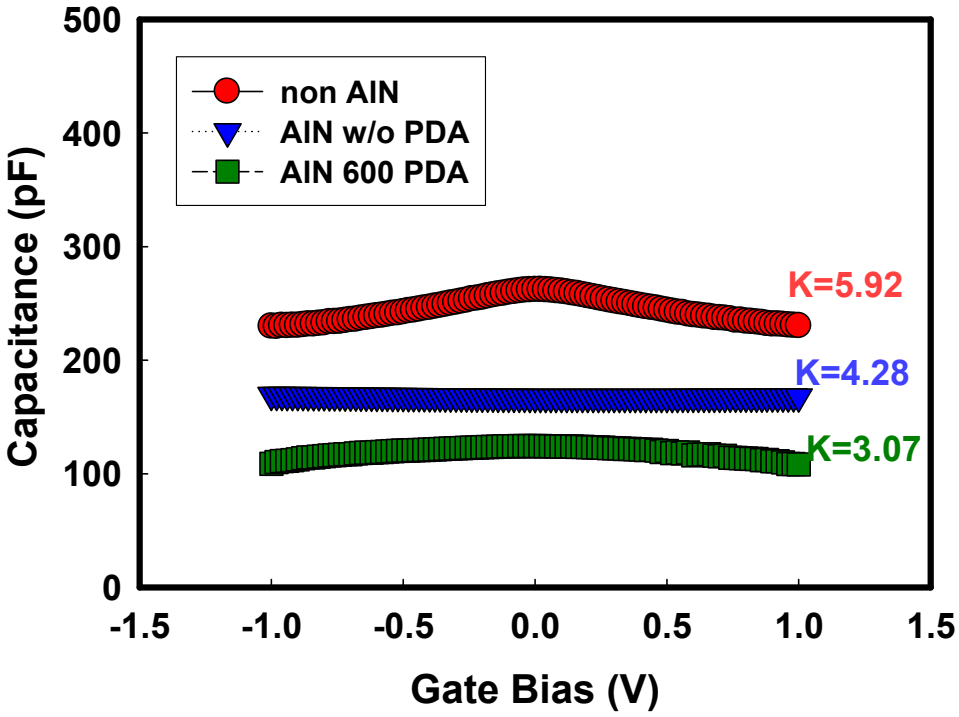
	Frequency	α (ppm/V^2)	β (ppm/V)
As	10K	4087	5683
	100K	2870	4113
	1000K	1780	2297
800˚C PDA	10K	7429	6824
	100K	4238	4426
	1000K	4487	3107

Table 3-1 Summary of α and β extracted from MIM structure (Al/Al_2O_3/TiN) without and with 800˚C PDA.

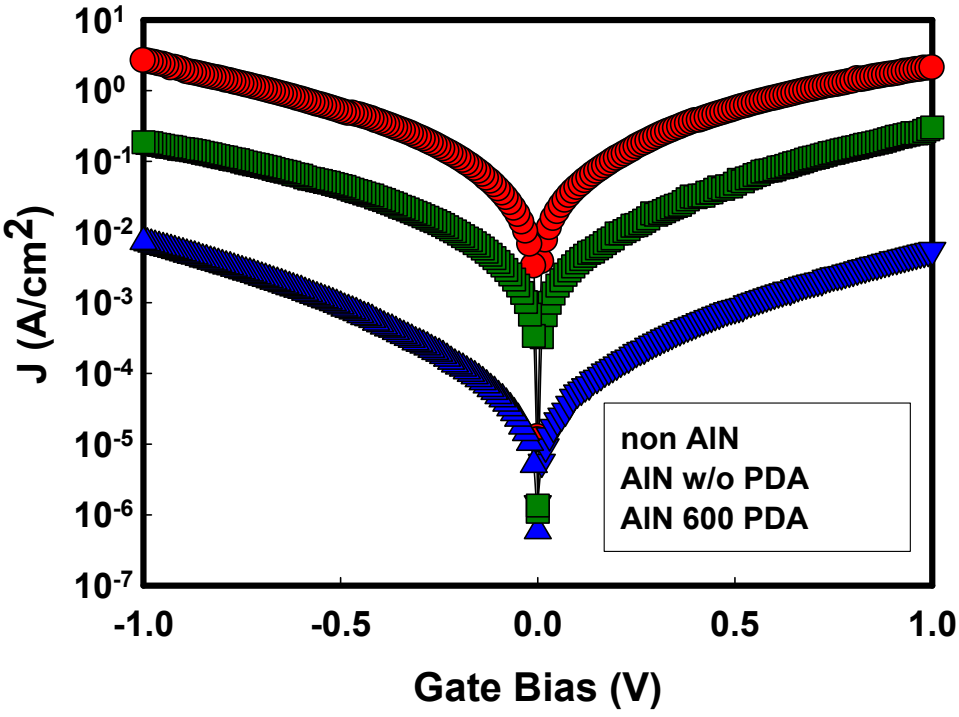


(a) (b)

Figure 3-4 AFM topography of TiN electrode after RTA 30 sec at (a) 900˚C and (b) 1000˚C.



(a)



(b)

Figure 3-5 The (a) C-V and (b) J-V curves of AlN inserted MIM structure ($TiN/Al_2O_3/AlN/TiN$).

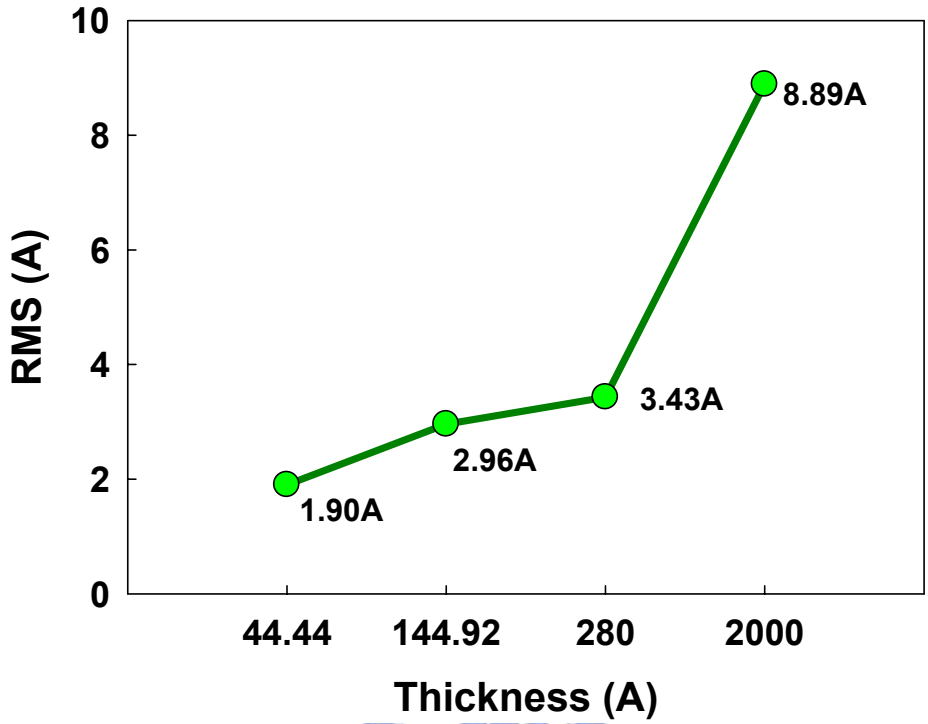
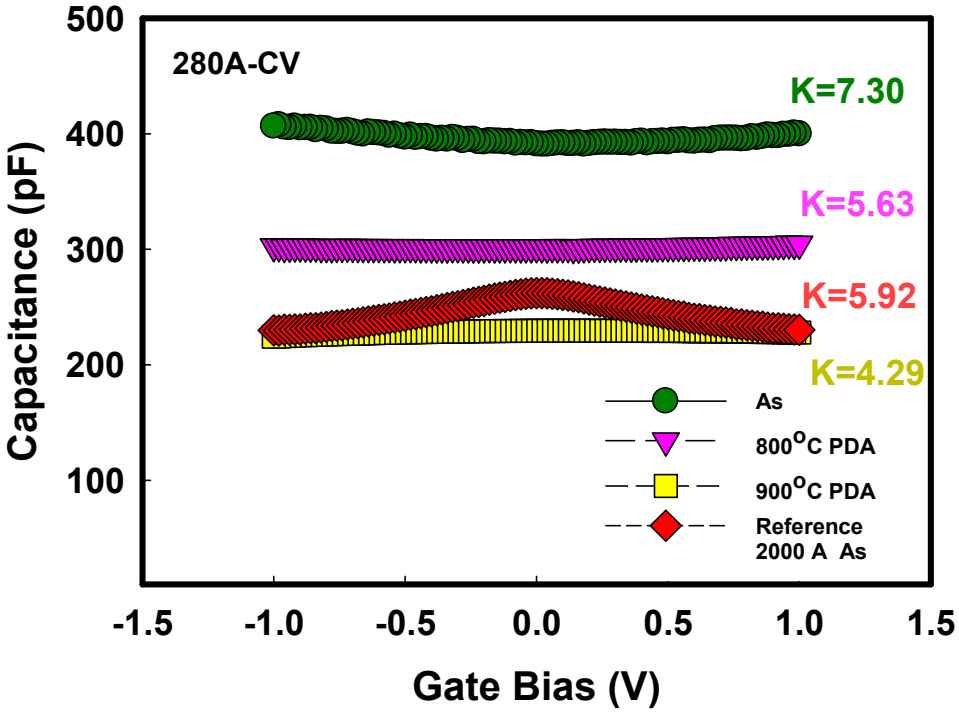
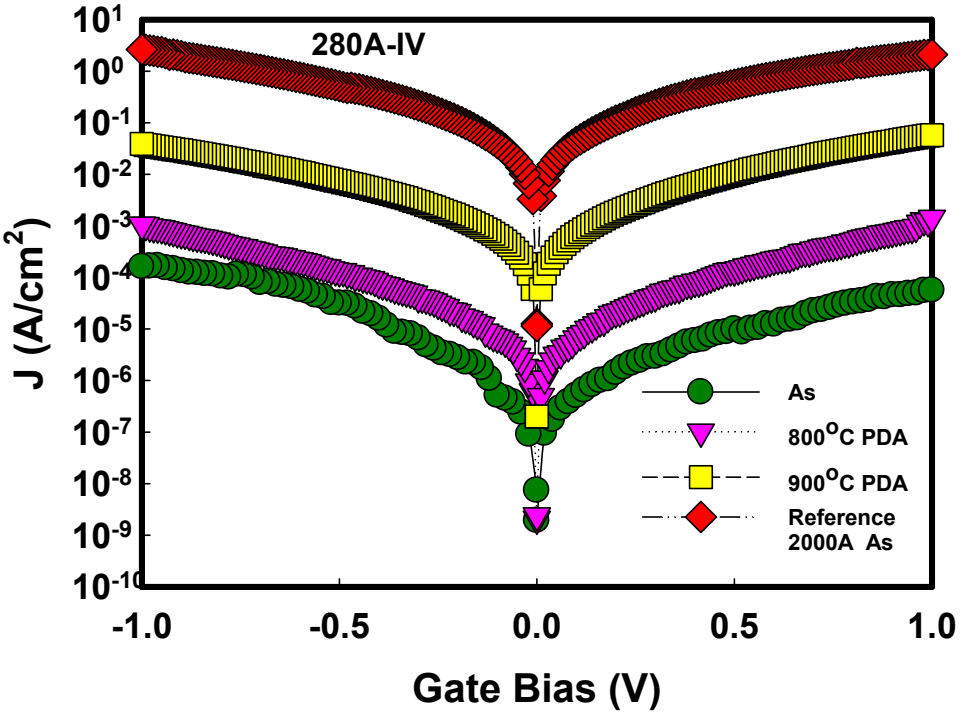


Figure 3-6 The relationship between surface roughness and different thicknesses of below TiN electrode.

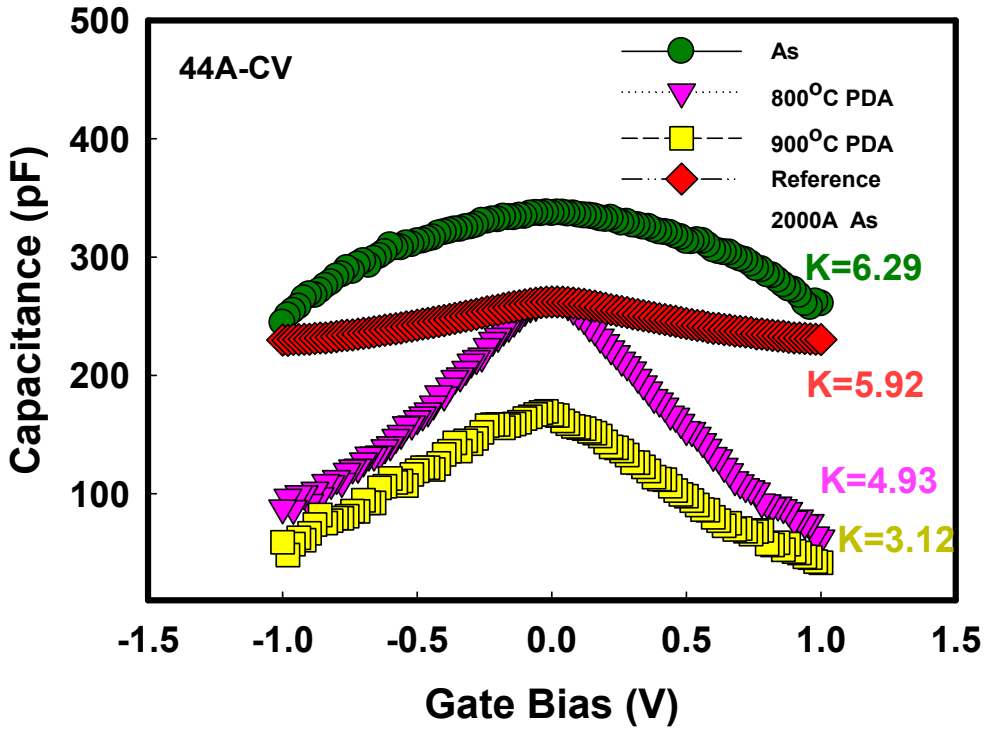


(a)

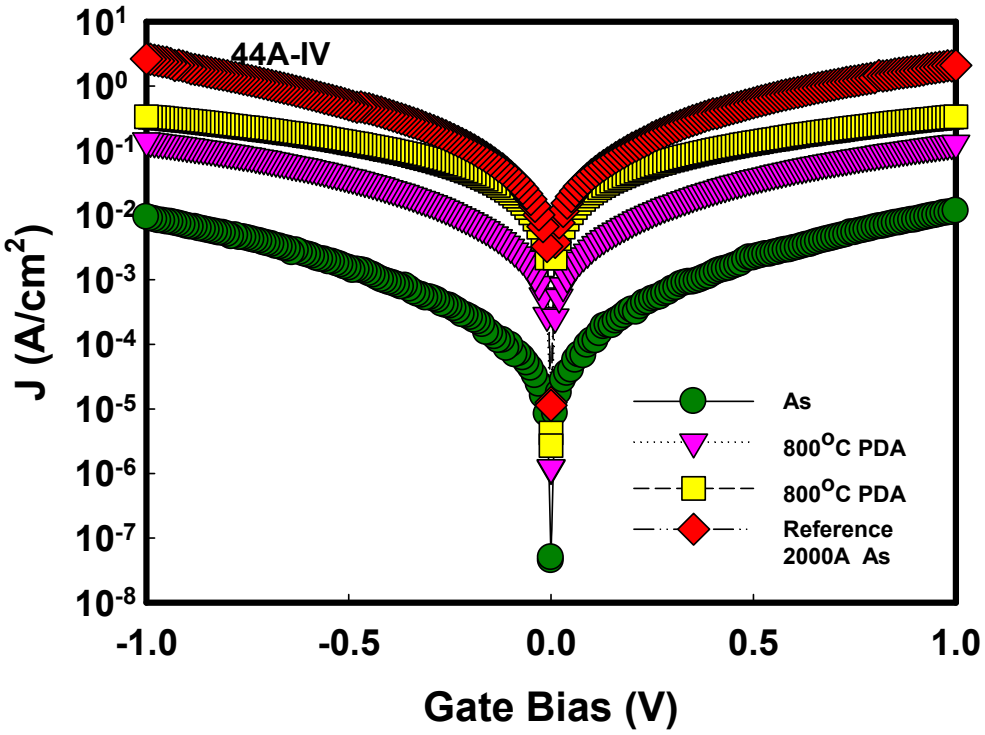


(b)

Figure 3-7 The (a) C-V and (b) J-V curves of the ultra-thin below TiN electrode 280Å, comparing to 2000Å without PDA.



(a)



(b)

Figure 3-8 The (a) C-V and (b) J-V curves of the ultra-thin below TiN electrode 44Å, comparing to 2000Å without PDA.

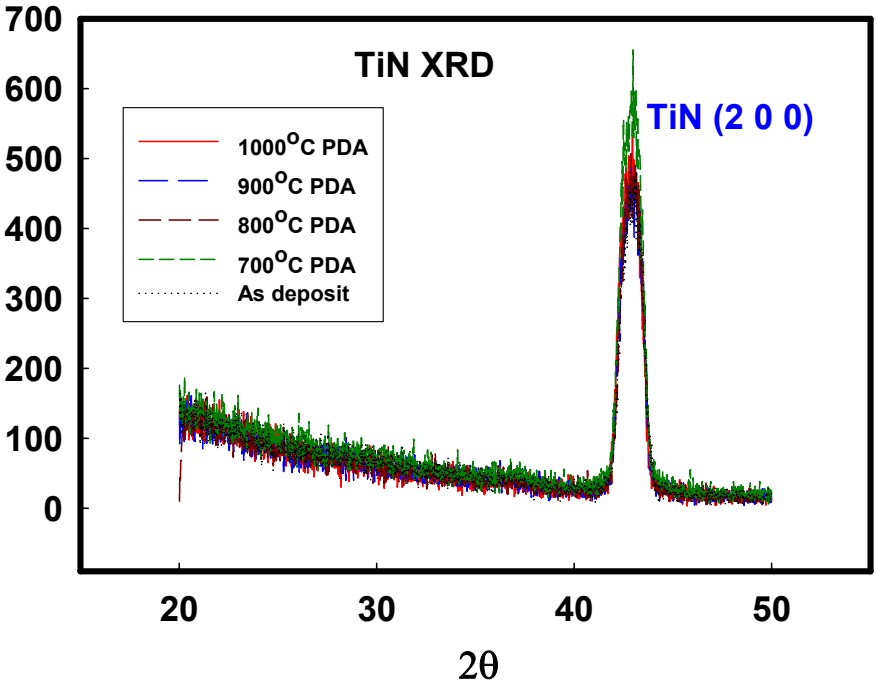
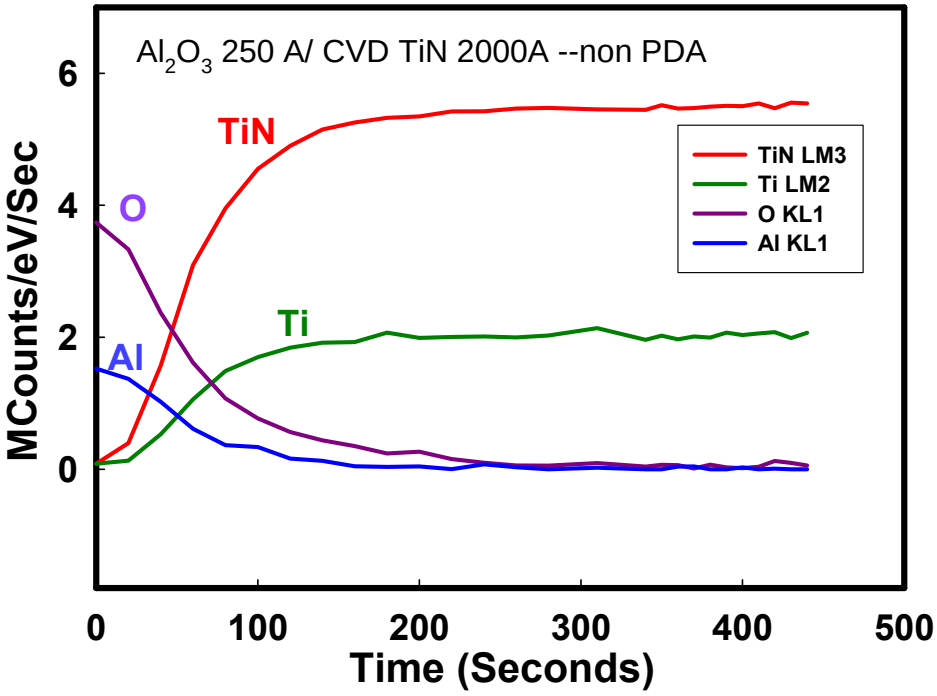
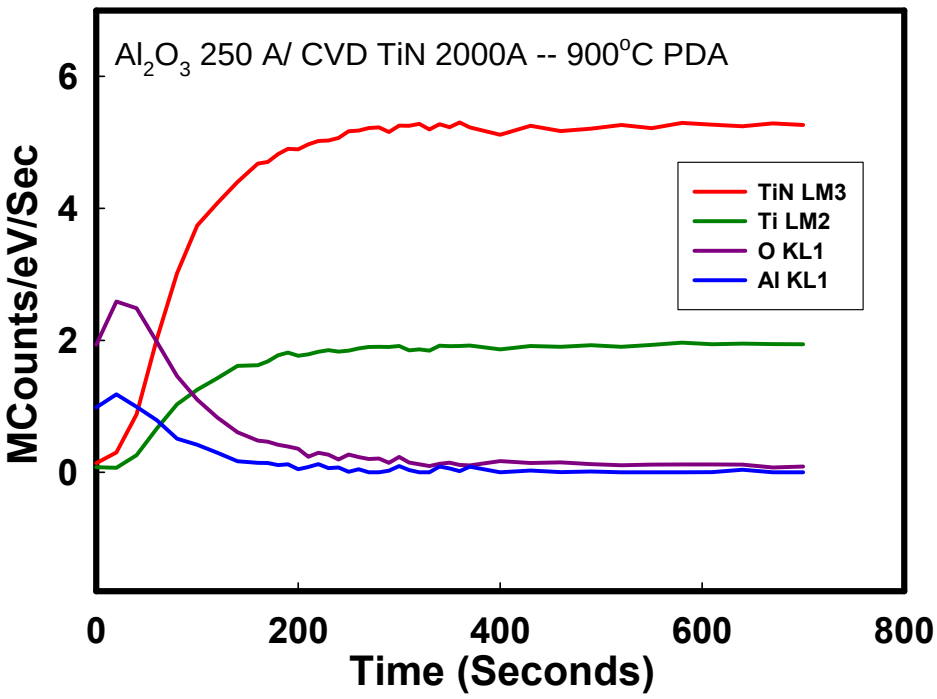


Figure 3-9 X-ray diffraction spectra of CVD TiN after high temperature annealing.



(a)



(b)

Figure 3-10 Auger depth profiles of Al_2O_3 250Å/TiN with (a) non PDA and (b) 900°C for 30 sec.

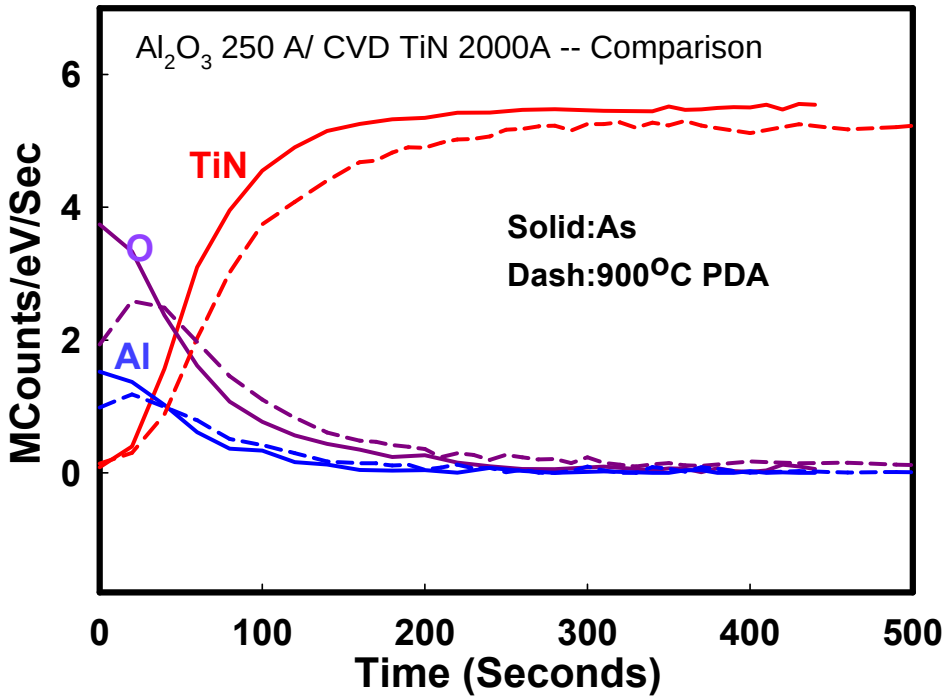


Figure 3-11 Comparison of Auger depth profiles of Al_2O_3 250Å/TiN with and without 900˚C for 30 sec.

CHAPTER 4

Conclusions and Suggestions For Future Work

4.1 Conclusions

In the first part of this thesis, the optimum conditions of Al_2O_3 deposition by MOCVD were investigated. Describe as follows.

Firstly, we found out optimum deposition temperature and PDA temperature is 400°C and 900°C. Much lower leakage current and little hysteresis was obtained with these conditions. Secondly, we studied the oxygen purge effect, including oxygen purge time before/after Al_2O_3 thin film deposition and oxygen purge flow. We found out the optimum condition of oxygen purge process is below:

O_2 Purge 30 sec -> Al_2O_3 deposition -> O_2 Purge 30 sec

And oxygen purge flow is 1000 sccm.

Finally, we discussed the PMA effect. PMA effect can decrease EOT and suppress leakage current. From TEM and XPS analyses, we demonstrated that the interfacial layer between electrode TiN and Al_2O_3 thin film is TiO_2. The κ value of TiO_2 is above 80 resulting in shrinkage of the EOT of whole dielectric gate stack. This was coincident with the electrical characteristics.

In the second part of this thesis, we deposited Al_2O_3 thin film on TiN metal

electrode using these optimum conditions. Several important phenomena were observed and summarized follows. Firstly, we focused on PDA effect on MIM structure. Large leakage current density was observed under high temperature annealing. Secondly, AlN buffer layer is inserted between Al_2O_3 and below TiN electrode to reduce thermal expansion stress from TiN electrode. However, the improvement was not obvious. Thirdly, we changed thickness of below TiN electrode to diminish residual stress on TiN surface and get a smooth interface between Al_2O_3 and below TiN electrode. It does work, however improvement was compressed after high temperature annealing.

Finally, form Auger depth profiles, the reaction of TiN and Al_2O_3 is observed. Ti and Al might diffuse each other. A lot of metal ion Ti in the Al_2O_3 bulk and incomplete structure of Al_2O_3 thin film might be the reason of high leakage current density.

4.2 Recommendations for Future Works

In this thesis, AlN inserted MIM structure (TiN/Al_2O_3/AlN/TiN) was failure. In the future, Pt can be chosen as buffer layer in MIM structure (TiN/Al_2O_3/Pt/TiN) due to its inactive property. If all of the improvement on TiN could not work, maybe we should replace TiN with other metal material, such as Pt, Ir.

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個人簡歷

姓名 ： 陳彥廷

性別 ： 男

出生年月日 ： 民國 69 年 8 月 10 日

籍貫 ： 台灣省台中市

住址 ： 台中市國光號 389 巷 8 號

學歷 ：

國立台灣大學工商管理學系學士 (87.9－92.6)

國立交通大學電子工程研究所碩士 (92.9－94.6)

碩士論文題目 ：

高介電常數材料氧化鋁之特性研究

The Integrated Investigation of High-κ Material Al_2O_3