PAPER

A Low-Power *K*-Band CMOS Current-Mode Up-Conversion Mixer Integrated with VCO*

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SUMMARY A low-power *K*-band CMOS current-mode up-conversion mixer is proposed. The proposed mixer is realized using four analog current-squaring circuits. This current-mode up-conversion mixer is fabricated in 0.13-μm 1P8M triple-well CMOS process, and has the measured power conversion gain of −5 dB. The fabricated CMOS up-conversion mixer dissipates only 3.1 mW from a 1-V supply voltage. The VCO can be tuned from 20.8 GHz to 22.7 GHz. Its phase noise is −108 dBc/Hz at 10-MHz offset frequency. It is shown that the proposed mixer has great potential for low-voltage and low-power CMOS transmitter front-ends in advanced nano-CMOS technologies.

key words: *CMOS, current-mode, K-band, up-conversion mixer*

1. Introduction

Over the last decade, the rapid growth in the field of RF wireless applications has led to considerable effort being expended in the design of high-performance and low-cost RF integrated circuits (RFICs) in advanced CMOS technologies. In addition to the application in the industrial, scientific, and medical (ISM) radio band within 24–24.25 GHz, the FCC has opened the 22–29-GHz frequency band in 2002 for short-range automotive radar systems and autonomous cruise control (ACG) systems [1]. Therefore, the design of *K*-band CMOS RFICs has become very important for these applications.

As the CMOS technology reaches the scale of nanometer nodes, the supply voltage is reduced accordingly to around 1 V or less. The lower the supply voltage, the smaller the voltage headroom left for designing CMOS RFICs. Since a large voltage swing is required to keep signal information in voltage-mode circuits, voltage-mode circuits gradually face the problem of insufficient voltage headroom and become difficult to operate under lower supply voltage. As a result, different circuit design techniques need to be explored.

Current-mode circuit techniques offer the opportunity for low-voltage operations due to the signal information being mainly carried with the time-varying current signals. Therefore, it is possible to design current-mode circuits suitable for smaller voltage headroom. Moreover, a summation of current signals can easily be realized by connecting signal paths together without the use of additional amplifiers; thus, further saving power. With the afore-mentioned advantages, the current-mode circuit techniques offer great potential in the design of RFICs in nano-CMOS technologies.

Among all proposed current-mode CMOS RF front-end circuits [2]–[6] so far, a 24-GHz CMOS current-mode power amplifier is proposed in [2] which offers large output power with high power-added efficiency. Both the *K*-band current-mode CMOS receiver [3] and the 24-GHz CMOS current-mode transmitter [4] as proposed by the present authors have demonstrated the advantages of low supply voltage and low power consumption. A CMOS current-mode preamplifier with low voltage and low power dissipation is presented in [5]. Moreover, a 2-GHz current-mode self-switching up-converter with a 1-V supply is also proposed in [6]. It requires a LO signal power as small as −15 dBm; however, it dissipates 49 mW.

Generally, a large LO signal power of more than 0 dBm is required for voltage-mode mixers, Gilbert-type mixer [7] and dual-gate mixer [8] for example. The high voltage swing is in general required to keep signal information. Nevertheless, the voltage headroom has gradually become insufficient for nano-CMOS technologies which utilize low voltage supplies. In short, these problems may make it difficult for voltage-mode mixers to maintain their operating performance in advanced nano-CMOS technologies.

In this work, a current-mode design technique for *K*-band RF double-balanced up-conversion mixer has been proposed and been verified through a silicon-proven chip in 0.13-μm CMOS process. The short channel effects of this current-mode mixer are also analyzed. The design goal of the proposed current-mode up-conversion mixer is to investigate the new design concept in the CMOS RF front-end circuits. The desired conversion gain is 0 dB at the operation frequency of 24-GHz band with the power consumption as small as possible.

The measurement results have demonstrated that the proposed mixer has advantages of a small power dissipation of 3.1 mW from a low power supply of 1 V. Besides, a small LO signal power level of −4 dBm is required to achieve the measured power conversion gain of −5 dB.

In Sect. 2, the analyses and implementations of the circuits are described. The measurement results are presented in Sect. 3. Finally, the conclusion is given in Sect. 4.

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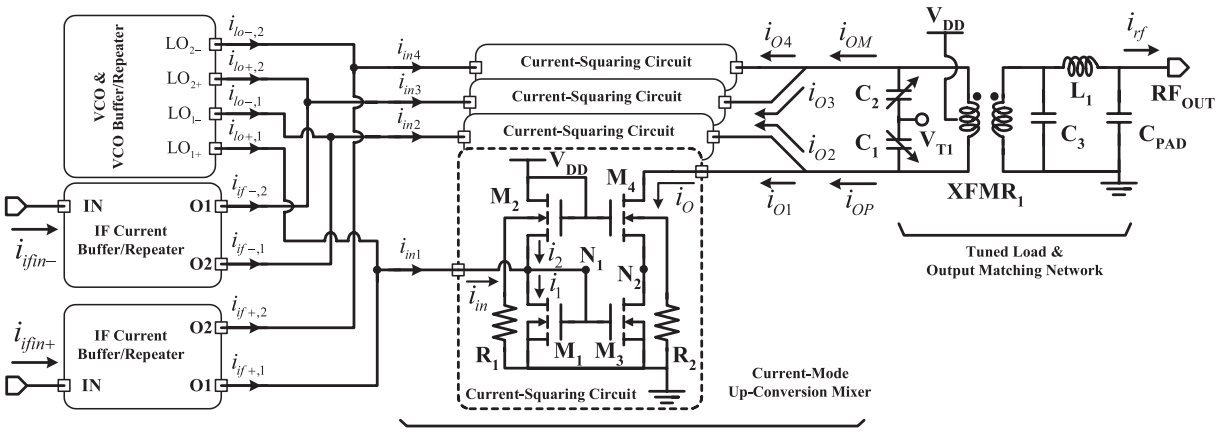


Fig. 1 The circuit of double-balanced current-mode up-conversion mixer.

2. Circuit Analysis and Implementation

2.1 Double-Balanced Current-Mode Up-Conversion Mixer

The circuit diagram of the proposed double-balanced CMOS up-conversion mixer is shown in Fig. 1. The core of the mixer is composed of four analog current-squaring circuits which are originally modified from [9]. The transistors M_1–M_4 are biased in the saturation region. The bulk and source of M_2 and M_4 are separated to reduce the parasitic capacitances at the nodes N_1 and N_2. Lower signal loss is achieved due to smaller parasitic capacitances appeared at nodes N_1 and N_2. With the resistor R_1 (R_2), the impedance of the path from the node N_1 (N_2) to ground through the source-to-bulk parasitic capacitance of M_2 (M_4) is increased. Hence, the signal loss to ground is further reduced.

The squaring circuit is improved by adding the transistor M_4 which acts as a current buffer and keeps the V_{DS} of M_3 the same as the V_{DS} of M_1 in order to alleviate the channel length modulation. The current i_1 is multiplied by the current-mirror circuit formed by M_1 and M_3 where the aspect ratio of M_3 is N times that of M_1. The sum of the gate-to-source voltages of M_1 and M_2 is kept constant and equal to V_{DD}. Based on the square-law drain current equation for simplicity, the relationship between i_{in} and i_O is expressed as [4]

$$i_O = N \times i_1 = N\left(\frac{i_{in}^2}{16I_B} + \frac{i_{in}}{2} + I_B\right) \tag{1}$$

$$I_B \equiv \frac{1}{8}k_n\frac{W}{L}(V_{DD} - 2V_{th})^2 \tag{2}$$

where V_{th} is the threshold voltage, W/L is the channel width to channel length ratio of the MOS devices, and $k_n = \mu_n C_{ox}$ is the zero vertical-field mobility μ_n multiplied by the oxide capacitance per unit area C_{ox}. From the first term of (1), the current-squaring function is realized. The second and third terms of (1) are unwanted components and are to be removed.

The four inputs of the mixer are $i_{in1} = (i_{lo+,1} + i_{if+,1})$, $i_{in2} = (i_{lo-,1} + i_{if-,1})$, $i_{in3} = (i_{lo+,2} + i_{if-,2})$, and $i_{in4} = (i_{lo-,2} + i_{if+,2})$. $i_{if+,1}$, $i_{if-,1}$, $i_{if+,2}$, and $i_{if-,2}$ are two-pair differential IF signals where $i_{if+,1} = i_{if+,2} = i_{if+} = I_{IF}\cos\omega_{IF}t$ and $i_{if-,1} = i_{if-,2} = i_{if-} = -I_{IF}\cos\omega_{IF}t$. Furthermore, $i_{lo+,1}$, $i_{lo-,1}$, $i_{lo+,2}$ and $i_{lo-,2}$ are two-pair differential LO signals where $i_{lo+,1} = i_{lo+,2} = i_{lo+} = I_{LO}\cos\omega_{LO}t$ and $i_{lo-,1} = i_{lo-,2} = i_{lo-} = -I_{LO}\cos\omega_{LO}t$. The summation of IF and LO current signals is performed by directly connecting the wires of LO and IF together without additional power dissipations.

With the differential LO and IF signals, the LO and IF leakages which result from the second term of (1) can be eliminated at the mixer output if the output currents $i_{O1} - i_{O4}$ of the four current-squaring circuits are summed together as $i_{OP} = (i_{O1} + i_{O2})$ and $i_{OM} = (i_{O3} + i_{O4})$. The summations of current signals are performed using wire connections. In addition, the even-order harmonics resulted from square terms of LO and IF current signals are eliminated by the subtraction of i_{OP} and i_{OM}.

Some circuits that perform subtraction of current signals have been reported [10], [11]. As for the circuit in [10], current signals flowing through two unequal paths will result in gain and phase differences, and additional poles will lead to signal losses in high frequency. Besides, higher voltage headroom and additional power are required. In [11], LC network is adopted to perform current subtraction. However, only it can have good subtraction only at the resonant frequency.

In the proposed design, the transformer $XFMR_1$ is adopted to achieve high frequency and wideband subtraction of current signals. The $XFMR_1$ avoids excessive voltage drop. This also ensures that the proposed mixer operates well at a low power supply. From (1) and with the four inputs of the mixer, the resultant RF output current $i_{rf} = \eta(i_{OP} - i_{OM})$ can be derived as

$$i_{rf} = \frac{\eta N I_{LO} I_{IF}}{4I_B}\left[\cos(\omega_{LO}+\omega_{IF})t + \cos(\omega_{LO}-\omega_{IF})t\right] \tag{3}$$

where η represents the losses from the on-chip transformer $XFMR_1$ and the output impedance matching network. From

(3), it can be seen that the mixer function is realized. With the exclusion of the losses η, the intrinsic current conversion gain $CG_{intrinsic}$ of the proposed current-mode mixer is expressed as

$$CG_{intrinsic} \equiv \frac{(i_{OP} - i_{OM})|_{\omega=(\omega_{LO}+\omega_{IF}) \text{ or } \omega=(\omega_{LO}-\omega_{IF})}}{2(i_{if+} - i_{if-})\big|_{\omega=\omega_{IF}}} = \frac{NI_{LO}}{16I_B}. \quad (4)$$

As can be seen from (4), the intrinsic current conversion gain is proportional to the magnitude of the LO current I_{LO}.

The designed parameters (W/L) of M_1, M_2, M_3 and M_4 of the current-squaring circuit in Fig. 1 are (6 μm/0.13 μm), (6 μm/0.13 μm), (48 μm/0.13 μm), and (48 μm/0.13 μm), respectively. Moreover, R_1 and R_2 are with the value of 8 kΩ. In the advanced deep sub-micron CMOS technologies, the relationship between the drain current i_{DS} and the gate overdrive voltage $v_{OV} = (v_{GS} - V_{th})$ of CMOS devices is not exactly square due to short channel effects. As the proposed mixer is designed in the supply voltage of 1 V, the threshold voltages V_{th} of M_1 and M_2 are about 420 mV and 500 mV, and the gate-to-source voltages v_{GS} of M_1 and M_2 are about 455 mV and 545 mV, respectively. M_1 and M_2 are operated in the saturation region, and the v_{OV} of M_1 and M_2 are small. Hence, the drain current i_{DS} is approximated as the following equation to analyze the second-order effects of the proposed mixer [3].

$$i_{DS} \approx \frac{1}{2}k_n\frac{W}{L}v_{OV}^2(1 + \lambda v_{DS}). \quad (5)$$

where the coefficient λ models the effect of the channel length modulation which is related to v_{DS}.

Although both M_1 and M_2 are with the same device size and are diode-connected, the drain-to-source voltages of M_1 and M_2 are different due to the fact that the latter suffers from body effect. Therefore, the channel length modulation effect should be considered. From Fig. 1, $V_{DD} = (v_{DS,M1} + v_{DS,M2})$. If $\delta = (v_{DS,M2} - v_{DS,M1})/2$ is assumed, $v_{DS,M1} = (V_{DD} - 2\delta)/2$ and $v_{DS,M2} = (V_{DD} + 2\delta)/2$. After some derivations, the expression i_O in (1) is modified and expressed as

$$i_{O,short} \approx N\left(\chi_1\frac{i_{in}^2}{16I_B} + \chi_2\frac{i_{in}}{2} + \chi_3 I_B\right) \quad (6)$$

where

$$\chi_1 = \frac{2(2+\lambda V_{DD}-6\lambda\delta)}{(2+\lambda V_{DD})(2+\lambda V_{DD}-4\lambda\delta)+2\lambda\delta(2+\lambda V_{DD}+2\lambda\delta)} \quad (7)$$

$$\chi_2 = \frac{\left[2(2+\lambda V_{DD})(2+\lambda V_{DD}-4\lambda\delta)-(2+\lambda V_{DD}-2\lambda\delta)^2\right]}{[(2+\lambda V_{DD})(2+\lambda V_{DD}-4\lambda\delta)+2\lambda\delta(2+\lambda V_{DD}+2\lambda\delta)]} \quad (8)$$

$$\chi_3 = \frac{(2+\lambda V_{DD})(2+\lambda V_{DD}+2\lambda\delta)(2+\lambda V_{DD}-4\lambda\delta)}{2[(2+\lambda V_{DD})(2+\lambda V_{DD}-4\lambda\delta)+2\lambda\delta(2+\lambda V_{DD}+2\lambda\delta)]}. \quad (9)$$

Note that χ_1 and χ_2 are less than 1, whereas χ_3 is greater than 1. As $V_{DD} = 1$ V, $\lambda \approx 0.77\,\text{V}^{-1}$, and $\delta \approx 45$ mV, $\chi_1 \approx 0.68$, $\chi_2 \approx 0.97$, and $\chi_3 \approx 1.38$. Furthermore, the above derivations only consider body effect and channel length modulation effect, and the rest of short channel effects are ignored because of small v_{OV}.

From the above derivations (4), (6) and (7), the current conversion gain with the channel length modulation effect can be further expressed as

$$CG_{intrinsic,short} \approx \chi_1\frac{NI_{LO}}{16I_B}. \quad (10)$$

This indicates that the conversion gain of the mixer with short-channel devices is less than that of the mixer with long-channel devices. Besides, the parameter λ that models channel length modulation has a significant effect on $CG_{intrinsic}$.

Under the simulated conditions of the IF Frequency at 200 MHz and the LO frequency at 24 GHz, the relationship among the simulated $CG_{intrinsic}$, the equivalent calculated input LO power $P_{LO,IN}$, and the amplitude of the differential LO current signal $i_{diff-loin} = 2(i_{lo+} - i_{lo-})$ is depicted in Fig. 2. It can be seen that the simulated $CG_{intrinsic}$ is higher than 0 dB if the amplitude of $i_{diff-loin}$ is greater than 1.5 mA or $P_{LO,IN}$ is greater than −8.2 dBm. Shown in Fig. 3 is the relationship between the simulated $CG_{intrinsic}$ and the amplitude of differential IF current signal $i_{diff-ifin} = 2(i_{if+} - i_{if-})$. When

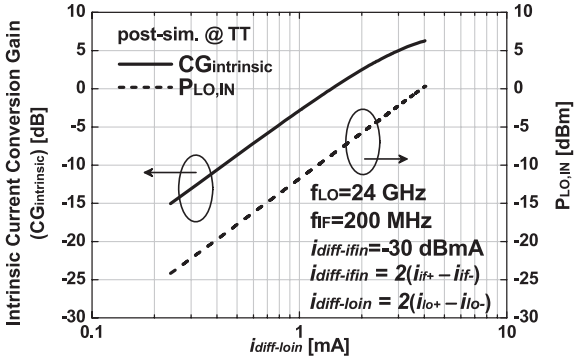


Fig. 2 The relation among simulated $CG_{intrinsic}$, the equivalent $P_{LO,IN}$, and the amplitude of the differential LO current signal $i_{diff-loin}$ of the mixer.

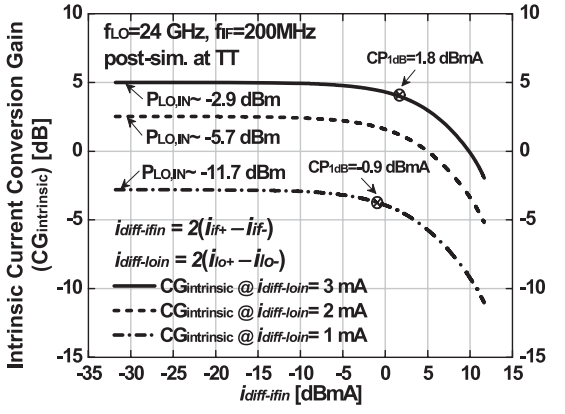


Fig. 3 The relation between simulated $CG_{intrinsic}$ and the amplitude of the differential IF current signal $i_{diff-ifin}$ of the mixer.

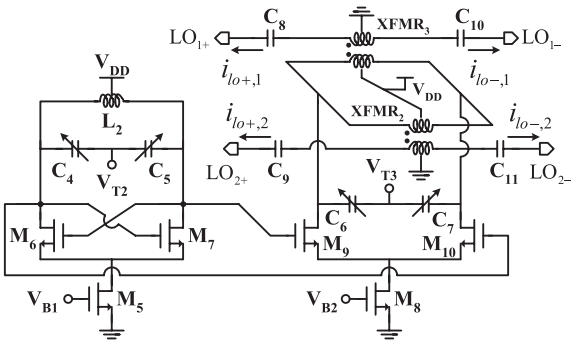


Fig. 4 The circuits of VCO and transformer-based VCO buffer/repeater.

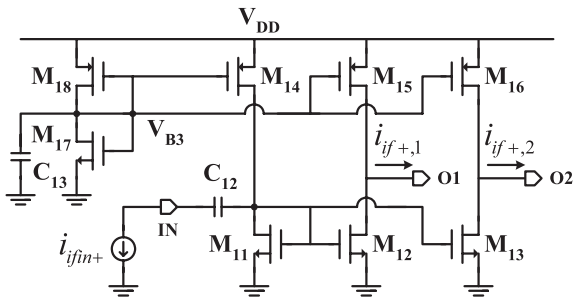


Fig. 5 The circuit of IF current buffer/repeater.

the amplitude of $i_{diff-loin}$ is equal to 1 mA where the equivalent $P_{LO,IN}$ is equal to −11.7 dBm, the simulated $CG_{intrinsic}$ is −2.3 dB and the 1-dB compression point of intrinsic current conversion gain ($CP_{1\,dB}$) is −0.9 dBmA. As the amplitude of $i_{diff-loin}$ is increased to 3 mA where the equivalent $P_{LO,IN}$ is equal to −2.9 dBm, the simulated $CG_{intrinsic}$ achieves 5 dB and the $CP_{1\,dB}$ equals 1.8 dBmA.

The operating frequency of the mixer can be altered by varying the control voltage V_{T1} in order to change the values of N+/N-Well varactors C_1 and C_2. The output matching network of the mixer formed by C_3, C_{PAD}, and L_1 is designed to equal 50 Ω for the purpose of measurement.

2.2 VCO, Transformer-Based VCO Buffer/Repeater and IF Current Buffer/Repeater

The circuits of VCO and transformer-based VCO buffer/repeater are shown in Fig. 4. The designed VCO is a conventional cross-coupled negative-g_m oscillator which has attracted considerable interest because of its easy startup and good phase noise characteristics [12], [13]. The transistors $M_5 - M_7$ are biased in the saturation region where M_5 is operated as a current source and $M_6 - M_7$ are operated to provide negative transconductances of $-(g_{m6}/2)$ in order to cancel the parasitic resistances of the on-chip inductor L_2 and the N+/N-well varactors C_4 and C_5 such that the oscillation is guaranteed. The output frequency of the VCO can be altered by varying the voltage V_{T2} in order to change the values of C_4 and C_5.

The transformer-based VCO buffer/repeater is realized by a fully differential amplifier. $M_8 - M_{10}$ are biased in the saturation region. M_8 with long channel length is operated as a current source and provides the capability for common-mode rejection. The design utilizes two identical on-chip transformers, $XFMR_2$ and $XFMR_3$, in parallel and two N+/N-well varactors, C_6 and C_7, as the load. $C_8 - C_{11}$ are dc blocking capacitors. The operating frequency is altered by varying the control voltage of V_{T3}. As a result of the magnetic coupling of the transformers, four LO output currents $i_{lo+,1}$, $i_{lo-,1}$, $i_{lo+,2}$, and $i_{lo-,2}$ are provided where $i_{lo+,1} = i_{lo+,2}$ and $i_{lo-,1} = i_{lo-,2}$.

The equivalent value of inductance look at the primary turn of the $XFMR_2$ and $XFMR_3$ in parallel of the transformer-based VCO buffer/repeater has been design to be the same as the value of the inductance of the VCO. The device parameters of the N+/N-Well MOS varactors $C_4 - C_7$ are the same where the width is 1 μm, the length is 0.3 μm and the finger number is 32. The tuning voltage V_{T3} of the transformer-based VCO buffer/repeater is tracked with the V_{T2} of the VCO. Consequently, the center frequency of the narrow band transformer-based VCO buffer/repeater can be set the same as the VCO output frequency. The bandwidth of the transformer-based VCO buffer/repeater and the operation frequency of the VCO are extended by changing the resonant frequency of the LC network through varying the N+/N-Well MOS varactors $C_4 - C_7$.

Compared with generating the LO current signals $i_{lo,1}$ and $i_{lo,2}$ by active current mirrors with the technique of series inductive peaking to extend the bandwidth, the proposed circuit has the advantage of lower power consumption and smaller phase and magnitude differences between the two differential currents $i_{lo,1}$ and $i_{lo,2}$, but at the cost of moderate increase of chip area.

Shown in Fig. 5 is the IF current buffer/repeater based on current-mirror circuit. The input current signal i_{ifin+} is copied to two identical output current signals $i_{if+,1}$ and $i_{if+,2}$. $M_{11} - M_{16}$ are biased in the saturation region. Both M_{17} and M_{18} are diode-connected to provide bias voltage V_{B3} for $M_{14} - M_{16}$. C_{12} is the dc blocking capacitor. C_{13} is the bypass capacitor used to keep V_{B3} stable. Transistors $M_{11} - M_{16}$ need to be laid out carefully to minimize the number of possible mismatches.

2.3 Design of On-Chip Transformer

The on-chip transformer is realized with two planar symmetric windings where the primary winding is 1 turn and the secondary winding is also 1 turn. The metal structure and equivalent circuit diagram of the designed transformer are shown in Fig. 6. The drawing parameters of this on-chip transformer are with R = 80 μm, W = 9 μm, and S = 3 μm. The primary and secondary windings have center-tap point connections. This symmetric octagonal on-chip transformer is implemented by the top metal of Cu and the thickness is 3.35 μm. The equivalent relative permittivity ε_{eff} is 4.2. The electromagnetic tool HFSS is used to evaluate the performance and extract the characteristics of the designed on-

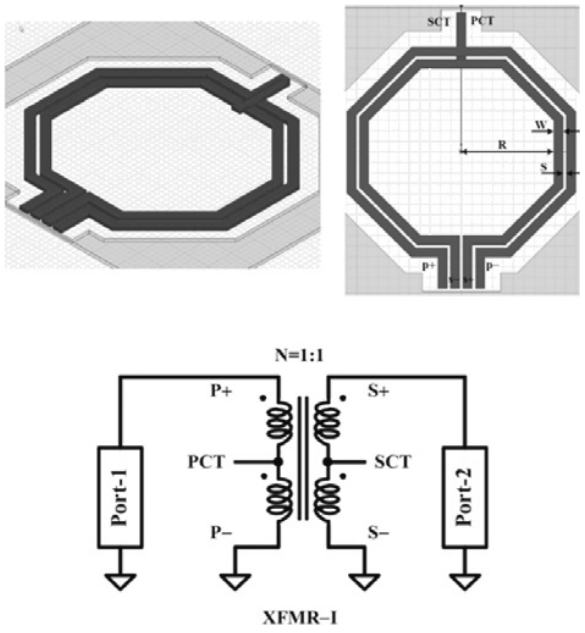


Fig. 6 The metal structures and equivalent circuit diagram of the designed on-chip transformer.

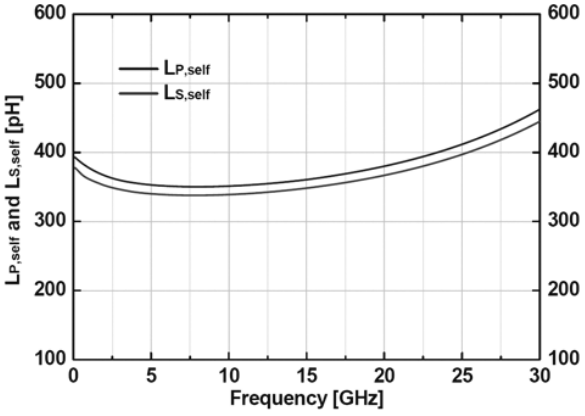


Fig. 7 The extracted self-inductance of the primary winding $L_{P,self}$ and of the secondary winding $L_{S,self}$, respectively, of the designed on-chip transformer.

chip octagonal transformers.

Figure 7 illustrates the extracted self-inductance of on-chip transformer as a function of frequency. The self-inductance can be derived from the impedance parameters by

$$L_{P,self} = \frac{\mathrm{Im}\,[Z_{11}]}{\omega} \tag{11}$$

$$L_{S,self} = \frac{\mathrm{Im}\,[Z_{22}]}{\omega} \tag{12}$$

where $L_{P,self}$ and $L_{S,self}$ presents the self-inductance of the primary and of the secondary winding, respectively. Z_{11} is the input impedance seen from the Port-1 (primary side) and the Port-2 (secondary side) is open circuit. In addition, Z_{22} is the input impedance seen from the Port-2 and the Port-1 is open circuit. Moreover, the extracted coupling-coefficient

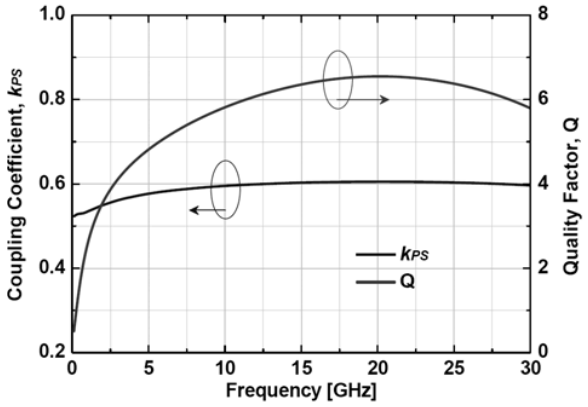


Fig. 8 The extracted coupling-coefficient k_{PS} and quality factor Q of the designed on-chip transformer as a function of frequency.

k_{PS} and the quality factor Q of the on-chip transformer as a function of frequency are also depicted in Fig. 8. The k_{PS} denotes the strength of magnetic coupling between the primary and the secondary windings, and can be expressed by the mutual inductance M and self-inductances, $L_{P,self}$ and $L_{S,self}$, of the windings as the following.

$$k_{PS} = \frac{M}{\sqrt{L_{P,self} L_{S,self}}} \tag{13}$$

The mutual inductance M is extracted from the impedance and admittance parameters as

$$M = \sqrt{\left(Y_{11}^{-1} - Z_{11}\right) \frac{Z_{22}}{\omega^2}} \tag{14}$$

where Y_{11} is the input admittance seen at the primary side when the secondary side is short circuit. From (11)–(14), it follows

$$k_{PS} = \sqrt{\frac{\left(Y_{11}^{-1} - Z_{11}\right) Z_{22}}{\mathrm{Im}\,[Z_{11}]\,\mathrm{Im}\,[Z_{22}]}}. \tag{15}$$

Note that the k_{PS} has its minimum value at the self-resonant frequency. Beyond the self-resonant frequency, k_{PS} grows over than a value of 1. However, it is not physically possible because the coupling in a passive system is limited to a maximum value of 1. In addition, such a behavior can be explained by taking (15) into consideration as the relation is validated to frequencies below resonant frequency. The quality factor of the transformer is extracted from the impedance of admittance parameters as

$$Q = \frac{\mathrm{Im}\,[Z_{11}]}{\mathrm{Re}\,[Z_{11}]} = \frac{\mathrm{Im}\left[Y_{11}^{-1}\right]}{\mathrm{Re}\left[Y_{11}^{-1}\right]}. \tag{16}$$

3. Experimental Results

The proposed *K*-band current-mode up-conversion mixer was fabricated in 0.13-μm 1P8M triple-well CMOS process. The chip photo of the proposed mixer is illustrated

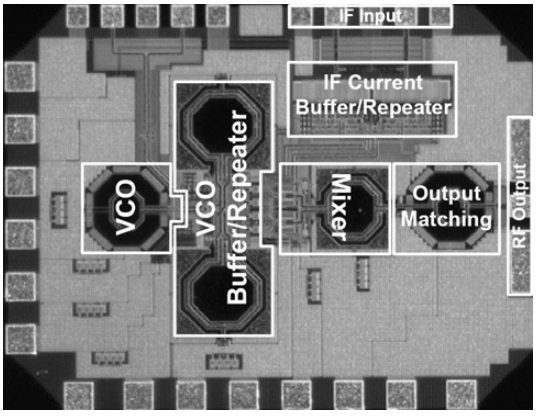


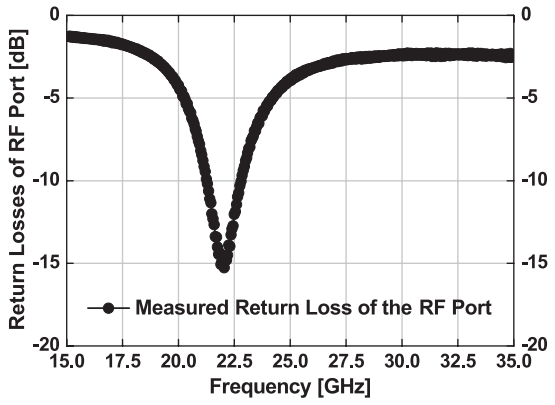
Fig. 9 Chip microphotograph of the current-mode up-conversion mixer.

in Fig. 9 The distance among each inductor and transformer is more than 100 μm in order to mitigate the magnetic coupling. Besides, large on-chip decoupling capacitors are placed between each bias/power supply and ground to reduce the occurrence of high-frequency noises and to obtain stable biases and supplies of the mixer. The chip area is 1.65 mm^2 including testing pads. However, the dimension of the proposed current-mode up-conversion mixer itself is 0.6 mm $\times$ 0.3 mm, where the area is of 0.18 mm^2.

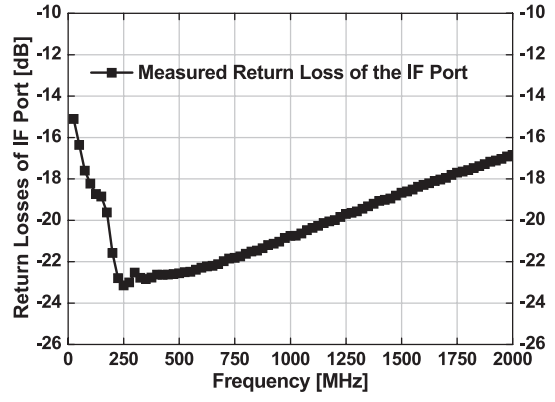
The proposed mixer was measured through on-wafer probing. The measured return losses of the RF output port and IF input port are shown in Fig. 10(a) and Fig. 10(b), respectively. The return loss of the RF port is below -10 dB within the frequency range from 21.2 GHz to 22.8 GHz. The return loss of the IF port is below -20 dB within the frequency range from 170 MHz to 1.2 GHz. Under the 1-V supply, the proposed mixer dissipates a very small amount of power of 3.1 mW. The VCO, VCO buffer/repeater, and IF current buffer/repeater circuits dissipate 2.2 mW, 3.3 mW, and 3.1 mW, respectively. As the control voltage V_{T2} is varied from 0 V to 2 V, the output frequency of the on-chip VCO can be tuned from 20.8 GHz to 22.7 GHz. As the output frequency of the on-chip VCO is increased from 20.8 GHz to 22.7 GHz, the calculated LO signal power to the mixer $P_{LO,IN}$ is from -4 dBm to -12 dBm. Furthermore, the measured phase noise is -85 dBc/Hz and -108 dBc/Hz at 1-MHz and 10-MHz frequency offset from 22.7 GHz, respectively.

The LO leakage of the proposed double-balanced mixer is around -16 dBc. The LO suppression capability is not good in this design, and it should be improved to the value of around -30 dBc. To improve the LO suppression capability, the device size of the four current-squaring circuits can be further increased to decrease the mismatch of threshold voltage due to the process variations. Moreover, symmetric layout for the differential signal paths should be carefully considered to further improve the LO suppression capability of the proposed double-balanced current-mode up-conversion mixer.

The losses from the RF cables, probes, adaptors, 180° phase shifter, and power combiner are compensated. The



(a)



(b)

Fig. 10 (a) Measured return loss of the RF output port. (b) Measured return loss of the IF input port.

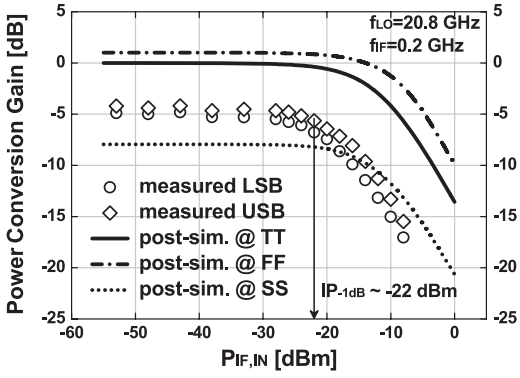


Fig. 11 Measured and post-simulated power conversion gain versus IF input power from one-tone testing result.

measured and post-simulated power conversion gains versus the IF input powers are shown in Fig. 11. In the measurement, the IF frequency is at 200 MHz, and the LO frequency is at 20.8 GHz where V_{T2} is equal to 0 V. The double-sideband RF output signals are observed at the frequencies of 21 GHz (upper sideband, USB) and 20.6 GHz (lower sideband, LSB). The measured power conversion gain is about -5 dB where the losses from on-chip transformer and output matching network are included. From the EM ex-

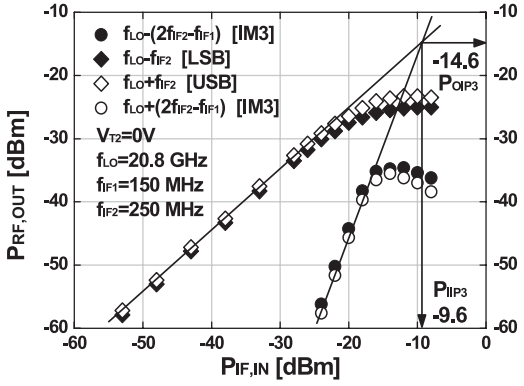


Fig. 12 Measured 3rd-order intermodulation from two-tone testing result.

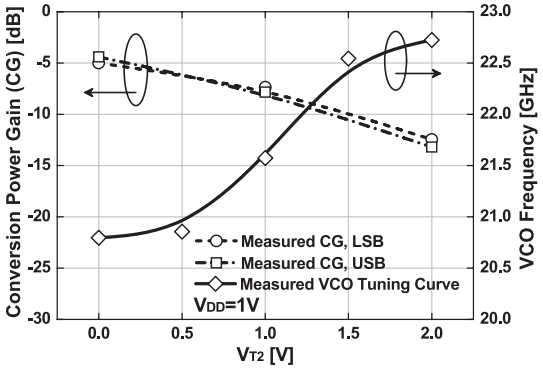


Fig. 13 Measured conversion gain versus VCO tuning frequency.

traction by HFSS, the coupling loss of the designed on-chip transformer $XFMR_1$ in Fig. 1 is about 5 dB in *K*-Band. The average single sideband (SSB) noise figure (NF) is around 12.7 dB.

The measured input 1-dB compression point ($IP_{-1\,\mathrm{dB}}$) and output 1-dB compression point ($OP_{-1\,\mathrm{dB}}$) are −22 dBm and −28 dBm, respectively. The performance of intermodulation is measured by two-tone testing. Two IF inputs with the same signal power level are at the frequencies of 150 MHz and 250 MHz. The LO frequency is also tuned to 20.8 GHz where V_{T2} is equal to 0 V. The measured results under these conditions are represented in Fig. 12. It reveals that the proposed mixer has the measured input 3rd-order intermodulation intercept point (P_{IIP3}) and output 3rd-order intermodulation intercept point (P_{OIP3}) of about −9.6 dBm and −14.6 dBm, respectively.

As the LO frequency is increased, the measured power conversion gain decreases because of the reduced output magnitude of on-chip VCO at the higher frequency and hence the reduced LO current signal. As shown in Fig. 13, the measured power conversion gain of the proposed mixer is from −5 dB to −14 dB and the calculated $P_{LO,IN}$ is reduced from −4 dBm to −12 dBm where the output frequency of on-chip VCO is tuned from 20.8 GHz to 22.7 GHz.

As shown in Fig. 11, the measured power conversion gain is about −5 dB at the LO frequency of 20.8 GHz. The measured results of the fabricated chip are close to the simulated results in the process corner SS. Due to the process variation to corner SS, the biasing current of VCO is reduced, and the g_m of M_6 and M_7 decreases. It leads to smaller equivalent negative resistances. The output magnitude of VCO is reduced, and thus small LO current signals are generated through the transformer-based VCO buffer/repeater. The measured results well agree with the simulation results in the process corner SS. Therefore, the measured results are reasonable and can support our theory and simulated results. These initial experimental results are successful to verify the concept of the proposed low-voltage and low-power *K*-band CMOS current-mode up-conversion mixer.

The performance of the proposed mixer is given in Table 1, along with comparisons with previously published CMOS current-mode up-conversion mixers [6]–[8]. As can be seen from Table 1, the proposed CMOS current-mode up-conversion mixer has the advantage of a very low power consumption of 3.1 mW from a 1-V power supply, which is much smaller than the CMOS current-mode self-switching up-conversion mixer [6] and the *K*-band CMOS voltage-mode up-conversion mixers [7], [8]. Another advantage is that the proposed mixer needs the equivalent LO signal power as small as −4 dBm to achieve the measured power conversion gain of −5 dB, which is smaller than other published CMOS voltage-mode up-conversion mixers [7], [8]. The experimental results have demonstrated that the proposed mixer is successful to perform the high-frequency mixing in low-voltage and low-power operation.

4. Conclusion

The current-mode design technique of CMOS RFICs has been developed and applied to the design of the first *K*-band CMOS current-mode up-conversion mixer. This current-mode mixer has been designed and fabricated in 0.13-μm 1P8M triple-well CMOS process. From the experimental results, we observe that the proposed current-mode up-conversion mixer has a low power consumption of 3.1 mW under the low power supply of 1 V. In addition, a small LO signal power is required. The integrated VCO provides LO frequency from 20.8 GHz to 22.7 GHz. This work presents the first *K*-band CMOS current-mode up-conversion mixer. The results demonstrate that the proposed current-mode mixer offers great potential for the application in low-voltage and low-power transmitter front-ends in advanced nano-CMOS technologies.

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Table 1 Performance comparison with previously published low-voltage low-power CMOS up-conversion mixers.

	This work			[6]	[7]	[8]
Mixer Feature	Current Mode, Current-Squaring			Current Mode, Self-switching	Voltage Mode Gilbert	Voltage Mode Dual-Gate
Technology	0.13-μm CMOS			0.25-μm CMOS	90-nm CMOS	0.13-μm CMOS
F_{RF} (GHz)	20.9 ~ 23	20.8 ~ 22.7	20.75 ~ 22.5	2	20 ~ 26	18 ~ 28
F_{LO} (GHz)	20.9 ~ 23 [a]	20.8 ~ 22.7 [a]	20.75 ~ 22.5 [a]	2.38	17.3 ~ 23.3	14 ~ 26
F_{IF} (GHz)	0.2			0.38	2.7	2.3
Supply (V)	0.9	1	1.1	1	1.2	1.2
Current (mA)	1.6	3.1	5.8	49	9.25	6.67
Power (mW)	1.54	3.1	6.4	49	11.1	8
Gain (dB)	–8 ~ –15	–5 ~ –14	–9 ~ –17	6.7	2	–2 ~ 0.7
IP_{-1dB} (dBm)	–23	–22	–20.5	-	–14.8	-
OP_{-1dB} (dBm)	–32	–28	–31	-	-	–7 ~ –5.2
P_{IIP3} (dBm)	–11	–9.6	–8	-	-	-
P_{OIP3} (dBm)	–21	–14.6	–19	6.5	-	3 ~ 5.8
Area (mm^2)	1.65 [b]			2.25	1.85	0.47
$P_{LO,IN}$ (dBm)	–7 ~ –15	–4 ~ –12	–2 ~ –9	–15	5	3

[a] This denotes the measured tuning frequency of the on-chip VCO.
[b] This denotes whole chip area. The area of mixer itself is 0.18 mm^2.

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