應變矽奈米 CMOS 元件的熱載子
可靠性研究與分析

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摘要

在最近這幾年，由於應變矽元件有較大的電子漂移率，所以被視為是高速和低功率邏輯 CMOS 有潛力的元件之一。為了能夠了解應變矽元件的優點和缺點，探討應變矽元件的可靠度分析是必須的。然而，現在並沒有太多的論文是專注於應變矽元件的可靠度分析,所以本論文的探討主要是著重在先進應變矽元件的可靠性分析。

為了研究應變矽元件的介面可靠性,我們將利用本研究群新近發展出的差頻電荷幫浦量測法，從實驗數據分析，我們首次發現了兩階的電荷幫浦電流特性，經由這種方法，我們可以分別探測到兩層的介面缺陷，包含氧化層/矽基板，與矽/矽化鍺這兩層介面。

在論文一開始，我們先討論應變矽元件的基本特性，並利用差頻電荷幫浦量測法對這個新世代元件，進行熱載子加壓之後的各種電性分析。從實驗的結果，我們發現應變矽元件有較大的熱載子衰退，並藉由和傳統的矽元件比較撞擊游離電流和等效漂移率,我們發現應變矽元件的熱載子衰退會因為元件本身較高的垂直增益和較窄的能隙而增大。因此，對於應變矽元件這種下個世代的邏輯元件，熱載子衰退的改善是非常重要的。

接著，藉由探討應變矽元件的熱載子衰退的溫度效應，我們發現雖然應變矽元件的熱載子退化在高溫時和常溫時一樣均是比普通的矽元件還大，但由於溫度對撞擊游離的影響是普通的矽元件比較大，因此應變矽的熱載子衰退在高溫時和普通的矽元件相比是較不敏感。此外，藉由熱載子加壓來探討鍺濃度和應變矽基板的深度對元件的可靠度影響，我們發現熱載子退化會隨著應變程度的增加而增加。在本論文的最後，我們利用橫向觀測方法來觀察應變矽元件的表面缺陷的分佈，其結果顯示，由於應變矽元件和傳統元件相比遭受較大的應變力，造成應變矽元件本身有較多的表面缺陷產生。藉由觀察應變矽元件的表面缺陷的分佈，可以幫助我們能夠更深入了解應變矽元件的可靠度。

Investigation of Hot Carrier Reliabilities in Strained-Silicon Nanoscale CMOS Devices

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Abstract

In more recent years, strained-Si device has been evolved as a potential candidate for high speed and low power logic CMOS technologies as a result of the mobility enhancement in devices. To explore the advantages or the shortcomings of the strained-Si devices, further understanding of the reliability is of critically important. However, little study has been paid on the reliability of these devices. Therefore, the objective of this work is focused on the reliability characterization of most advanced strained-silicon CMOS devices with sub-100um feature size.

In order to investigate the interfacial property of strained-silicon MOSFET's, an advanced charge-pumping measurement, Incremental Frequency Charge-Pumping (IFCP), is developed from our group. From the experimental data, we found a *two-level maximum*

charge-pumping current for the first time. From this two-level curve, we can separate the contribution of the generated interface traps coming from different layers underneath the gate, i.e., gate oxide/silicon and silicon/silicon germanium interfaces.

In the beginning, basic characteristics of the devices were discussed and by applying hot carrier stress, the electrical reliability of this new generation devices using IFCP method has been evaluated. From the results, we have been able to identify the enhanced hot carrier degradation in strained-Si device. According to impact ionization current and effective mobility, comparing to conventional bulk devices, we reported that the hot carrier degradation behavior was enhanced by the lateral field and band gap narrowing in strained-Si devices. Therefore, in strained-Si devices, hot carrier degradation is one of the major concerns for developing next generation logic devices.

Then, we followed by studying the temperature dependence hot carrier degradation. Although the degradation of strained-Si device is larger than that of bulk devices at the room temperature, we found that the temperature dependence hot carrier degradation for strained device is less sensitive to an increase of the temperature as a result of the influence of high temperature on the impact ionization is larger in bulk Si devices. Moreover, advanced analysis for different Ge contents and thickness of strained-Si layer is proposed. Based on the hot carrier stress, we found that the denser Ge content and deeper thickness strained Si layer induce much more degradations for the devices. Finally, we used the lateral profiling method to plot the distribution of interface traps in strained-Si devices and found a larger generated N_{it} since strained-Si device exhibits a much larger strain. The interface traps distribution provides us important information for the understanding of the device reliabilities of strained-Si devices.

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