Chapter 1
Introduction

1.1 The Motivation of This Work

Scaling has been the primary means of the performance improvement of CMOS devices in the last 30 years. However, device scaling faces many challenges which make the difficulty in maintaining the trend of device performance improvement. Adjusting Carrier mobility might be a factor offering further dramatic advances of CMOS devices. In order to realize high-speed scaled CMOS devices for logic applications, it is very important to increase the carrier mobility, especially for gate length down to 65Å and below. From this viewpoint, a number of groups have shown that short channel NMOS devices incorporating thin strained-Si surface channels have been a potential candidate for high speed and low logic CMOS technologies [1]. Consequently, it is found that silicon under biaxial tensile strain features enhanced electron mobility can achieve significant driving current enhancement.

In order to effectively investigate the advantages of the Si/SiGe heterostructure and to establish a good device design methodology, it is necessary to clarify the relationship between device characteristics and the introduced Si/SiGe heterostructure. For this reason, we perform the charge pumping measurement and provide the method to analyze it for the strained-Si devices. Furthermore, the hot carrier measurement including temperature dependence of the strained-Si device is important for us to understand the reliability and to learn about the device degradation mechanism. Besides, in order to investigate the influence of Ge concentrations and thickness of strained-Si layer, improved charge pumping measurement has been employed. Finally, we use lateral profiling method to clarify the interface trap distribution between the

strained-Si/SiGe interface and gate oxide/strained-Si interface. The knowledge of interface trap distribution can help us to further understand the reliability problems of strained-Si devices.

1.2 Organization of This Thesis

This thesis is divided into five chapters. Chapter 2 describes the experiment setup and the analysis method used in this study. In Chapter 3, we will introduce the strained-Si device technology. Then we will discuss interface state analysis and its correlation to the hot carrier reliabilities of stained-Si devices. In Chapter 4, we will study the temperature dependence of reliability studies, influence of Ge concentrations and thickness of Si layer, and the interface trap distribution for stained-Si devices. Finally, a summary and conclusion will be given in Chapter 5.

Chapter 2
Experimental Measurement Setup and Basic Theory

2.1 Introduction

The strained-silicon device is an effective approach for improving carrier mobility for high speed and low power logic CMOS device applications. To analyze the structure technology and reliability property of strained-Si device in the following chapters, we need to perform several kinds of experimental measurement. In this chapter, we will describe the measurement setup and basic theory of the measurement methods we used for the strained-Si devices.

This chapter is divided into several sections. At first, we will illustrate the fundamental experimental setup for characterizing the strained-Si devices. Then, two different kinds of experimental analysis methods used in this thesis will be introduced, including the charge pumping method and gated diode method. We will show their experimental setup, fundamental theory, improved method, and their application to probe the interface quality of the device are introduced. Furthermore, to observe the NBTI effect of the strained-Si device, some measurements need high temperature setup of the equipment.

2.2 Experimental Setup

The experimental setup for the I-V measurement of MOSFET's is illustrated in Fig. 2.1. Based on the PC controlled instrument environment, the complicated and long-term characterization procedures for analyzing the intrinsic and degradation behavior in MOSFET's can be easily achieved. As shown in Figure 2.1, the

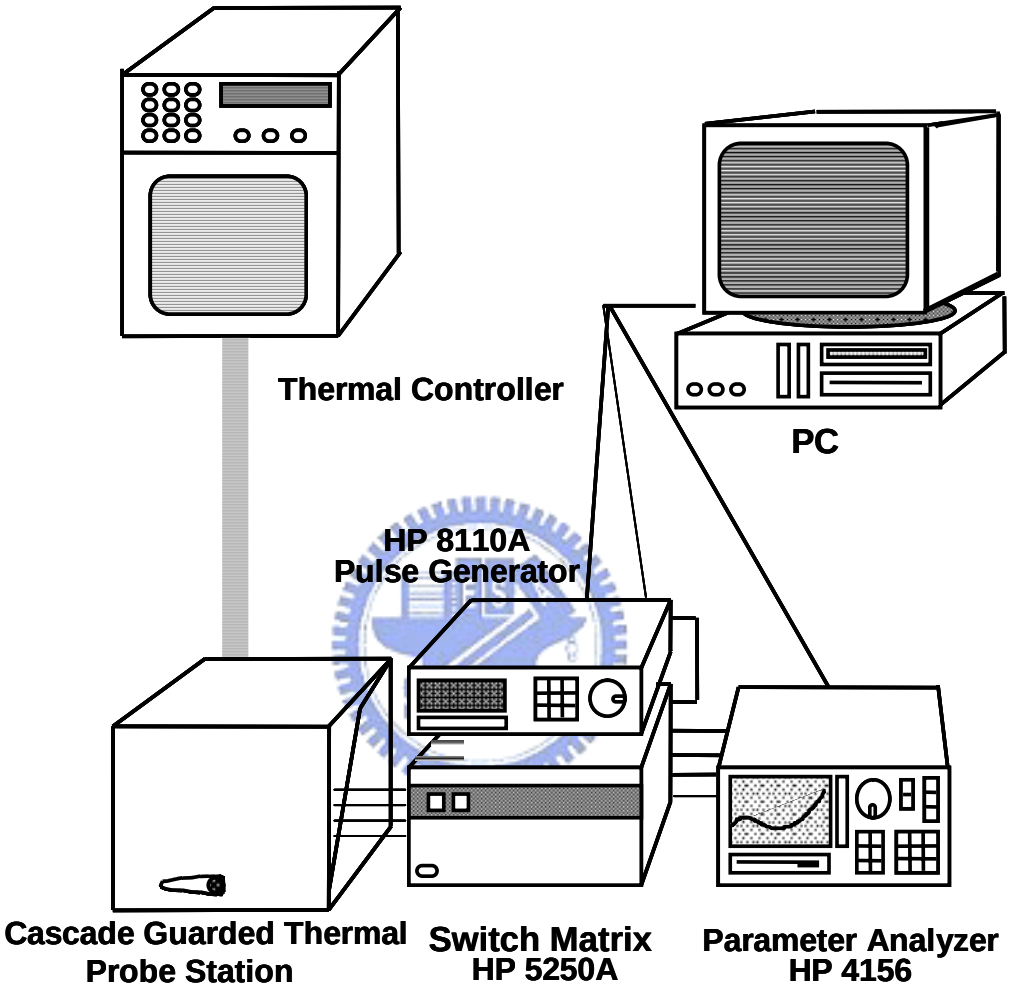


Fig. 2.1 The experimental setup and environment for basic I-V measurement of MOSFET's.

characterization equipment, including semiconductor parameter analyzer (HP4156C), dual channel pulse generator (HP8110A), low leakage switch mainframe (HP E5250A), cascade guarded thermal probe station and thermal controller, provides an adequate capability for measuring the device I-V characteristics. Besides, the PC program used to control all the measurement process is VEE and HT-basic.

2.3 Charge Pumping Measurement

2.3.1 Basic Experimental Setup

The basic setup of charge pumping measurement is shown in Fig. 2.2. The source, drain and bulk electrodes of tested devices are grounded. A 1MHz (the frequency can be modulated for different devices) square pulse waveform provided by HP8110A with fixed base level (V_{gl}) is applied to the NMOS gate, or with fixed top level (V_{gh}) is applied to the PMOS gate. We keep V_{gl} at –1.0V while increase V_{gh} from –1.0V to 1.0V by step 0.1V, or keep V_{gh} at 1.0V while decrease V_{gl} from 1.0V to –1.0V by step –0.1V. With a smaller voltage step, we get a higher profiling resolution. The parameter analyzer HP4156C is used to measure the charge pumping current (I_{CP}).

2.3.2 Basic Theory

The charging pumping principle for MOSFET's has been applied to characterize the fast interface traps in MOSFET's. The original charge pumping method was introduced by Brugler and Jespers, and the technique was developed by Heremans [2]. This technique is based on a recombination process at the Si/SiO_2 interface involving the surface traps. It consists of applying a constant reverse bias at the source and

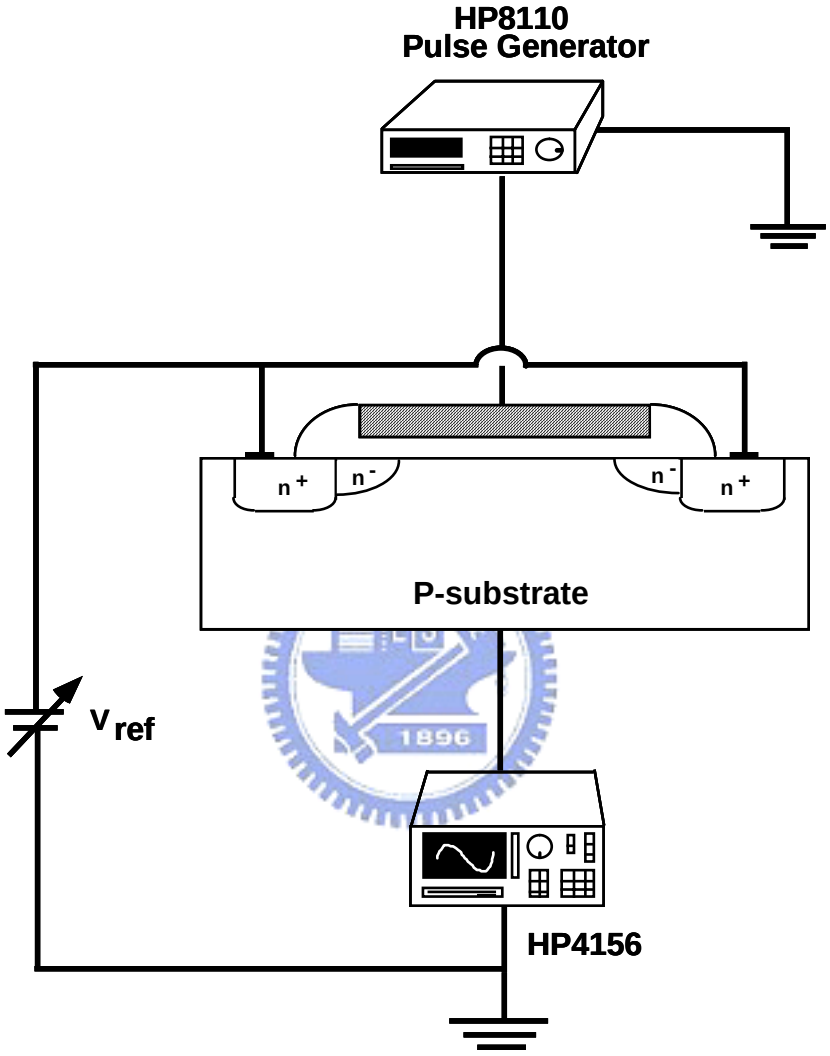


Fig. 2.2 The experimental setup of charge pumping method.

drain, while sweeping the base level of the gate pulse train from a low accumulation level to a high inversion level. The frequency and the rise/fall time are kept constant. When the base level is lower than that flat-band voltage while the top level of the pulse is higher than the threshold voltage, the maximum charge pumping current occurs. This means that a net amount of charge is transferred from the source and drain to the substrate via the fast interface traps each time the device is pulsed from inversion toward accumulation. The charge pumping current is caused by the repetitive recombination at interface traps. As a result, the recombination current measured from the bottom (substrate) is the so-called charge pumping current [3]. The CP current can be given by:

$$I_{CP} = q \cdot f \cdot W \cdot L \cdot N_{IT}. \tag{2.1}$$

According to this equation, the current is directly proportional to the interface trap density in the channel, the frequency, and the area of the device. However, when the top level of the pulse is lower than the flat-band voltage or the base level is higher than the threshold voltage, the fast interface traps are permanently filled with holes in accumulation or the electrons in inversion in n-MOSFET's, which no holes reach the surface at the time, respectively. As a result, there is no recombination current and then the charge pumping current cannot be discovered.

Charge pumping measurements can be performed with several different ways. For our experimental requirement, we perform the charge pumping measurement by applying a gate pulse with the fixed base voltage (V_{gl}) and increasing the pulse amplitude. While the channel operates between accumulation and inversion as the fixed base voltage lower than flat-band voltage and high voltage above the threshold voltage respectively; this gives rise to the charge pumping current (I_{CP}) from the bulk

and reaches saturation situation. If we use another method which changes base voltage with fixed pulse amplitude, the current saturation region is not extensive enough for research because of the limit that the saturation current happens only when the gate pulse train from a low accumulation level to a high inversion level.

2.3.3 Principle of the Low Leakage IFCP Method

Figures 2.3 (a) and (b) show the schematic of a low leakage IFCP measurement for CMOS developed by our group in [4]. With both S/D grounded and by applying a gate pulse with a fixed base level (V_{gl}) and a varying high-level voltage (V_{gh}) for NMOS, the channel will be switched between the accumulation and inversion. This gives rise to the charge pumping current I_{CP} ($=I_B$) measured from the bulk. From Fig. 2.3, when t_{ox} >30Å, the leakage current I_G of I_{CP} is very small. However, when t_{ox} is slow down than 20Å, the leakage current I_G is unavoidable. The unexpected leakage current will influence our research. From the measured I_{CP} at two frequencies, f_1 and f_2, can be expressed as

$$I_{CP,\ f1\ \text{with-leakage}} = I_{CP,\ f1\ \text{correct}} + I_{CP,\ \underline{\text{leakage@}f1}} \quad (2.1)$$

and

$$I_{CP,\ f2\ \text{with-leakage}} = I_{CP,\ f2\ \text{correct}} + I_{CP,\ \underline{\text{leakage@}f2}}. \quad (2.2)$$

When the frequency is sufficiently high, the leakage components in these two frequencies are almost the same ($I_{CP,\ \text{leakage@}f1} \approx I_{CP,\ \underline{\text{leakage@}f2}}$). We then take the difference of I_{CP} ($\Delta I_{CP,\ f1-f2}$) between two frequencies. From equations (2.1) and (2.2), the difference of these two CP curves gives

$$\Delta I_{CP,\ f1-f2} = I_{CP,\ f1\ \text{with-leakage}} - I_{CP,\ f2\ \text{with-leakage}}. \quad (2.3)$$

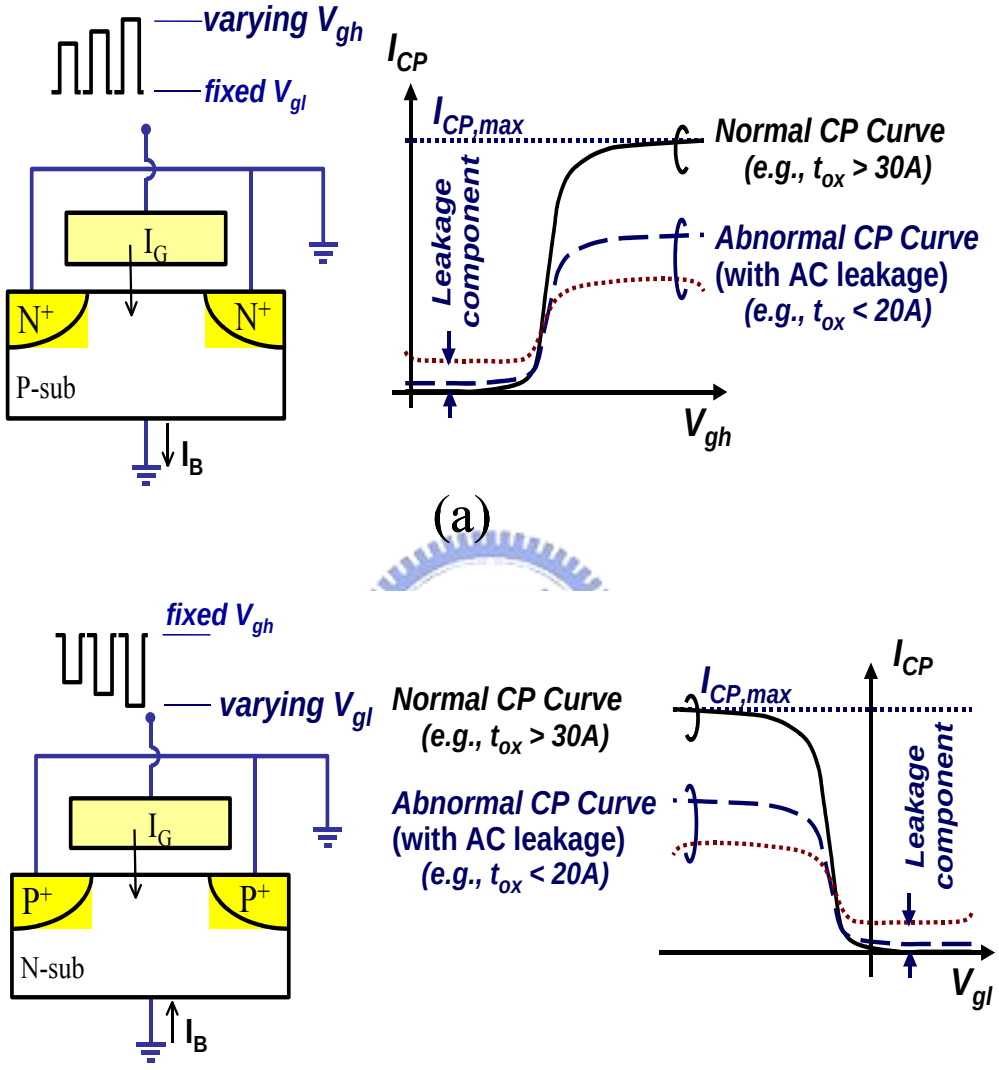


Fig. 2.3 The schematic of charge pumping (CP) for
(a) nMOSFET measurement.
(b) pMOSFET measurement.
Induced leakage current(I_G) occurs when tox< 20A.

Since the correct CP curve is directly proportional to the frequency, it will be equal to the difference of two CP curves. Therefore, in the IFCP method, the correct CP curve at frequency ($f1$- $f2$) can be given by

$$I_{CP,\ f1-f2} = \Delta I_{CP,\ f1-f2}. \tag{2.4}$$

For example, $I_{CP(2MHz)} - I_{CP(1MHz)}$ is regarded as the I_{CP} at their difference frequency, 1MHz. The result of the charge pumping measurement for the strained-Si device is shown in Fig. 2.4 curve (1) and curves (2). From this figure, we can find a huge gate leakage current appears in the charge pumping cure when the voltage of gate pulse is higher than 1V. Because the correct charge pumping current is directly proportional to the frequency of gate pulse and the leakage of current is irrelevant to the frequency, so we can receive the correct charge pumping current by taking the difference of the measured I_{CP} between two frequencies theoretically. To see the result, we finally get a correct curve with commonly known saturation charge pumping current, curve (3), in Fig. 2.4.

2.3.4 Extraction of the Effective Channel Length

Figure 2.5 shows the non-uniform interface trap distribution for the extraction of effective channel length. Using two different channel lengths, the interface traps can be represented by

$$N_{it,\ 1,\ total} = N_{it,\ 11}(\text{edge}) + N_{it,\ 12}(\text{center}) \tag{2.5}$$

and

$$N_{it,\ 2,\ total} = N_{it,\ 21}(\text{edge}) + N_{it,\ 22}(\text{center}). \tag{2.6}$$

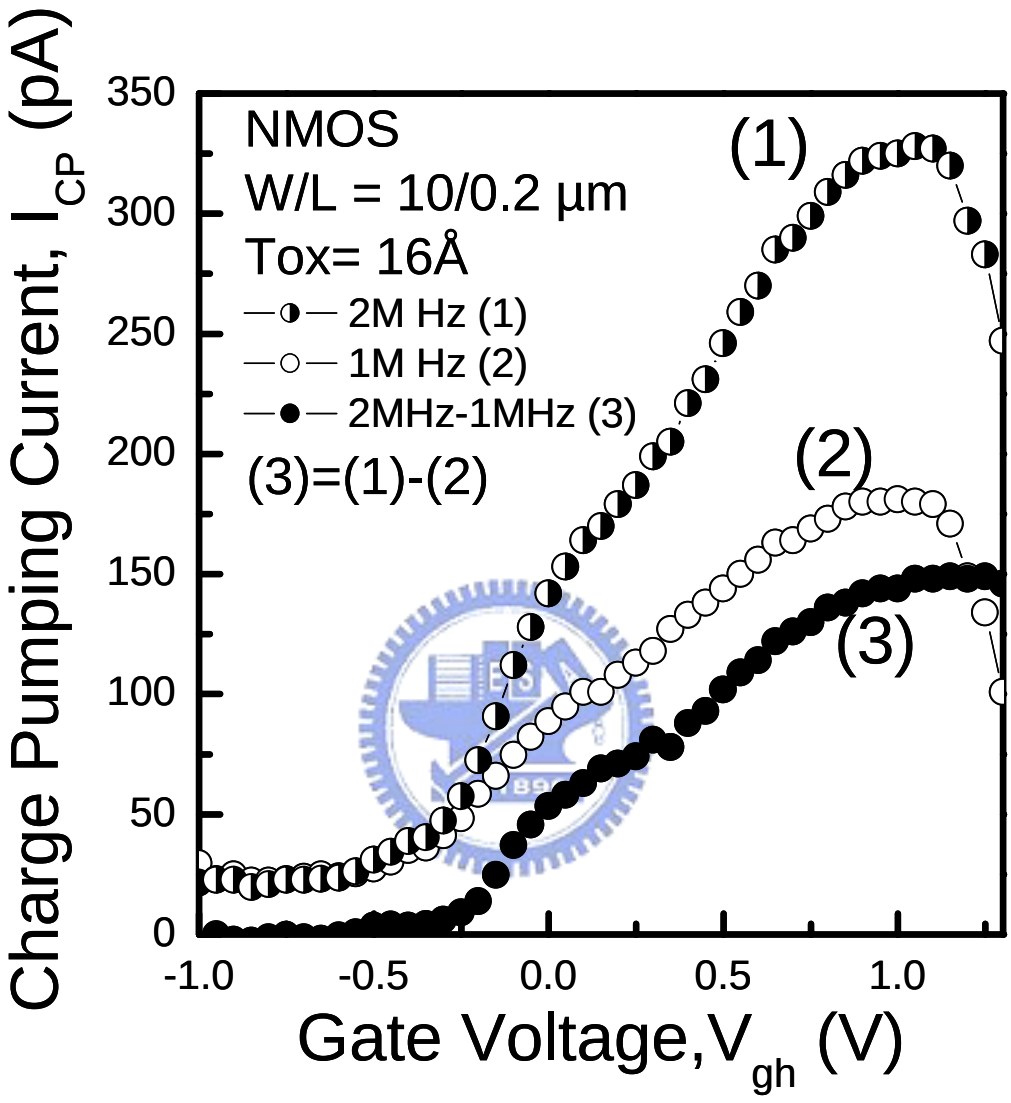


Fig. 2.4 Measurement of I_{CP} at two different frequencies. The low leakage IFCP method is achieved by subtracting their respective I_{CP}'s at two successive frequencies.

Since the mechanical stress in the edge region is more critical than the center region, the interface traps in the edge is larger than that in the center region and the mechanical stress in two different channel devices are almost the same, $N_{it,\ 11}$ is approximately equal to $N_{it,\ 21}$. To eliminate the traps generated at the edge region, the difference of these two interface traps can be used, which is directly proportional to the ΔL. Hence, we have

$$\Delta I_{CP,\ max} \propto \Delta N_{it,\ total} = N_{it,\ 1,\ total} - N_{it,\ 2,\ total} = N_{it,\ 12} - N_{it,\ 22} \propto \Delta L. \quad (2.7)$$

Figure 2.5 (a) shows the definitions of ΔL_1, ΔL_2, and ΔL_0, which can be expressed as

$$\Delta L_1 = L_{MASK} - L_{gate},$$

$$\Delta L_2 = L_{gate} - L_{eff},$$

and

$$\Delta L_0 = L_{MASK} - L_{eff} = \Delta L_1 + \Delta L_2. \quad (2.8)$$

Figures 2.6 (a) and (b) show the calculated interface traps, N_{it}, per unit width and offset length, $\Delta L_0 = L_{MASK} - L_{eff}$, from the measured 20 devices with nMOSFET and pMOSFET in this work.

2.4 Gated Diode Measurement

2.4.1 Basic Experimental Setup

The basic setup of gated diode measurement is shown as the following. The source of the device is floating, while the substrate is grounded. The gate voltage V_g was varied from weak inversion to accumulation region of the device and the drain is applied with small bias to keep the junction of drain and substrate with little forward.

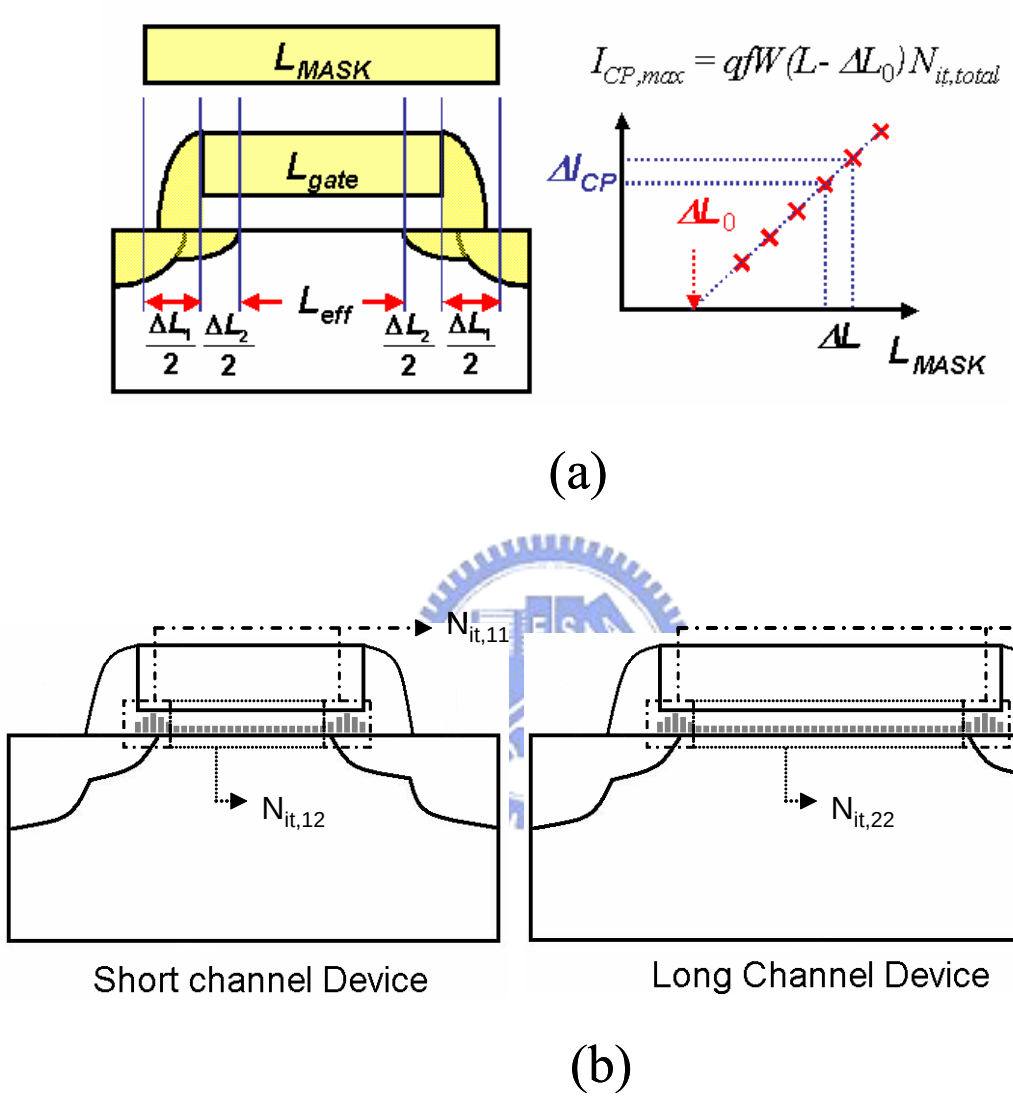


Fig. 2.5 Illustration of ΔL_0 extraction from CP data.
(a) Parameter definition and extraction method.
(b) Interface traps distribution is short and long channel length devices.

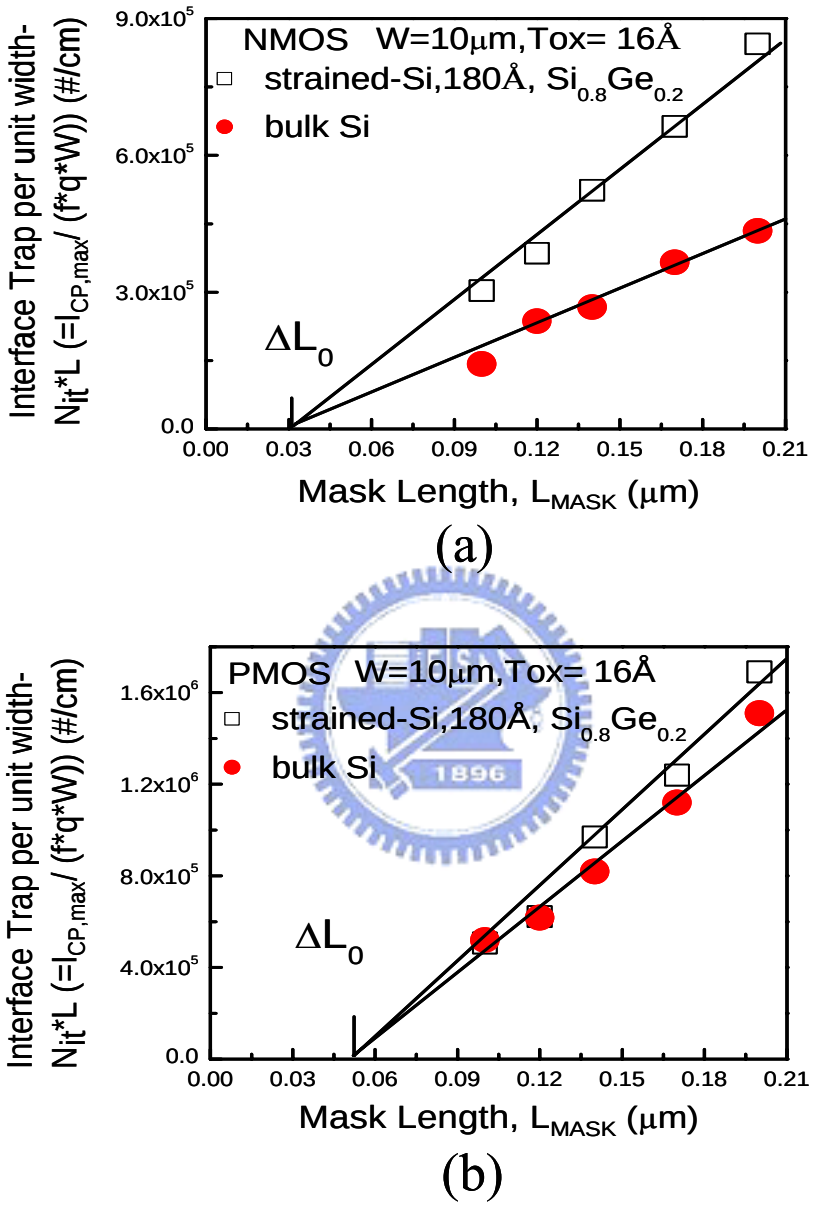


Fig. 2.6 Calculated (a) $\Delta L_0 \approx 0.03\mu m$ for nMOSFET, (b) $\Delta L_0 \approx 0.05\mu m$ for pMOSFET in this work.

Moreover, the variation of the drain current with gate voltage will be recorded. The HP4156C semiconductor parameter analyzer is used to measure the gated diode current.

2.4.2 Basic Theory

The gated-diode measurement was first introduced as a means of detecting interfacial deep-level defects in MOS structures. In order to monitor the increased surface-state density and generated fixed oxide charge after hot-carrier degradation, Giebel and Goser in [5] introduced this technique recently. The gated-diode principle is illustrated in Fig. 2.7. To monitor the interface-state defects and oxide damages near the drain side of the device after stress, the gated-diode measurement applies a small positive voltage V_D (p-MOSFET's) to the drain to forward-bias the drain-substrate junction and measures the drain current as a function of the gate voltage V_G. Assuming a broad and uniform energy distribution of the defect states around the intrinsic level E_i, the active interface centers are physically located in the narrow band between Φ_e and Φ_h (pointer in Fig. 2.7). The lines define respectively the position where the quasi-Fermi levels for electrons Φ_e and holes Φ_h coincide with the intrinsic level E_i. When the gate voltage V_G is swept from inversion region, through depletion into increasingly strong accumulation, the effective zone (Δx) moves like a pointer of decreasing width along the interface toward the drain side. The area of contact with the interface changes with V_G rises from 0V to –2V or even more. Finally, it separates completely from the interface.

According to the Shockley-Read-Hall (SRH) theory [6] and by assuming that the defect capture cross section for electrons is the same as that for holes (i.e., $\sigma_n=\sigma_p=\sigma$), the surface component of gated-diode current (I_{GD}) is mainly determined by

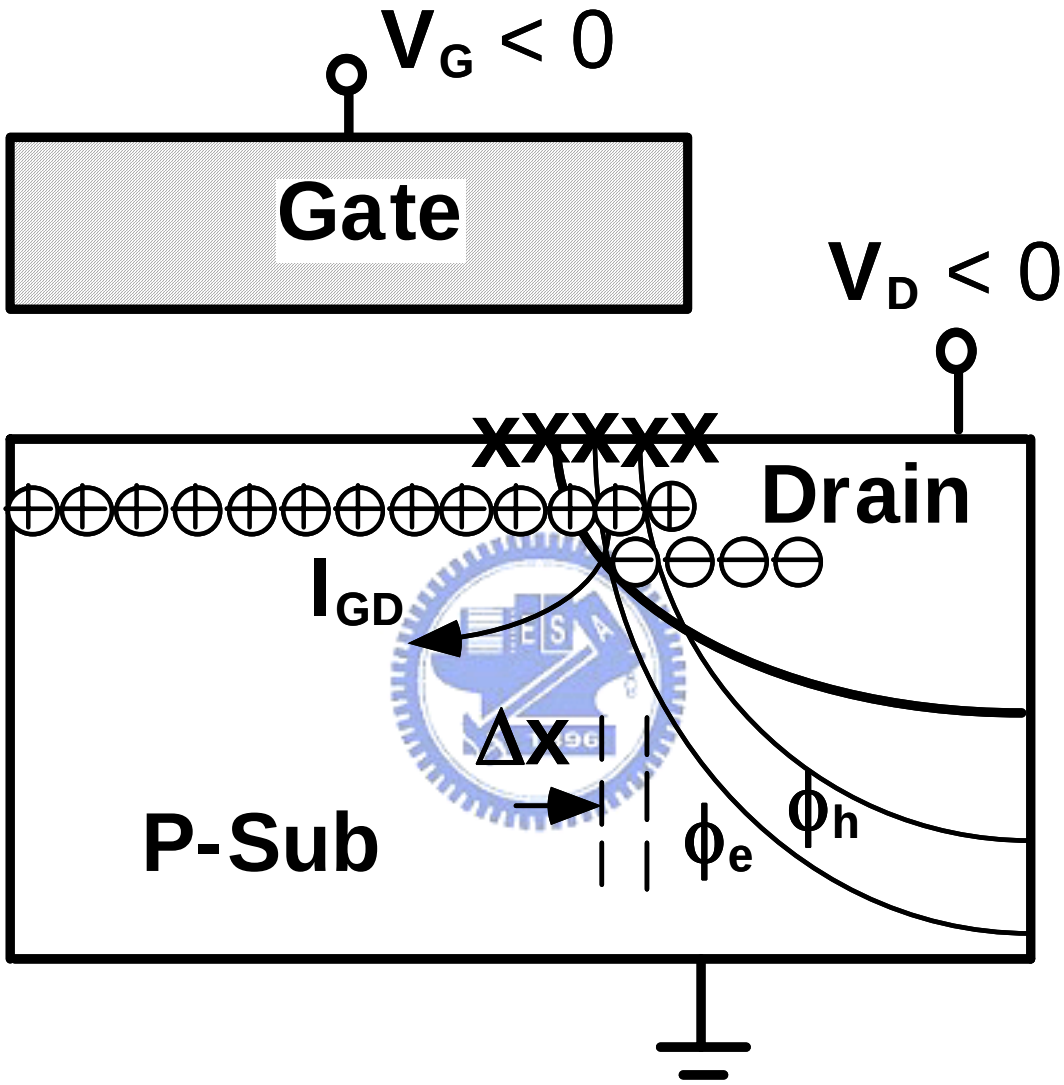


Fig. 2.7 Demonstration of the gated-diode measurement.

the recombination in the region where the electron and hole concentrations are nearly equal, that is, the surface potential is close to the midgap. For the device in the inversion region, the electron concentration is higher than the hole concentration at the interface so that interface traps do not contribute to the I_{GD} current, the measured current is due to the recombination and diffusion in the p-n junction. When the channel is in the accumulation, the condition n= p is only satisfied in the gate-drain overlap region. Only traps in the narrow band between Φ_e and Φ_h (Δx as shown in Fig. 2.7) contribute to the recombination current. By increasing V_g, Δx moves toward the drain region. From the difference of measured I_{GD} (V_G) between fresh and stressed devices, the spatial distribution of N_{it} can be determined. The excess recombination current I_{GD} after the stress can be expressed as in [7].

2.4.3 Principle of the Improved Gate-Diode Method

As gate oxide thickness reduces, previous gated-diode method cannot work well for very thin gate oxide device. The three-peak experimental result of the previous gate diode current cannot be obtained because of the limit by the tunneling leakage through the gate oxide during the measurement since direct tunneling exists. An improved novel L^2-GD method by our group in [8] which gives a larger drain forward bias to increase the forward current of the p-n junction between the drain and substrate raises the original gated-diode current to avoid the limit from the gate tunneling leakage. Based on a new characterization strategy, this newly proposed gated-diode method will still be valid down to the ultra-thin gate oxide regime, even though the direct tunneling leakage exists and couples with the measured current.

2.5 Summary

In this chapter, we described the experimental setups and the basic theory of the measurement methods. In later chapters, we will use these experimental techniques to study the reliabilities of the strained-Si device. By using the basic I-V measurement, charge pumping method, and the gated diode method, the characteristics of reliability and stress degradations in the strained-Si device can be monitored and analyzed. Finally, we use lateral profiling technology to monitor the interface state distribution of the SiGe/Si heterostructure devices.

Chapter 3
Analysis of HC Degradation in Strained-Silicon MOSFET's by Charge Pumping Method

3.1 Introduction

With the scaling of the device size, performance improvement of CMOS devices faces a number of obstacles. Mobility enhancement technology is one way to offer dramatic advances of CMOS devices. In order to realize high-speed scaled CMOS devices, it is necessary to increase the carrier mobility for device gate length down to the sub-100-nm and below. Recently, a number of groups have shown that short channel NMOS devices incorporating thin strained-Si surface channels can achieve significant drive current enhancement. It is necessary to study the influence about device characteristics of the introduced SiGe/Si heterostructure for the strained-Si device application and design methodology. In this chapter, the basic characteristic of device and the reliability have been studied by the charge pumping measurement.

Hot carrier degradation of MOSFET's is an important reliability issue in deep-submicron technology [9]. Strained-Si device is a promising candidate for enhancement of CMOS performance. However, little research has been done on its reliability issues. To exploit the advantage or the shortcoming of the strained-Si device and investigate the reliability issue of the device, in later discussion, we use hot carrier measurement to study that. We will use the improved charge pumping method to exactly analyze the interface state situation after hot carrier degradation of strained-Si device and try to explain the mechanism of the degradation of the device by way of the extent of the mobility enhancement and impact ionization.

3.2 Device Technology

3.2.1 Device Preparation

The schematic cross section of the strained-Si nMOSFET's used in this chapter is shown in Fig. 3.1. The devices were fabricated on bulk Si substrates and relaxed SiGe virtual substrates with a tensile strained Si cap layer. The V_T shift due to enhanced arsenic diffusion in the SiGe buffer was controlled by a modified halo implant and an optimized dopant anneal process. A nickel silicide process was adopted to avoid the problem of Ge segregation during silicide formation on SiGe. These test devices were made with the same physical thickness (16Å) of nitrided gate oxide and with different channel lengths. The relaxed Si_{1-x}/Ge_x has different ratio x=20% and 30%and with Si cap layer thickness 100Å or 180Å. Both technologies used the same processes except for the channel engineering to match the V_T shift.

3.2.2 Strained-Si Device Physics

Due to the lattice mismatch as shown in Fig. 3.2(a), a pseudo-morphic layer of Si on relaxed SiGe is under biaxial tensile strain, which modifies the band structure and enhances carrier transport [10]. It was found that silicon under biaxial tensile strain features splits the six-fold degenerate conduction band minimum into a two-fold (△2) and a four-fold (△4) degenerate band in Fig 3.2(b). Since electrons preferentially popular the △2 band, which is lower in energy, the increase in energy splitting reflects the reduction in the inter-valley phonon scattering and lower in-plane electron effective mass [11]. Figure 3.3 shows an expression introducing comparison about electron effective mass with strained-Si device and bulk device. The effective mass can be determined from Fowler-Nordheim tunneling current formula, which is

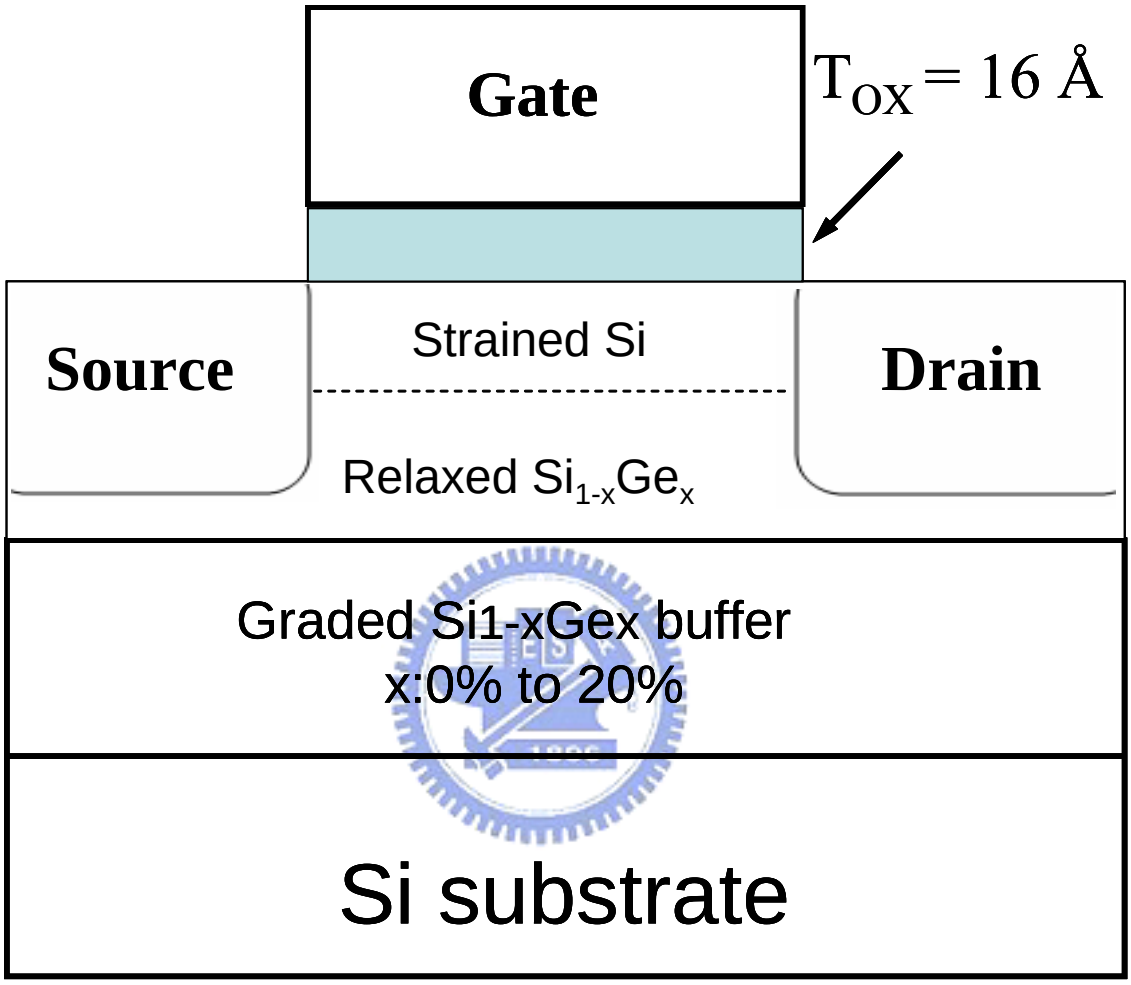


Fig. 3.1 Schematic cross section of strained devices with SiGe channel.

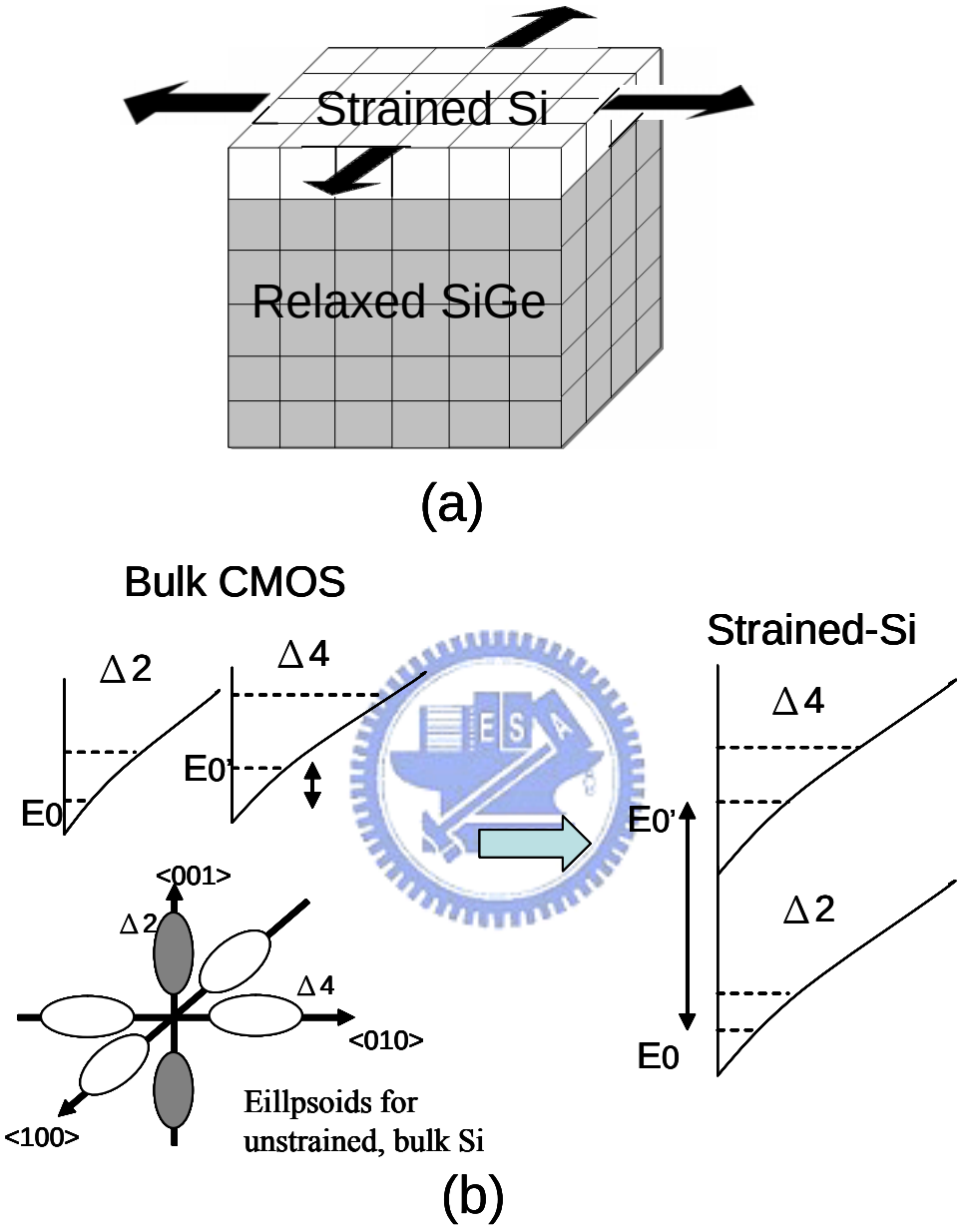


Fig. 3.2 (a) Pseudomorphic, strained-Si on relaxed SiGe (b) Energy splitting between the Δ_2 (2-fold degenerate) and Δ_4 (4-fold degenerate) conduction bands for strained-Si device and bulk device.

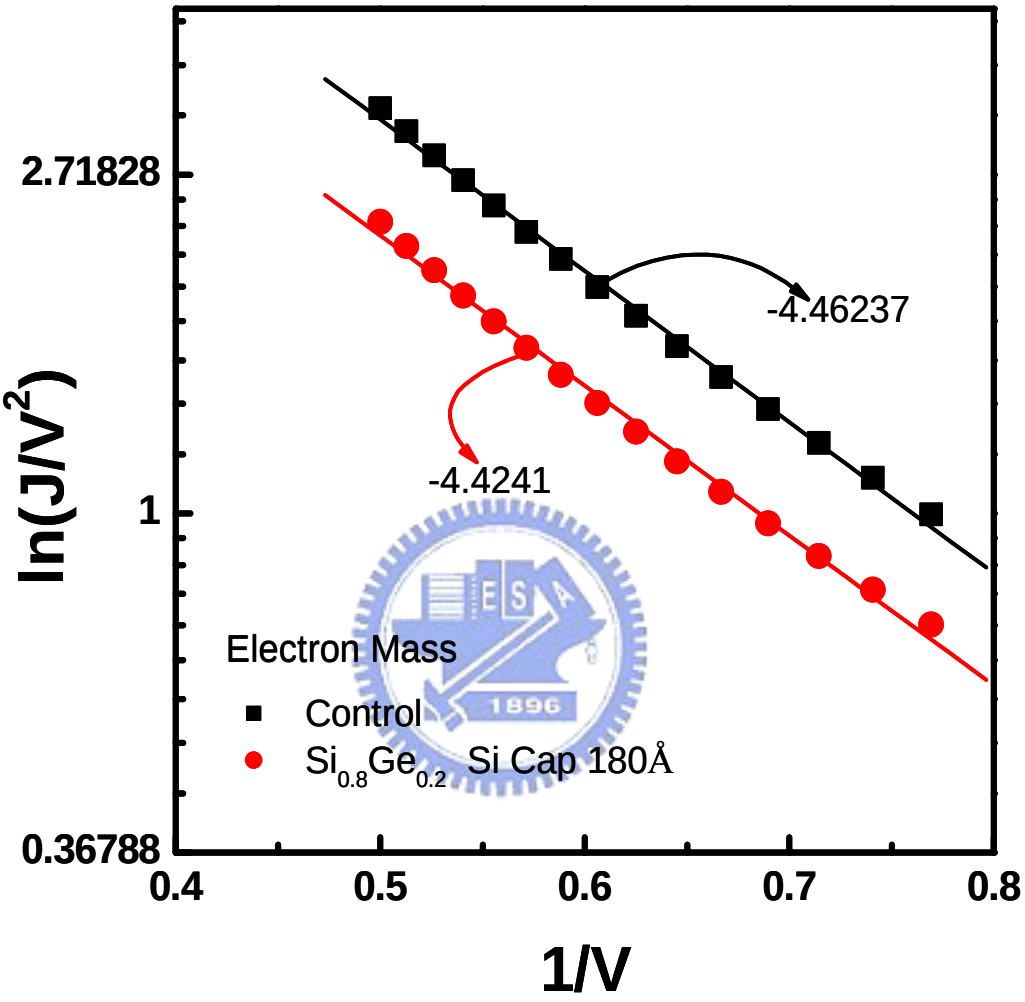


Fig. 3.3. The comparison of electron effective mass in strained-Si device and bulk devices.

expressed as:

$$J = E^2 \exp\left[\frac{-4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E}\right] \sim V^2 \exp\left(-\frac{b}{V}\right). \quad (3.1)$$

For the formula, the effective mass is directly proportional to the slope of the figure. From the figure, we can find that the effective mass with strained-Si device is smaller than that with bulk device. Therefore, the silicon under biaxial tensile strain features can enhance electron mobility.

3.3 Results and Discussion

3.3.1 Analysis with the Improved Charge Pumping Method

The strained-silicon device has the SiGe/Si heterostructure with several kinds of layers. In order to fully analyze the structure of the device, we make use of the charge pumping method, which is presented in the experimental setup paragraph in Chapter 2 previously. Using common charge pumping method, we can find a huge gate leakage current appear in the charge pumping cure when the voltage of gate pulse is higher. For achieving good charge pumping curve to observe the interface characteristics, we can use the *incremental frequency charge pumping method*, which is described in Chapter 2. The result is shown in Fig. 3.4.

By employing the *incremental frequency charge pumping method*, the two-level saturation charge pumping current of the n-type strained-Si device has been observed as shown in Fig. 3.4(a). The saturation level of charge pumping current is reached when the high voltage of gate pulse is higher than threshold voltage of the device. From our results of the measurement, we think that the two-level charge pumping

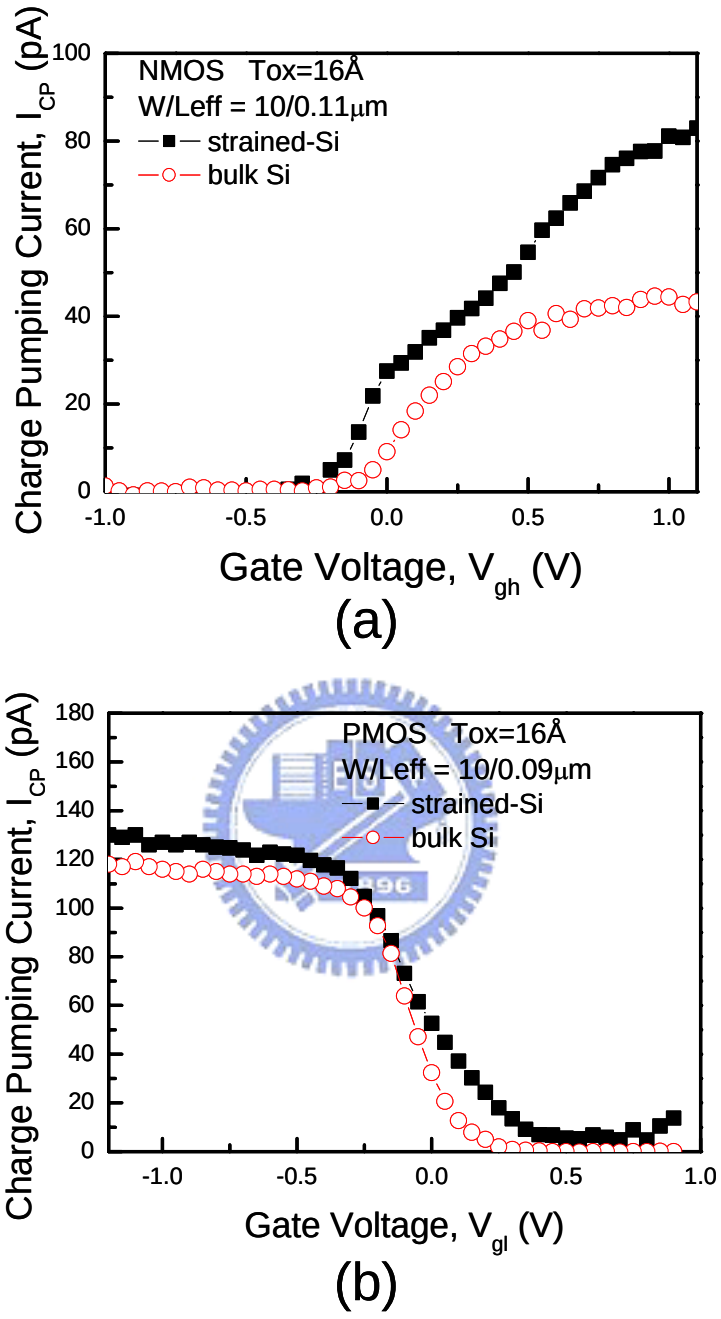


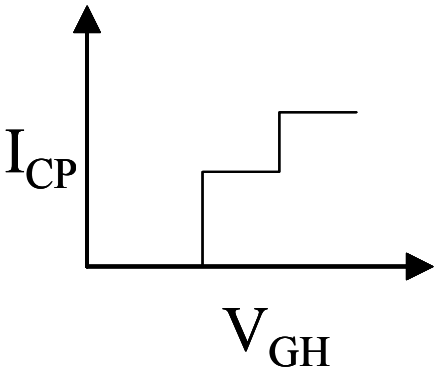
Fig. 3.4 The comparison of charge pumping currents in strained-Si and bulk Si devices, including (a)n- and (b) p-types.

current is contributed to the SiGe/Si heterostructure. We believe that the second saturation level is contributed to the SiGe/Si interface, in which the threshold voltage is higher than that of the Si/Gate-oxide interface almost at 1V. The combination mechanism of two saturation charge pumping currents is illustrated in Fig.3.5. The phenomenon that the recombination of the SiGe/Si hetero-interface needs higher voltage of gate pulse is explained in two ways, which are described as below:

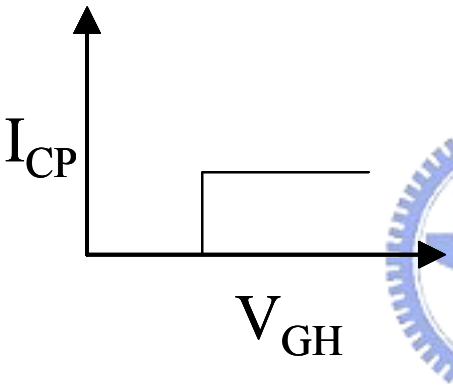
(1) The conduction band and the valence band of SiGe are higher than those of Si [12]. The energy band structure needs higher gate voltage to complete the charge recombination at the interface.
(2) In our test devices, the position of SiGe layer is around 180Å deeper than channel surface. In order to keep the interface layer in inversion state, the gate voltage must be high, too.

Furthermore, we take advantage of the energy band diagram to explain the higher corresponding gate voltage for saturation of charge pumping current in SiGe/Si hetero-interface, as shown in Fig. 3.6, where the dotted line and solid line signify the band diagram at $V_G = 0V$ and $V_G = V_T$.

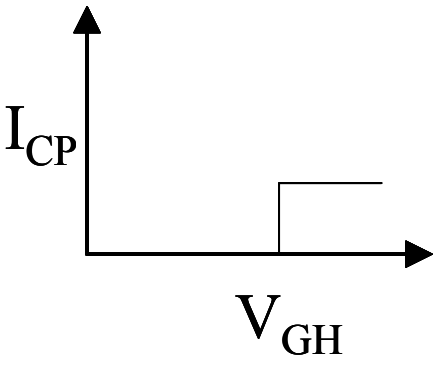
Comparing to n-MOSFET's, the charge pumping current of p-MOSFET's is shown in Figure 3.4(b). In this figure, we find that the second saturation effect of the charge pumping current is not obvious. We explain the situation according to the energy band diagram of p-MOSFET's strained-Si device shown as Fig. 3.7. As reveals in the firgue, we find a situation that there is a little difference between the conduction bands level of SiGe and that of Si, and the valence band level has the same condition. The discontinuity in the valence band confines the holes and forms a parasitic buried channel [13]. The mobility in this SiGe channel is expected to be low, and the



The measured CP curve can be separated to two parts.



The first CP curve contributes to the recombination at Si/SiO_2 interface.



The second CP curve contributes to the recombination at SiGe/Si interface.

Fig. 3.5 Illustration of two level CP curve in the strained-Si n-MOSFET's.

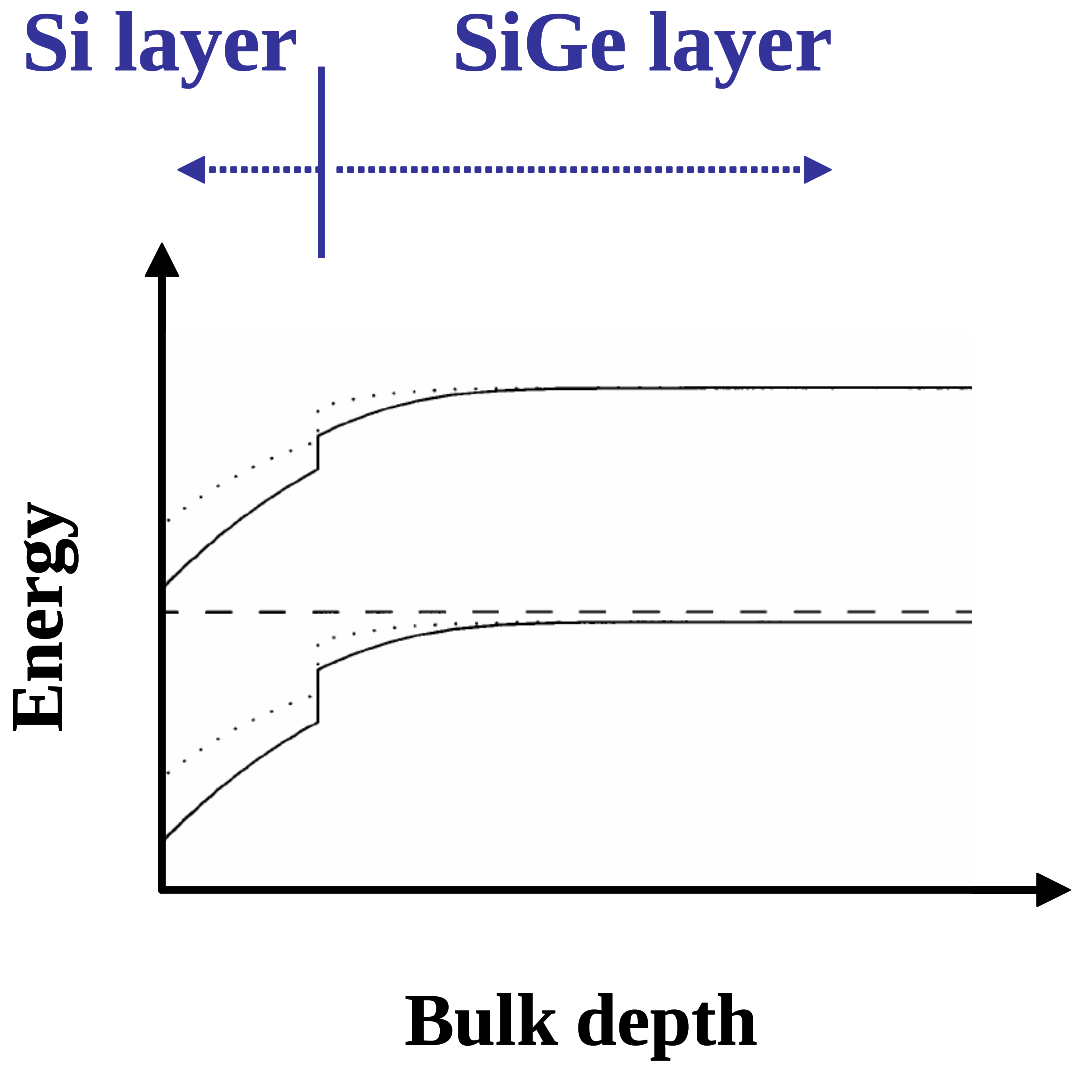


Fig. 3.6 The predicted energy band diagram in the strained Si n-MOSFET's as a function of bulk depth. The dotted and solid lines show curves at V_G =0V and $V_G = V_T$.

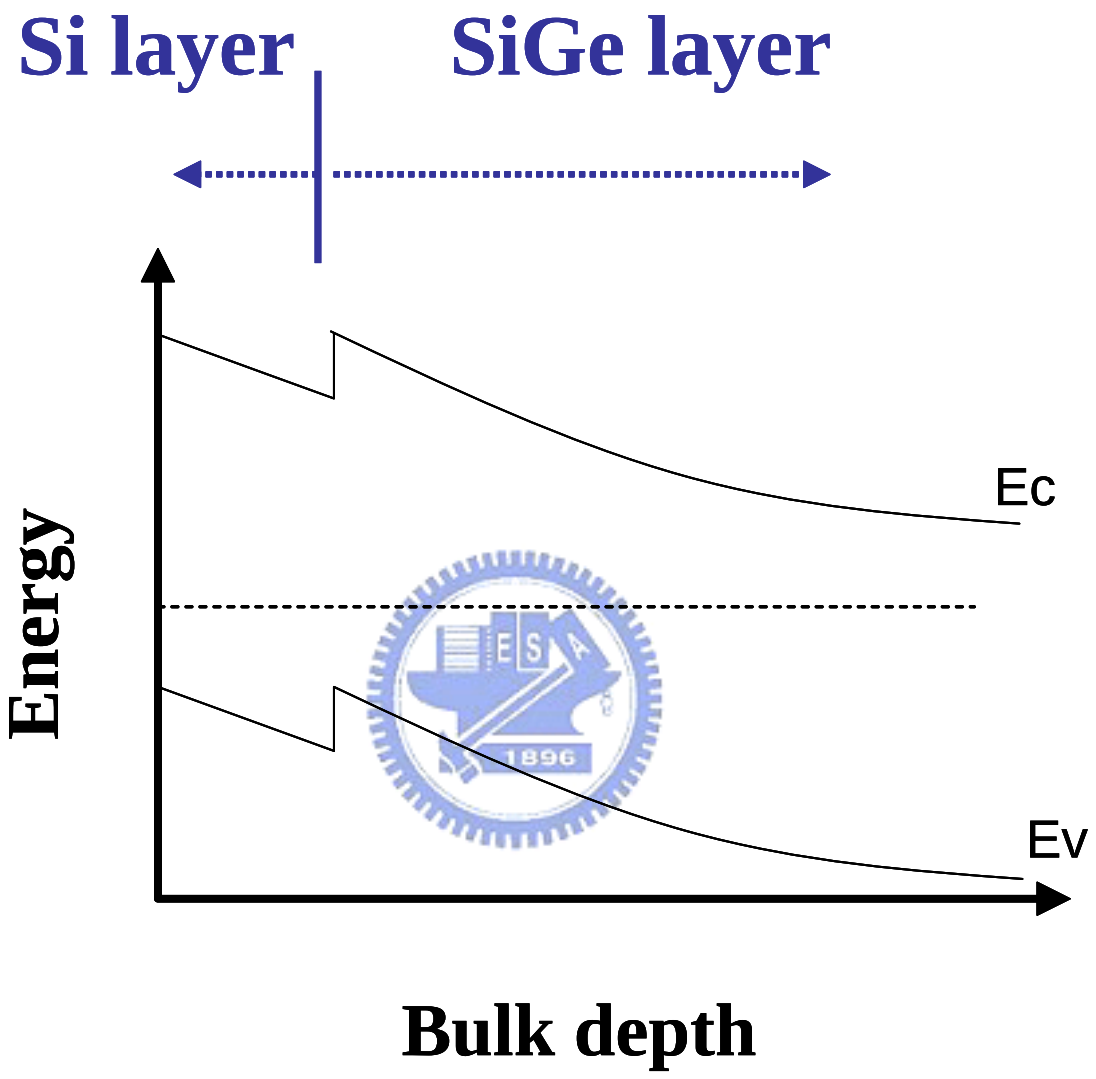


Fig. 3.7 The predicted energy band diagram in the strained Si p-MOSFET's as a function of bulk depth.

increased separation between the gate and the buried channel will degrade the transconductance, $g_{m,}$ which limits the performance enhancement of p-MOSFET's strained-Si device. Besides, from Fig. 3.7, we can find that the conduction band and the valence band of SiGe are almost equal height for those of Si. The energy band structure doesn't need loser gate voltage to complete the charge recombination at the SiGe/Si interface for p-type devices. For the above reasons, the difference of the gate voltage to complete the charge recombination at the interface between the SiGe/Si interface and the SiO_2/strained-Si interface are suppressed so that the charge pumping current second saturation level of p-MOSFET's is not be discovered. The variation between the p-MOSFET's and n-MOSFET's just certifies our explanation about two level saturation current of charge pumping current.

From the above incremental frequency charge pumping method and energy band diagram analysis, the interface trap density in a SiGe/Si heterostructure is successfully evaluated for the first time in the strained-Si device at the room temperature. In the later discussion, we use the information about the two layers of saturation charge pumping current to further study the influence of the SiGe/Si heterostructure by comparing it with traditional bulk-Si device.

3.3.2 Hot Carrier Degradation in Strained-Si Devices

3.3.2.1 Analysis of HC Degradation with Impact Ionization Substrate Current

Figure 3.8 shows the I_D-V_D characteristic of n-type and p-type device including bulk Si and strained-Si device. From the figure, it reveals the enhancement of the driven current both on n-type and p-type strained-Si devices. The result can be explained as the enhancement of the effective mobility. Compared with n-type device,

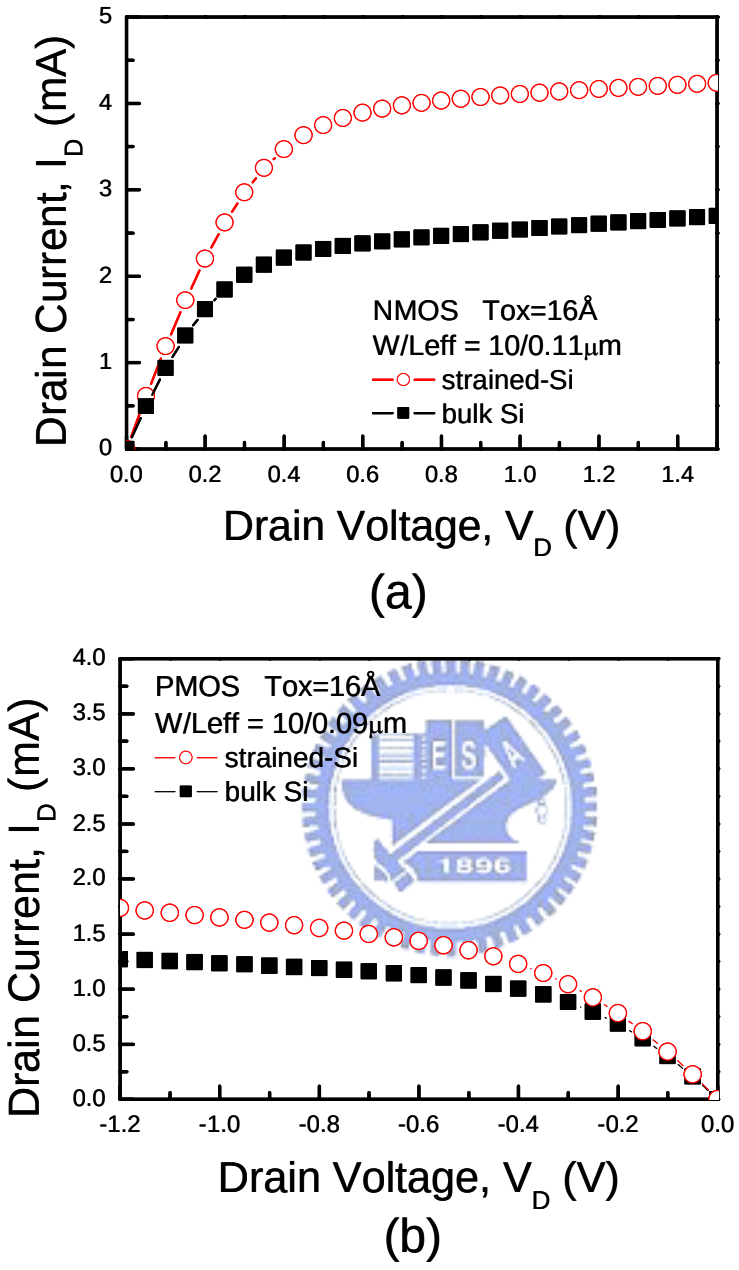


Fig. 3.8 The comparison of I_D-V_D characteristics of strained-Si and bulk Si devices, including (a) n-and (b) p-types.

the p-type strained-Si device has little enhancement, attributed to that discontinuity of the p-type strained-Si device energy band diagram, as aforementioned.

The hot carrier degradation is shown in Fig. 3.9, in which we found that the drain current degradation of the strained-Si device is much larger than that of the bulk Si device, where the stress condition is the worst case, $V_G = V_D$ stress. The result of the transconductance is shown in Fig. 3.10, which reveals the same tendency. Before the stress, the g_m of the strained-Si device is larger than that of bulk Si devices because the strained-Si devices has higher mobility. However, the enhancement of the strained-Si devices will decrease or even disappear after the worst-case stress if the degradation is sufficiently large.

In order to completely study the hot carrier stress of the strained-Si devices, we use IFCP with the measurement results as given in Fig. 3.11 We can find that the enhancement of the strain-Si device is mainly in SiO_2/Si interface layer. This phenomenon can be attributed to that the path of hot carrier is the direction to drain and passes the SiO_2/strained-Si channel, not via Si/SiGe interfaces. From this figure, we can also find that there is a huge increase of charge pumping current in the strained-Si devices, which means that interface trap density increases dramatically. We find that ΔN_{IT} of the strained-Si device is almost 30 times than that of the bulk Si device because the charge pumping current is proportional to the interface trap density.

We measured the charge pumping current after FN stress in Fig.3.12 and found that the degradation is not enhanced in the strained-Si devices. This means that the quality of SiO_2/Si interface is not worse than that in bulk Si devices. In the following, we compare impact ionization substrate current of both devices in Fig.3.13 (a). The

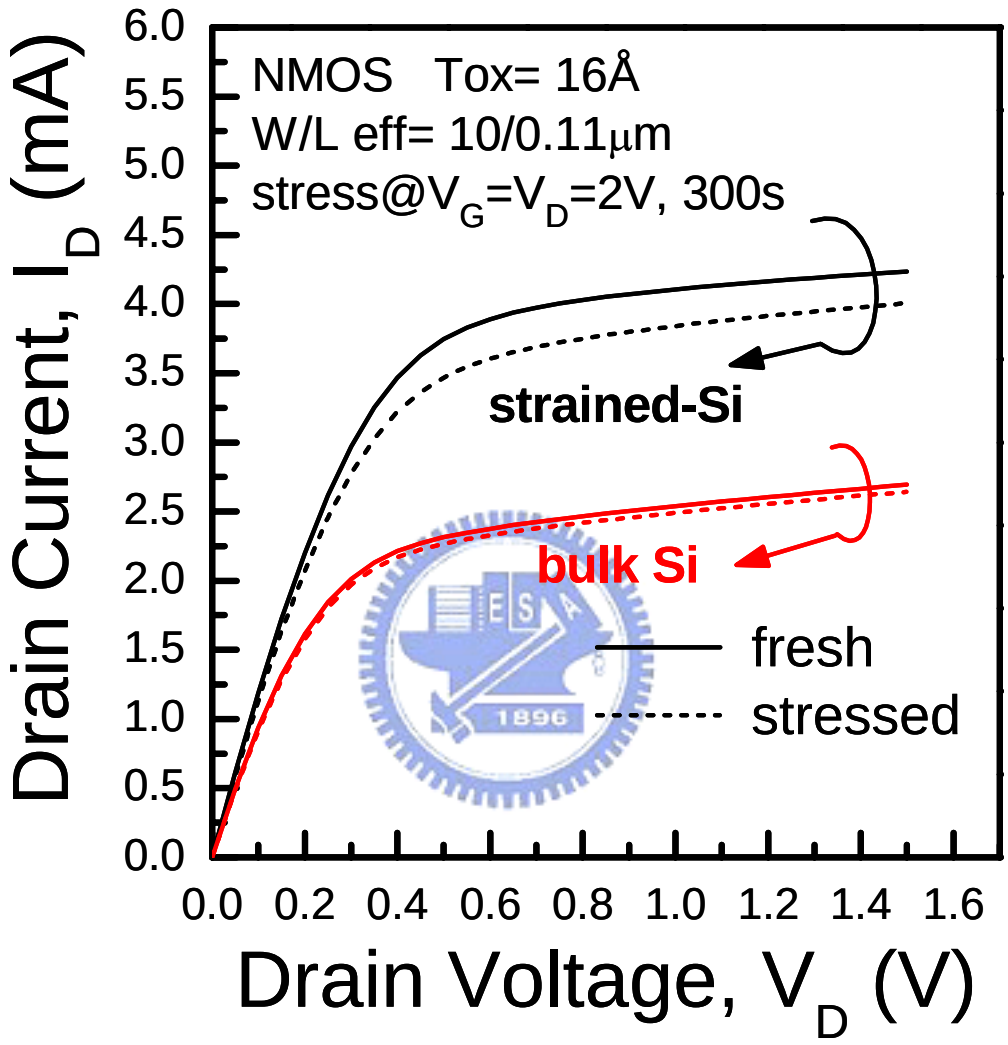


Fig. 3.9 The I_D-V_D characteristics of both devices, including strained-Si and bulk Si devices before and after worst HC stress at $V_G = V_D$. Worse HC degradation exhibits in the strained-Si devices.

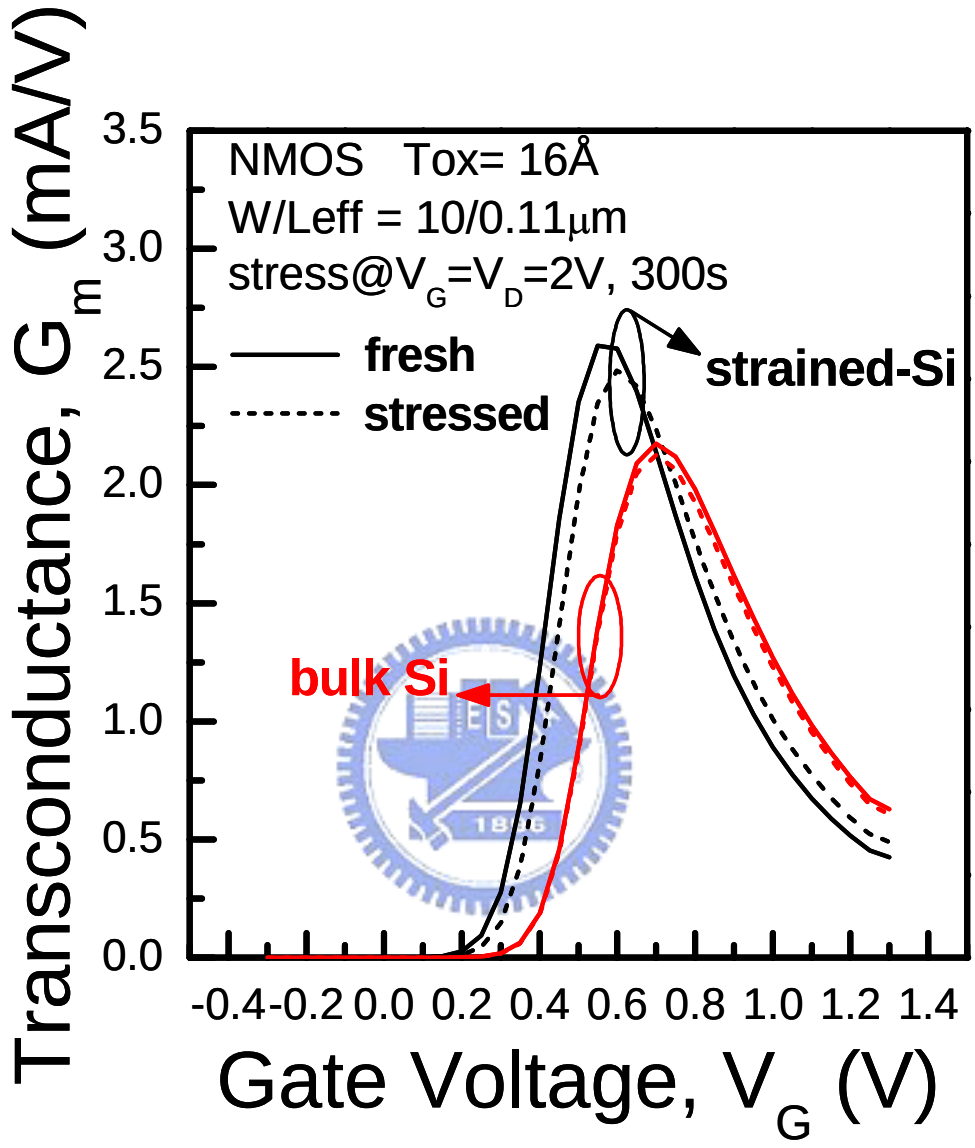


Fig. 3.10 Transconductance as a function of V_G is plotted. The strained-Si devices shows higher G_m and decay quickly after the HC stress.

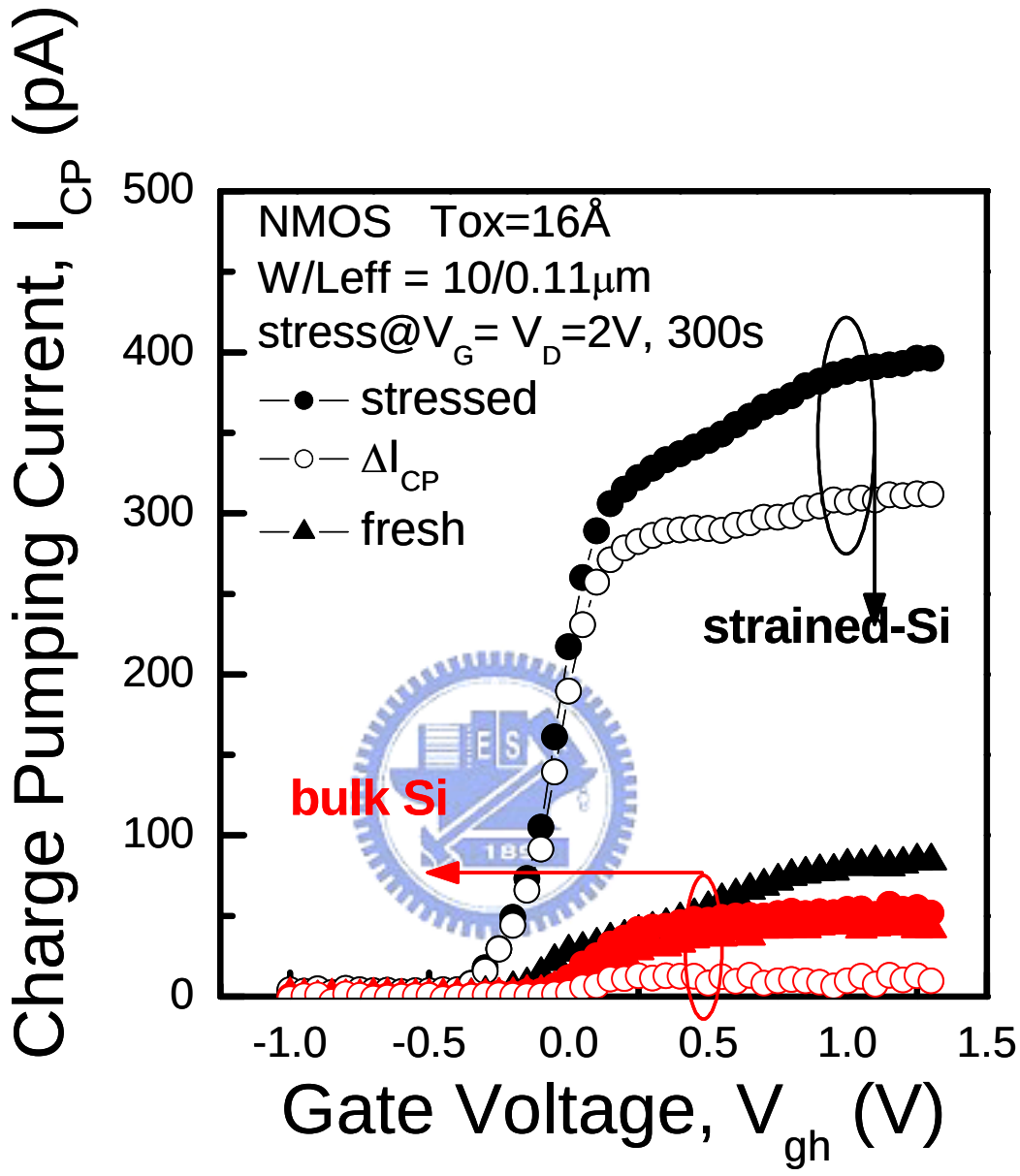


Fig. 3.11 The charge pumping characteristics of short channel strained-Si n-MOSFET's, compared to the bulk Si devices, after HC stress at $V_G = V_D$.

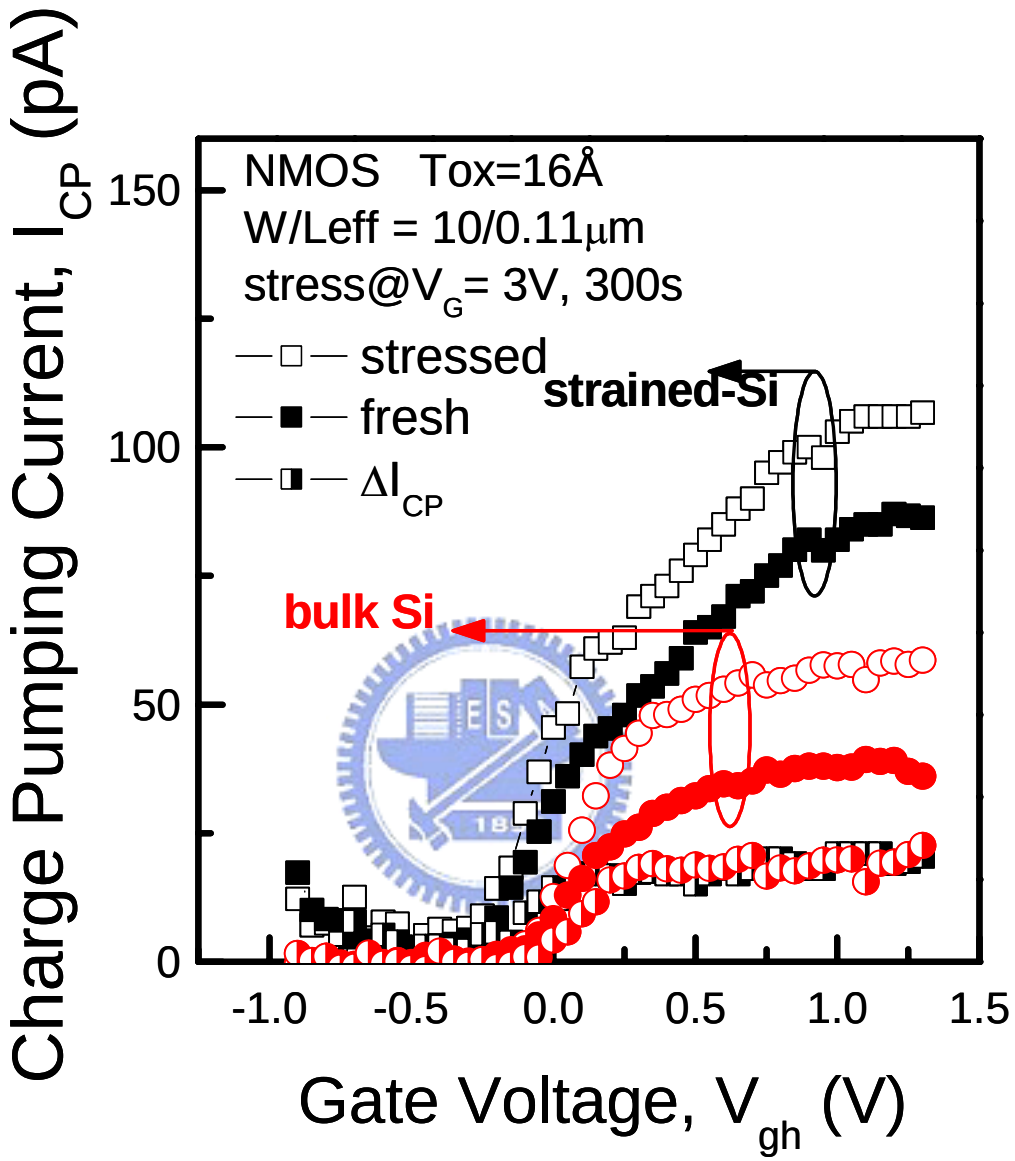


Fig. 3.12 The charge pumping characteristics of short channel strained-Si n-MOSFET's , compared to the bulk Si devices, after FN stress.

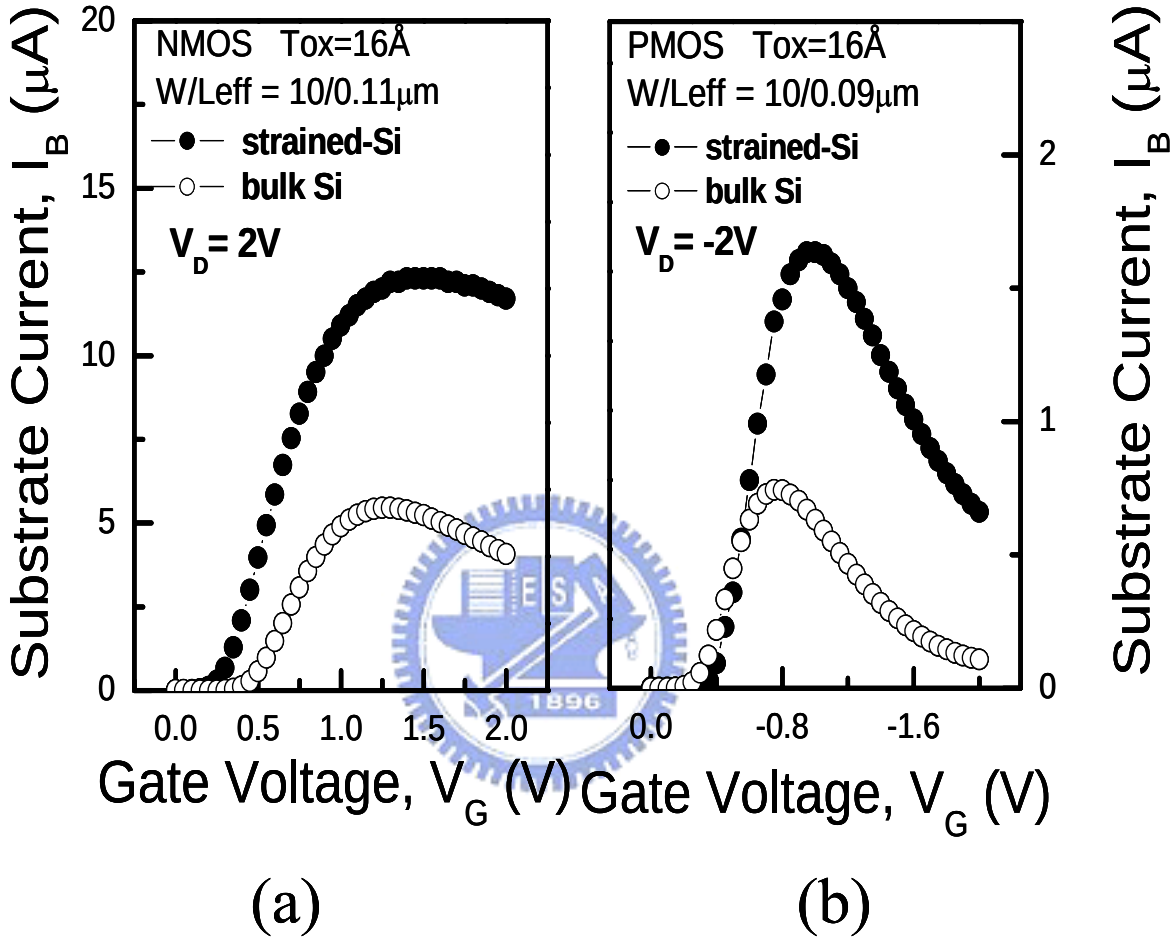


Fig. 3.13 The comparison of impact ionization substrate currents in strained-Si and bulk Si devices, including n- and p-types.

impact ionization current in the strained-Si device is obviously larger than that in bulk Si device as can be seen from the narrowing band gap of strain-Si device in contrast to the bulk Si device [14] shown in Fig. 3.14. In the figure, the gate tunneling leakage current comes from the conduction band electron tunneling current and the valence band electron tunneling current dominates the substrate tunneling leakage current. The different of tunneling barrier height is just the band gap of channel Si substrate. Besides narrowing band gap, the mobility enhancement of strained-Si device is another matter to have larger impact ionization current in strained-Si devices. When biased at $V_G=V_D$, the substrate current is four times than that in bulk Si devices. Consequently, we conclude that the larger impact ionization current as a result of the narrowing of the band gap energy is the reason for the enhancement of the hot carrier degradation in strained-Si devices. Because of the lack of the influence about impact ionization current, the degradation is almost the same for both devices after FN stress. It indicates that the degradation is weaker in the vertical direction but stronger in the lateral direction.

Compared to that in n-MOSFET's, we measure the charge pumping current after hot carrier stress and impact ionization substrate current in p-MOSFET's, as shown in Figs. 3.15 and 3.13(b). The results show that the increase of $\Delta I_{CP,MAX}$ in p-type strained-Si devices is smaller than that in n-type strained-Si devices, however, the enhancement of impact ionization substrate current is still larger than that of bulk Si device. The situation implies us that there is another cause besides the impact ionization rate to enhance the hot carrier degradation in strained-Si devices.

3.3.2.2 Analysis of HC Degradation with Channel Carrier Mobility

Besides the effect of impact ionization rate as described above, we think that the

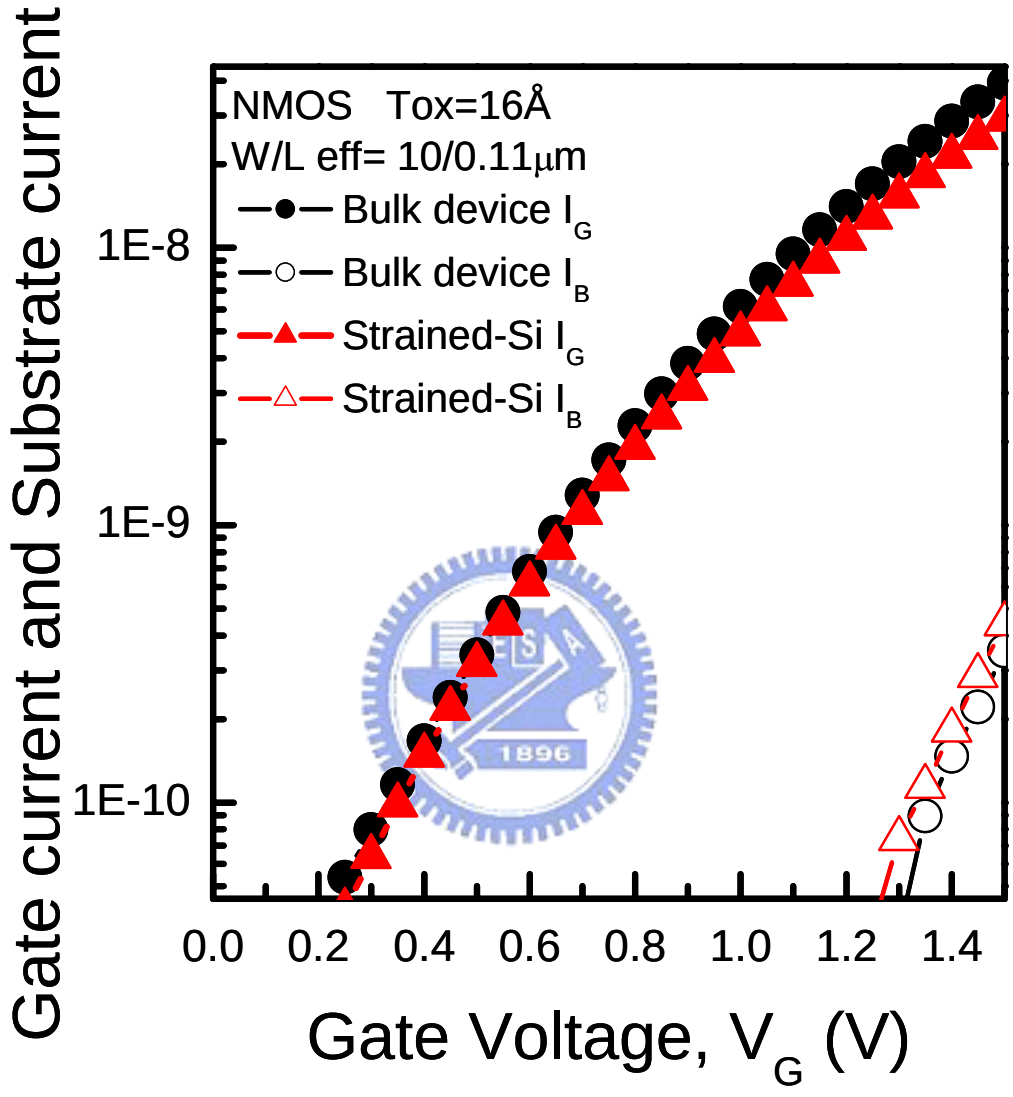


Fig. 3.14 Gate and substrate current versus gate bias in strained-Si device and bulk devices.

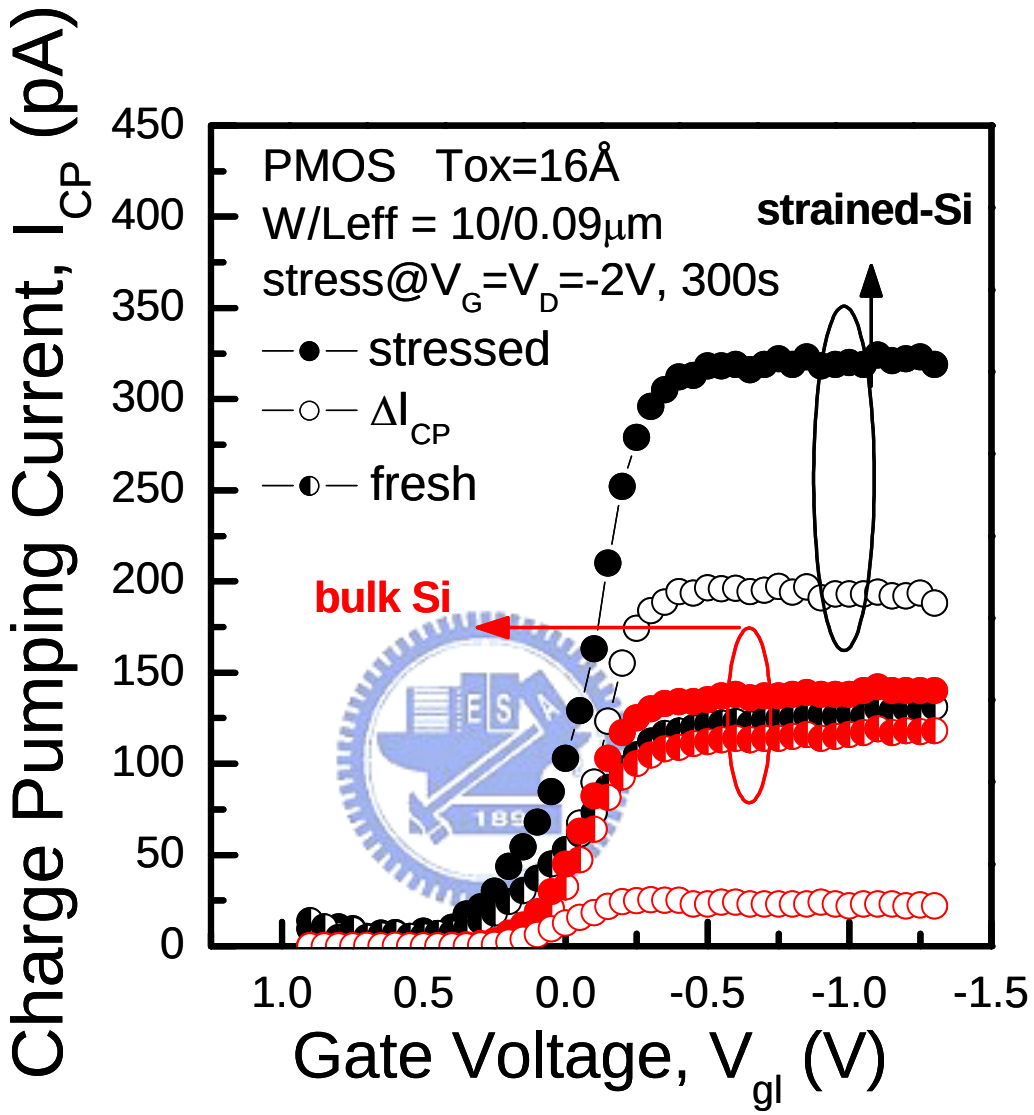


Fig. 3.15 The charge pumping characteristics of short channel strained-Si p-MOSFET's , compared to the bulk Si devices, after HC stress at V_G = V_D. Note the enhancement of ΔI_{CP} in the strained-Si p-MOSFET's is less than that in n-MOSFET's.

higher effective lateral mobility in the strained-Si devices can enhance the energy and acceleration of hot carriers and then make the hot carrier degradation worse. Figure 3.16 shows that transconductance, g_m, of the strained-Si device compared with bulk Si device for both n-type and p-type devices. In n-type devices, the transconductance of the strained-Si devices is larger at both low and high gate biases. However, in p-type devices, the peak transconductance in strained-Si devices is still larger at low gate bias, but the enhancement will decay faster at higher gate bias and even disappear [15].

In addition to the transconductance, we also measure the effective mobility to explain this phenomenon in Fig. 3.17. From this figure, it shows the effective mobility of n- and p-MOSFET's as a function of vertical effective field, we can obtain similar resultant as that for the transconductance. Because of the high gate bias at $V_G=V_D$ stress, we pay attention to the effective mobility at high effective vertical field. For the strain (20%Ge), the effective electron mobility increases over the all range of effective vertical field. The peak hole mobility also increases, however, the hole mobility enhancement diminishes at higher effective vertical field [16]. The case of p-type strained-si device is explained by the reason about the discontinuity of the energy band diagram, as previously discussed.

According to the discussion above, we can make a short conclusion that the smaller enhancement of ΔN_{IT} after hot carrier stress at $V_G=V_D$ condition in p-type strained-Si devices is mainly caused by the diminishment of the enhancement of the effective hole mobility in higher effective vertical field. In conclusion, the more enhancements in channel mobility are, and then the more degradation in strained-Si device can be seen.

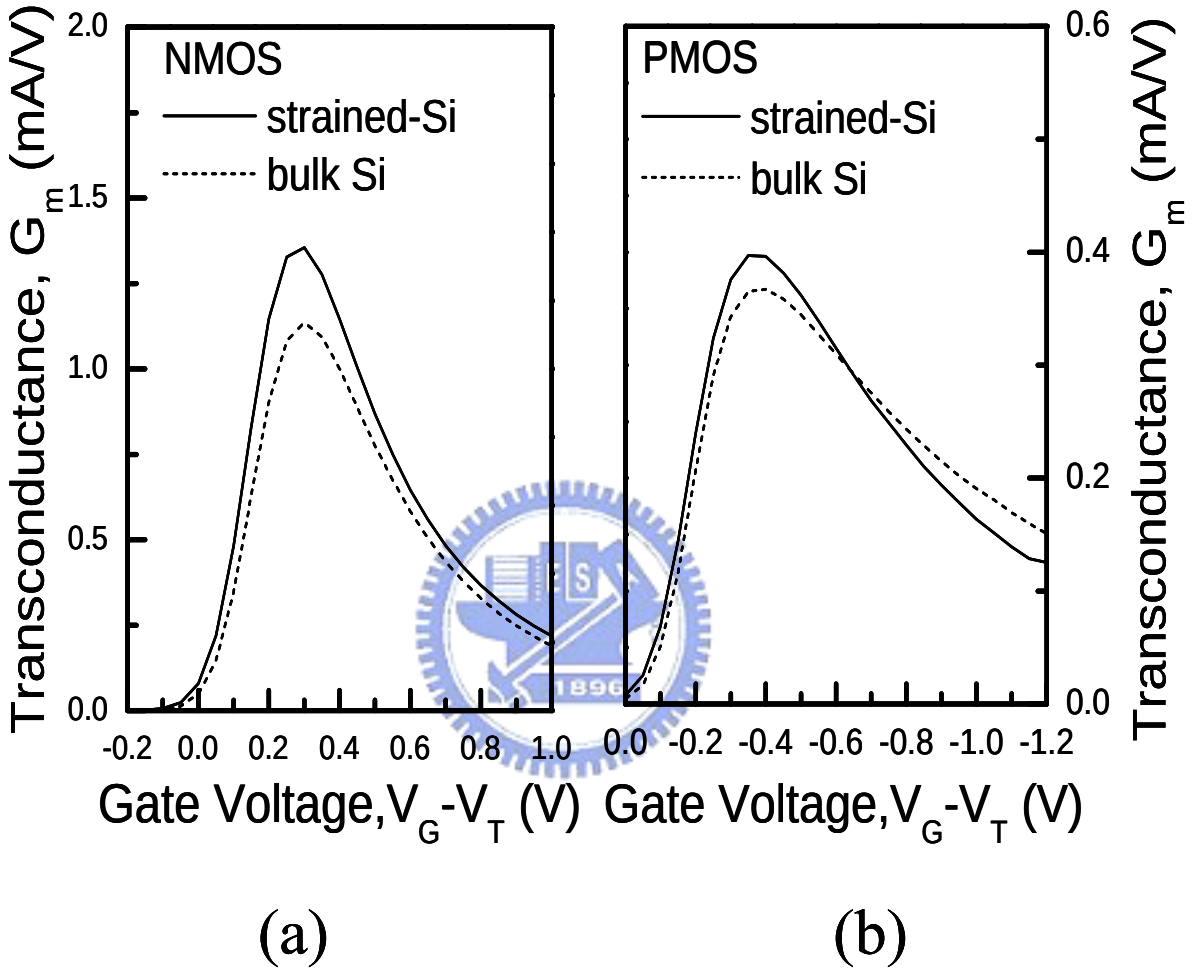


Fig. 3.16 The comparison of transconductance in both devices, including n- and p types. Note the enhancement in strained-Si p-MOSFET's decays severely at high V_G.

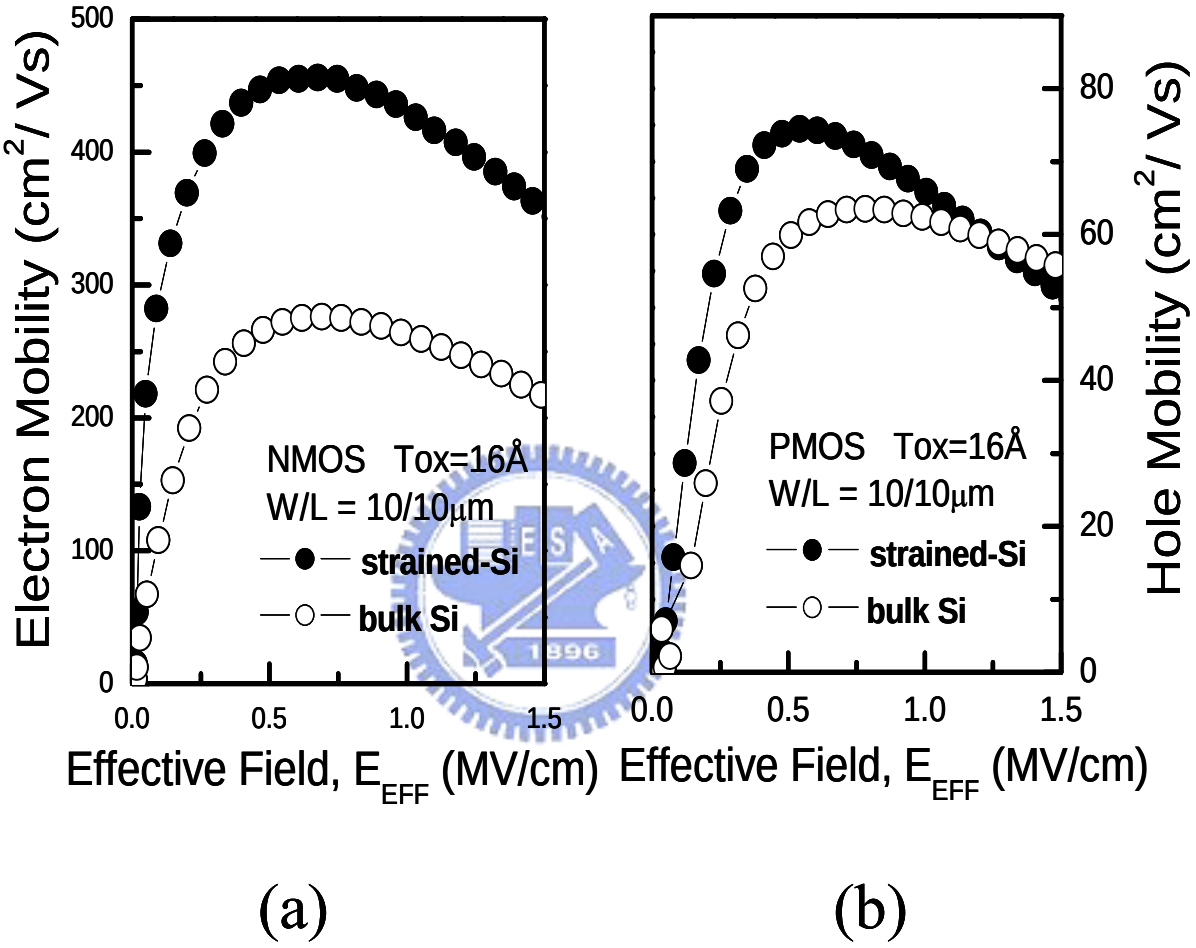


Fig. 3.17 The comparison of mobility in both devices, including n- and p-types. Note the enhancement in strained-Si p-MOSFET's decays at high effective field.

In addition to that, Fig. 3.18 shows the charge pumping current of p-MOSFET's after FN stress. The trend, which the degradation is not enhanced in the strained-Si device of the figure, is the same as that in n-MOSFET's. It indicates that the quality of SiO_2/Si interface is not worse than that in bulk Si devices also for p-MOSFET's. We can find that the degradation of strained-Si device is a little smaller than that in bulk device and the situation can be explained by the lower mobility at higher gate bias for strained-Si devices. Compared with the result of hot carrier stress, it also indicates that is weaker in the vertical direction but stronger in the lateral direction for p-type strained-Si devices.

3.4 Summary

In addition to the discussion on the basic theory of strained-Si devices, the charge pumping method for strained-Si devices is analyzed in detail for the first time and used to check the device degradation. In this chapter, we found the two saturation-level charge pumping current in strained-Si device and reported that the hot carrier degradation behavior in strained-Si technology was enhanced by high lateral acceleration and larger impact ionization current which results from narrowing band gap. The worst case of hot carrier degradation occurs at V_G=V_D condition and the degradation will follow the trend of impact ionization rate and effective mobility.

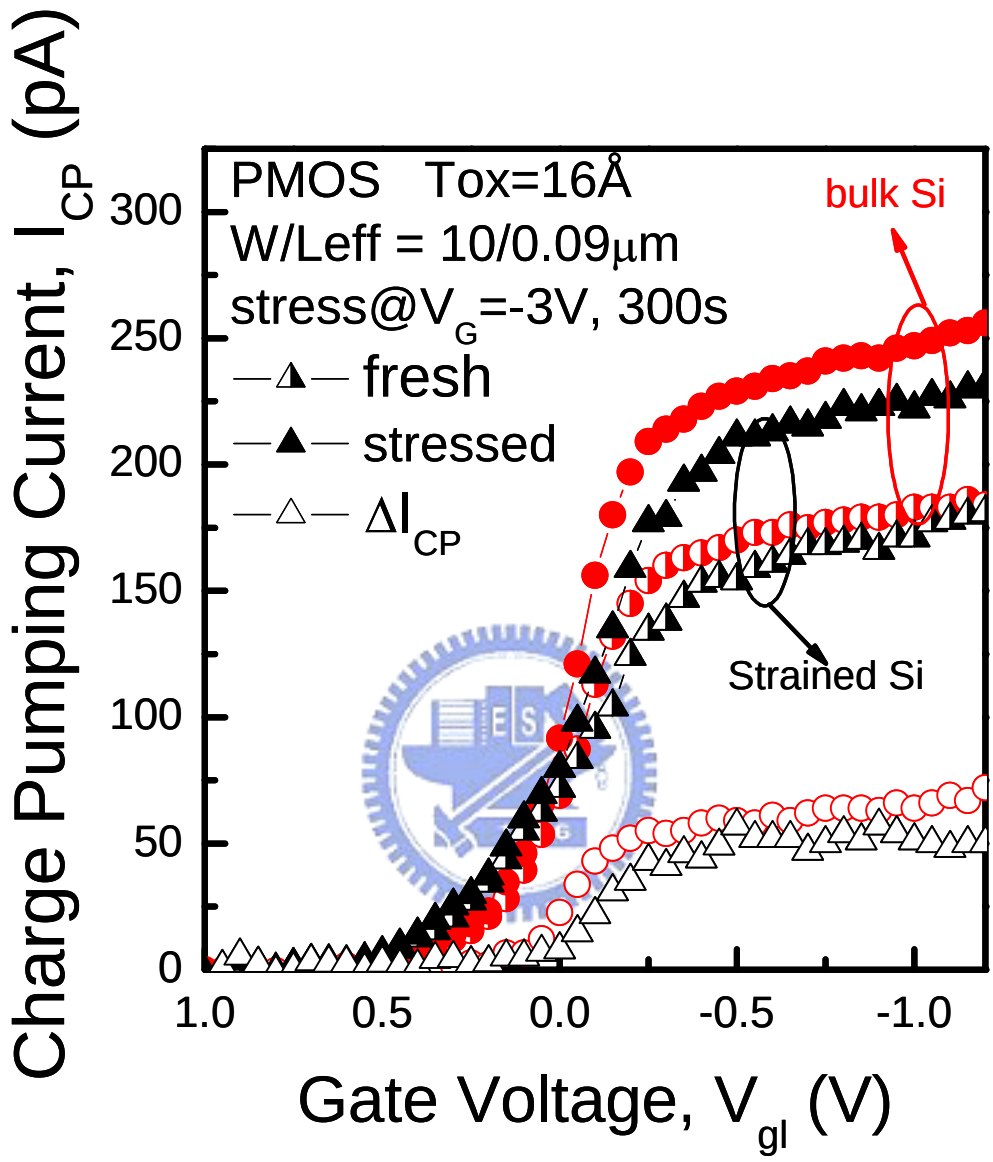


Fig. 3.18 The charge pumping characteristics of short channel strained-Si p-MOSFET's , compared to the bulk Si devices, after FN stress.

Chapter 4
Analysis of NBTI Degradation and Induced Traps Distribution in Strained-Silicon MOSFET's

4.1 Introduction

In order to improve the electron mobility, the strained-Si device is one of the promising ways to reach the goal. However, it has been found to significantly increase the device degradation after hot carrier stress in room temperature above. In addition, the NBTI in pMOSFET has been a key factor for device [17-19]. In order to further study the reliability of the device, we will focus on the temperature dependence hot carrier degradation in this chapter. We will also investigate the diversity of the NBTI degradation and the NBTI enhancement HC effect. Finally, we will use charge pumping method and Gated-diode method to investigate the temperature dependent HC degradation.

On the other hand, the different Ge contents and thickness of strained layer make different strained stress which might influence the reliability of devices. Although the denser Ge content and deeper thickness of strained layer can enhance the mobility, they also degrade the reliability of devices. It is necessary to understand the tendency of reliability degradation about strained degree. Here, we rely on comparing the impact ionization current and using charge pumping method to complete the study. Finally, we use lateral profiling method to plot the distribution of interface traps in strained-Si devices. Taking advantage of the distribution, we can understand the influence of strained-Si layer and Ge out-diffusion on the device reliability.

4.2 Analysis of Temperature Dependent HC Degradation

In this section, we discuss the temperature dependence of short channel strained-Si devices. Fig. 4.1 shows the measured temperature dependence from charge pumping cures of strained and bulk devices. From the results in Fig. 4.1, we can easily find that the hot carrier degradation of both devices is enhanced at high temperatures. Although the degradation of strained-Si device is also larger than that of bulk device after high temperature stress, Fig. 4.1 also shows that the enhancement of the degradation between high temperature stress and room temperature stress in bulk Si devices is more severe than that in strained-Si devices. Here, we see that the generated N_{it}(in%) for strained device is much smaller than bulk ones since N_{it} is proportional to $I_{cp,max}$. In order to observe in more detail, the calculated ΔN_{IT} versus stress time for a varying temperature is plotted in Fig. 4.2, where we can get the same results described as above obviously. The increase of interface trap density after hot carrier stress at high temperature is enhanced more severely in bulk Si devices. One interesting results is that the strained-Si device is less sensitive to temperature for an increase of the temperature from room-T to 80℃. This phenomenon can be explained that the driving force to enhance impact ionization is changing from the enhanced lateral electric field in strained-Si devices to the lattice temperature in bulk Si devices [20-21]. In other words, the influence of high temperature on the impact ionization is larger in bulk Si devices. Besides, by borrowing from one of author's previous data for I_D at room-T and high-T(Fig.12 in [22]), it shows that there is a larger degradation in strained-Si device at high temperature than that in bulk device, so that the influence of mobility enhancement for hot carrier stress in strained-Si device will be suppressed. Consequently, we can find the worse temperature dependent hot carrier degradation in bulk Si devices from the experimental results.

To explore the temperature dependence HC effect, gated-diode measurement,

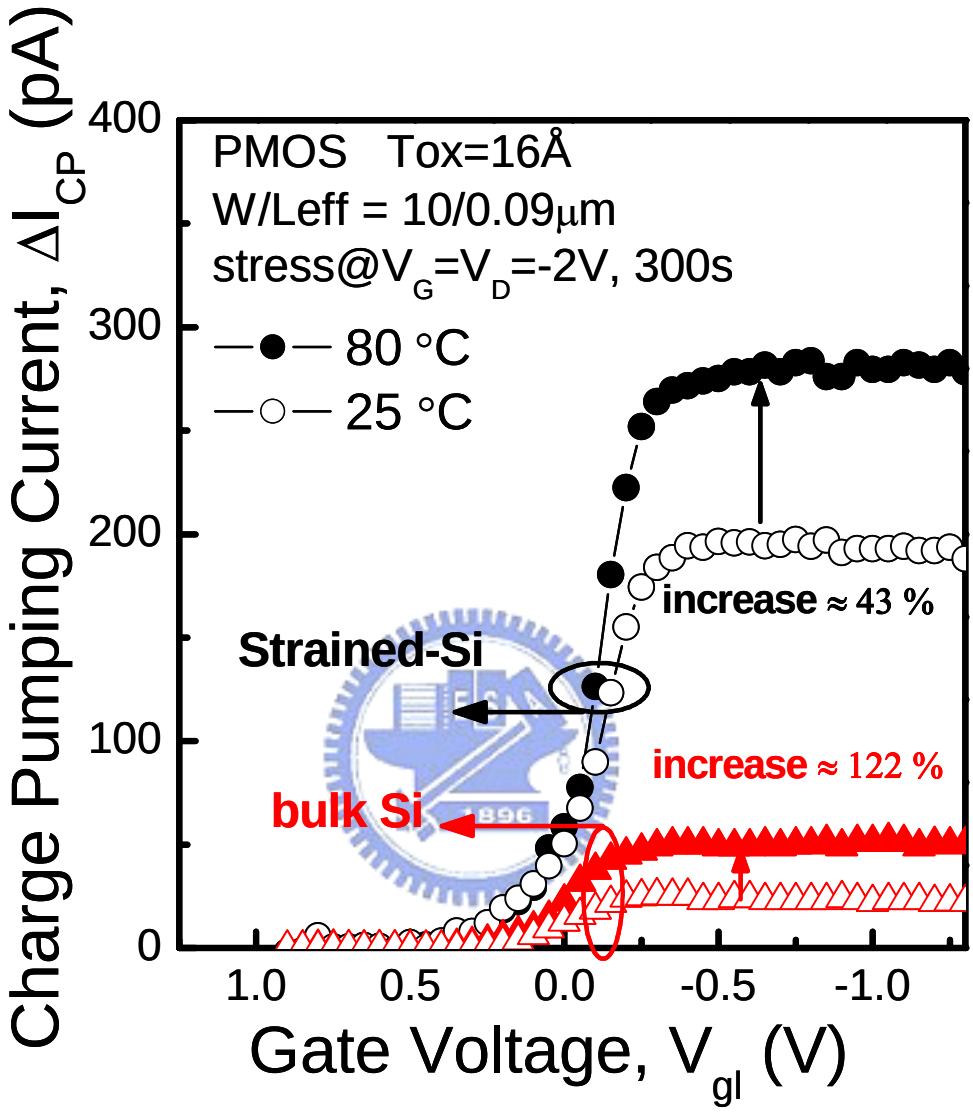


Fig. 4.1 The comparison of charge pumping characteristics of both devices after hot carrier stresses under V_G=V_D= -2V at 25 ºC and 80ºC. Note the enhancement in bulk Si devices is larger.

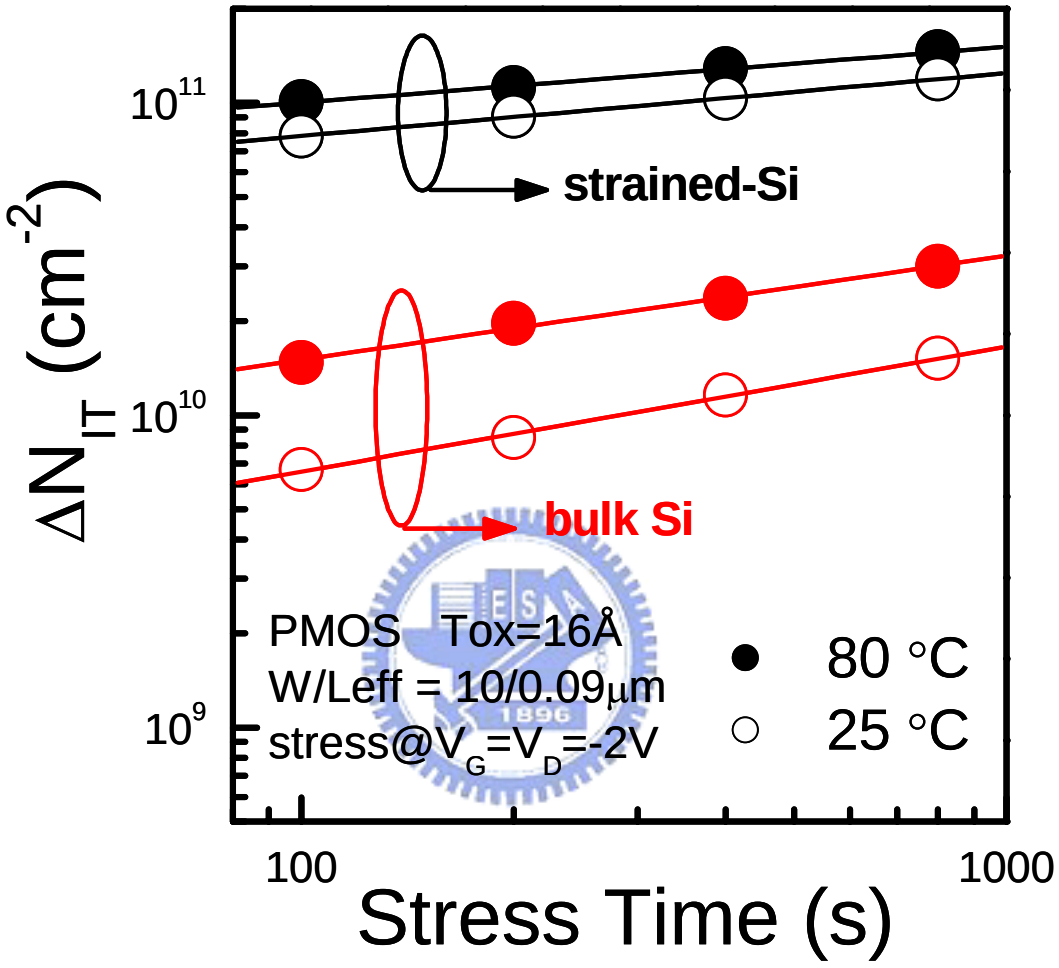


Fig. 4.2 The increase of interface trap density versus stress time. The stress condition is under V_G=V_D= -2V at 25 ºC and 80ºC.

which we presented in chapter 2, has been carried out as shown in Figure 4.3, where NBTI like stress [8] has been compared. From the principle of gated-diode method, the 2nd peak of $\triangle I_{GD}$ is related to the generation of N_{it} in the drain/Source junction region. A localized N_{it} at this peak is plotted as a function of stress time in Fig. 4.4, where we see that the increment with temperature in strained-Si device is indeed smaller than bulk ones. The result is consistent with the previous result in Fig.4.2. In short (1) the NBTI like stress in strained device exhibit higher amount of N_{it}, while (2) the NBTI like stress dependence on temperature for strained device is less sensitive to an increase of temperature, and (3) NBTI like stress in strained devices can extend their lifetime for high temperature operation if the Si/Ge out-diffusion can be well controlled by low temperature gate oxide process or with less defect at S/D junctions.

In the following, we measure charge pumping current for both strained-Si device and bulk device after NBTI stress in Fig. 4.5. As revealed in this figure, we find that the degradation of both device are almost alike comparing with high temperature hot carrier stress in Fig. 4.1. The smaller degradation of strained-Si device than that in bulk device from the figure, we can explain by the lower mobility at higher gate bias for p-type strained-Si devices. Not need to consider the influence of impact ionization effective, the temperature dependence of degradation level for both devices is approximate. The trend of NBTI stress for both devices is the same as the FN stress at room temperature. Then, we compare the degradation between NBTI stress and NBTI like hot carrier stress for strained-Si device in Fig. 4.6. We can easily find that the degradation in NBTI like hot carrier stress is larger than that in NBTI stress and the degradation in NBTI like hot carrier stress mostly produces the approach of drain region. This phenomenon can be easily explained that the NBTI like hot carrier stress additionally poses the influence of impact ionization effective comparing with pure NBTI stress. The result in this figure is also the same as

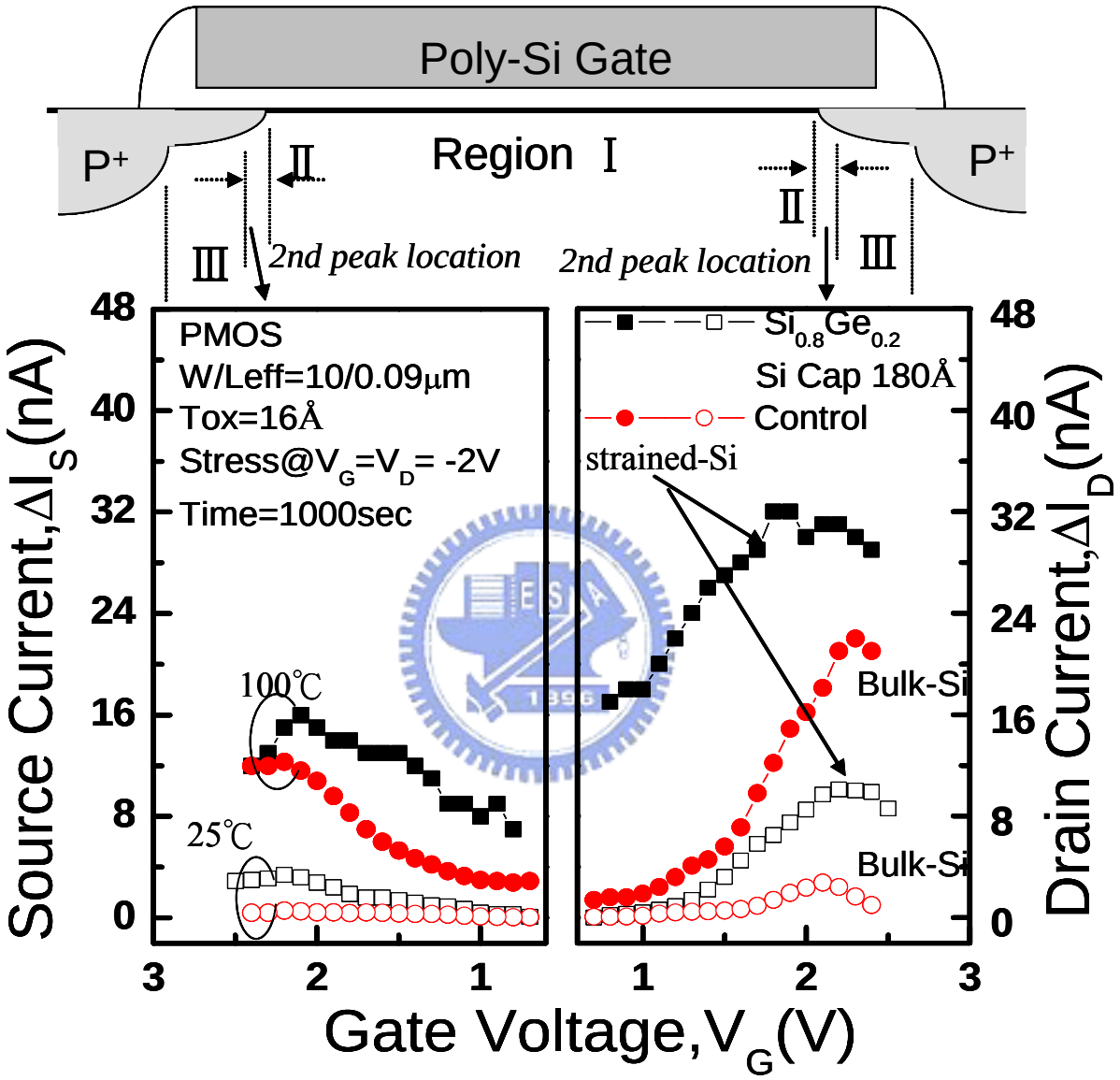


Fig. 4.3 Gated-diode measurement for strained and bulk device after V_G=V_D NBTI stress. The peak in region II represents the localized N_{it}, which is localized at the source and drain junctions.

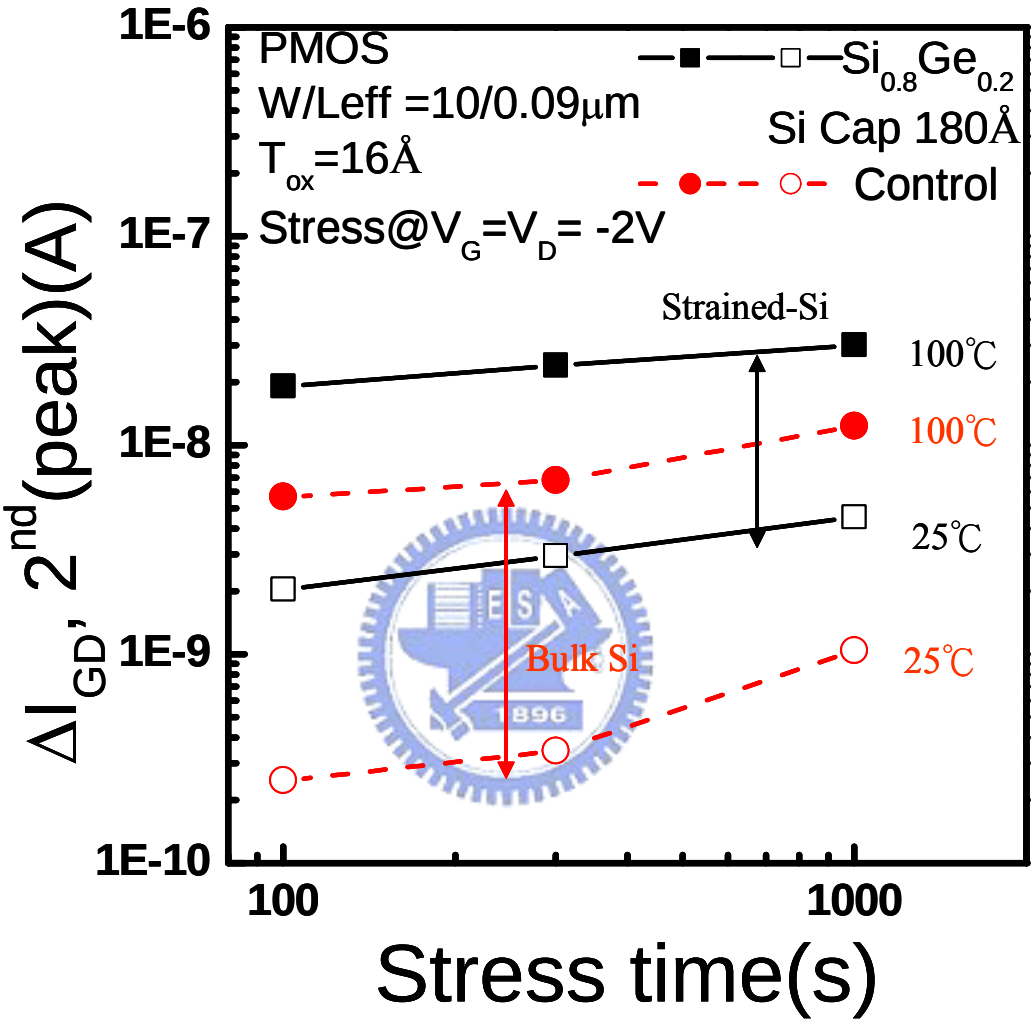


Fig. 4.4 The values of 2nd peak in Fig 4.3 plotted as a function of stress time.

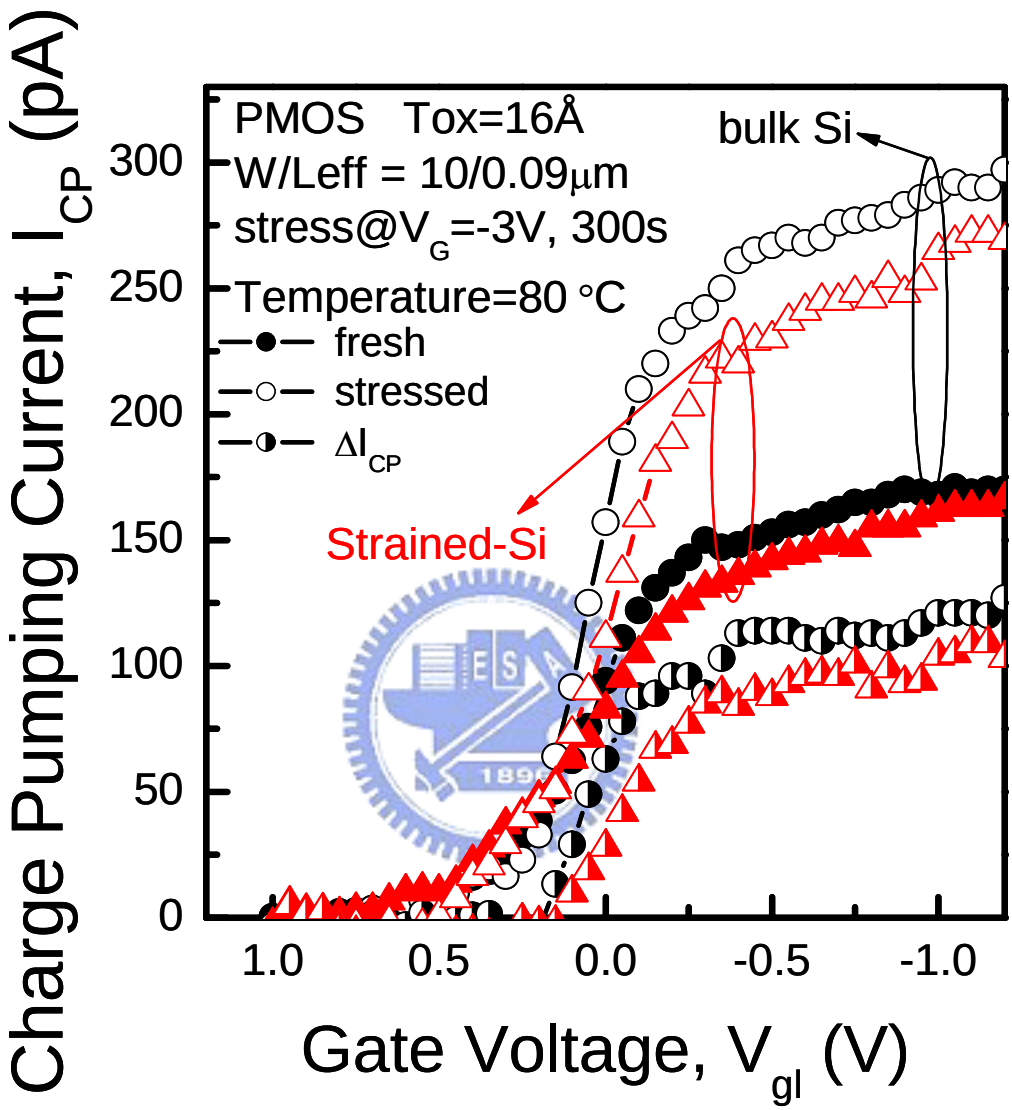


Fig. 4.5 The charge pumping characteristics of short channel strained-Si p-MOSFET's , compared to the bulk Si devices, after NBTI stress under V_G=-3V at 80℃.

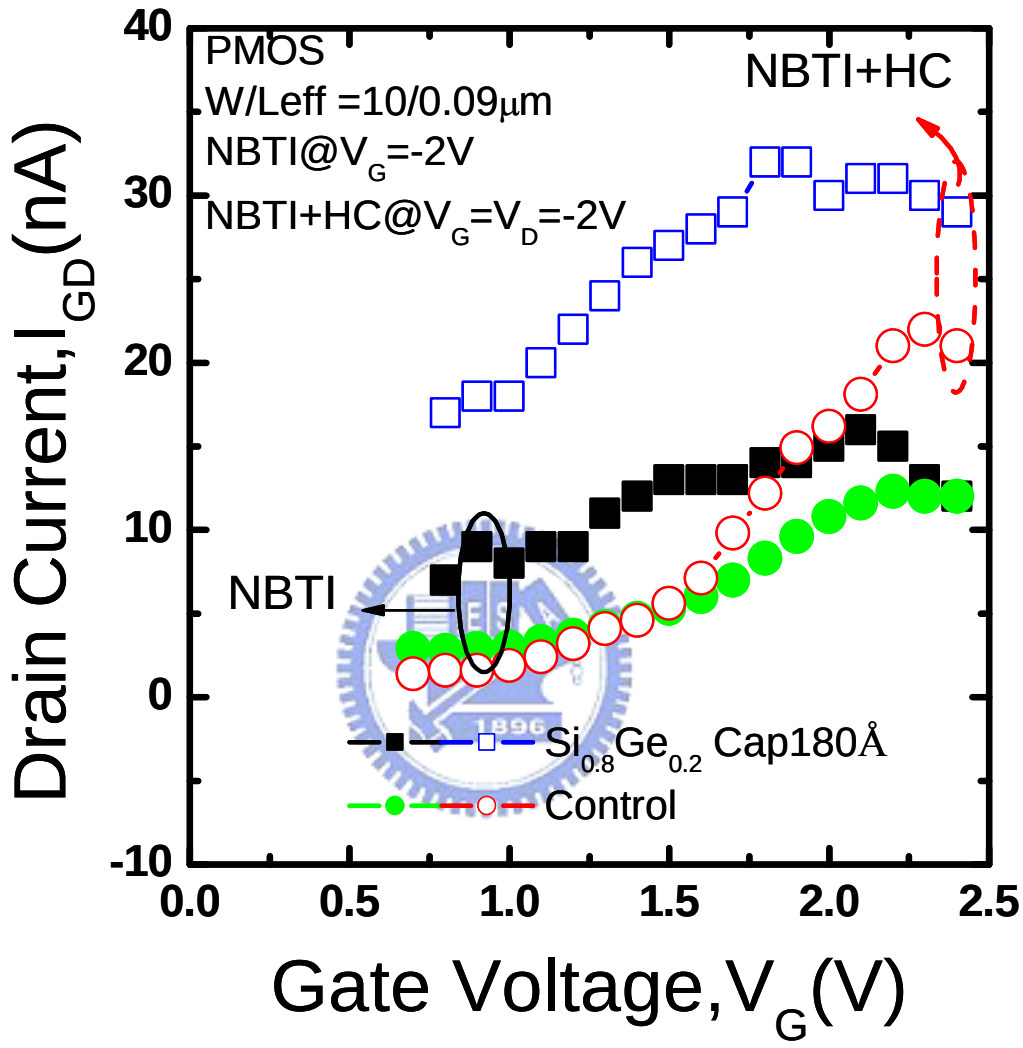


Fig. 4.6 The comparison of gated-diode currents of strained-Si devices after NBTI stress and NBTI-like stress.

discussed for room temperature, which was analyzed by using charge pumping method in chapter 3.

4.3 Analysis with Ge Concentration and Thickness of Si Layer

In the section, we analyze the characteristics with different fraction of Ge in the strained-Si devices. The strained-Si devices with 30% Ge content has a much larger drain current than that with 20% Ge content [23], as shown in Fig. 4.7, which also shows the comparison with different thickness of Si layer, 100Å and 180Å. Although we known that hole mobility only increases primarily at low E_{eff} when substrate Ge fractions on 20% from previously figure, we see that devices with incorporating a high-Ge-content and thicker Si layer exhibit higher strain and induce greater drain currents especially for the device with 30% Ge content and Si cap thickness 180Å From Fig. 4.7. The formation of lower strain in the devices with thinner Si layer is caused by the upward diffusion of Ge.

As revealed in Figs. 4.8 and 4.9, the deeper strained thickness makes higher impact ionization rate and effective carrier mobility. We can also find that the high Ge content contributes to high impact ionization from Fig. 4.10. Consequently, the high strain contributes to high impact ionization rate and effective carrier mobility, so that the hot carrier degradation of devices with 30% Ge content will keep worse. We perform the charge pumping measurement again to check the degradation after hot carrier stress. Fig. 4.11 shows the worse interface state degradation after hot carrier stress for the strained-Si devices with 180Å $Si_{0.7}Ge_{0.3}$ layer as predicted above.

Besides the enhancement of hot carrier degradation, there are other severe problems in the $Si_{0.7}Ge_{0.3}$ strained-Si devices. If the thickness of Si layer is too thin, the mobility will degrade because Ge diffuses upward to the strained channel, as

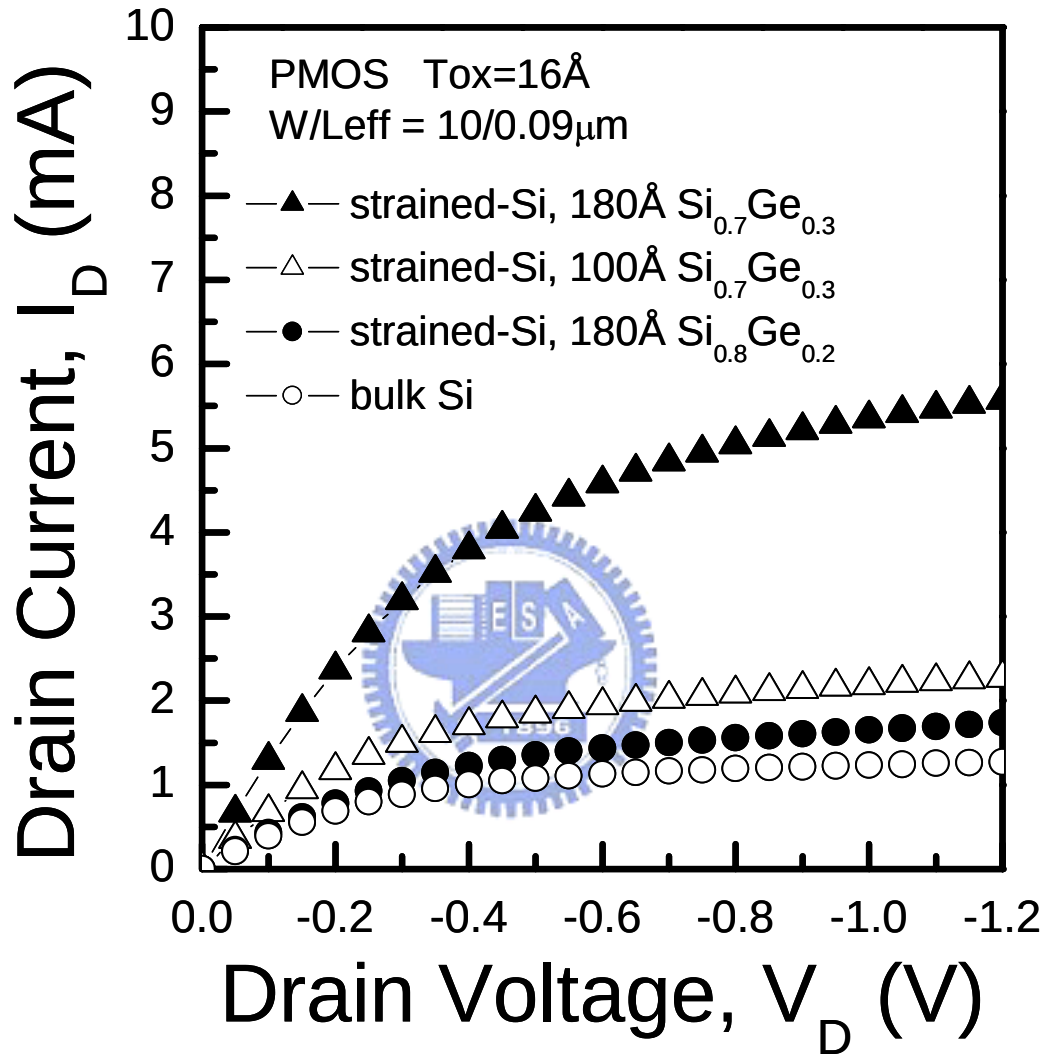


Fig. 4.7 The I_D-V_D characteristics of the strained-Si p-MOSFET's with different Ge concentration and thickness of Si layer.

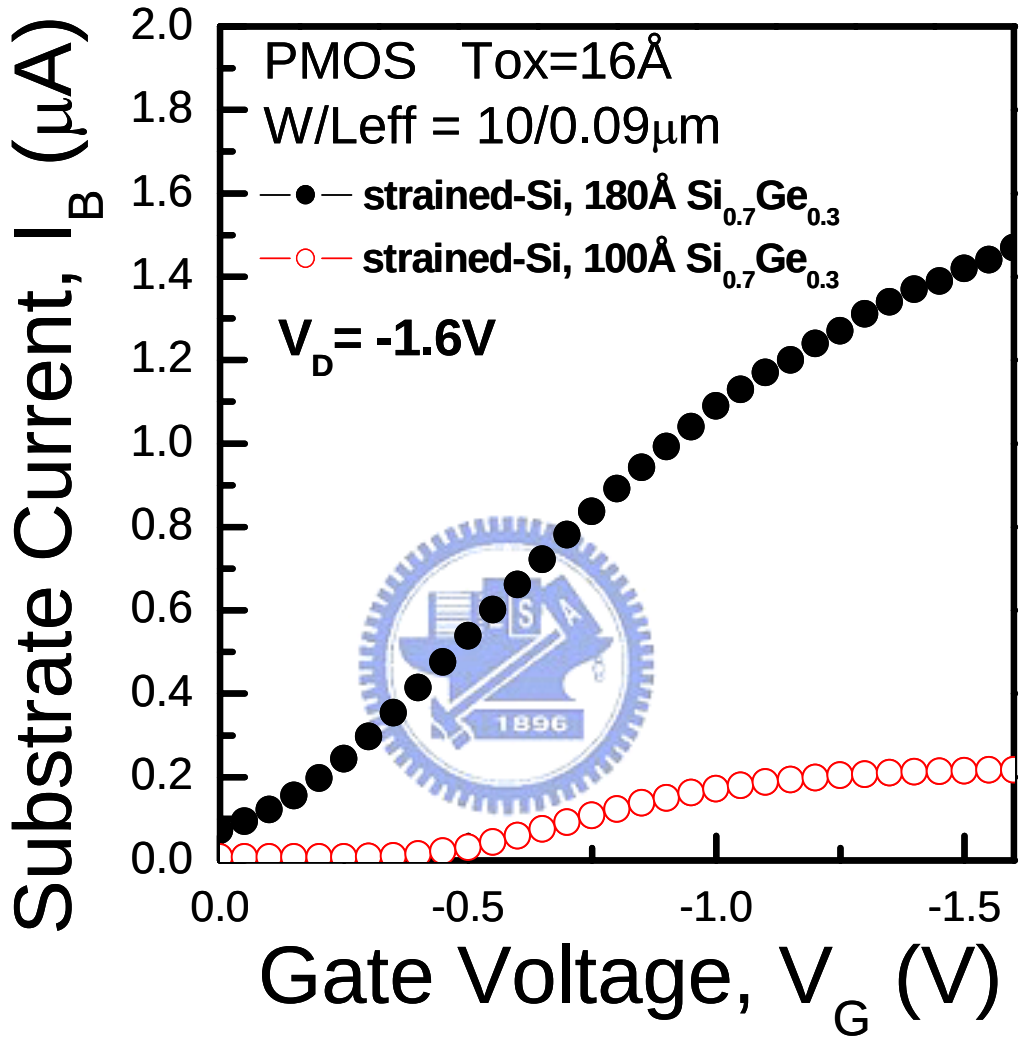


Fig. 4.8 The comparison of impact ionization substrate currents of $Si_{0.7}Ge_{0.3}$ strained-Si p-MOSFET's with different thickness of Si layer.

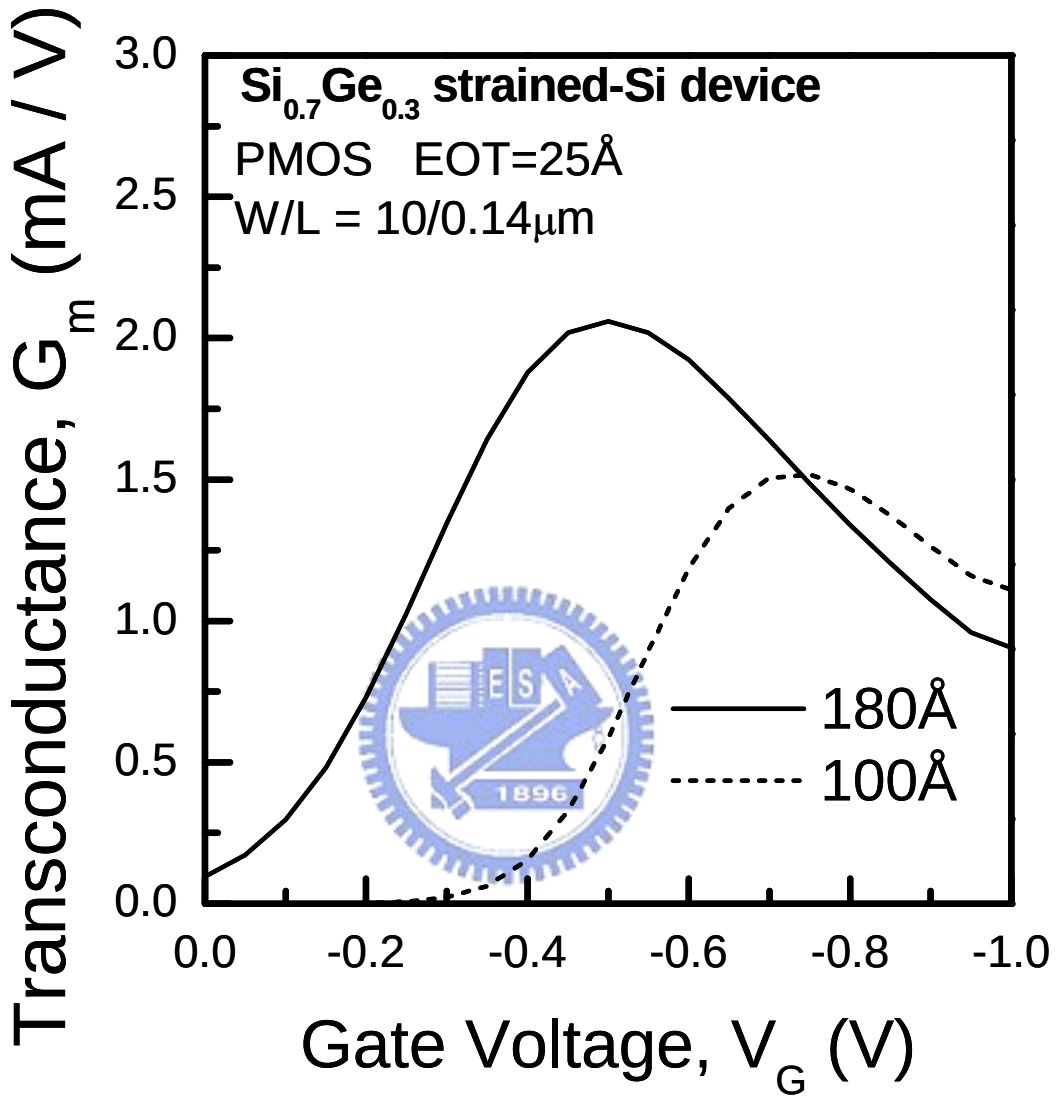


Fig. 4.9 The comparison of transconductance with two thickness of Si layer. The devices with thick Si layer exhibit higher G_m but G_m decays at high V_G.

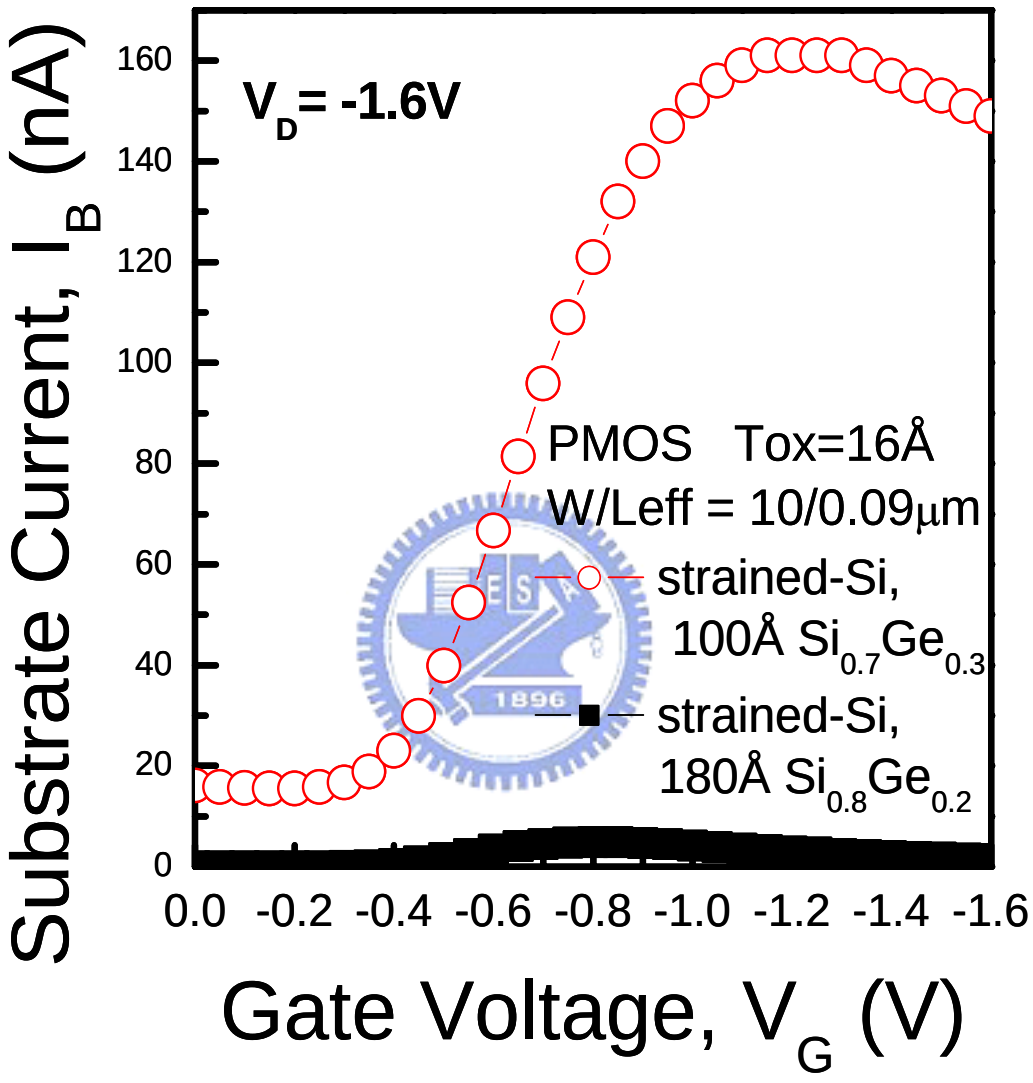


Fig. 4.10 The comparison of impact ionization substrate currents of $Si_{0.8}Ge_{0.2}$180Å and $Si_{0.7}Ge_{0.3}$100Å strained-Si p-MOSFET's.

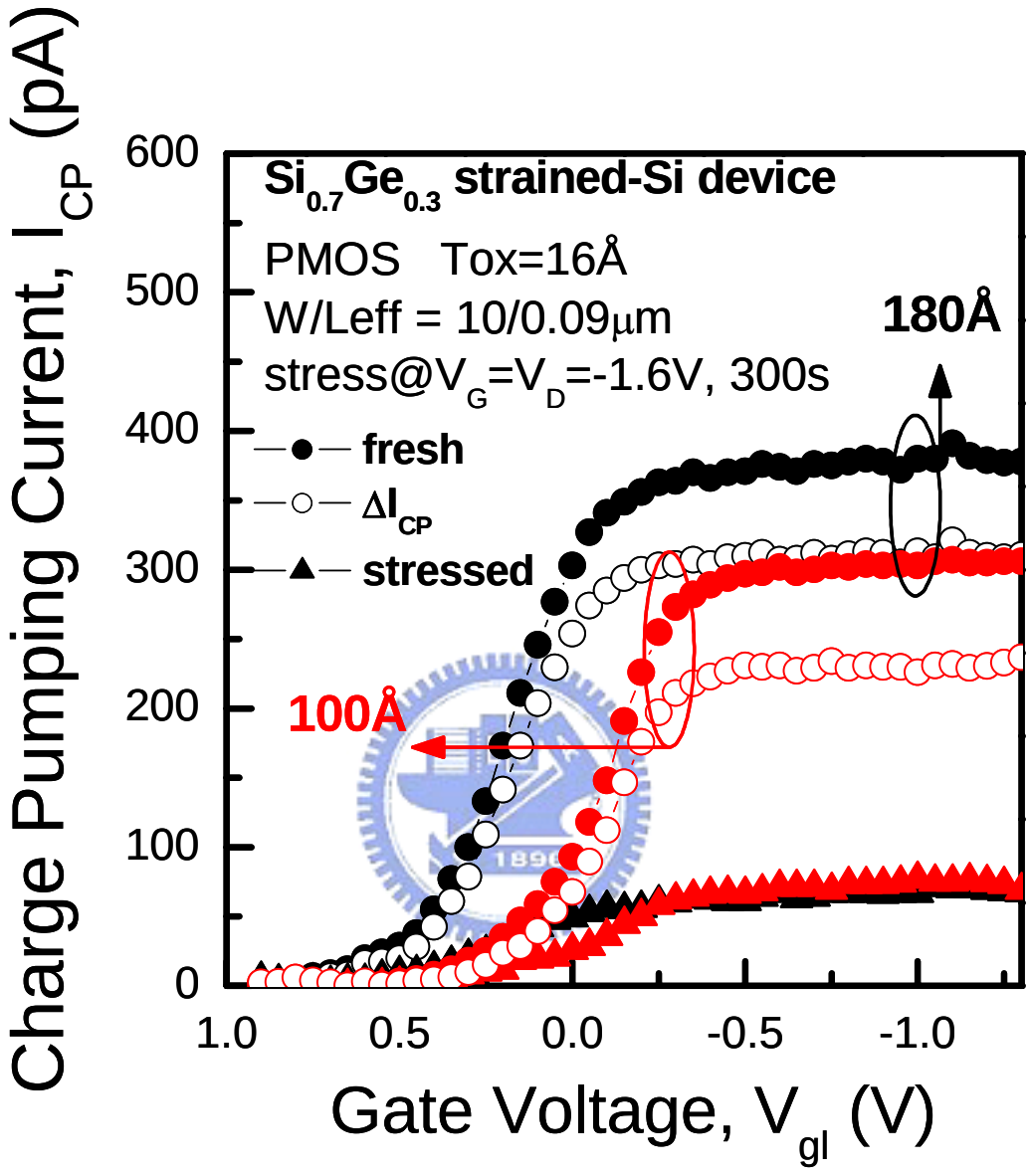


Fig. 4.11 The comparison of charge pumping characteristics of short channel $Si_{0.7}Ge_{0.3}$ strained-Si p-MOSFET's with different thickness of Si layer are compared. Note the larger ΔI_{CP} occurs in devices with 180Å Si layer.

shown in Fig. 4.9. If the thickness of Si layer is too thick, the defect via partial relaxation will occur [24]. In addition, when thickness of strained-Si layer increase, the band offset makes the Fermi level closer to the valence band, in turn, induces more holes in the inversion layer for same gate bias for p-type strained-Si device. Thus, the band offset lowers the threshold. The V_T shift can be observed by the charge pumping curve in Fig. 4.11.

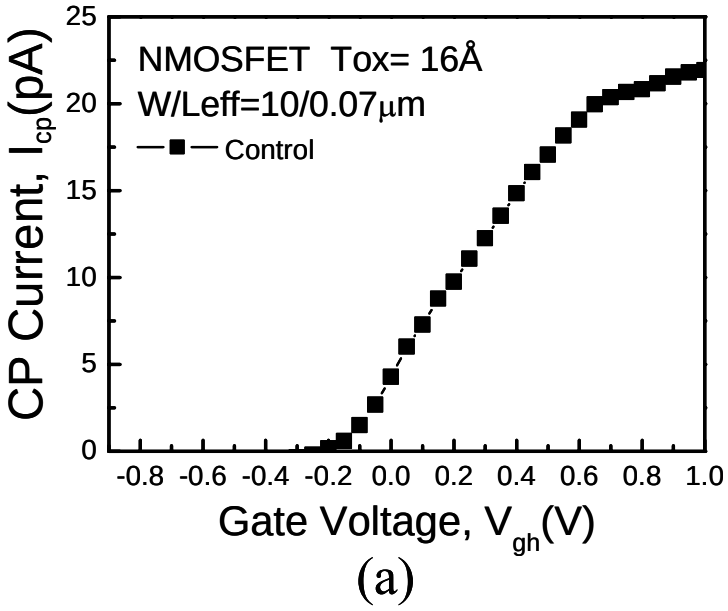
4.4 Analysis of the Distribution of Interface Trap for Strained-Si Devices

In order to identify the Ge out-diffusion effect and understand the distribution of interface trap between the strained-Si/SiGe interface and gate oxide/strained-Si interface, we use the characteristic about the two-level saturation charge pumping current of strained-Si device and the traps profiling method based on [25] to plot the lateral profiling of interface traps in strained-Si devices.

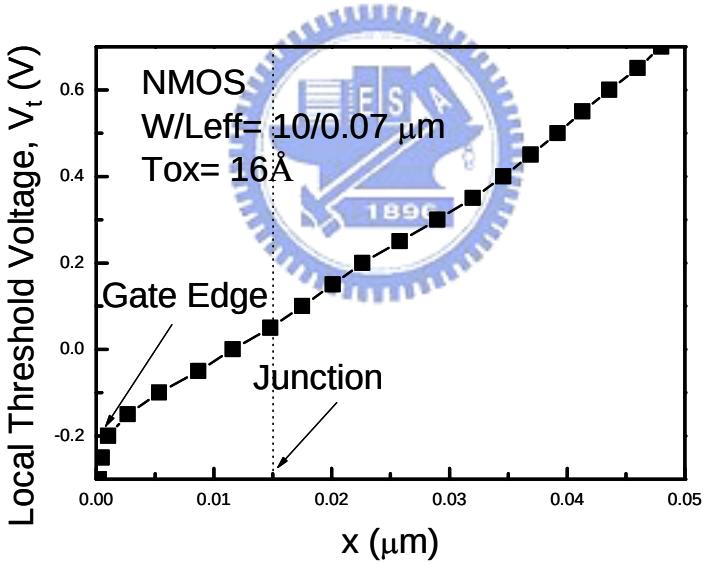
According to the Charge pumping current (Fig. 4.12(a)), we can get the local threshold voltage distribution. We select the $I_{cp,max}$ at $V_{gh=}$ 0.5V and use Eq. (4.1) to calculate the relation figure of x(the position of the channel length)-V_t(local threshold voltage), as in Fig.4.12(b), i.e.,

$$\frac{dV_{gl}}{dx} = \frac{dV_T(x)}{dx}. \qquad (4.1)$$

In Fig. 4.13, curve 1 and curve 2 show the charge pumping current for Bulk Si device and Strianed-Si devices. Because the effective length we have chosen are short length about 0.07 μm, the strained-Si threshold voltage is smaller than that of bulk Si device about 0.02mV. This is because the band alignments in the strained Si/SiGe structure result in a threshold voltage shift in strained-Si device with respect to the



(a)



(b)

Fig. 4.12 (a) Charge pumping current with correction for control device (bulk).
(b) Local threshold voltage distribution for control device (bulk).

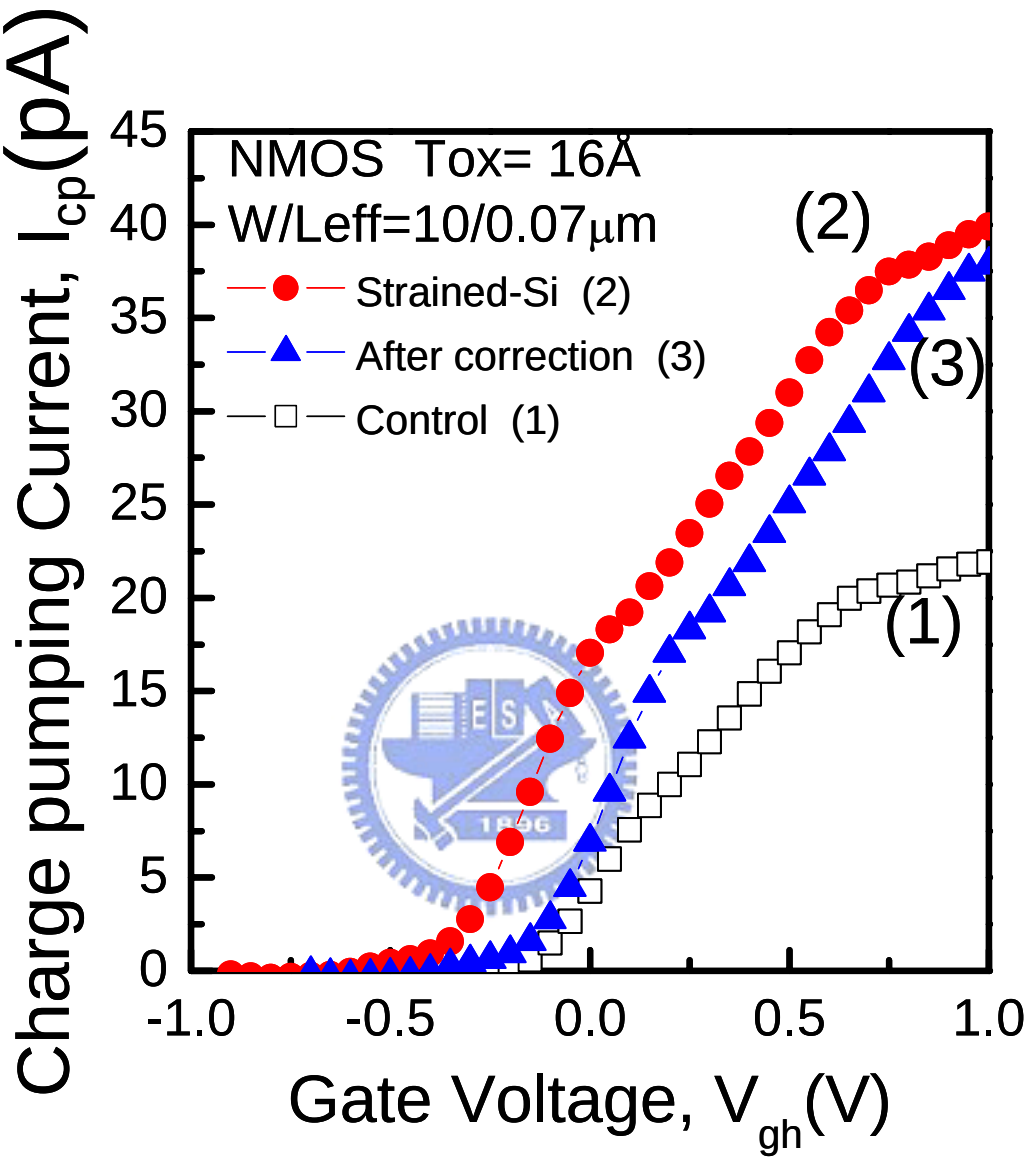


Fig. 4.13 Measured I_{cp} currents for control(bulk)(1), strained-Si device(2), and after correction(3).

conventional Si device. We suppose that the energy gap both of bulk Si device and strained-Si device are almost the same, in which we can find the difference between both device energy gaps is small from figure 3.11 presented above and the influence of oxide trap for both devices are also almost the same. So, we adjust the charge pumping curve of strained-Si device to confirm the V_T distribution of bulk Si device, let the current curve of both devices be the same function of V_{gh}. The curve after the correction is given in Fig. 4.13 with curve 3.

In accordance with Eq. (4.2) and Eq. (4.3), we calculate the vale of $d\triangle I_{cp}$ and dV_{gh}/dx to obtain the $N_{it}(X)$ distribution, where

$$\Delta I_{cp} = qfW \int_0^X N_{it}(x)\,dx \tag{4.2}$$

and

$$N_{it}(x) = \frac{1}{qfW}\frac{d\Delta I_{cp}}{dV_{gl}}\frac{dV_{gl}}{dX}. \tag{4.3}$$

We adopt the method for n-type and p-type strained-Si devices and then we obtain the lateral profiling of interface traps $N_{it}(x)$, as in Fig. 4.14. Similarly, results have been shown for p-MOSFETs with different Ge composition. To identify the observed Si/Ge interface effect, we see that in nMOSFET (1) the interface traps are more pronounced at the drain junction region of SiO_2/Si interface and near the channel center with the interface traps in Si/SiGe interface, (2) the interface traps in Si/SiGe interface is smaller than that in SiO_2/Si interface, and (3) it has a larger generate N_{it} which may be the result of Ge out-diffusion since n-channel exhibits a much larger strain.

4.5 Summary

In this chapter, we analyze the temperature dependence of hot carrier degradation

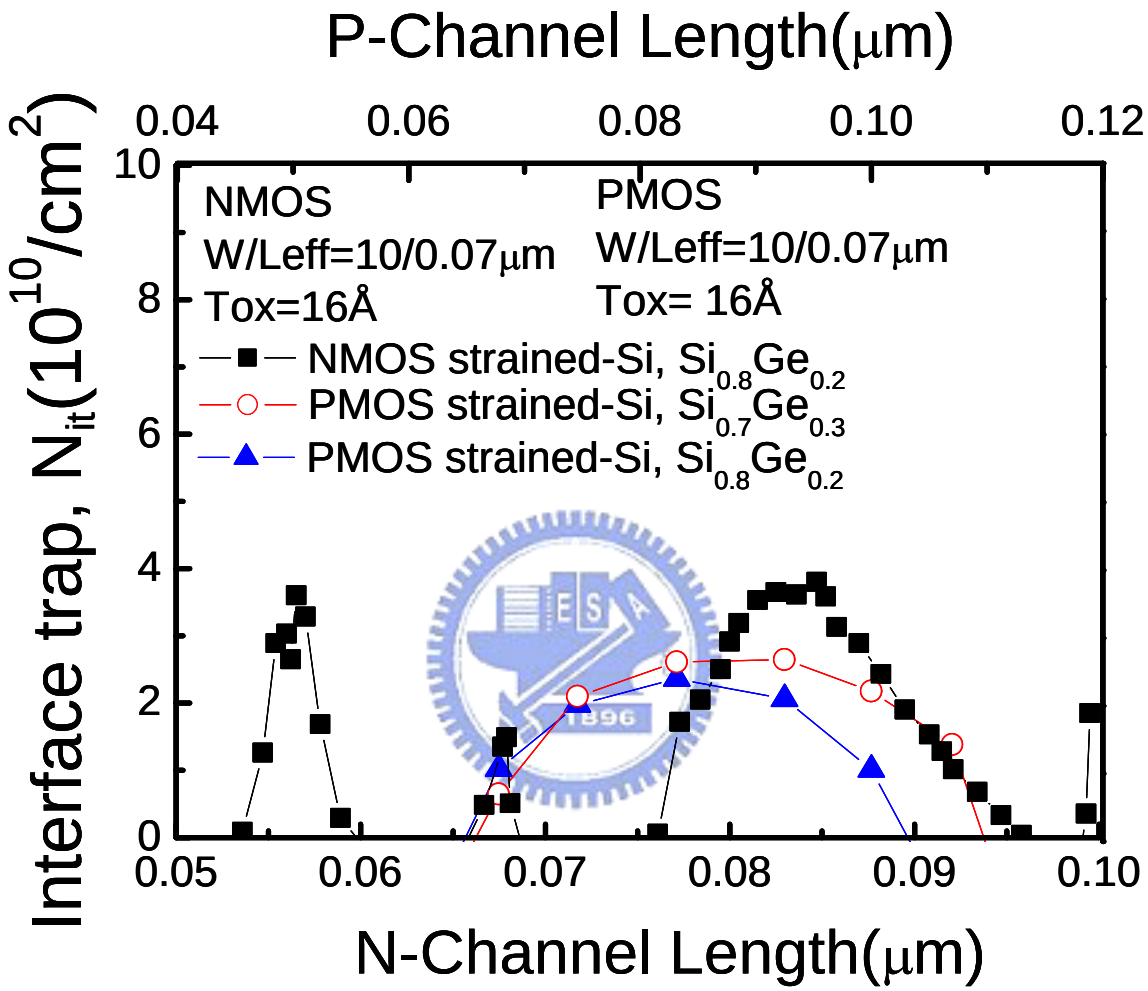


Fig. 4.14 Calculated Si/SiGe interface generated N_{it} distribution for both n- and p-MOSFET's along the device channel.

for strained-Si device compared with bulk Si devices. We have investigated that the temperature dependent hot carrier degradation is more severe in bulk Si devices. Besides, advanced analysis for different Ge content and thickness of Si layer is proposed. We conclude that denser Ge content and deeper thickness of Si layer make more severe degradation after the stress since the either methods has a larger strain. Finally, we use the lateral profiling method to probe the distribution of interface traps in strained-Si device and find that interface traps are more pronounced at the drain junction region of SiO_2/Si interface and near the channel center with the interface traps at the Si/SiGe interface.

Chapter 5
Summary and Conclusion

In order to realize high-speed scaled CMOS devices for logic applications, short channel NMOS devices incorporating thin strained-Si surface channels, which can enhance electron mobility, have evolved as a potential candidate for high speed and low power logic CMOS technologies.

First, we discussed the basic characteristic of strained device and found the two level behavior of the charge pumping current of the devices. Charge pumping method has been employed to the reliability study of devices. We reported that the hot carrier degradation was enhanced by a high lateral acceleration and band gap narrowing in strained-Si devices. The worst case of hot carrier degradation in short channel strained-Si devices occurs at $V_G=V_D$ stress condition and the degradation will follow the trend of impact ionization rate and effective mobility. Therefore, even in strained-Si devices, hot carrier degradation is crucial for developing next generation logic devices.

Then, the results on the temperature dependence hot carrier degradation have been studied. Although the degradation of strained-Si device is larger than bulk device similar to room temperature case, we also found that the temperature dependence hot carrier degradation for strained device is less sensitive to an increase of temperature compared with bulk device. Moreover, advanced analysis for different Ge content and thickness of SiGe layer is proposed. We know that the more strain induces larger degradation from experiment results. Finally, we used the lateral profiling method to clarify the distribution of interface traps in strained devices and found a larger generated N_{it} since strained-Si device exhibits a much larger strain. Therefore, from

reliability test results, the reliability is an important issue for strained device, which needs further improvement.

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