Chapter 3.

Device Structure, Simulation, and Fabrication

3-1. Pattern-dependent MILC（PDMILC）TFT

Structure and Simulation

In this work, a series of Ni-MILC poly-Si TFTs were fabricated, including one with a single-gate length of 5 um and a single-channel width of 1 um (G1S1)、one with a single-gate length of 5 um and a two strips of 0.5 um wire channels (G1M2)、one with a single-gate length of 5 um and a five strips of 0.18 um wire channels (G1M5)、one with a single-gate length of 5 um and ten strips of 84 nm wire channels (G1M10)、one dual-gate, each gate with a length of 2.5 um and ten strips of 84 nm wire channels (G2M10)、one three-gate, each gate with a length of 1.7 um and ten strips of 84 nm wire channels (G3M10)、one four-gate, each gate with a length of 1.25 um and ten strips of 84 nm wire channels (G4M10), as listed in Table 3-1. Figure 3-1a presents the schematic plot and figure 3-1b presents the top-view of G2M10 Ni-MILC poly-Si TFT with source, drain, nanowire channels, a Ni-MILC seeding window and a dual–gate. Figure 3-2 presents the cross-sectional view of Ni-MILC poly-Si TFT, with a conventional top dual-gate, self-aligned offset MOSFET structure. Figure 3-3 presents the direction of metal induced lateral crystallization. As the anomalous

off-current (leakage current) in the poly-Si TFTs is related to the lateral electrical field in the channel. Figure 3-4 presents the simulation results obtained using an ISE TCAD 2-D device simulator of the lateral electrical field of the single-gate (G1) and dual-gate (G2) TFTs with the same device dimension and bias condition. The peak lateral electrical field (E_m) of the dual-gate TFT is lower than that of the single-gate TFT, indicating that the dual-gate (G2) structure effectively reduces the leakage current of poly-Si TFTs.

3-2. Fabrication of Pattern-dependent MILC TFT

In this experiment, the PDMILC TFTs device layout and top view with standard four masks are shown in figure 3-1a、figure 3-1b, and the cross sectional view of devices with conventional top-gate structure is shown in figure 3-2.

The fabrication procedure is described as follows.

Step1. Substrate.

6-inch p-type single crystal silicon wafers with (100) orientation were used as the starting materials. After an RCA initial cleaning procedure. Si wafers were coated with 400-nm-thick thermally grown SiO_2 in steam oxygen ambient at 1000°C.

Step2. Active region formation (Mask1).

Uundoped 50nm-thick amorphous-Si layer were deposited by low-pressure chemical vapor deposition (LPCVD) on buried oxide by pyrolysis of silane (SiH_4)

at 550°C. The active islands (mask1), including source, drain and channel with different dimension were patterned by Electron Beam (Ebeam) lithography and transferred by reactive ion etching (RIE).

Step3. Gate oxide formation

After defining the active region, the wafers were boiled in H_2SO_4 + H_2O_2 to ensure cleanliness of the wafers before deposition. A buffered HF dip was performed to remove the native oxide on the silicon surface. Soon, the gate insulator was deposited in a horizontal furnace using TEOS and O_2 gases at 700°C. The thickness of the TEOS oxide thin film is 50 nm.

Step4. Gate electrode formation (Mask2).

After deposition of gate oxide, 150 nm-thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD at 620 °C. The poly-Si layers were patterned by Ebeam lithography and transferred by RIE to define the gate electrode and to be the mask for self-aligned implantation.

Step5. MILC window and contact hole (Mask3).

After gate formation, a 100nm-thick TEOS oxide layer as passivation layer was deposited by LPCVD. Then, we define the MILC window and contact hole with the same mask (as shown in figure 3-1a and figure 3-1b).

Dopants were activated by rapid thermal annealing (RTA) at 780 ºC for 60 sec.

Step6. Metal induced lateral crystallization

Then, a thin 10nm-thick nickel (Ni) layer was deposited by physical vapor

deposition (PVD). The MILC crystallization was carried out at 550°C for 48hrs in an N_2 ambient. After long time annealing, the unreacted nickel on passivative TEOS oxide were removed by H_2SO_4 solution

Step7. Self-aligned offset Source/drain formation.

Phosphorus ions at a dose of 5×10^{15} cm^{-2} were implanted to form the n^+ gate, source/drain regions and the self-aligned offset region were formation in the same process step (as shown in Fig. 3-1b).

Step8. Metallization.

The 300nm-thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned for source, drain and gate metal pads. Finally, the finished devices were sintered at 400°C for 30 minutes in an N_2 ambient.

3-3. Fabrication results of Pattern-dependent MILC TFT

Figure 3-5~8 shows SEM image of active region PDMILC TFT of G1M10, G2M10, G3M10, and G4M10 respectively. In this thesis we have two main topics to be discussed in section 4-1 and section 4-2. They are the results from different processes. In section 4-1, the active region SEM photography of G1M10 is shown at figure 3-9. The each nanowire width is 67nm. In section 4-2, the active region SEM photography of G1M10 is shown at figure 3-10. The each nanowire width is 84nm. These different nanowire widths come from the critical dimension (C.D.) variation in lithography.