Table 3-1 Devices dimension of all proposed Ni-PDMILC poly-Si TFTs.

Device name	Gate number	Each gate length (L)	Total gate length (L_{eff})	Channel number	Each channel width (W)	Total channel width (W_{eff})
G1S1	1	5 um	5 um	1	1 um	1 um
G1M2	1	5 um	5 um	2	0.5 um	1 um
G1M5	1	5 um	5 um	5	0.18 um	0.9 um
G1M10	1	5 um	5 um	10	84 nm	0.84 um
G2M10	2	2.5 um	5 um	10	84 nm	0.84 um
G3M10	3	1.7 um	5 um	10	84 nm	0.84 um
G4M10	4	1.25 um	5 um	10	84 nm	0.84 um

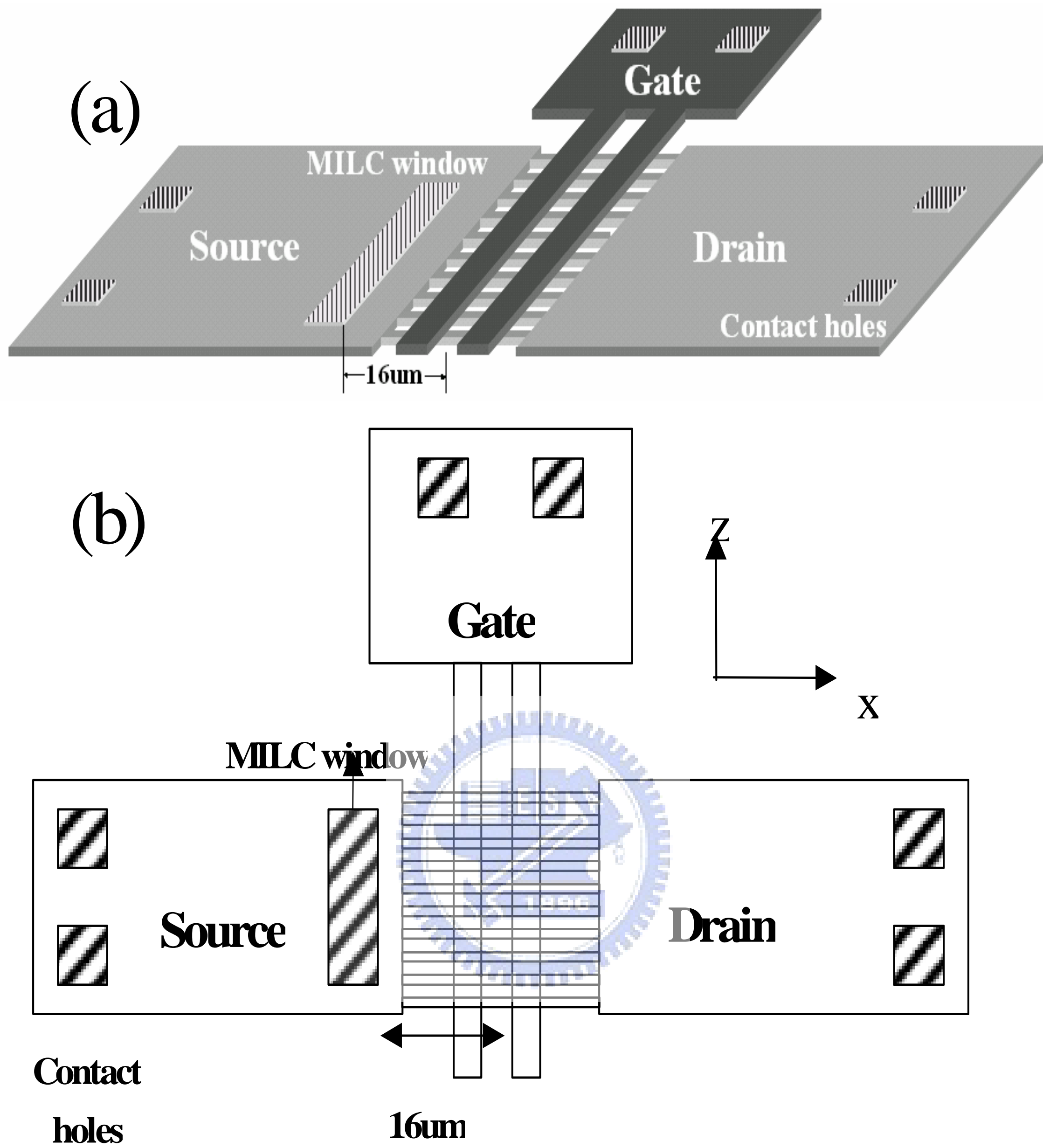

Fig.3-1 (a) Schematic diagram of proposed G2M10 Ni-MILC poly-Si TFT. (b) Topview of Fig. 3-1a.

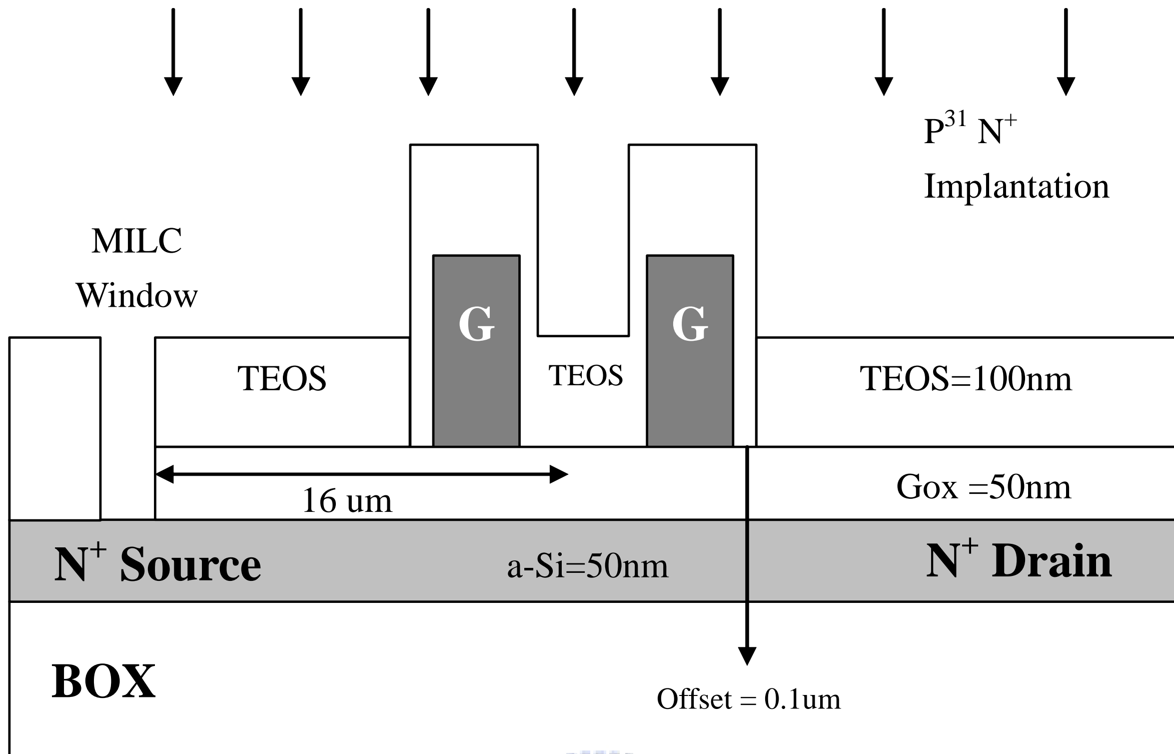

Fig.3-2 Cross-section view of Ni-MILC poly-Si TFT, which was a conventional top-gate, self-aligned offset MOSFET structure.

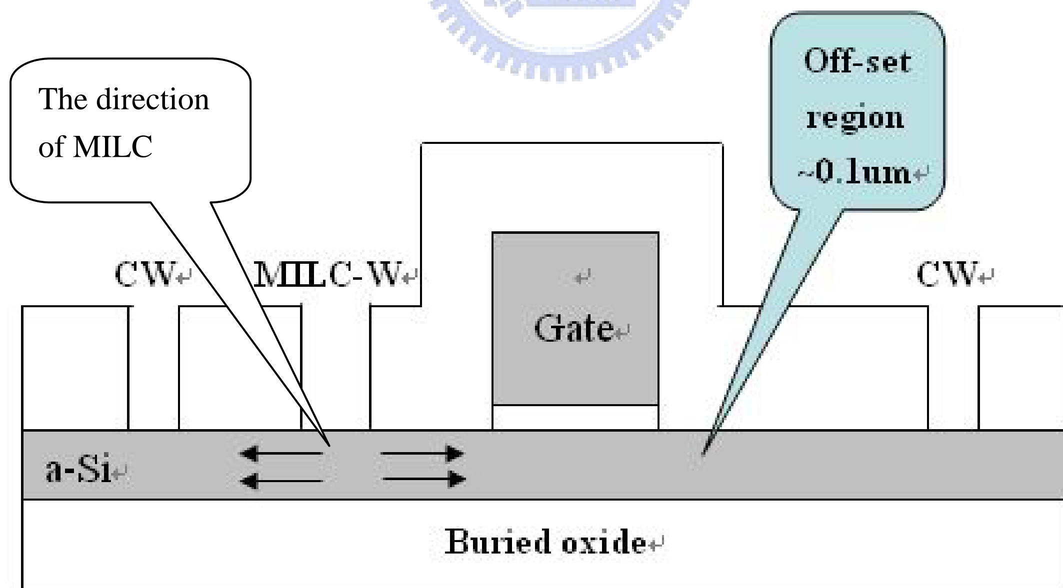

Fig.3-3 the direction of metal induced lateral crystallization

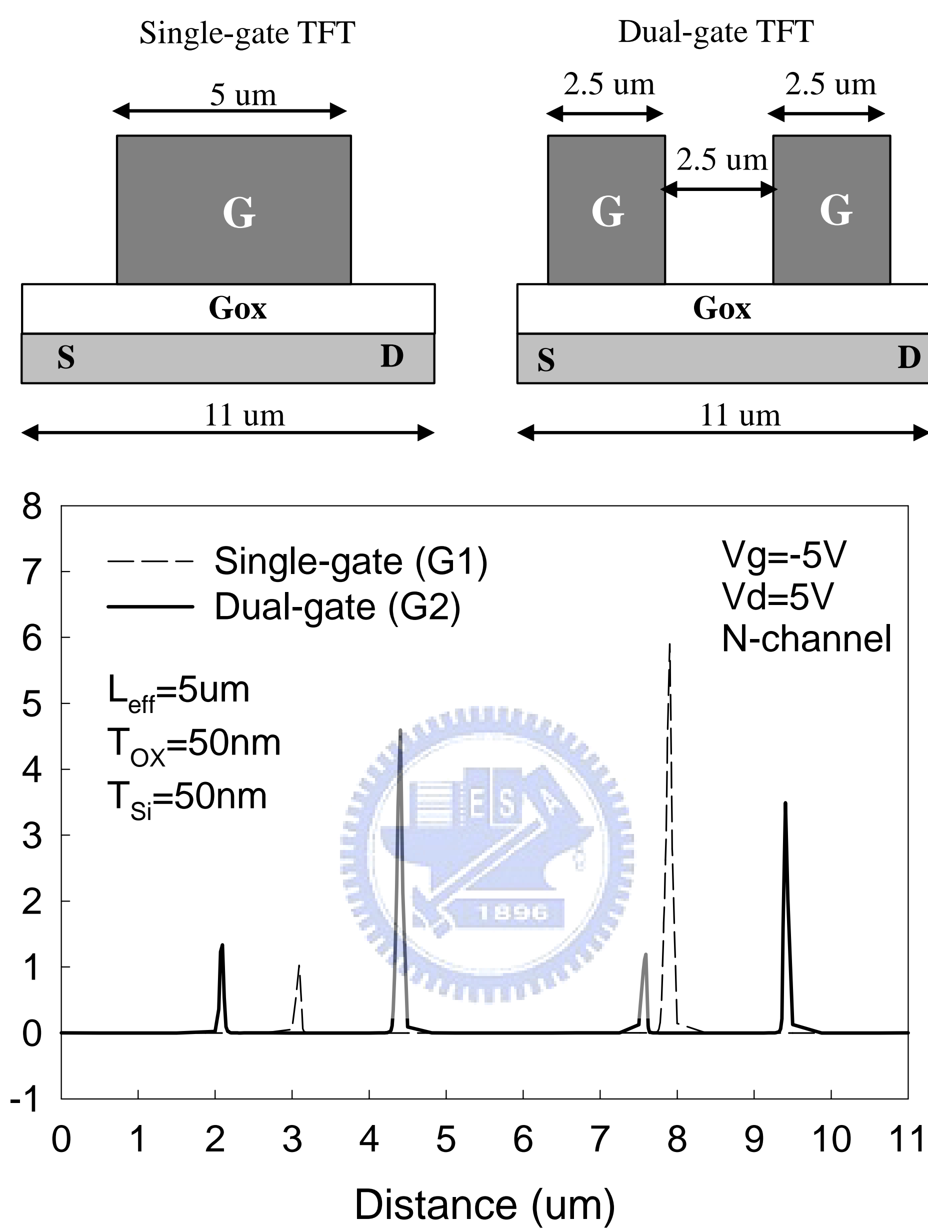

Fig. 3-4 Off-state electrical field simulation results of single-gate and dual-gates poly-Si TFT b y ISE TCAD v. 7(a 2-D device simulator).

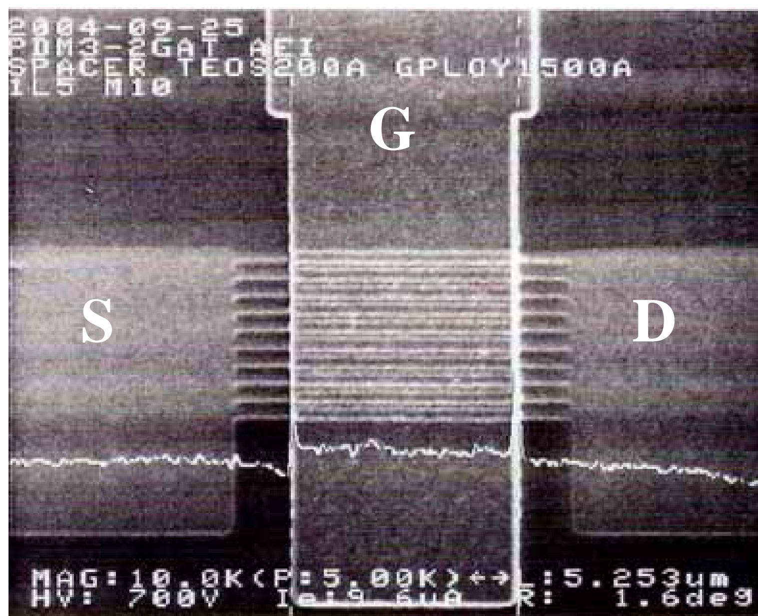

Fig. 3-5 SEM photography of G1M10 TFT active pattern with multiple nanowire channels, and one-gates. The gate length is about 5um.

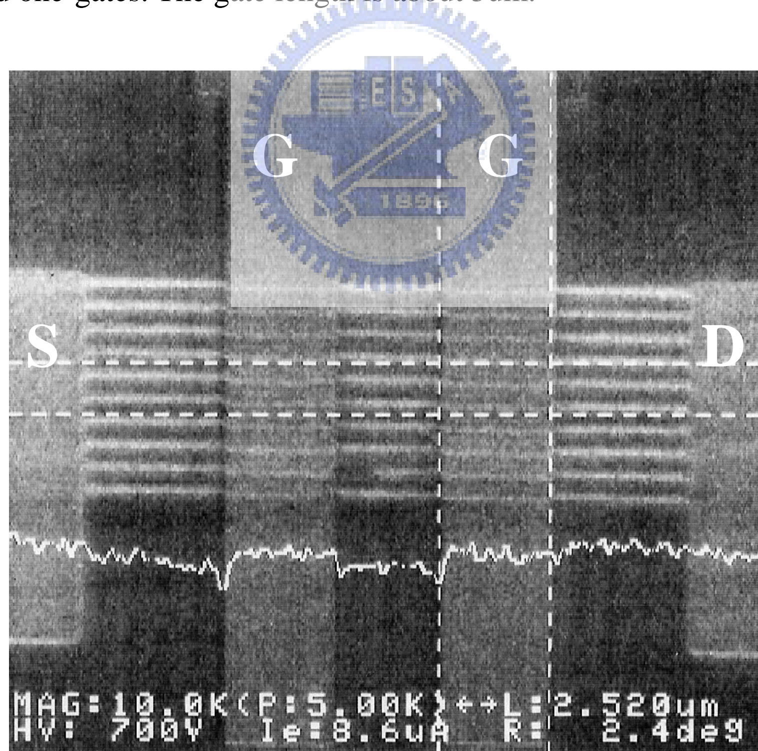

Fig. 3-6 SEM photography of G2M10 TFT active pattern with the source, the drain, multiple nanowire channels, and two-gates. The each gate length is about 2.5um

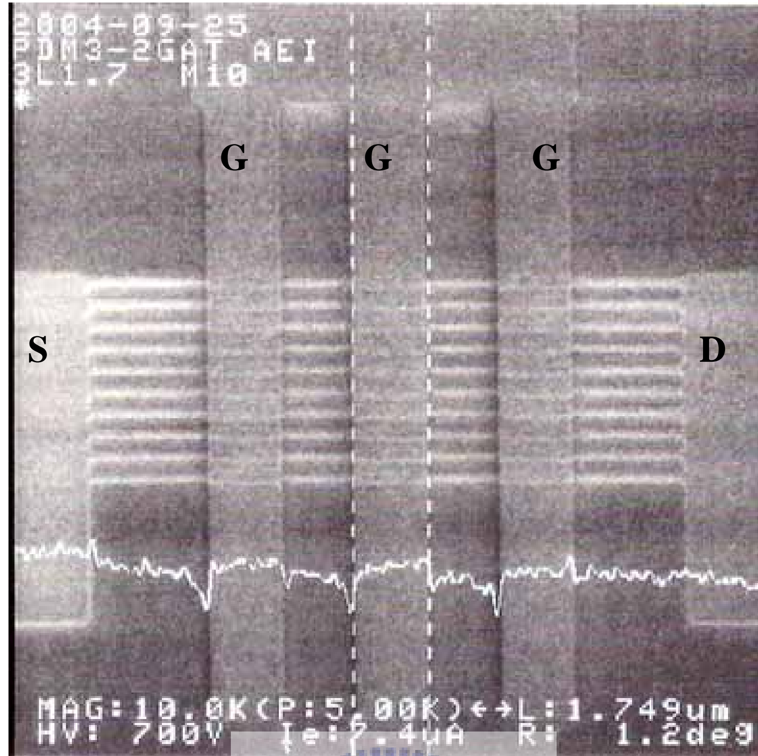

Fig. 3-7 SEM photography of G3M10 TFT active pattern with multiple nanowire channels, and one-gates. The gate length is about 1.7um.

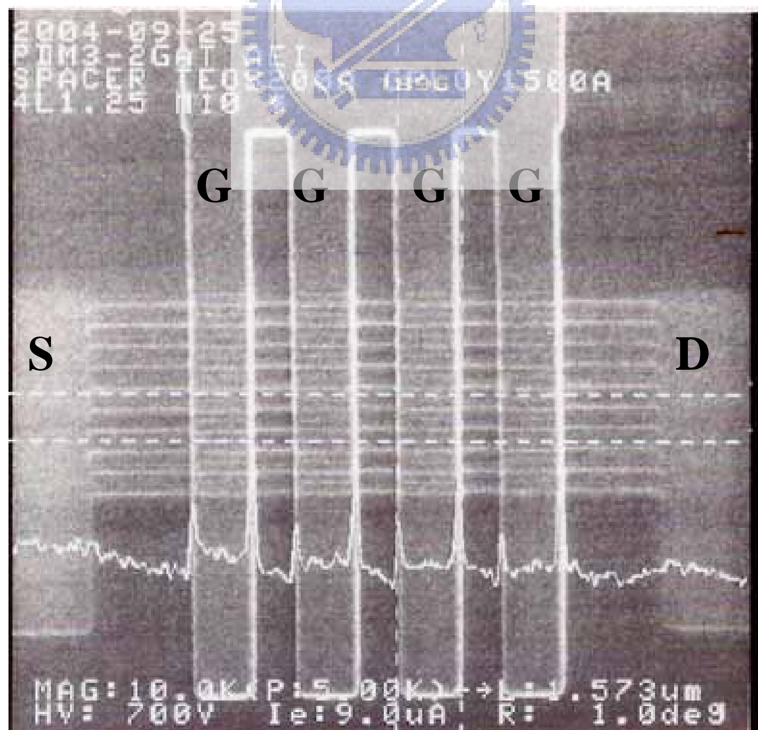

Fig. 3-8 SEM photography of G4M10 TFT active pattern with multiple nanowire channels, and one-gates. The gate length is about 1.25um.

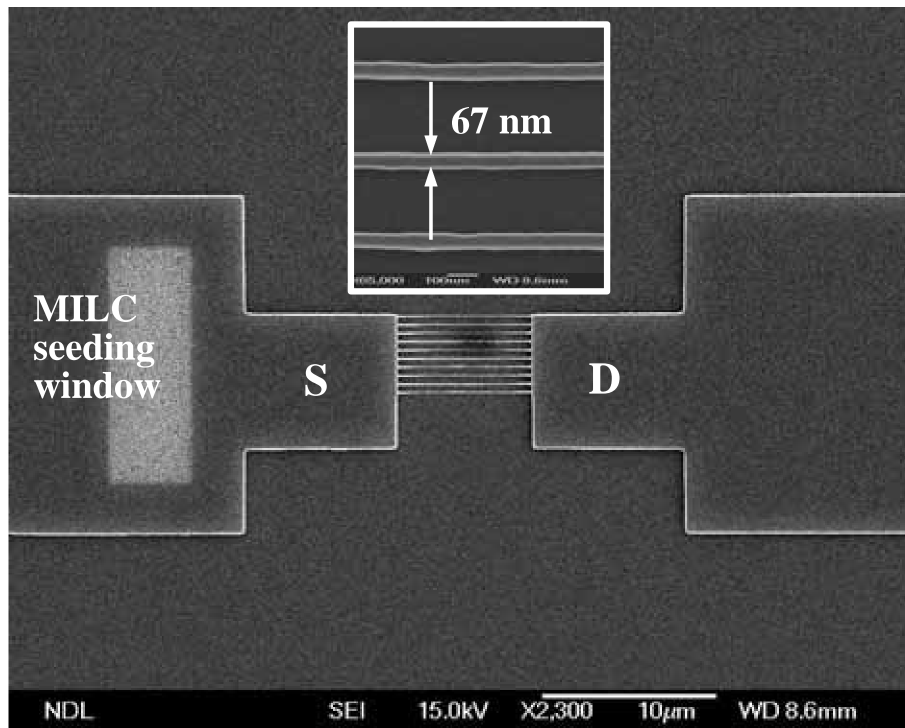

Fig. 3-9 Scanning electron microscopy (SEM) photography of active pattern with the source, the drain, ten nanowire channels and MILC seeding window. The inset plot shows the each nanowire width of 67 nm.

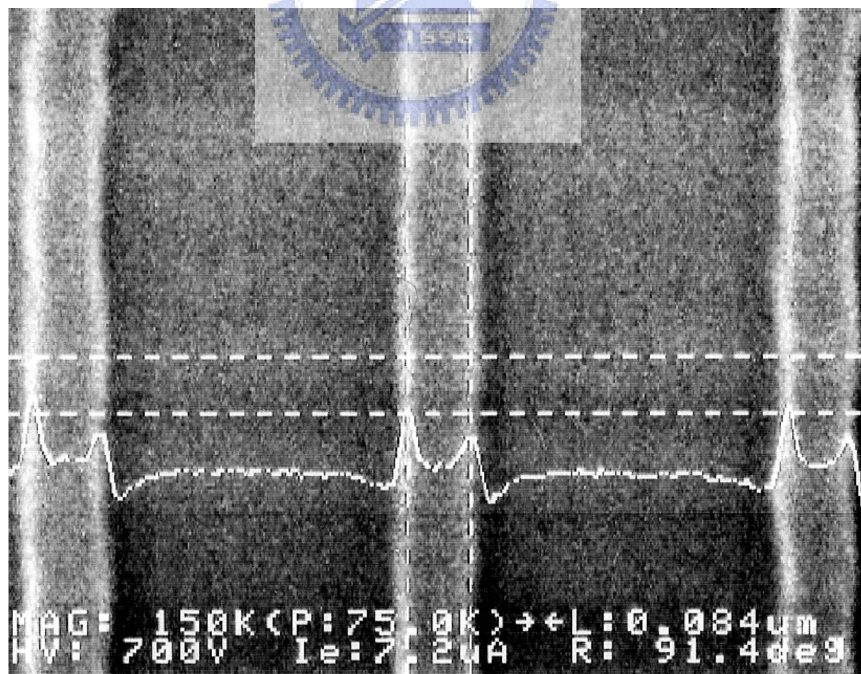

Fig. 3-10 Magnified area of multiple nanowire channels. The each nanowire width is 84 nm.