Chapter 4

Results and Discussion

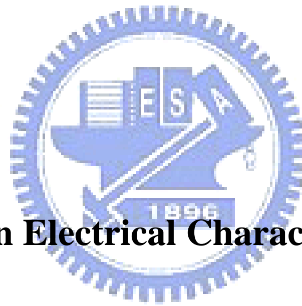
4-1. Effects of channel width and NH_3 Plasma Passivation on Electrical Characteristics

Figure 4-1-1 presents a after etching investigation (AEI) scanning electron microscope (SEM) photograph of the poly-Si active region of the M10 TFT, including the source, the drain, ten multiple nanowire channels and MILC seeding window. Inset plot presents a magnified area of the multiple nanowire channels in the M10 TFT, each of which is 67-nm-wide. Figure 4-1-2 presents SEM photograph of the MILC poly-Si grains in active region of the proposed TFTs. The average grain size in the polysilicon channel formed by MILC is approximately 250 nm. Figure 4-1-3, figure 4-1-5, figure 4-1-7, and figure 4-1-9 show that the PDMILC TFTs that has undergone NH_3 plasma passivation outperforms and that without NH_3 plasma passivation. The former has higher field effect mobility (μ_{FE}), higher *ON/OFF* ratio, lower threshold voltage (V_{th}), lower subthreshold slope (*SS*) and lower drain-induced barrier lowering (*DIBL*). Figure 4-1-4, figure 4-1-6, figure 4-1-8, and figure 4-1-10 show that the PDMILC TFT that had undergone NH_3 plasma passivation has higher output current than that without NH_3 plasma passivation. In particular, the M10 PDMILC TFT has the highest output current, because it has the highest μ_{FE}. Table

4-1-1 lists all the parameter of the PDMILC poly-Si TFTs, including μ_{FE}, the *ON/OFF* ratio, the V_{th}, the *SS*, and the grain boundary defects density (N_t). The μ_{FE} is extracted from the linear region ($V_d = 0.1$ V) of transcendence (g_m). The V_{th} is defined as the gate voltage required to yield normalized drain current of I_d / (W/L) = 10^{-7} A at $V_d = 5$ V. The I_{ON} is defined as the maximum drain turn-on current at $V_d = 5$ V. The I_{OFF} is defined as the minimum drain turn-off current at $V_d = 5$ V. Thus, the *ON/OFF* ratio is defined as I_{ON} / I_{OFF}. The device parameters versus multi-channel with different widths are plotted to elucidate the effect of NH_3 plasma passivation on each of the dimensions of PDMILC TFTs. Figure 4-1-11 plots the PDMILC TFTs' μ_{FE} versus the multi-channel with different widths, with and without NH_3 plasma passivation. This curve reveals that NH_3 plasma passivation improves the μ_{FE} of a PDMILC TFT, suggesting that the NH_3 plasma effectively hydrogen-passivated the dangling bonds at the grain-boundary and the pile-up of nitrogen at the SiO2/poly-Si interface. The M10 PDMILC TFT has the highest μ_{FE} of 84.63 cm^2/Vs, because it has a split nanowire structure, which is exposed effectively to an atmosphere of NH_3 plasma. Figure 4-1-12 plots the PDMILC TFTs' *ON/OFF* ratio against the multi-channel with different widths, with and without NH_3 plasma passivation. This curve reveals that the *ON/OFF* ratio of all PDMILC TFTs after NH_3 plasma passivation, except S1 TFT, is increased. NH_3 plasma is effectively passivated on

poly-Si grain boundaries reducing leakage current, which is generated by the thermionic field emission of grain boundary defects in the off-state. Because hydrogen passivated the grain boundary defect states, and the strong Si-N bond formatted to terminate the dangling bonds at the grain boundaries of the poly-Si films. Figure 4-1-13 plots the PDMILC TFTs' V_{th} versus the multi-channel with different widths. After NH_3 plasma passivation, the V_{th} of each TFT device was approximately 4 V lower. NH_3 plasma passivation reduced the barrier height (E_B) of the poly-Si grain boundary, so the electrons can easily overcome E_B, producing a high current and allowing the TFT to be easily turned on. Such a low value of V_{th} of the PDMILC TFTs is appropriate in low-power AMLCD applications. Figure 4-1-14 plots the PDMILC TFTs' subthreshold swing (*SS*) versus the multi-channel with different widths, with and without NH_3 plasma passivation. NH_3 plasma passivation reduces the *SS*, because the pile-up of nitrogen at the SiO2/poly-Si interface is of major importance, while the hydrogen-passivation of the dangling bonds at the grain-boundary is of minor importance. Moreover, *SS* decreases gradually from S1, M2 and M5 to M10 TFT, and M10 TFT has the smallest *SS* of 230 mV/decade. A steep *SS* of M10 PDMILC TFT is desired to facilitate the switching off of the transistor, because M10 exhibits the greatest NH_3 plasma passivation because it has ten split nanowires, most of which are exposed to the NH_3 plasma passivation. The amount of effects of NH_3 plasma

passivation on PDMILC TFTs poly-Si grain boundaries can be evaluated from the by grain boundary defects density (N_t) [1]. Figure 4-1-15 plots extraction curves of N_t of M10 PDMILC TFTs, with and without NH_3 plasma passivation. Figure 4-1-16 plots PDMILC TFTs' N_t versus the multi-channel with different widths, with and without NH_3 plasma passivation. The N_t decreases gradually from S1, M2 and M5 to the M10 PDMILC TFT with the TFTs' channel numbers increasing. Moreover, after NH_3 plasma passivation substantially reduces N_t, providing high electrical performance. In addition, the M10 TFT has the lowest N_t (3.07×10^{12} cm^{-2}), which value is consistent with its best performance.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4-2. Multi-gate Effects on Electrical Characteristics

Figure 4-2-1 and figure 4-2-2 present the simulation results obtained using an ISE TCAD 2-D device simulator of the lateral and total electrical field of the single-gate (G1) and dual-gate (G2) TFTs with the same device dimension and bias condition. The peak lateral electrical field (E_m) of the dual-gate TFT is lower than that of the single-gate TFT, indicating that the dual-gate (G2) structure effectively reduces the leakage current of poly-Si TFTs. Figure 4-2-3 presents E_m versus different gate number TFT structure. The E_m is decreasing with the gate number increasing. Figure 4-2-4 shows scanning electron microscopy (SEM) photography of active pattern with

the source, the drain, ten nanowire channels and dual-gate. The each dual-gate length is 2.5 um. Figure 4-2-5 shows SEM photography of magnified area of multiple nanowire channels. The each nanowire width is 84 nm. Figure 4-2-6 shows SEM photography of MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm.

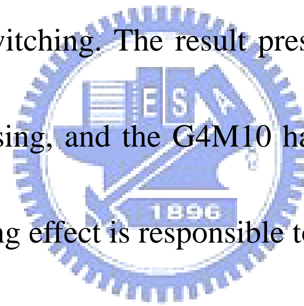
Figure 4-2-7 compares typical transfer curves of all proposed Ni-MILC poly-Si TFTs. Firstly, by compassion of the single-gate with the single-channel (G1S1) and the ten nanowire channels (G1M10) TFTs, the G1M10 has a higher *ON* current, a higher *ON/OFF* ratio and a steeper *SS* than the G1S1. These results reveal that the multiple nanowire channels have fewer defects at grain boundaries [2]. Secondly, by comparison of the single-gate (G1M10) and multi-gate (G2M10, G3M10, and G4M10) with the same ten nanowire channels Ni-MILC poly-Si TFT revealed that the electrical performance was significantly enhanced with the multi-gate increasing. Figure 4-2-8 presents the transfer cure of G4M10 TFT with linear and saturation region. The G4M10 shows superior performance than others TFT, including a low leakage current, a high *ON/OFF* ratio ($>10^7$), a low V_{th}, a steep SS, and a near-free drain-induced barrier lowering *(DIBL)*.

Figure 4-2-9 compares the output curves of all proposed Ni-MILC poly-Si TFTs with the same gate length (L) of 5 um. The kink-effect of multi-gate (G2M10, G3M10

and G4M10) is suppressed relative to those of the other TFTs (G1S1 and G1M10). Consequently the multi-gate structure effectively reduces the lateral electrical field (figure 4-2-3), reducing the impaction ionization in the active channel of the Ni-MILC poly-Si TFT.

Figure 4-2-10 presents the leakage current and *ON/OFF* ratio versus different structure TFTs. The leakage current is defined as the drain current at V_d = 5 V and V_g = -7 V, and the *ON/OFF* ratio is defined as the maximum drain current value of I_{ON} / I_{OFF} at V_d = 5 V. For single-gate TFT, by applying nanowire channels (G1M10), the low leakage current can be achieved due to the lower defects at grain boundaries than single-channel TFT (G1S1). Moreover, by comparison of the single-gate (G1M10) and multi-gate (G2M10, G3M10, and G4M10) with the same ten nanowire channels Ni-MILC poly-Si TFT revealed that the leakage current was significantly decreasing with and the *ON/OFF* ratio was increasing with the multi-gate increasing, the G4M10 has lowest leakage current of 5.12×10^{-12} A and highest *ON/OFF* ratio of 1.81×10^{7}. These findings reveal that the multi-gate structure can reduce the peak lateral electrical field in the drain depletion region. Therefore, the leakage current that arises from the field emission of carriers through the poly-Si grain traps and the defects associated with Ni contamination was reduced. This finding is consistent with the simulation value of the lateral electrical field of multi-gate TFT in figure 4-2-3.

Figure 4-2-11 presents the V_{th} and *SS* versus different structure TFTs. The V_{th} is defined as the gate voltage to yield the normalized drain current of $I_d/(W/L)$ equal to 10^{-7} A at V_d = 5 V. By comparison of G1S1 and G1M0 TFT, the V_{th} is reduced by applying the ten nanowire channels structure. The result reveals that the ten nanowire channels structure has fewer defects at grain boundaries than single-channel [2]. Moreover, the V_{th} further decreases with the multi-gate structure applying, and the G4M10 has lowest V_{th} of – 0.41 V. The results reveal that the multi-gate structure has gate length-shortening effect for early turning on the TFT. The *SS* is describable for the capability of transistor switching. The result presents that the *SS* decreases with the multi-gate number increasing, and the G4M10 has lowest *SS* of 0.44 V/dec. For the same gate length-shortening effect is responsible to the *SS* lowering. Figure 4-2-12 presents the effect of Drain Induced Barrier Lowing (*DIBL*) versus different structure TFTs. The result can be presented that the multi-gate structure reduces the lateral field, thus the effect of *DIBL* reduces with the gate number of multi-gate increased. Figure 4-2-13 shows that the field effect mobility versus different multi-gate structure Ni-PDMILC poly-Si TFTs. The field effect mobility decrease with multi-gate number increasing. These results reveal that the multi-gate structure let the additional series channel resistance increased



4-3. Reliability of Multi-gate PDMILC TFT under Static Stress

Figure 4-3-1 presents a series of G1M10 TFT transfer curves after different hot-carrier stress conditions with 1000-second duration. Until the extreme hot-carrier stress condition at V_d = 45 V and V_g = 22.5 V, only the transfer curves of G1M10 TFT has degradation. Figure 4-3-2 presents the degradation in MILC and SPC of G1M10 TFT transfer curves before and after hot-carrier stress with 1000-second duration These results reveal that the ten nanowire channels structure of Ni-MILC TFT has more excellent hot-carrier immunity and has more capability in high-voltage application than that in SPC TFT. The similar hot-carrier stress results are also found in others multi-gate with ten nanowire channels Ni-MILC TFT. Figure 4-3-3 to Figure 4-3-6 show the electrical characteristic in $\Delta G_m max$ / $G_m max$, ΔI_{on} / I_{on}, *ON/OFF* ratio, and Vth versus different PDMILC with multi-gate and ten nanowire structure after different hot-carrier stress conduction with 1000-second duration. The detail mechanism of the multi-gate Ni PDMILC TFTs' reliability after static stress is under investigation. We will keep studying in our future work.