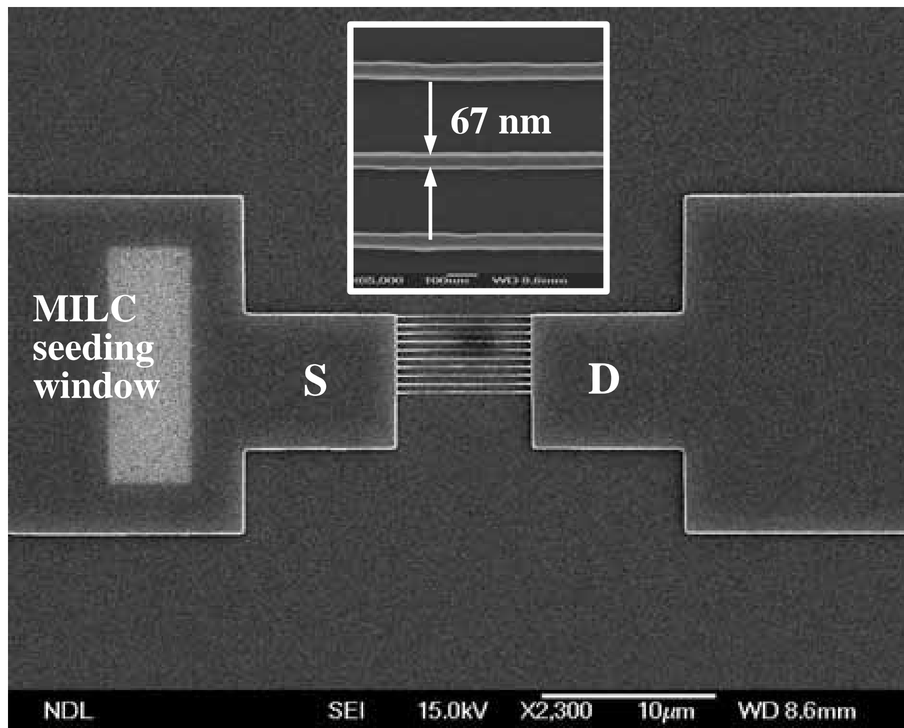

Fig. 4-1-1 Scanning electron microscopy (SEM) photography of active pattern with the source, the drain, ten nano-wire channels and MILC seeding window. The inset plot shows the each nano-wire width of 67 nm.

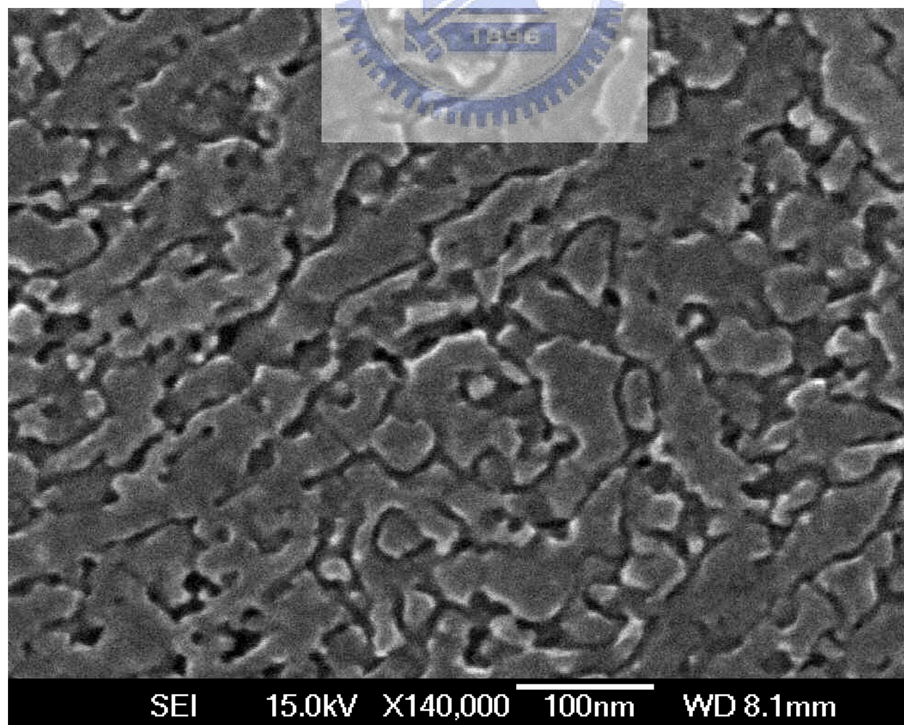

Fig.4-1-2 SEM photography of MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm.

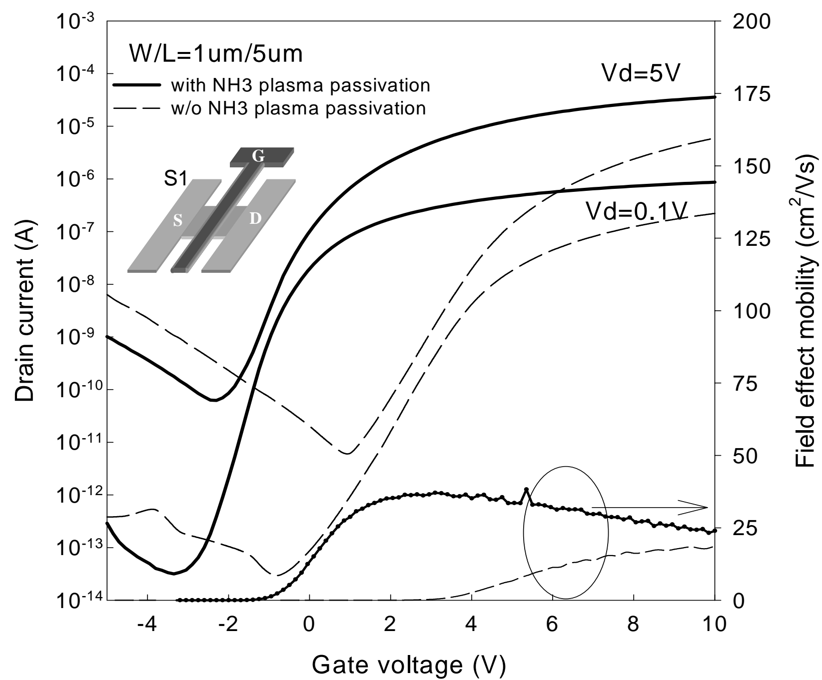

Fig. 4-1-3 Device characteristics of S1 (W / L = 1 um / 5 um) PDMILC poly-Si TFT transfer I_d - V_g curve with (solid-line) and without (dash-line) NH_3 plasma passivation.

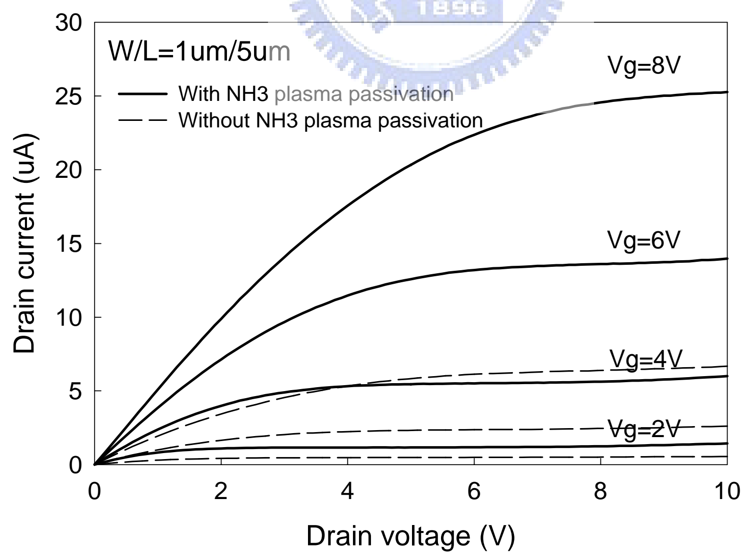

Fig. 4-1-4 Device characteristics of S1 (W / L = 1 um / 5 um) PDMILC poly-Si TFT output I_d - V_d curve with (solid-line) and without (dash-line) NH_3 plasma passivation.

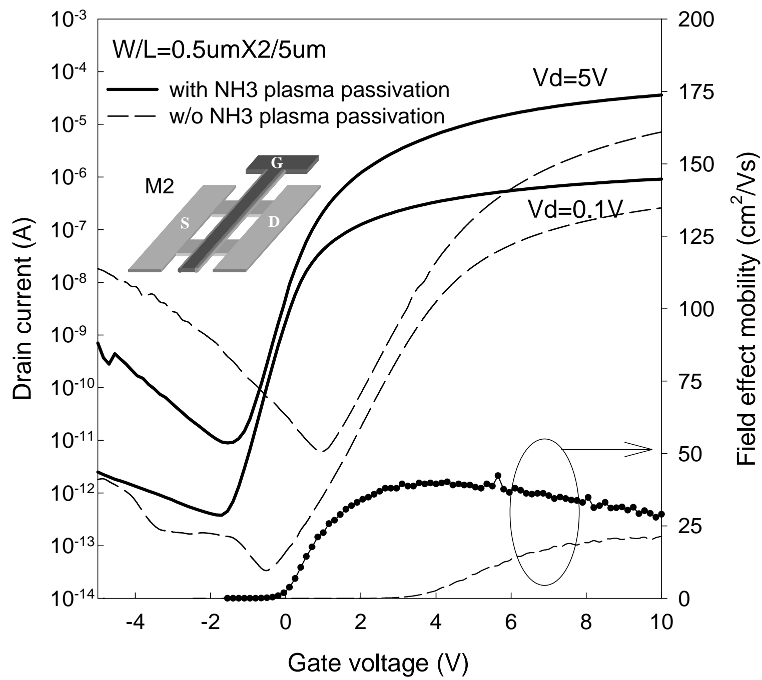

Fig. 4-1-5 Device characteristics of M2 (W / L = 0.5 um × 2 / 5 um) PDMILC poly-Si TFT transfer I_d - V_g curve with (solid-line) and without (dash-line) NH3 plasma passivation.

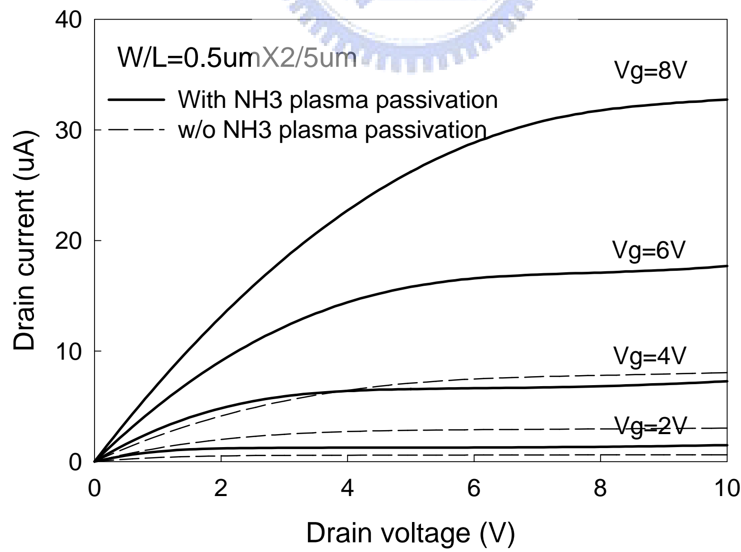

Fig. 4-1-6 Device characteristics of M2 (W / L = 0.5 um × 2 / 5 um) PDMILC poly-Si TFT output I_d - V_d curve with (solid-line) and without (dash-line) NH3 plasma passivation.

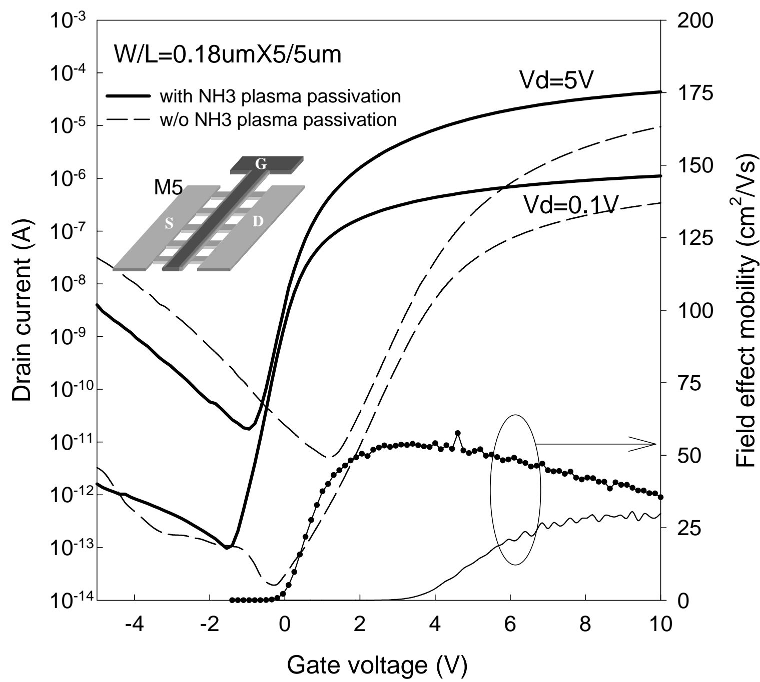

Fig. 4-1-7 Device characteristics of M5 (W / L = 0.18 um × 5 / 5 um) PDMILC poly-Si TFT, transfer I_d - V_g curve with (solid-line) and without (dash-line) NH_3 plasma passivation.

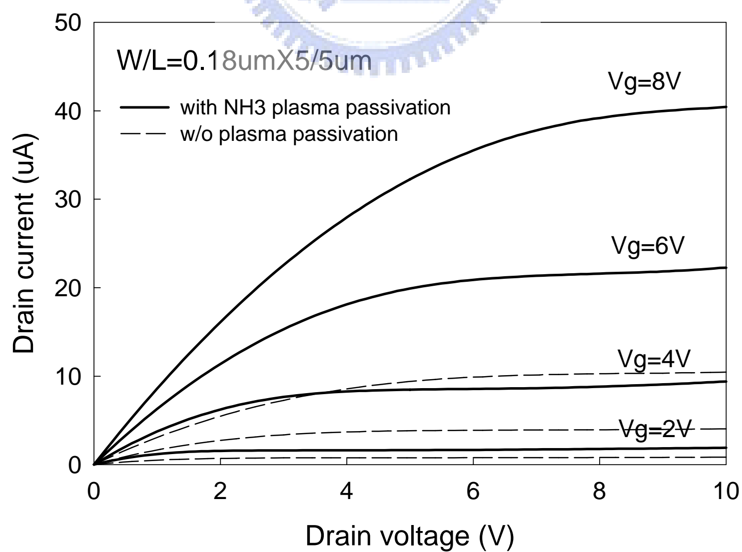

Fig. 4-1-8 Device characteristics of M5 (W / L = 0.18 um × 5 / 5 um) PDMILC poly-Si TFT, output I_d - V_d curve with (solid-line) and without (dash-line) NH_3 plasma passivation.

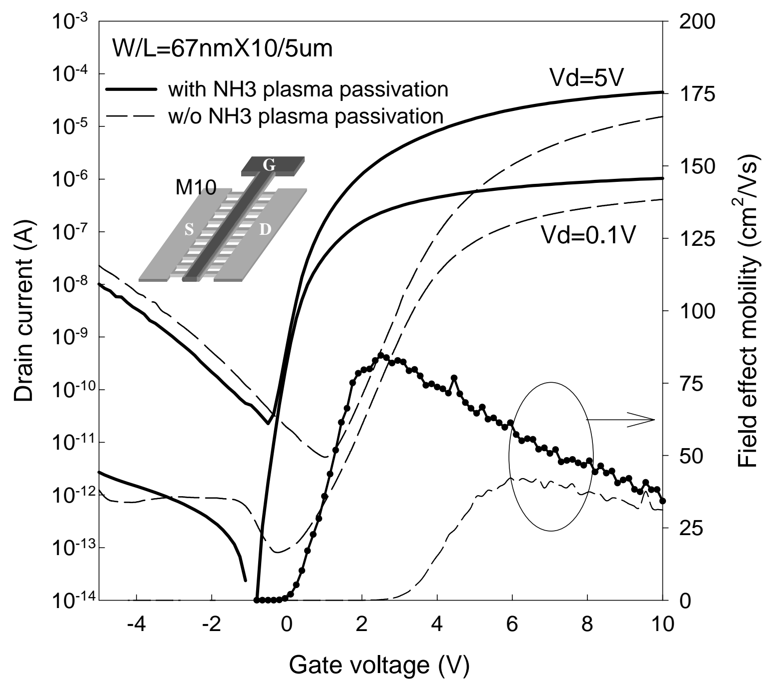

Fig. 4-1-9 Device characteristics of M10 (W / L = 67 nm × 10 / 5 um) PDMILC poly-Si TFT, transfer I_d - V_g curve with (solid-line) and without (dash-line) NH_3 plasma passivation.

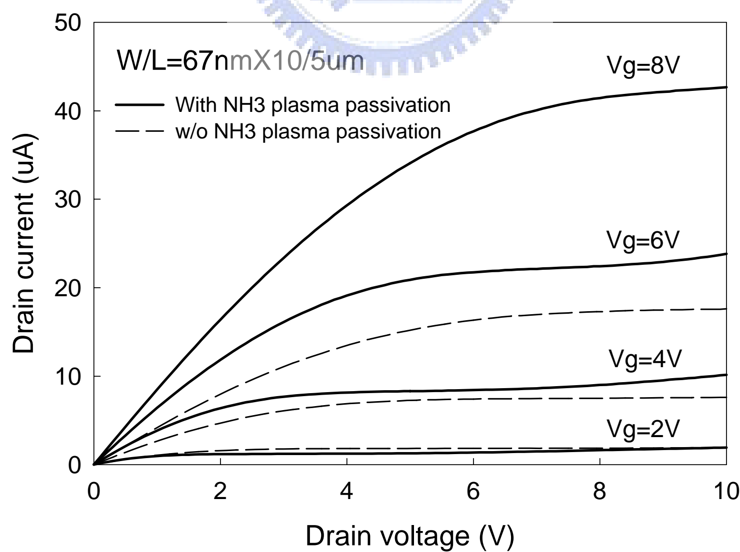

Fig. 4-1-10 Device characteristics of M10 (W / L = 67 nm × 10 / 5 um) PDMILC poly-Si TFT, output I_d - V_d curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.

Table 4-1-1. Device parameters of PDMILC TFTs with the same L = 5 um at different widths. All parameters were extracted at V_d = 5 V, except for the field-effect mobility (μ_{FE}) which were extracted at V_d = 0.1 V.

Device name	NH3-plasma passivation	μ_{FE} (cm^2/VS)	V_{th} (V)	SS (V/dec.)	I_{ON} / I_{OFF} $\times 10^6$	N_t $\times 10^{12}$ (cm^{-2})
S1	w/o	18.11	4.79	0.80	2.93	10.60
	with	38.25	0.31	0.48	1.87	3.66
M2	w/o	21.39	4.70	0.78	1.15	9.87
	with	42.37	0.27	0.40	4.02	3.81
M5	w/o	30.62	4.56	0.67	1.87	8.87
	with	57.54	0.24	0.32	2.46	3.51
M10	w/o	42.29	4.05	0.59	2.93	7.92
	with	84.63	0.06	0.23	4.61	3.07

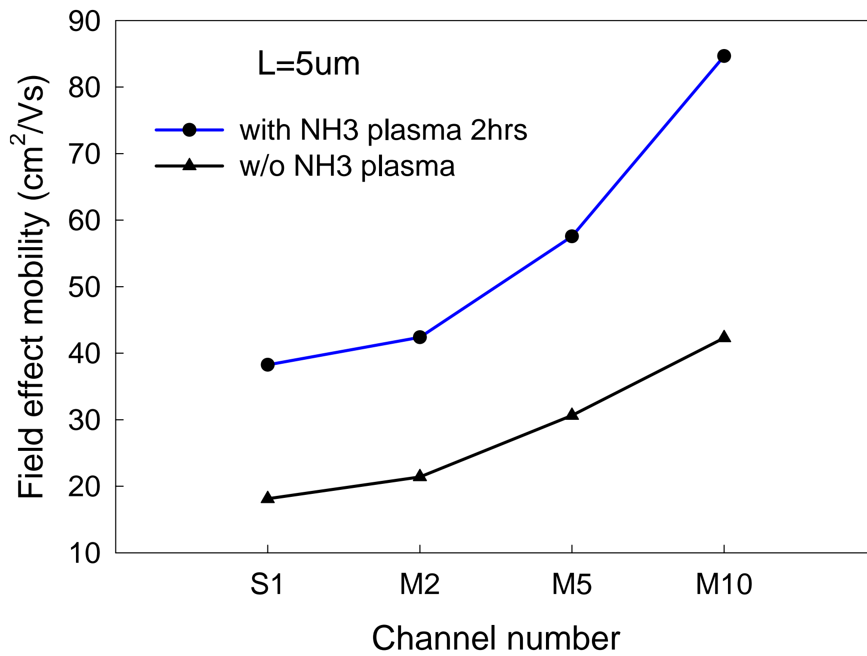

Fig. 4-1-11 PDMILC poly-Si TFTs' μ_{FE} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

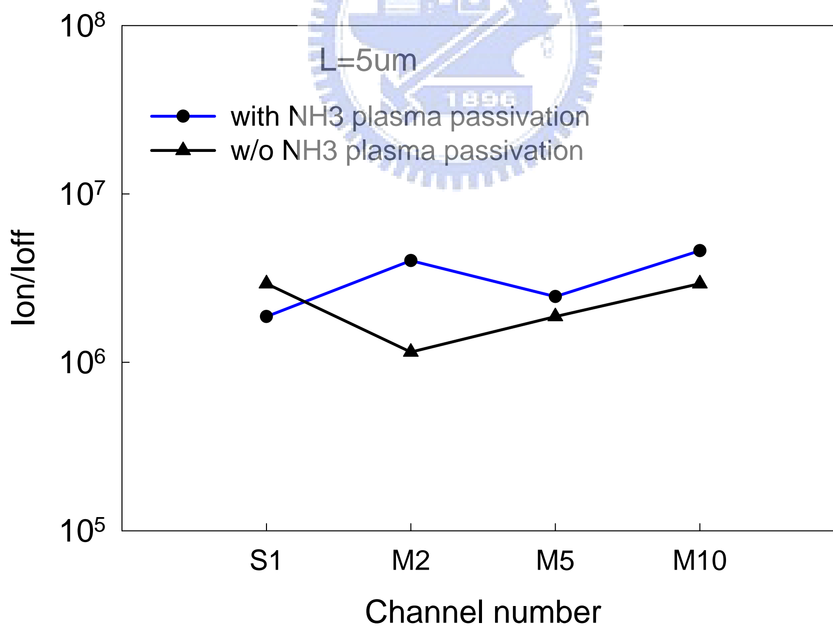

Fig. 4-1-12 PDMILC poly-Si TFTs' I_{on}/I_{off} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

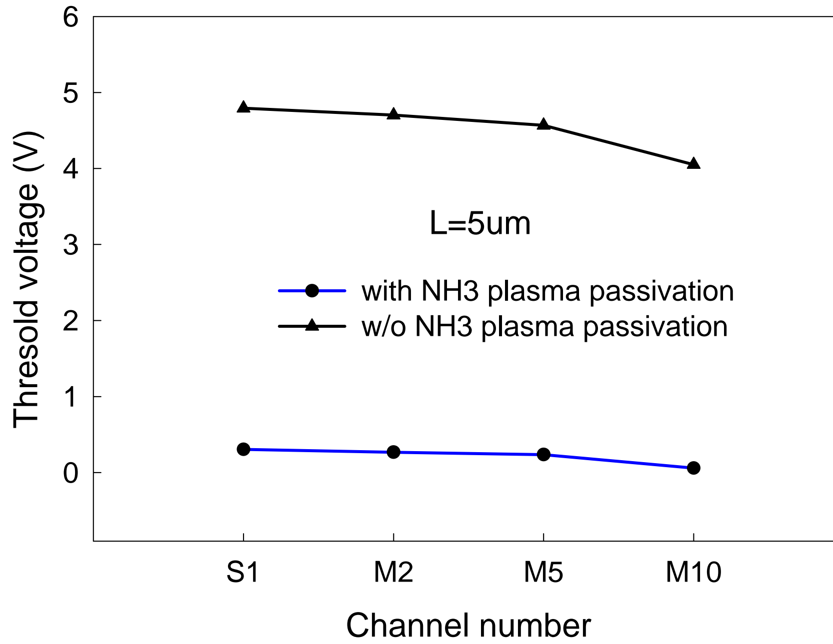

Fig. 4-1-13 PDMILC poly-Si TFTs' V_{th} versus the multi-channel with different widths, with and without NH_3 plasma passivation.

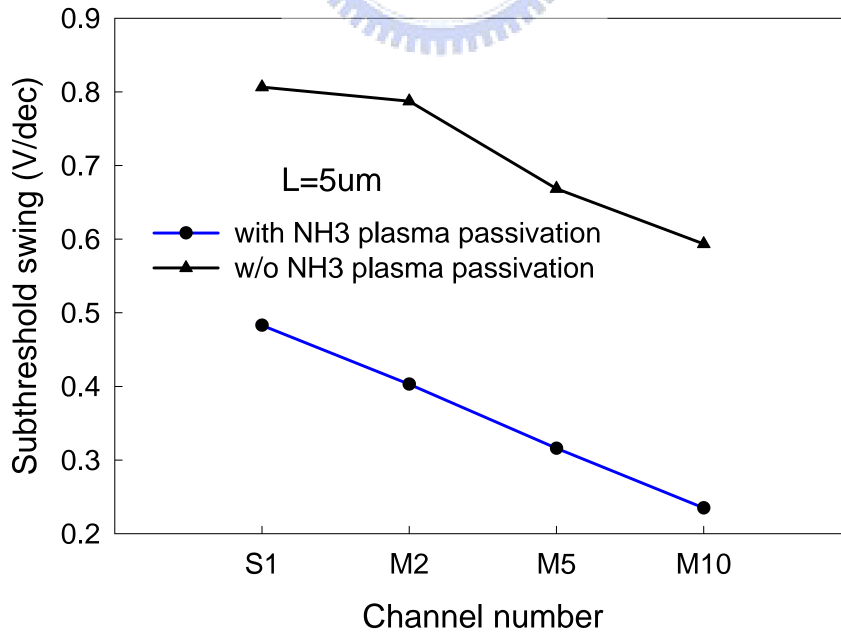

Fig. 4-1-14 PDMILC poly-Si TFTs' *SS* versus the multi-channel with different widths, with and without NH_3 plasma passivation.

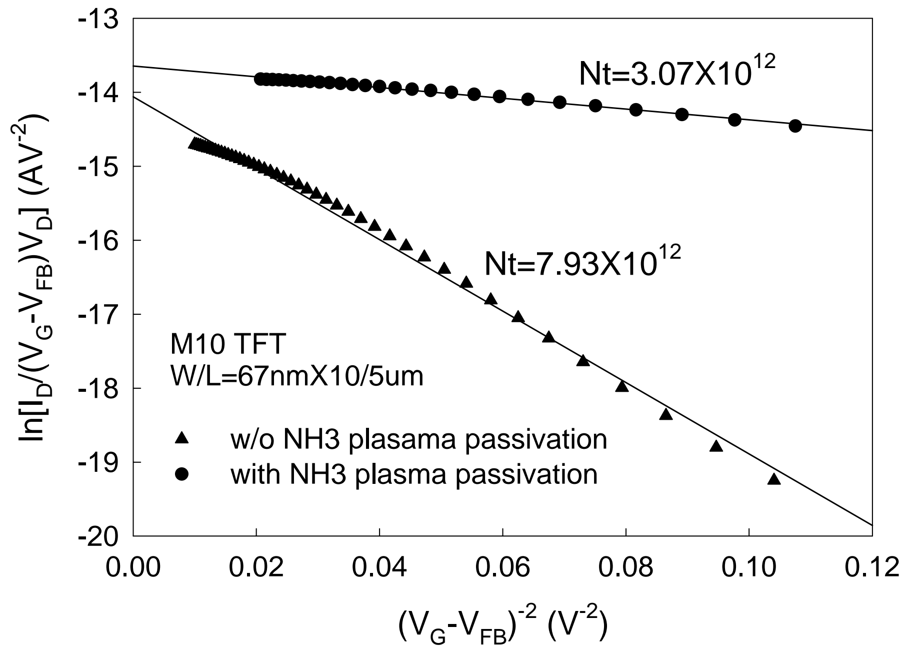

Fig. 4-1-15 Extraction of N_t plot of the M10 PDMILC TFTs, with and without NH_3 plasma passivation.

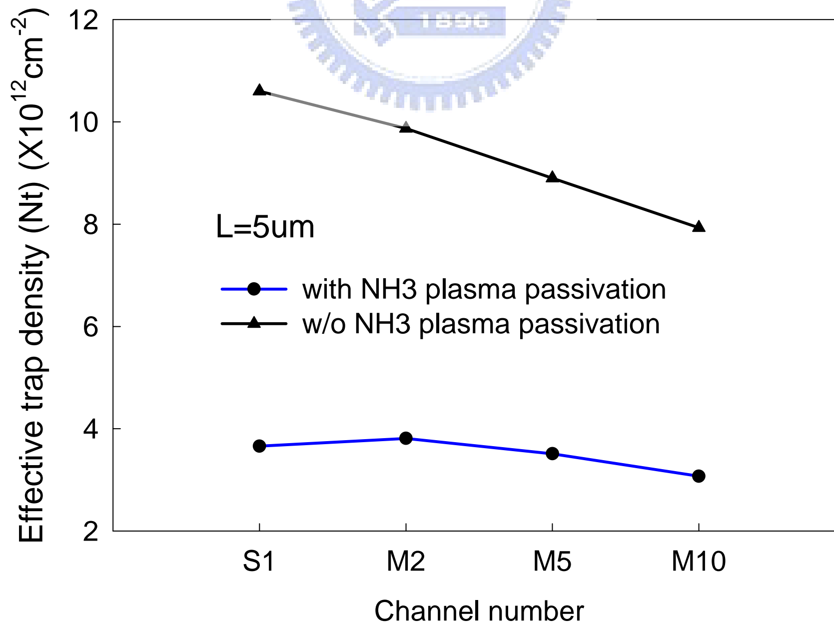

Fig. 4-1-16 PDMILC poly-Si TFTs' N_t versus the multi-channel with different widths, with and without NH_3 plasma passivation.

Table. 4-2-1 Devices dimension of all proposed Ni-PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm and gate TEOS-oxide thickness of 50 nm

Device name	Gate number	Each gate length (L)	Effective length (L_{eff})	Channel number	Each channel width (W)	Effective width (W_{eff})
G1S1	1	5 um	5 um	1	1 um	1 um
G1M10	1	5 um	5 um	10	84 nm	0.84 um
G2M10	2	2.5 um	5 um	10	84 nm	0.84 um
G3M10	3	1.67 um	5 um	10	84 nm	0.84 um
G4M10	4	1.25 um	5 um	10	84 nm	0.84 um

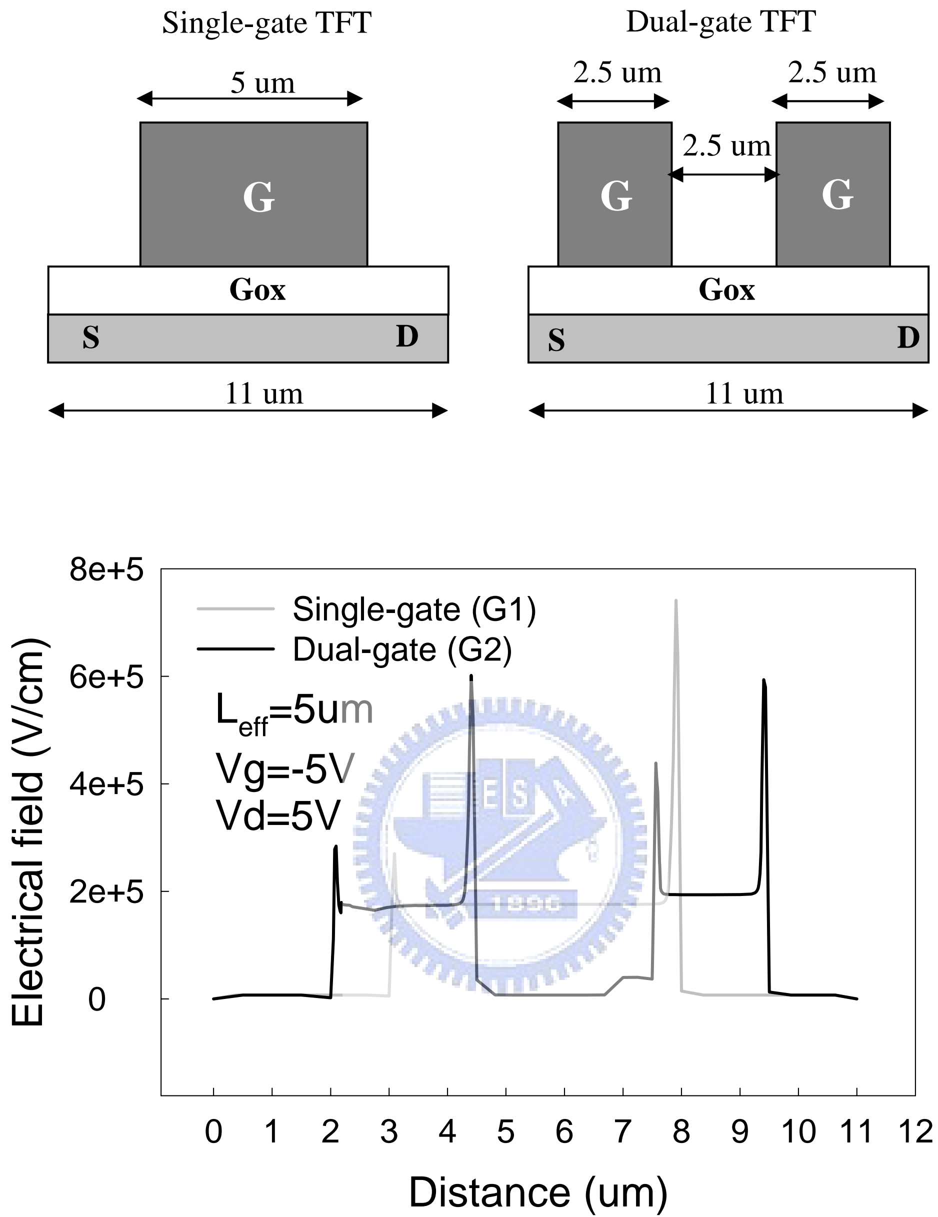

Fig. 4-2-1 Off-state electrical field simulation results of single-gate and dual-gates poly-Si TFT, by ISE TCAD v. 7 (a 2-D device simulator).

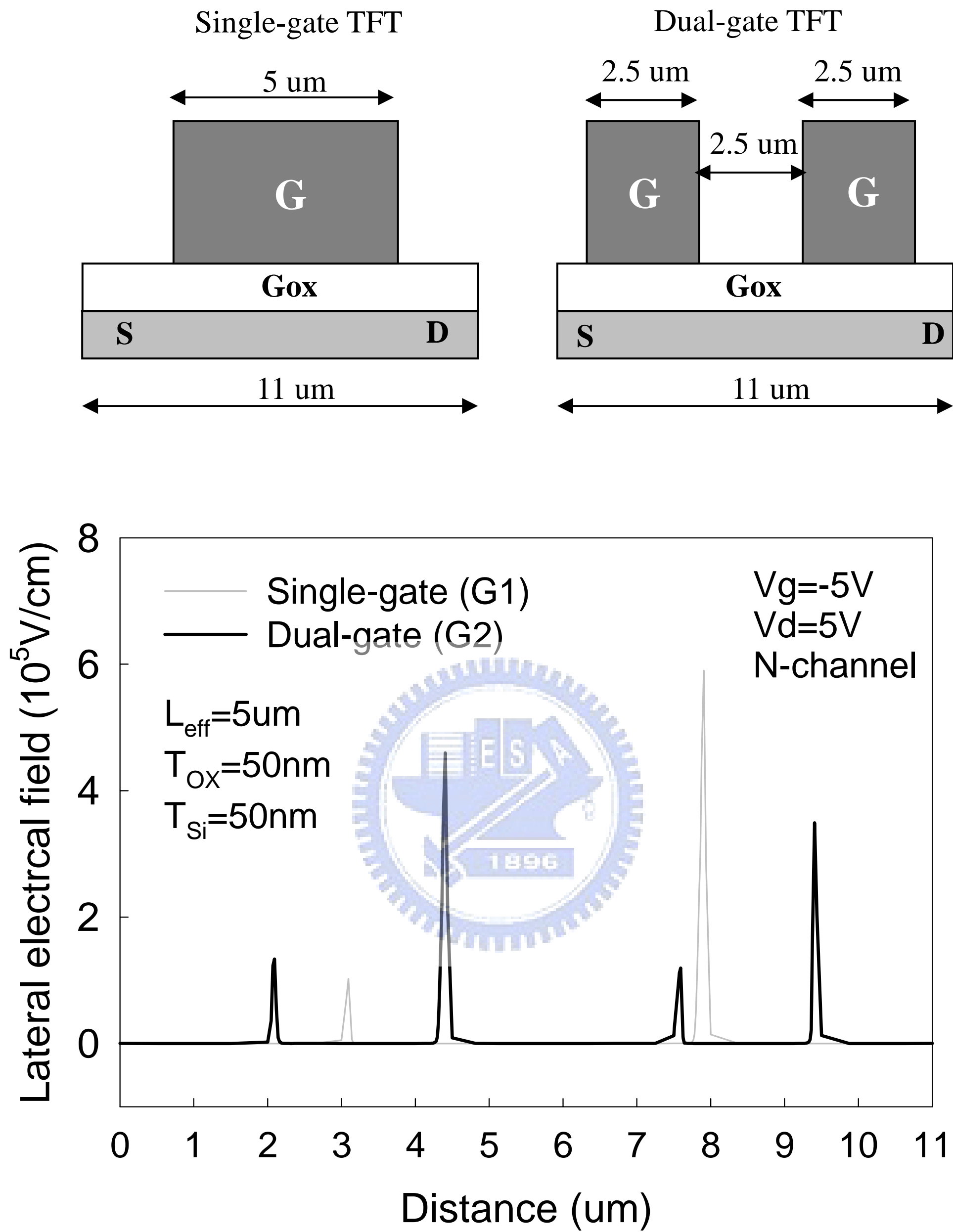

Fig. 4-2-2 Off-state lateral electrical field simulation results of single-gate and dual-gates poly-Si TFT b y ISE TCAD v. 7 (a 2-D device simulator).

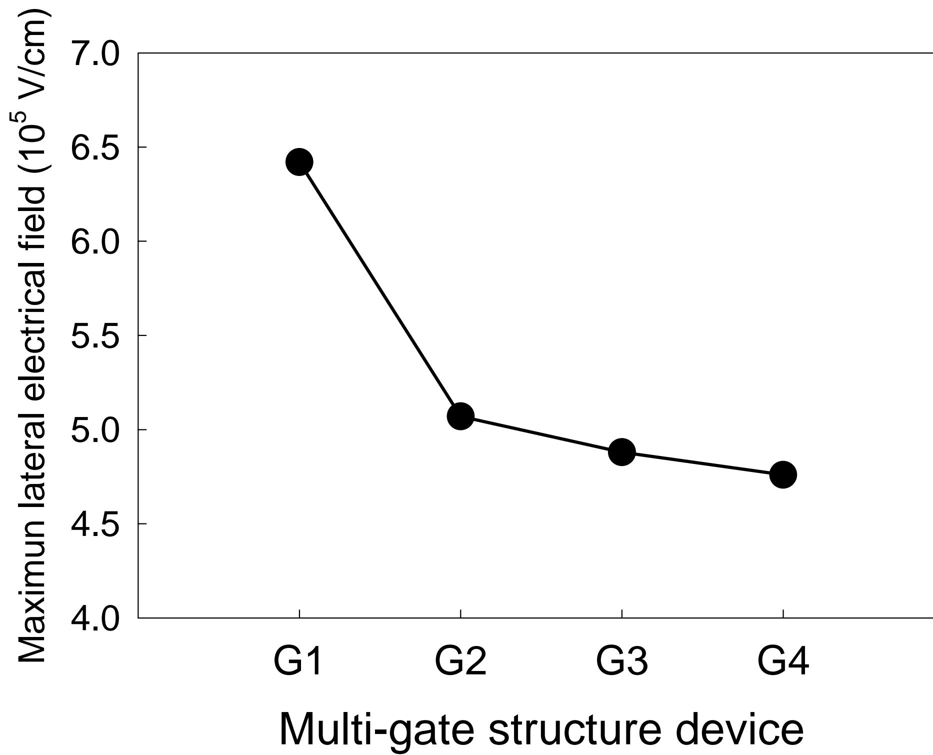

Fig. 4-2-3 The peak lateral electrical file (E_m) versus different gate number TFT structure. In off-state electrical field simulation results of multi-gate a poly-Si TFT by ISE TCAD v. 7 (a 2-D device simulator).

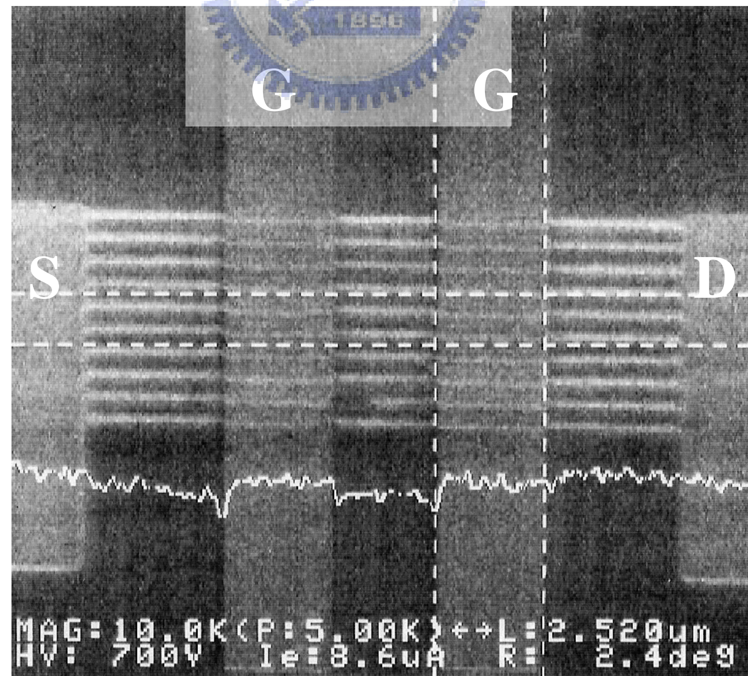

Fig. 4-2-4 Scanning electron microscopy (SEM) photography of active pattern with the source, drain, ten nanowire channels and dual-gate

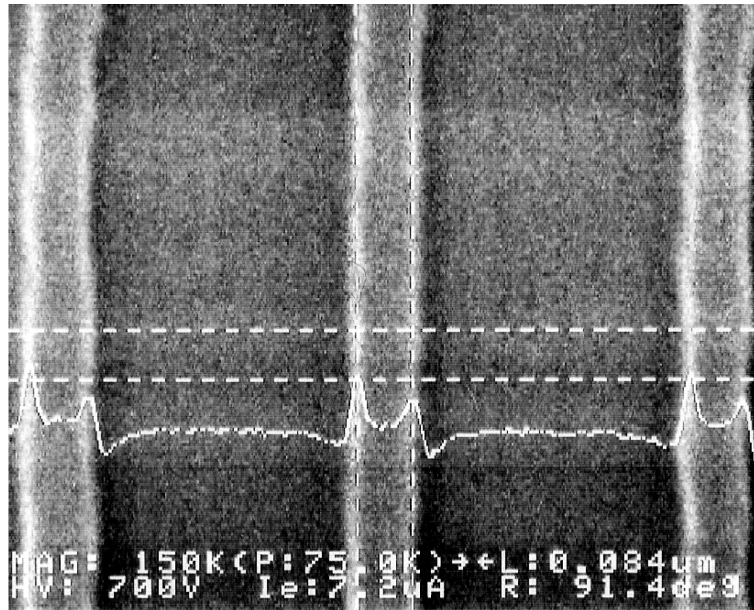

Fig.4-2-5 SEM photography of Magnified area of multiple nanowire channels. The each nanowire width is 84 nm.

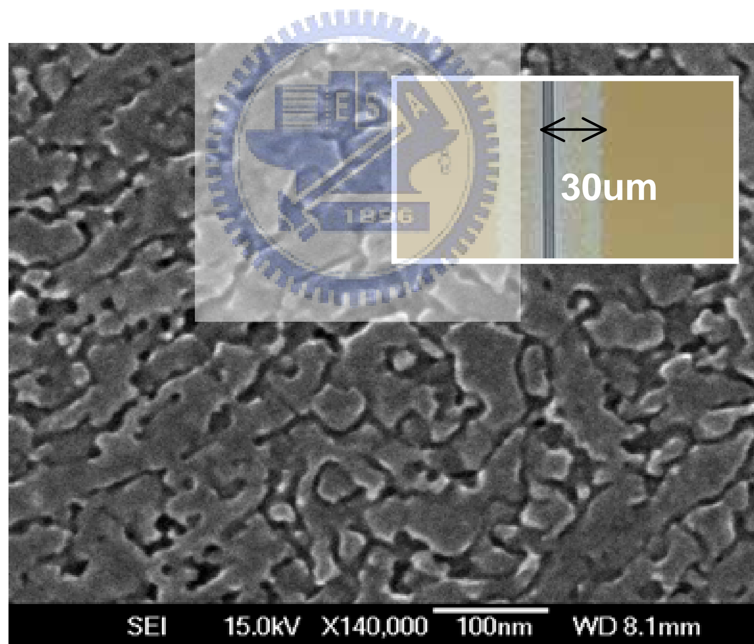

Fig. 4-2-6 The SEM photography of MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm. The inset optical microscopy photography depicts a MILC length of 30 um

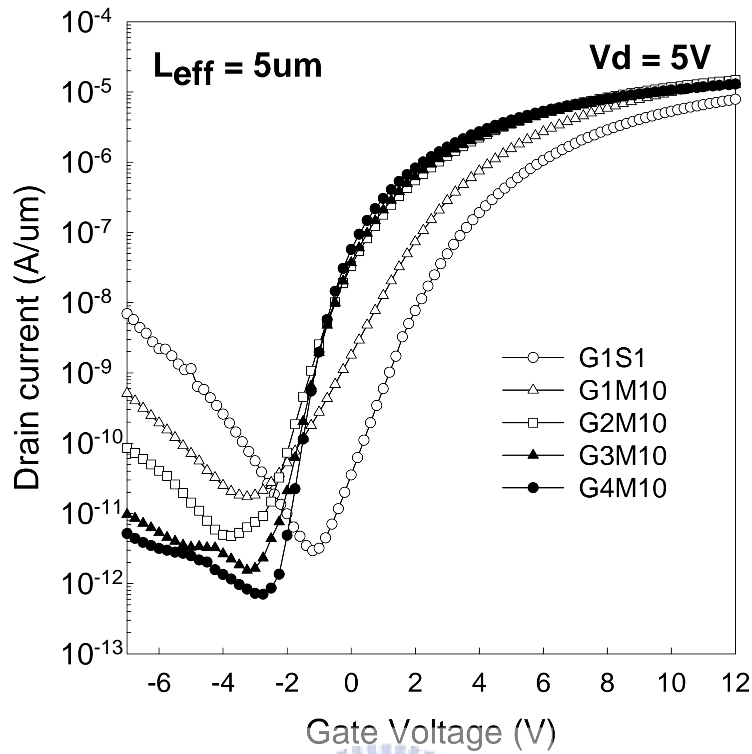

Fig. 4-2-7 Comparison of I_d - V_g transfer characteristics of of G1S1, G1M10,G2M10,G3M10, and G4M10 Ni-MILC poly-Si TFT with the same device effective length (L_{eff}) of 5 um.

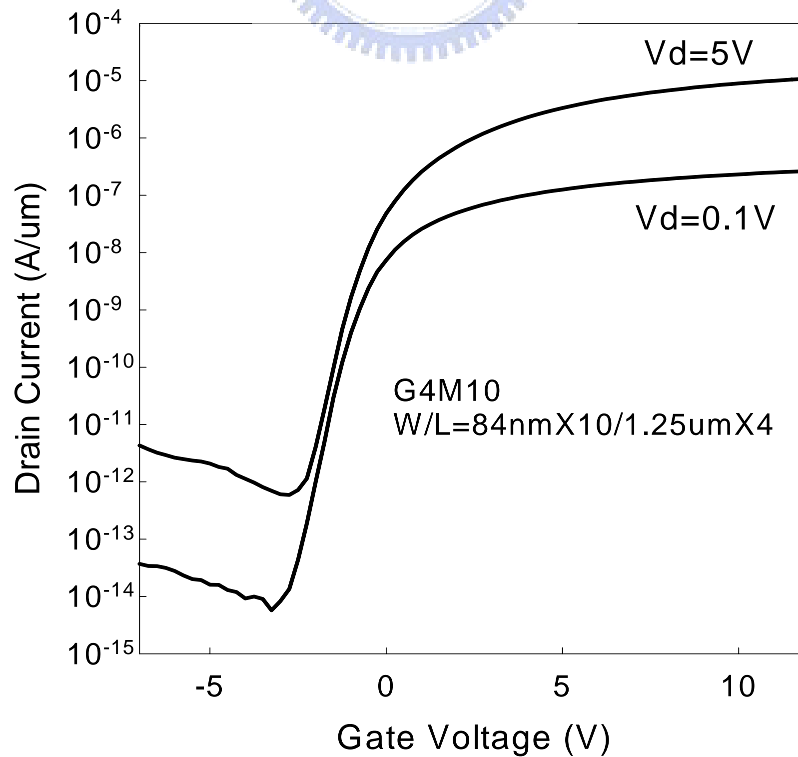

Fig. 4-2-8 The transfer curve of G4M10 TFT with linear and saturation region.

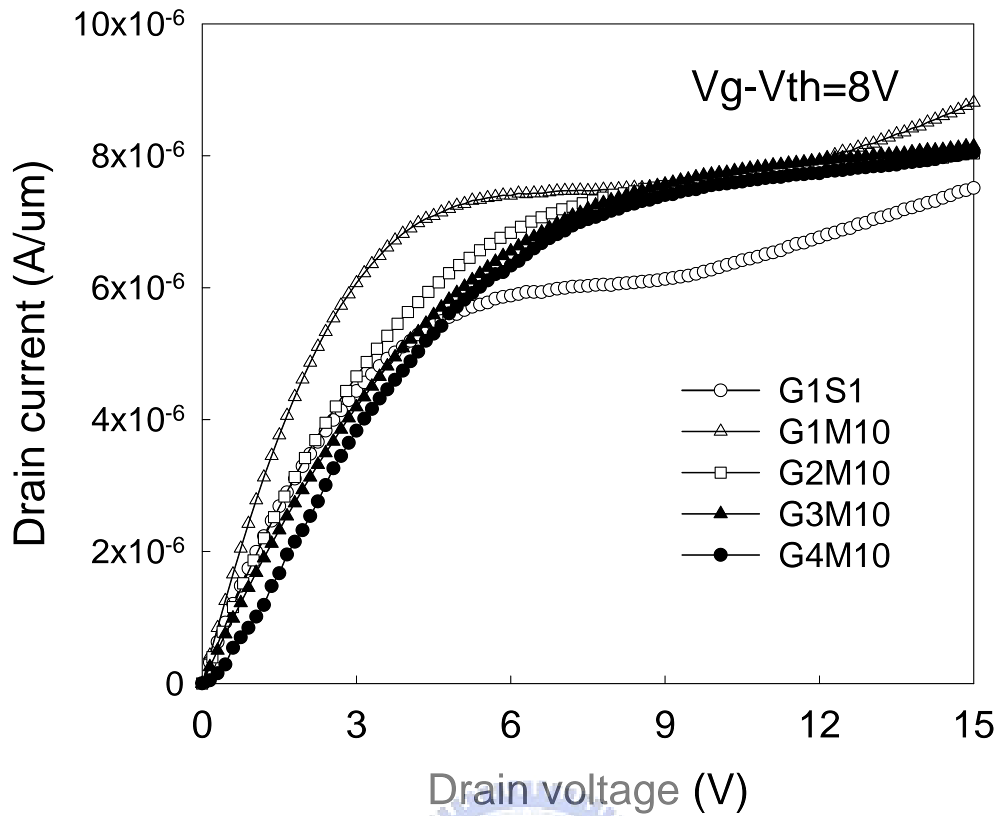

Fig. 4-2-9 Comparison of I_d - V_d output characteristics of G1S1, G1M10, G2M10, G3M10, and G4M10 Ni-MILC poly-Si TFT with the same device effective length (L_{eff}) of 5 um

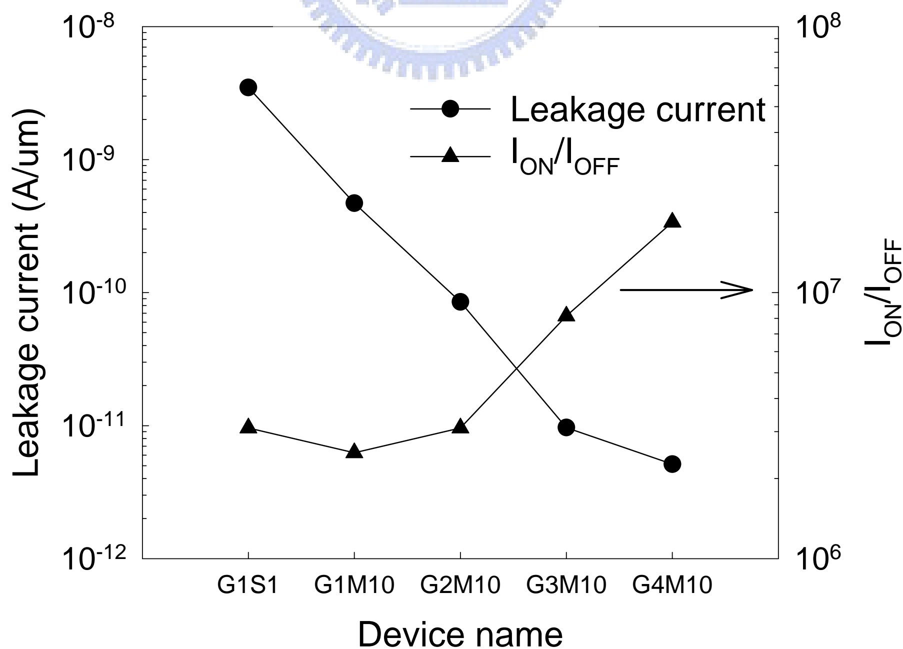

Fig. 4-2-10 Leakage current and maximum drain ON/OFF current ratio versus different multi-gate structure Ni-PDMILC poly-Si TFTs

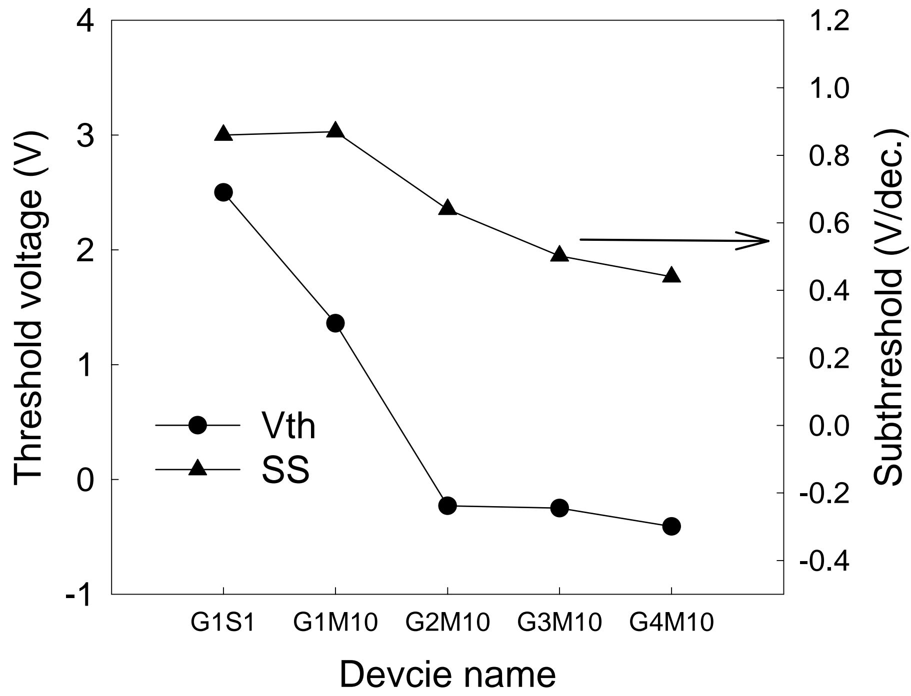

Fig. 4-2-11 The V_{th} and SS versus different multi-gate structure Ni-PDMILC poly-Si TFTs

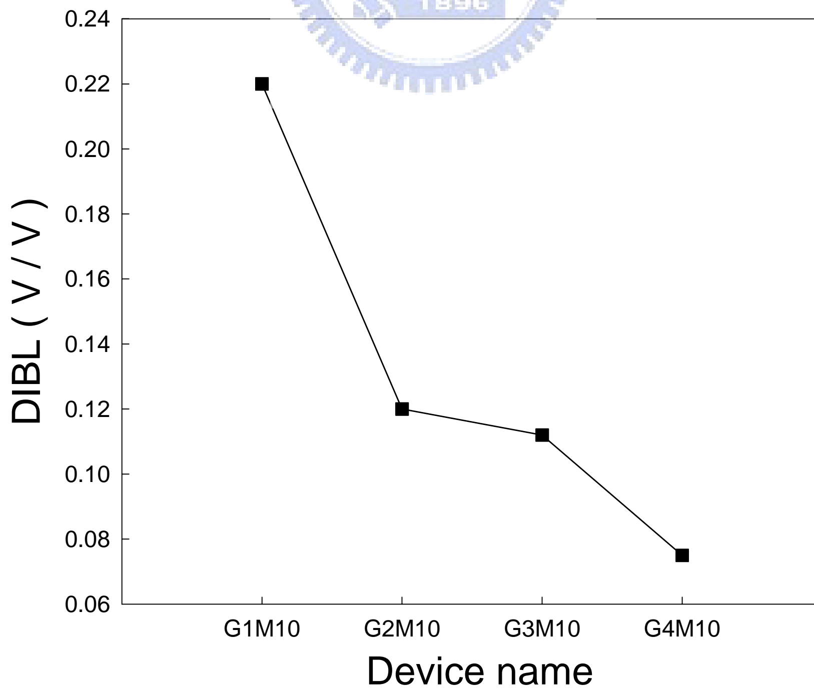

Fig. 4-2-12 The DIBL versus different multi-gate structure Ni-PDMILC poly-Si TFTs

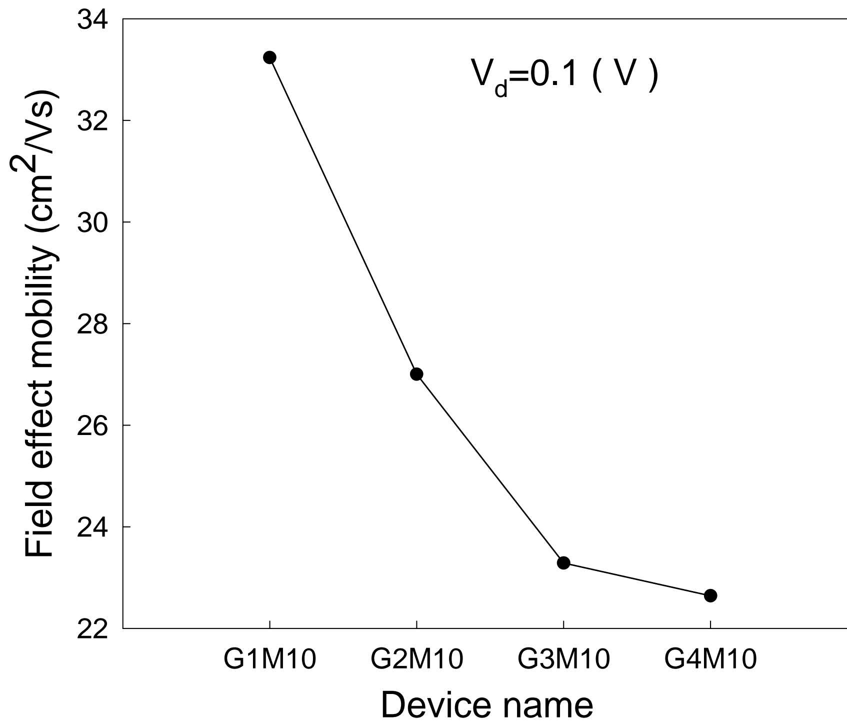

Fig. 4-2-13 The field effect mobility versus different multi-gate structure Ni-PDMILC poly-Si TFTs

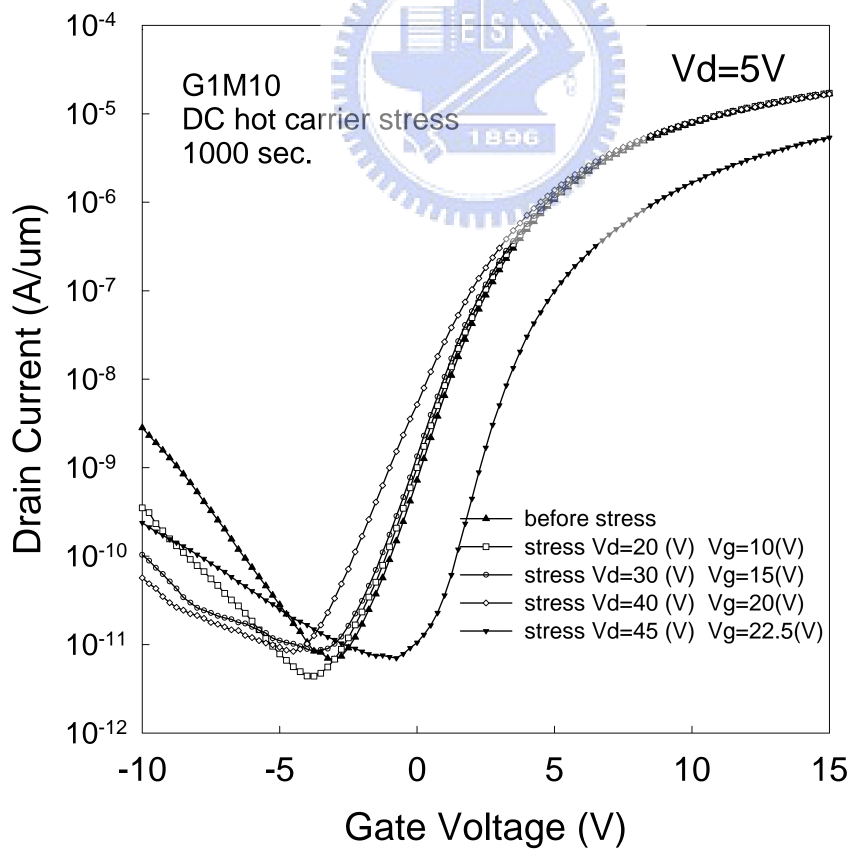

Fig. 4-3-1 A series of G1M10 TFT transfer curves after different hot-carrier stress conditions with 1000-second duration.

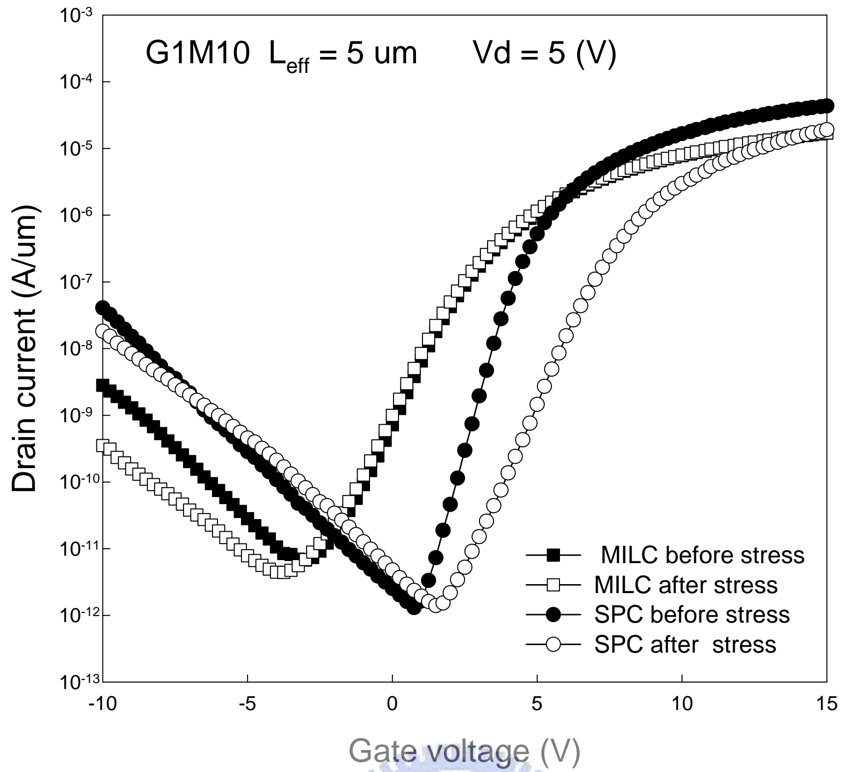

Fig. 4-3-2 The degradation in MILC and SPC of G1M10 TFT transfer curves before and after hot-carrier stress with 1000-second duration.

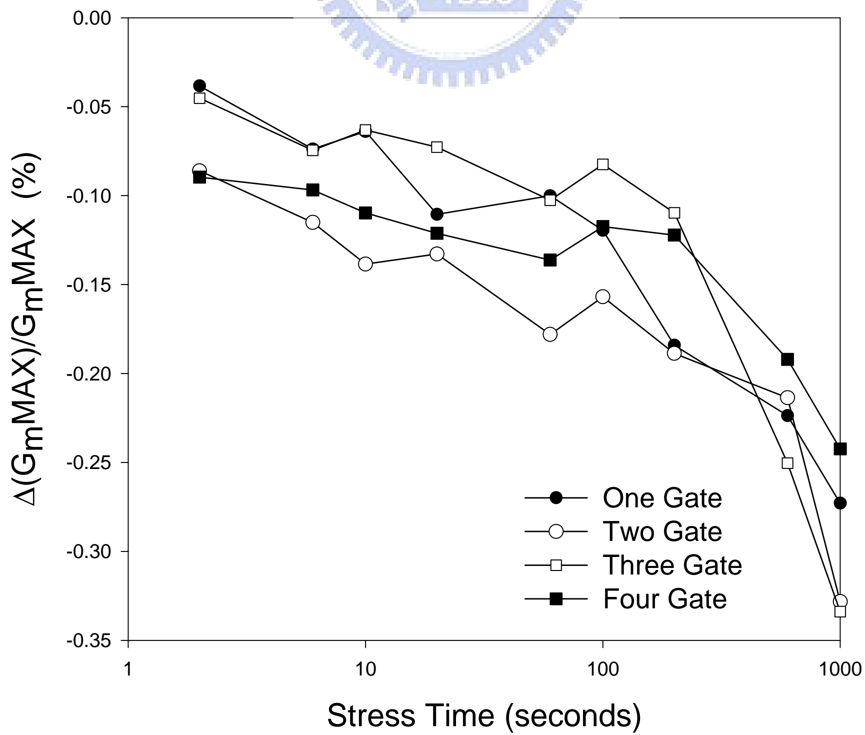

Fig. 4-3-3 Gm degradation as a function of the stress time with different multi-gate number TFTs

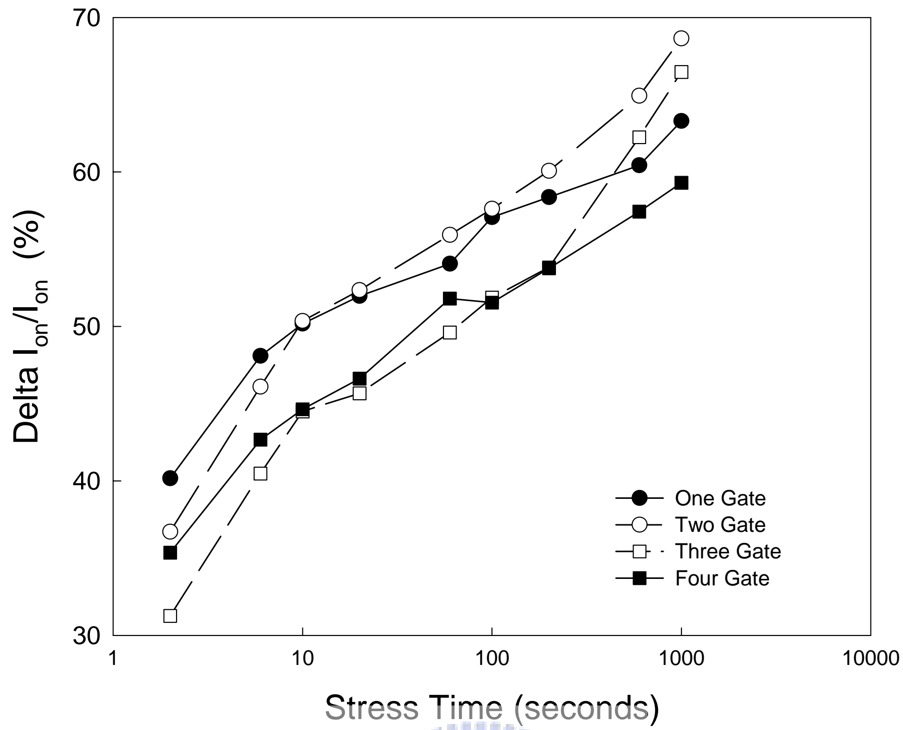

Fig. 4-3-4 I_{on} degradation as a function of the stress time with different multi-gate number TFTs

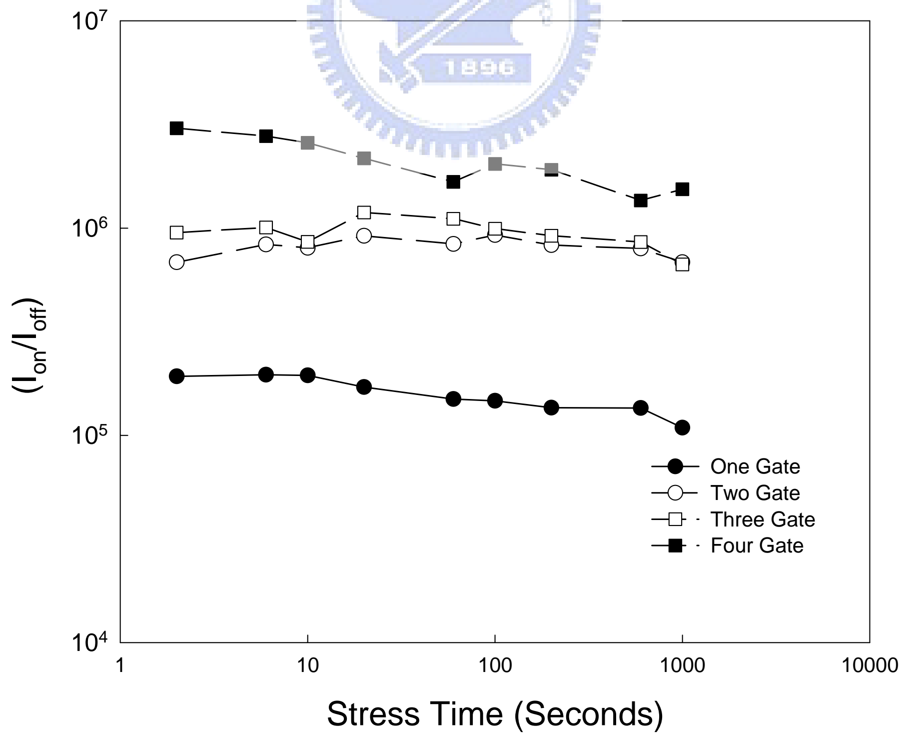

Fig. 4-3-5 *ON/OFF* ratio degradation as a function of the stress time with different multi-gate number TFTs.

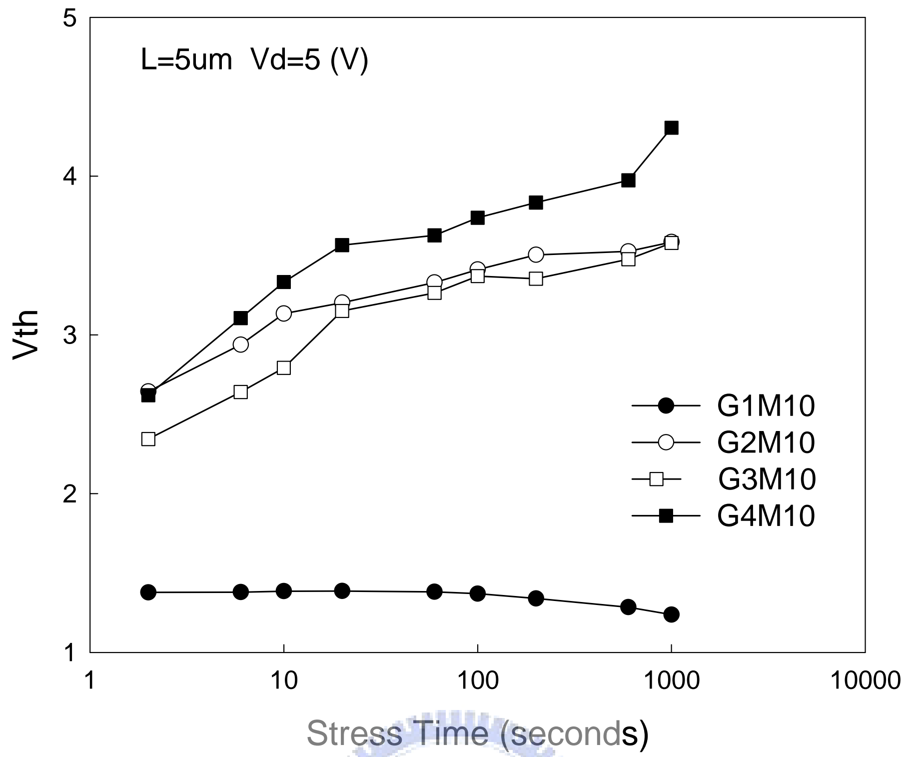

Fig. 4-3-6 Threshold voltage (V_{th}) degradation as a function of the stress time with different multi-gate number TFTs

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