Chapter 5

Conclusion

In section 4-1, the experimental results of PDMILC TFTs indicate that the performance of devices improves as the number of channels increases from the S1, M2 and M5 to the M10 PDMILC TFT, with the increase in the strength of the effect of the NH_3 plasma passivation. The defect density (N_t) in the grain boundary reveals a strong consistency between theory and experimental results. Additionally, NH_3 plasma passivation influences M10 TFT more strongly than it does to other TFTs. Because the M10 TFT has a split nanowire structure, most of which undergoes NH_3 plasma passivation, further reducing the number of defects at grain boundaries. These high performance NH_3 plasma passivated PDMILC TFTs are compatible with complementary metal oxide semiconductor (CMOS) technology, thus highly suitable for use in future SOP applications. In Section 4-2, the experiment spell out results show that employing ten nanowire channels enhances the Ni-MILC poly-Si TFT performance. Moreover, using the multi-gate structure can further enhance the TFT performance, including a lower leakage current, a higher *ON/OFF* ratio, a lower V_{th}, and a lower *SS* than single-gate TFT. In output characteristics, the multi-gate with ten nanowire TFT can reduce the kink-effect. We have also found that the Ni-MILC TFT

has excellent hot-carrier immunity and is suitable for high-voltage applications. This novel multi-channel and dual-gate Ni-MILC poly-Si TFT is quite easy to fabricate and involves no additional processes, thus, it is highly suitable for high-performance MILC poly-Si TFT applications. The lateral electrical field of M10 TFT can be effectively reduced by additional two side-gates control.