Fabrication and Characterization of Metal-induced Lateral Crystallization Polysilicon Thin-film Transistor with Multi-channel and Multi-gate

Student: Cheng-Wei Chou Advisors: Prof. Simon M. Sze
Prof. Ting-Chang Chang

Department of Electronics Engineering and Institute of Electronics
National Chiao Tung University, Hsinchu, Taiwan

Abstract

I have studied the effects of NH_3 plasma passivation on the electrical characteristics of pattern-dependent metal-induced lateral crystallization (PDMILC) polysilicon thin-film transistors (poly-Si TFTs). These transistors have various numbers of multiple channels. PDMILC TFTs with NH_3 plasma passivation outperform those without such passivation. This is because of the effective hydrogen passivation of the grain-boundary dangling bonds, and the pile-up of nitrogen at the SiO_2/poly-Si interface. Additionally, the performance of such devices improves as the number of multi-channels increase. In particular, the electrical characteristics of a nano-scale TFT with ten 67 nm-wide split channels (M10) are superior to other TFTs. For example, the M10 TFT has a higher field effect mobility of 84.63 cm^2/Vs, a higher *ON/OFF* current ratio (>10^6), a steeper subthreshold slope (*SS*) of 230

mV/decade, an absence of drain-induced barrier lowering (*DIBL*) and favorable output characteristics. We have found that the active channels of the M10 TFT have exhibit for the best NH_3 plasma passivation, due to its split nanowire channels structure. We have also studied for the pattern-dependent nickel (Ni) metal-induced lateral crystallization (Ni-MILC) polysilicon thin-film transistors (poly-Si TFTs) with ten nanowire channels and multi-gate. Experiment results show that employing ten nanowire channels improves the Ni-MILC poly-Si TFT performance, including a higher *ON/OFF* ratio and a lower threshold voltage (V_{th}) than single-channel TFT. Furthermore, experimental results reveal that a combination the multi-gate structure and ten nanowire channels can further enhance the entire performance of Ni-MILC TFT, including a low leakage current, a high *ON/OFF* ratio, a low V_{th}, a steep subthreshold swing (*SS*), and a kink-free output characteristics. From our studies, we conclude that the performance of the PDMILC TFTs can be improved by NH_3 plasma passivation. The lateral electrical field of a ten multiple nanowire channels TFT can be effectively reduced by additional multi-gate control. The PDMILC TFTs process is compatible with CMOS technology, and involves no extra mask. Such high performance PDMILC TFTs are thus promising for use in future high-performance poly-Si TFT applications, especially in AMLCD and 3D MOSFET stacked circuits.

Key words: Pattern-depended metal induced lateral crystallization, Mobility, Polysilicon thin film transistor, AMLCD, Multi-gate, nanowire.