

Table captions

➤ Chapter 3

Table 3-1 Devices dimension of all proposed Ni-PDMILC poly-Si TFTs.

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Table 4-1-1. Device parameters of PDMILC TFTs with the same $L = 5$ μm at different widths. All parameters were extracted at $V_d = 5$ V, except for the field-effect mobility (μ_{FE}) which were extracted at $V_d = 0.1$ V.

Table. 4-2-1 Devices dimension of all proposed Ni-PDMILC poly-Si TFTs. All devices have the same active channel thickness of 50 nm and gate TEOS-oxide thickness of 50 nm



Figure captions

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Fig. 2-1. Energy band diagram in the lateral direction along the channel of a n-channel polysilicon TFTs.

Fig. 2-2. Sketch of the band diagram of the polycrystalline silicon films.

Fig. 2-3. A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model.

Fig. 2-4. Extraction of N_t plot of the M10 PDMILC TFTs, with and without NH_3 plasma passivation.

Fig. 2-5. Three possible mechanisms of leakage current in poly-Si TFTs, including thermionic emission, thermionic field emission and pure tunneling.

Fig. 2-6 The kink effect in the output characteristics of an *n*-channel SOI MOSFET.

Fig. 2-7 MILC polysilicon formation during annealing process. (a) At the beginning of the annealing process, many nickel atoms are trapped and nickel silicide is formed at the grain boundaries of the MILC polysilicon region. Those nickel silicide grain boundaries at the MIC to a-Si interfaces, which are reactive regions, are responsible for MILC formation. (b) During the annealing process, the nickel silicide RGB absorbs silicon atoms from the a-Si region and rejects them to the MIC polycrystalline silicon region. As a result, the polysilicon grain grows up in lateral direction.

Fig. 2-8 MILC polysilicon formation mechanism. (i) Most of nickel atoms are trapped at the nickel silicide RGB, which is a layer between the amorphous silicon (a-Si) and MILC crystalline silicon regions. (ii) The nickel atoms in the nickel silicide RGB diffuse to the a-Si region and bonds with silicon atoms. The activation energy of the a-Si crystallization is lowered by the nickel impurities. (iii) The silicon atoms are dissociated from the nickel silicide RGB and then bond to the MILC crystalline silicon region. (iv) Nickel atoms diffuse to the a-Si region and crystallize

the a-Si atoms continuously. This leads the shift of nickel silicide RGB and the growth of MILC polysilicon. (v) Only few nickel atoms are left and trapped inside the MILC silicon grain.

Fig. 2-9 Epitaxial silicon growth using nickel silicide, in which, the nickel silicide consumes the a-Si atoms at the leading edge and rejects the Si atoms to the crystalline silicon region.

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Fig.3-1 (a) Schematic diagram of proposed G2M10 Ni-MILC poly-Si TFT. (b) Topview of Fig. 3-1a.

Fig.3-2 Cross-section view of Ni-MILC poly-Si TFT, which was a conventional top-gate, self-aligned offset MOSFET structure.

Fig.3-3 the direction of metal induced lateral crystallization

Fig.3-4 Off-state electrical field simulation results of single-gate and dual-gates poly-Si TFT by ISE TCAD v. 7(a 2-D device simulator).

Fig.3-5 SEM photography of G1M10 TFT active pattern with multiple nanowire channels, and one-gates. The gate length is about 5 μ m.

Fig.3-6 SEM photography of G2M10 TFT active pattern with the source, the drain, multiple nanowire channels, and two-gates. The each gate length is about 2.5 μ m

Fig.3-7 SEM photography of G3M10 TFT active pattern with multiple nanowire channels, and one-gates. The gate length is about 1.7 μ m.

Fig.3-8 SEM photography of G4M10 TFT active pattern with multiple nanowire channels, and one-gates. The gate length is about 1.25 μ m.

Fig.3-9 Scanning electron microscopy (SEM) photography of active pattern with the source, the drain, ten nanowire channels and MILC seeding window. The inset plot shows the each nanowire width of 67 nm.

Fig.3-10 Magnified area of multiple nanowire channels. The each nanowire width is 84 nm.

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- Fig. 4-1-1 Scanning electron microscopy (SEM) photography of active pattern with the source, the drain, ten nano-wire channels and MILC seeding window. The inset plot shows the each nano-wire width of 67 nm.
- Fig.4-1-2 SEM photography of MILC poly-Si grain structure. The average poly-Si lateral grain size is about 250 nm.
- Fig. 4-1-3 Device characteristics of S1 ($W / L = 1 \text{ } \mu\text{m} / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT transfer $I_d - V_g$ curve with (solid-line) and without (dash-line) NH_3 plasma passivation.
- Fig. 4-1-4 Device characteristics of S1 ($W / L = 1 \text{ } \mu\text{m} / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT output $I_d - V_d$ curve with (solid-line) and without (dash-line) NH_3 plasma passivation.
- Fig. 4-1-5 Device characteristics of M2 ($W / L = 0.5 \text{ } \mu\text{m} \times 2 / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT transfer $I_d - V_g$ curve with (solid-line) and without (dash-line) NH_3 plasma passivation.
- Fig. 4-1-6 Device characteristics of M2 ($W / L = 0.5 \text{ } \mu\text{m} \times 2 / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT output $I_d - V_d$ curve with (solid-line) and without (dash-line) NH_3 plasma passivation.
- Fig. 4-1-7 Device characteristics of M5 ($W / L = 0.18 \text{ } \mu\text{m} \times 5 / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT, transfer $I_d - V_g$ curve with (solid-line) and without (dash-line) NH_3 plasma passivation.
- Fig. 4-1-8 Device characteristics of M5 ($W / L = 0.18 \text{ } \mu\text{m} \times 5 / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT, output $I_d - V_d$ curve with (solid-line) and without (dash-line) NH_3 plasma passivation.
- Fig. 4-1-9 Device characteristics of M10 ($W / L = 67 \text{ nm} \times 10 / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT, transfer $I_d - V_g$ curve with (solid-line) and without (dash-line) NH_3 plasma passivation.
- Fig. 4-1-10 Device characteristics of M10 ($W / L = 67 \text{ nm} \times 10 / 5 \text{ } \mu\text{m}$) PDMILC poly-Si TFT, output $I_d - V_d$ curve, with (solid-line) and without (dash-line) NH_3 plasma passivation.
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- Fig. 4-3-4 I_{on} degradation as a function of the stress time with different multi-gate number TFTs
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