Chapter 1

Introduction

1-1. Overview of polysilicon thin-film transistor technology

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have drawn much attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1], and organic light-emitting diodes (OLEDs) [2]. Except large area displays, poly-Si TFTs also have been applied for memory devices such as dynamic random access memory (DRAM) [3], static random access memory (SRAM)[4], electrically programmable read only memory (EPROM) [5], electrically erasable programmable read only memory (EEPROM) [6], linear image sensor [7], thermal printer head [8], photo-detector amplifier [9], scanner [10], and neutral network [10]. Lately, some superior performances of poly-Si TFTs have been reported by scaling down device dimensions or utilizing novel crystallization technologies to enhance poly-Si film quality [11-12]. These approaches provide an opportunity of using poly-Si TFTs for three-dimension (3-D) integrated circuit fabrication. Of course, the application in AMLCDs is the primary important, leading to rapid development of poly-Si TFT technology.

The major attraction of applying polycrystalline silicon thin-film transistors (poly-Si TFTs) in active matrix liquid crystal display (AMLCDs) lies in the greatly improved carrier mobility in poly-Si film, the capability of integrating the pixel switching elements, and the capability to integrate panel array and peripheral driving circuit on the same substrates [13-15]. In poly-Si film, carrier mobility larger than 10 cm^2/Vs can be easily achieved, that is high enough for peripheral driving circuit including n- and p-channel devices. This enables the fabrication of peripheral circuit and TFT array on the same glass substrate, bring the era of system-on-glass (SOG) technology. And the capacity of the high mobility to integrate the pixel switching elements and the capacity to integrate the panel array and the peripheral driving circuit on the substrates [16-18] will bring the era of system-on panel (SOP).The process complexity can be greatly simplified to lower the cost. In addition, the mobility of poly-Si TFTs is much better than that of amorphous ones, the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high density, high resolution AMLCDs, and the aperture ratio in TFT array can be significantly improved by using poly-Si TFTs as pixel switching elements. This is because that the device channel width can be scaled down while meeting the same pixel driving requirements as in α-Si TFT AMLCDs.

For making high performance poly-crystalline silicon (poly-Si) thin film

transistors (TFTs) [19], low-temperature technology is required for the realization of commercial flat-panel displays (FPD) on inexpensive glass substrate, since the maximum process temperature is limited to less than 600^0C. We have three major low-temperature amorphous-Si (a-Si) crystallization methods to achieve high performance poly-Si thin film: solid phase crystallization (SPC), excimer laser crystallization (ELC), and metal-induced lateral crystallization (MILC). MILC technology was initially developed as a low-temperature crystallization technique compared to other low temperature poly-Si technologies such as laser crystallization (LC) [20] or conventional solid-phase crystallization (SPC) [21].

MILC is superior because, unlike LC, it is a low-cost batch process and unlike SPC, better quality poly-Si thin film can be obtained [19]. However, most of all previous report of MILC TFTs, additional MILC trench mask process is necessary. In a practical of view, the additional mask will cause the fabrication complexity and decrease the product yield. In addition to this, the application of TFT's is mainly limited to low-temperature flat-panel display due to its substantially worse performance caused by the grain boundaries in the channel region. It is believed that electrical properties of the TFT's can be improved if the grain size can be enhanced and the number of grain boundaries in the channel region can be minimized. It is believed that electrical properties of the TFT's can be improved if the grain size can

be enhanced and the number of grain boundaries in the channel region can be minimized. In order to overcome above problems, a new pattern-depended MILC TFTs with standard four masks process [22] is presented. The experiment results also demonstrate that the electrical properties of TFT's can be significantly improvement by carrier mobility enhancement and robust gate controllability.

1-2. Motivation

Those applications of Ni-MILC poly-Si TFTs are still limited, because the grain boundaries of poly-Si himself in the channel region substantially degrade performance. However, the grain boundary effects can be reduced mainly by two techniques : 1) by passivating the dangling silicon bonds at the grain boundaries and thus reducing the density of the grain boundary states in the film; 2.) by enhancing the grain size and, thus, reducing the number of grain boundaries present within the active channel of the TFT device. [23] The poly-Si TFTs with several multi-channels has been reported to effectively reduce grain boundary defects [24.25]. Besides, the Ni-MILC poly-Si TFT was suffered from severe leakage current due to Ni contamination during MILC annealing process [26.27], which is directly related to lateral electrical field in drain depletion region. This is another major limitation of Ni-MILC poly-Si TFT application. The poly-Si TFTs with multi-gates has been reported to effectively reduce

leakage current [28.29].On the other hand, the NH_3 plasma passivation [30] has been reported to reduce the number of trap–states in poly-Si grain boundaries, yielding high-performance poly-Si TFTs. Addition to the electrical characteristic, the improved in reliability of poly-Si TFTs are also the most important requirements in the realization of high-performance displays. And there have been very few reports concerning low temperature poly-Si (LTPS) TFT reliability, especially in Ni-MILC poly-Si TFT [31].

Therefore, in this work, we develop a series of multi-gate with multiple nanowire channels Ni-MILC poly-Si TFT to study theirs leakage current and performance. The experiment results demonstrate that applying multi-gate with multiple nanowire channels structure can significantly reduce the leakage current, while keeping in high performance of Ni-MILC TFT. On the other hand, as we know that in order to obtain high-performance poly-Si TFT's, it is necessary to reduce the trap-states of the poly-Si films. So the effects of NH_3 plasma passivation on the electrical characteristics of a series of multi-channels with PDMILC poly-Si TFT structures of various (pattern-dependent) widths are initially investigated. Besides, the PDMILC TFT under static stress considering different stressing conduction is also analyzed in this thesis.

1-3. Thesis outline

Chapter 1. Introduction

1-1. Overview of polysilicon thin-film transistor technology

1-2. Motivation

1-3. Thesis outline

Chapter 2. Poly-Si TFT conduction mechanism & MILC formation mechanism

2-1. TFT transportation mechanism

2-2. Method of Device Parameter Extraction

2-3. TFT non-ideal effect

2-4. MILC formation mechanism

Chapter 3. Device Structure, Simulation, and Fabrication

3-1. Pattern-depended MILC（PDMILC）TFT Structure and Simulation

3-2. Fabrication of Pattern-depended MILC TFT

3-3. Fabrication results of Pattern-depended MILC TFT

Chapter 4. Results and discussion

4-1. Effects of channel width and NH3 Plasma Passivation on Electrical Characteristics

4-2. Multi-gate Effects on Electrical Characteristics

4-3. Reliability of Multi-gate PDMILC TFT under Static Stress