Chapter 2

Poly-Si TFT conduction mechanism & MILC formation

mechanism

2-1. TFT transportation mechanism

As mentioned in section 1-1 and 1-2, the device characteristics of poly-Si TFTs

are strongly influenced by the grain structure in poly-Si film. Even though the

inversion channel region is also induced by the gate voltage as in MOSFETs, the

existence of grain structure in channel layer bring large differences in carrier transport

phenomenon. Many researches studying the electrical properties and the carrier

transport in poly-Si TFTs have been reported. A simple grain boundary-trapping

model has been described by many authors in details [1]-[3]. In this model, it is

assumed that the poly-Si material is composed of a linear chain of identical crystallite

having a grain size L_g and the grain boundary trap density N_t. The charge trapped at

grain boundaries is compensated by oppositely charged depletion regions surrounding

the grain boundaries. From Poisson's equation, the charge in the depletion regions

causes curvature in the energy bands, leading to potential barriers that impede the

movement of any remaining free carriers from one grain to another. When the

dopant/carrier density n is small, the poly-Si grains will be fully depleted. The width

of the grain boundary depletion region x_d extends to be $L_g/2$ on each side of the

boundary, and the barrier height V_B can be expressed as

$$V_B = \frac{qn}{2\varepsilon_s}x_d^{\,2} = \frac{qnL_g^{\,2}}{8\varepsilon_s} \qquad\qquad (2\text{-}1)$$

As the dopant/carrier concentration is increased, more carriers are trapped at the

grain boundary. The curvature of the energy band and the height of potential barrier

increase, making carrier transport form one grain to another more difficult. When the

dopant/carrier density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si

grains turn to be partially depleted and excess free carriers start to spear inside the

grain region. The depletion width and the barrier height can be expressed as

$$x_d = \frac{N_t}{2n} \qquad\qquad (2\text{-}2)$$

$$V_B = \frac{qn}{2\varepsilon_s}(\frac{N_t}{2n})^2 = \frac{qN_t^{\,2}}{8\varepsilon_s n} \qquad\qquad (2\text{-}3)$$

The depletion width and the barrier hight turn to decrease with increasing

dopant/carrier density, leading to improved conductivity in carrier transport.

The carrier transport in fully depleted poly-Si film can be described by the

thermionic emission over the barrier. Its' current density can be written as [4]

$$J = qnv_c \exp[-\frac{q}{kT}(V_B - V_g)] \qquad\qquad (2\text{-}4)$$

where n is the free-carrier density, v_c is the collection velocity ($v_c = \sqrt{kT/2\pi m^*}$), V_B

is the barrier height without applied bias, and V_g is the applied bias across the grain

boundary region. For small applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decreases by an amount of $V_g/2$. In the reserve-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J_F = qnv_c \exp[-\frac{q}{kT}(V_B - \frac{1}{2}V_g]$$ (2-5)

$$J_R = qnv_c \exp[-\frac{q}{kT}(V_B + \frac{1}{2}V_g)]$$ (2-6)

the net current density is then given by

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_g}{2kT})$$ (2-7)

at low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage kT/q, Eq. (2-7) then can be simplified as

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\frac{qV_g}{2kT} = \frac{q^2nv_cV_g}{kT}[\exp(-\frac{qV_B}{kT})]$$ (2-8)

the average conductivity $\sigma = J / E = JL_g / V_g$ and the effective mobility $\mu_{eff} = \sigma / qn$ then can be obtained

$$\sigma = \frac{q^2nv_cL_g}{kT}\exp(-\frac{qV_B}{kT})$$ (2-9)

$$\mu_{eff} = \frac{qv_cL_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv \mu_0 \exp(-\frac{qV_B}{kT})$$ (2-10)

where μ_0 represents the carrier mobility inside grain regions. It is found that the conduction in poly-Si is an activated process with activation energy of approximately qV_B, which depends on the dopant/carrier concentration and the grain boundary trap

density.

Applying gradual channel approximation to poly-Si TFTs, which assumes that the variation of the electric field in the y-direction (along the channel) is much less than the corresponding variation in the y-direction (perpendicular to the channel), as shown figure 2-2. The carrier density n per unit area (cm^{-2}) induced by the gate voltage can be expressed as
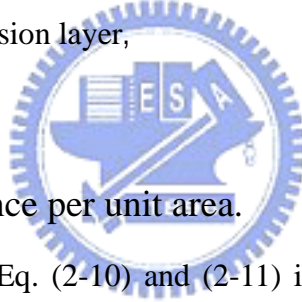
$$n = \frac{C_{ox}(V_G - V_{TH})}{q t_{ch}}$$ (2-11)

where

t_{ch} is the thickness of the inversion layer,

V_{TH} is the threshold voltage,

C_{ox} is gate oxide capacitance per unit area.

Therefore, by replacing Eq. (2-10) and (2-11) into Eq. (2-8), the drain current $I_D = J \times W \times t_{ch}$ of poly-Si TFT then can be given by

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_G - V_{TH}) V_D \exp(-\frac{q V_B}{kT})$$ (2-12)

where drain voltage $V_D = V_g \times n_g = V_g \times \frac{L}{L_g}$. Obviously, this *I-V* characteristics is very similar to that in MOSFETs, except that the mobility is modified.

2-2. Methods of Device Parameter Extraction

In this section, we will introduce the methods of typical parameters extraction such as threshold voltage (V_{th}), subthreshold slope (*SS*), drain current *ON/OFF* ratio,

field-effect mobility (μ_{FE}), and the trap density (N_t).

2-2-1. Determination of the threshold voltage

Many ways are used to determinate the V_{th} which is the most important parameter of semiconductor devices. In poly-Si TFTs, the method to determinate the threshold voltage is *constant drain current method*. The gate voltage at a specific drain current I_N value is taken as the threshold voltage. This technique is adopted in most studies of TFTs. Typically, the threshold current $I_N = I_D / (W_{eff} / L_{eff})$ is specified 100 nA for $V_D = 5V$ (saturation region) in this thesis.

2-2-2. Determination of the subthreshold slope

Subthreshold slope $SS_{(V/dec.)} = dV_G / d(\log I_D)$ is a typical parameter to describe the gate control toward channel. And in intrinsic polysilicon TFTs the parameter SS is directly related with the total trap states density N_T by the relationship

$$SS = \left(\frac{kT}{q} \right) \ln 10 \left(1 + \frac{q^2 t_{si} N_T}{C_{ox}} \right) \qquad (2\text{-}13)$$

where
kT is the thermal energy,
t_{si} is the polysilicon layer thickness.

Thus, the decrease of SS with stressing suggests a decrease in the total trap states density, which includes both bulk and interface traps. The SS should be independent of drain voltage and gate voltage. However, in reality, SS might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication,

and punchthrough-like effect. The *SS* is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this experiment, the *SS* is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude (from 10^{-8}A to 10^{-10}A).

2-2-3. Determination of *On/Off* Current Ratio

Drain *On/Off* current ratio is another important factor of TFTs. High *On/Off* ratio represents not only large turn-on current but also small off current (leakage current). It affects gray levels (the bright to dark state number) of TFT AMLCD directly.

There are many methods to specify the on and off current. The practical one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage is applied at 5V.
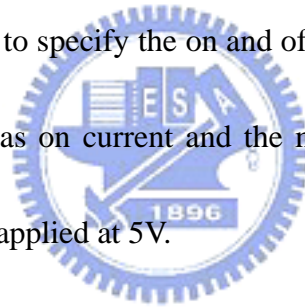
2-2-4. Determination of the field-effect mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain voltage ($V_d = 0.1$V). The transfer I-V characteristics of poly-Si TFT can be expressed as

$$I_D = \mu_{FE}C_{ox}\frac{W}{L}[(V_G - V_{TH})V_D] \qquad (2\text{-}14)$$

where

W is channel width,
L is channel length,

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\bigg|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \qquad (2\text{-}15)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox}WV_D}g_m \qquad (2\text{-}16)$$

Modification of effective field-effect mobility:

According Seto model [5], in uniform small grain poly-Si TFT, the effective

field-effect mobility can be expressed:

$$\mu_{eff} = \frac{qv_c L_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv \mu_0 \exp(-\frac{qV_B}{kT})$$

However, in poly-Si films with enlarged grains, the uniform trap distribution

model fails to give reliable results due to high nonuniformity of the polycrystalline

material. According to Farmakis *et al.* [6] model, the μ_{eff} depend on the number of

grain boundaries present within the channel of the transistor. Figure 2-2 represents the

energy band structure of the polysilicon in the neighborhood of the grain boundaries

of a n-channel polysilicon TFT along the channel in the linear region of operation

(low drain voltage V_D). This energy band structure has two resistances R_G and R_{GB}

equivalent to the grain region and the grain boundary respectively, both modulated by

the gate voltage V_G. The grain region is considered to behave as in a bulk MOSFET.

Therefore, considering an average number of *n GB's* and *n* entire grains within the

channel, according to the standard MOSFET theory, the total channel resistance R_{ch}

will be

$$R_{ch} = \frac{L}{W\mu_{eff}Q_{invG}} = nR_G + NR_{GB} = \frac{nL_G}{W\mu_G Q_{invG}} + \frac{nL_{GB}}{W\mu_{GB}Q_{invGB}} \tag{2-17}$$

where

μ_{eff} effective electron mobility

μ mobility

Q_{inv} charge in the inversion layer

L_G average intra-grain length;

L_{GB} average grain boundary length

Throughout the text, the indices G and GB will be referred to the intra-grain and grain boundary region respectively. Assuming that the main conduction mechanism through the grain boundaries is the thermionic emission over the grain-boundary energy potential barrier V_b, the charge in the grain boundaries Q_{GB} will be given by the relationship [6]

$$Q_{invGB} = e^{-qV_b(V_G)/kT}Q_{invG} \tag{2-18}$$

When the potential barrier V_b is high, Q_{invGB} Q_{invG} and according to Eq.(2-17) μ_{eff} is practically controlled by the grain boundary mobility being normally very low. When V_b is lowered enough by increasing the gate potential V_G, $Q_{invGB}=Q_{invG}$ and $\mu_{eff} \approx \mu_{eff}$ .By taking into account that $L= nL_G + nL_{GB}$, from Eq. (2-17) and (2-18), it is obtained

$$\frac{L}{\mu_{eff}} = \frac{L\text{-}nL_{GB}}{\mu_G} + n\frac{L_{GB}}{\mu_{GB}e^{-qV_b/kT}} \tag{2-19}$$

The average grain-boundary number inside the channel is

$$n = \frac{L}{L_G} \tag{2-20}$$

$$\frac{L}{nL_{GB}} = \frac{L_G}{L_{GB}} \tag{2-21}$$

For polysilicon TFTs with gate length and width of the same order of the grain size , n takes small values. In this case, for typical values of $L_{GB} = 1\text{-}2$ nm and L = 4-20 um, it is

$$\frac{L}{nLGB} \ggg 1 \tag{2-22}$$

Equation (2-19) is further simplified when Eq. (2-22) is taken into account

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_G} + \frac{nL_{GB}}{L}\frac{1}{\mu_{GB}e^{-qV_b/kT}} \tag{2-23}$$

So according to the polysilicon TFTs mobility model with separating grain and grain boundaries taking into account the average number of grain boundaries into the channel, in general the effective field-effect mobility (μ_{FE}) is given by,

$$\mu_{FE} = \mu_G \frac{1}{1 + (\mu_G / \mu_{GB})[(nL_{GB})/L]\exp(qV_b/kT)} \tag{2-17}$$

where $n = L/L_G$ is the average grain-boundary number.

2-2-5. Determination of the trap density

As described in Eq. (2-3), the grain boundary potential barrier height V_B is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density N_t can be extracted from the current-voltage characteristics of poly-Si TFTs. As proposed by Levinson et al. [7], the I-V characteristics including the trap density can be obtained by replacing Eq. (2-3) and Eq. (2-11) into Eq. (2-12) :

$$I_D = \mu_0 C_{ox}\frac{W}{L}(V_G - V_{TH})V_D \exp(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{TH})}) \tag{2-18}$$

This equation had been further corrected by Proano et al. by considering the mobility

under low gate bias [8]. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. Moreover, a better approximation for channel thickness t_{ch} in an undoped material is given by defining the channel thickness as the thickness at which 80 percent of the total charge resides. Therefore, by solving the Poisson's equation, the channel thickness is given by
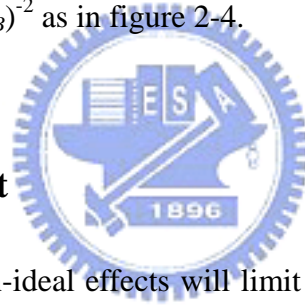
$$tch = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})} \tag{2-19}$$

The drain current of poly-Si TFTs then should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \exp(-\frac{q^2 N_t^2 \sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^2(V_G - V_{FB})^2}) \tag{2-20}$$

The effective trap state density then can be obtained from the slope of the curve $ln[I_D/(V_G\text{-}V_{FB})]$ versus $(V_G\text{-}V_{FB})^{-2}$ as in figure 2-4.

2-3. TFT non-ideal effect

There are two major non-ideal effects will limit the TFTs application, including leakage current, and kink-effect. The mechanism of these three non-ideal effects is described briefly as bellow.

2-3-1. Leakage current

In AMLCD, TFTs play a switching device to turn *ON/OFF* the current path for charging/discharging the liquid crystal capacitor. Thus, the leakage current should be low enough to remain a pixel gray level before it must be refreshed. The leakage current mechanism in poly-Si has been studied by Olasupe [9]. The leakage current resulted from carrier generation from the poly-Si grain boundary defects. There are

three major leakage mechanisms, as shown in figure 2-5. The dominant mechanism is a function of the prevailing drain bias. They pointed out carrier generation from grain boundary defects via thermionic emission and thermionic field emission to be prevalent at a low and medium drain biases, and carrier pure tunneling from poly-Si grain boundary defects to be the dominant mechanism at higher drain bias.

2-3-2. Kink effect [10]

During devices operation, a high field near the drain could induce impact ionization there. Majority carriers, holes in the p-substrate for an n-channel poly-Si TFTs, generated by impact ionization will be stored in the substrate, since there is no substrate contact to drain away these charges. Therefore the substrate potential will be changed and will result in a reduction of the threshold voltage. This, in turn, may cause an increase or a kink in the current-voltage characteristics. The kink phenomenon is shown in figure 2-6. This float-body or kink effect is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons. The kink effect can be reduced in TFTs by lowering lateral field inside the channel.

2-4. MILC formula mechanism [11].[12]

In the last few years, several articles have been devoted to study of the growth

mechanism of metal-induced-lateral-crystallization (MILC). Earlier observation of Ni

induced crystallization of a-Si revealed that the onset temperature for crystallization

of a-Si was significantly reduced in presence of $NiSi_2$ precipitates and crystallization

occurred at around 500^0C. The $NiSi_2$ precipitates acts as a good nucleus of Si, which

has similar crystalline structure (the fluorite type, CaF_2) and a small lattice mismatch

of 0.4% with Si. In the case of Ni induced crystallization, the growth of crystallites

depends strongly on the migration of $NiSi_2$ precipitates, and the driving force for the

migration of $NiSi_2$ precipitates is the reduction in free energy associated with the

transformation of metastable a-Si to stable c-Si.
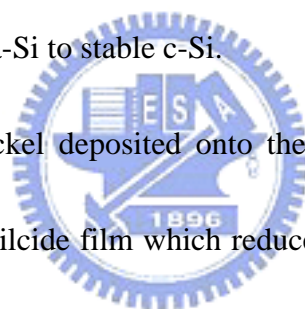
In the MILC process, nickel deposited onto the seed window first reacts with

silicon to form a thin nickel silcide film which reduces the activation energy for a-Si

crystallization. Thus, a-Si under the silicide is thermally crystallized into polysilicon,

and this is called the initial nucleation of crystalline Si on nickel silicide. As this

polysilicon is formed by a direct metal induced method, it is also referred as

metal-induced-crystallization (MIC) polysilicon. There are many grain boundaries

inside the MIC polysilicon layer and these grain boundaries provide good locations

for trapping the metal atoms. Due to the fast nickel diffusion in crystalline silicon

structure and good nickel trapping property at the crystalline silicon to a-Si interface,

most of nickel atoms in the MIC region diffuse to and are trapped at the grain

boundaries. The trapped metal atoms react with silicon atoms to form thin layers of

nickel silicide at the grain boundaries. At the MIC to a-Si interface, the nickel silicide

at grain boundaries exist as a continuous sandwich layer between MIC polysilicon and

a-Si as illustrated in figure 2-7a and figure 2-7b This continuous nickel silicide layer

is a reactive layer, which will be responsible for the grain growth, so it is called nickel

silicide reactive grain boundary (*RGB*). The nickel silicide *RGB* propagates toward

the a-Si region during MILC annealing and a-Si will then be crystallized.

The nickel concentration at the *RGB* is higher than the neighboring a-Si.

Continuous annealing after MIC leads metal atom diffusion to the a-Si layer in lateral

directions. Once the nickel atoms are pushed toward the a-Si region, those atoms

repair the intrinsic traps and form a new nickel silicide *RGB*. The nickel atoms lower

the activation energy of a-Si crystallization and construct the silicon atoms into a

crystalline structure. Since the nickel diffusion in crystalline silicon region is

relatively faster, the nickel atoms in the polysilicon region then diffuse to the new

silicon grain boundary quickly. This increases the nickel concentration at the *RGB*

and subsequently pushes the nickel atoms to the a-Si again and again. As a result, the

a-Si is crystallized to polysilicon in the lateral direction, and this polysilicon is called

metal-induced-lateral-crystallization (MILC) polysilicon. As the MILC formation is

led by the propagation of the nickel silicide *RGB*, the MILC polysilicon grains grow

along the direction of nickel diffusion. Figure 2-8 illustrates the silicon crystallization

process during the MILC annealing. The mechanism described does not only explain

the polysilicon growth of MILC, but also help to explain the epitaxial silicon growth

mechanism by nickel silicide layer propagation from crystalline silicon toward a-Si

(refer to figure 2-9) proposed by other researches. It tells us why the nickel silicide

absorbs silicon atoms from the a-Si region and rejects the excess Si atoms to the

crystalline silicon area during epitaxial silicon growth.