Chapter 6

Properties of $Sr_{0.8}Bi_{2.6}Ta_2O_{9+x}$ ferroelectric thin films with $SrTiO_3$ seeding layer on MIM and MFIS structures

6-1. Introduction

Recently, ferroelectric materials have attracted considerable interest for nonvolatile memory applications. The simplest structure of a ferroelectric-gate FET is an MFSFET, where a ferroelectric film is directly grown on Si (or semiconductor) as a gate insulator. The main problem of this structure is the difficulty in fabricating good ferroelectric/Si interface. In order to grow ferroelectric materials on Si substrates with good interface properties, an insulation buffer layer is usually inserted between the ferroelectric material and Si. Such a structure is called a metal-ferroelectric-metal-insulator -semiconductor (MFIS) structure. Another structure for ferroelectric-gate FET is the metal-ferroelectric- metal-insulator-semiconductor (MFMIS) structure. Compared to those of PZT, $SrBi_2Ta_2O_9$ (SBT) has been intensively investigated as a promising ferroelectric material for nonvolatile random-access memory due to its fatigue-free and low coercive field characteristics. The SiO_2 is one of most promising candidates as a dielectric buffer layer in MFIS and MFMIS. However, if the SiO_2 layer is too thin for scale shrink, a leakage current based on direct tunneling of electrons flows

through thin oxide layer and degrades the memory retention characteristics of FeFET. For this reason, it may be more desirable to fabricate the MIS structure using a high-k material as the gate insulator.

In MFIS structure, the excellent interface properties of insulator/Si are available. However, the dielectric constant of ferroelectric material is much higher than that of insulator material, leading to much smaller capacitance of the insulator layer than the ferroelectric layer. The smaller insulator capacitance and the higher ferroelectric capacitance cause the smaller electric field of ferroelectric than the insulator, which means that it is difficult to apply sufficient voltage to the ferroelectric film. In this study, we used the high-k material such as $SrTiO_3$ (STO), CeO_2 as an insulator. We also used multilayer insulator to enhance the dielectric constant and obtain a higher electric field of ferroelectric layer. The multilayer insulator is CeO_2 with seeding $SrTiO_3$ (STO) layer.

The CeO_2 thin film belongs to cubic structure and its lattice parameter, a=5.41Å, is very similar to that of Si substrate (a=5.43 Å). With the mismatch less than 0.1%, the stress between CeO_2 and Si is small enough to be ignored. Therefore the CeO_2 is suitable to use as the high-k dielectric material. The STO with a cubic perovskite structure and high dielectric constant of about 300 had been proposed as a good gate dielectric for CMOS.

Recently, some low temperature process techniques have been employed to improve the ferroelectric properties of SBT thin films, such as laser ablation method [120], chemical liquid deposition method [121], specific adhesion layer [122], and buffer or seeding layers [123-124]. The effects of various seeding layers and substrate configurations on the properties of PZT thin films have also been studied [125-127]. In this study, we used the STO seeding layer

to low annealing temperature and to improve the ferroelectricity of SBT thin film. The SBT ($Sr_{0.8}Bi_{2.6}Ta_2O_{9+x}$) thin film was prepared by MOD (metal-organic deposition) technique and deposited on metal and insulator, MIM and MFIS structure. The electronic properties of SBT thin film between with STO seeding layer and without seeding layer on those two structures were investigated.

6-2. Experiment

The metal-ferroelectric-metal-insulator-semiconductor (MFMIS) capacitors were fabricated using SBT ($Sr_{0.8}Bi_{2.6}Ta_2O_{9+x}$) thin films as the ferroelectric material and CeO_2 and STO thin films as the insulator material. The metal-ferroelectric-metal (MFM) structure is directly fabricated SBT thin films on Ir/SiO_2/Si substrate. The CeO_2 and STO thin films are deposited on p-type (100) Si wafer by rf magnetron sputtering method, respectively. The multilayer was first CeO_2 deposited on p-Si substrate and then STO deposited on CeO_2/Si by RF magnetron sputtering technique for 5 min to obtain a very thin STO seeded layer. The SBT thin films are deposited on CeO_2/Si, STO/CeO_2/Si, Ir/SiO_2/Si, STO/Ir/SiO_2/Si substrates by spin-coating at 5000 rpm for 30 sec followed by pyrolysis at 150℃ for 10 min to evaporate the solvent, then heated at 400℃ in air for 30 min to eliminate other organic compound. After repeating the process of spin coating and preheating several times, the gel films were crystallized at various temperatures for 10 min. The SBT precursor solution was prepared from $Sr(CH_3COO)_2$, $Bi(CH_3COO)_3$, $Ta(OCH_2CH_3)_5$, and acetic acid as a solvent. The mole ratios of Sr:Bi:Ta in the precursor solution were 0.8:2.6:2.0 in order to obtain good electrical characteristics.

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A platinum top electrode was deposited on the surface of the SBT film using the DC sputtering method for electrical measurement. Finally, the back-contact electrode Al for MFIS structure is deposited by using thermal evaporation on the whole surface of the backside of the Si substrate in order to reduce the contact resistance. The crystalline structure is investigated by standard X-ray diffraction (XRD) analysis with CuKα radiation at 30 kV and 20 mA. The thickness, microstructure and the surface morphology of SBT thin films is examined by field emission scanning electron microscopy (FESEM Hitachi model S4700). The CeO_2 thickness about 20 nm is measured by ellipsometry meter. The ferroelectric properties of Pt/SBT/Ir/SiO_2/Si, Pt/SBT/STO/Ir/SiO_2/Si samples are measurement by RT-66A (Radiant Technologies, Inc) with MIM structure. The current-voltage (I-V) measurements are performed by measuring the current through the sample with a Agilent 4155C semiconductor parameter analyzer. The leakage current of SBT thin films are measured with a voltage step of 0.1 V and elapsed time 10 sec. The C-V characteristic is measured at 100 kHz for the Pt/SBT/CeO_2/p-Si, Pt/SBT/STO/CeO_2/p-Si structure. The capacitance is measured at 100 kHz as a function of voltage from positive to negative bias.

6-3. Results and Discussion

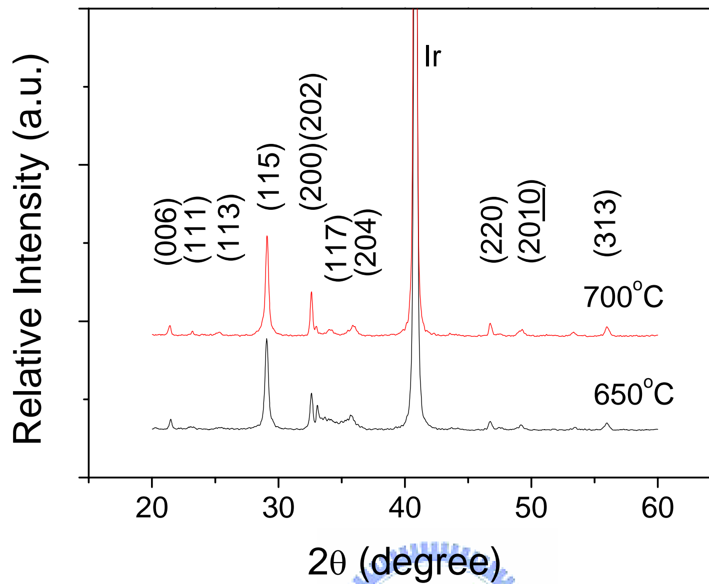


Fig. 6-1 XRD pattern of SBT thin films on Ir/SiO_2/Si substrate annealed at various temperatures.

Figures 6-1 show the x-ray patterns of SBT thin film is deposited on Ir/SiO_2/Si substrate and annealed at 650-700 ℃ for 10 min. The SBT thin films shows perfectly SBT single phase at those annealing temperatures. Figure 6-2 shows XRD patterns of SBT thin films is deposited on STO/Ir/SiO_2/Si and annealed from 600 to 700℃ for 10 min. The SBT thin films crystallized above 600℃ exhibited a high crystallinity and a random orientation with a relatively higher (115) diffraction intensity. The role of STO layers present to lower the processing temperature and enhance the crystallinity for SBT thin films. The STO thin film selected as a seeding layer

which has a similar perovskite structure is very match with the SBT film, and offers a nucleation site to reduce the activation energy for crystallization, leading to the lower processing temperature. The SBT thin films deposited on $CeO_2/SiO_2/Si$ substrate and with STO seeding layer also shows perfectly SBT single phase at 700℃ annealing temperature (show in Fig.6-3). The insertion of a STO seeding layer between the SBT layer and the substrate exhibited a random orientation with a relatively high (006) and (115) diffraction intensity on MFIS structure.

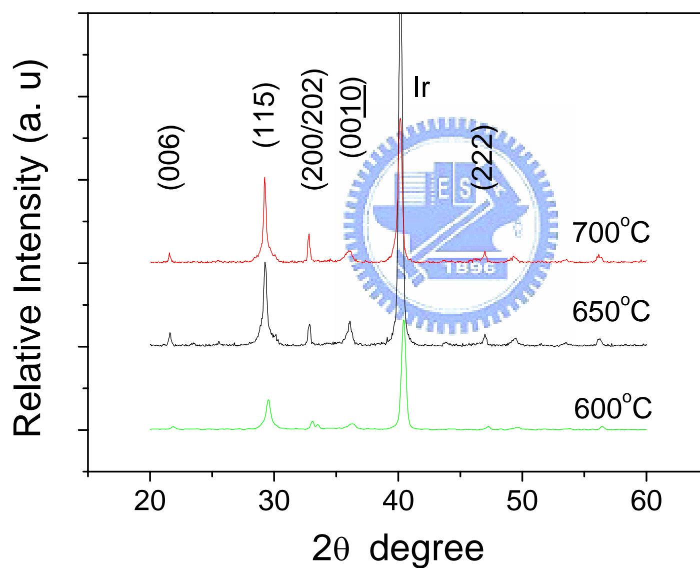


Fig. 6-2 XRD pattern of SBT thin films on $STO/Ir/SiO_2/Si$ substrate annealed at various temperatures.

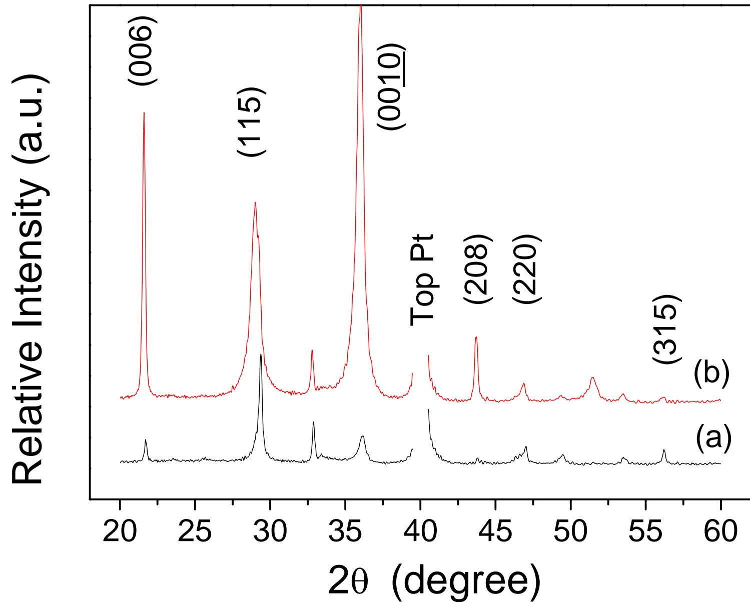
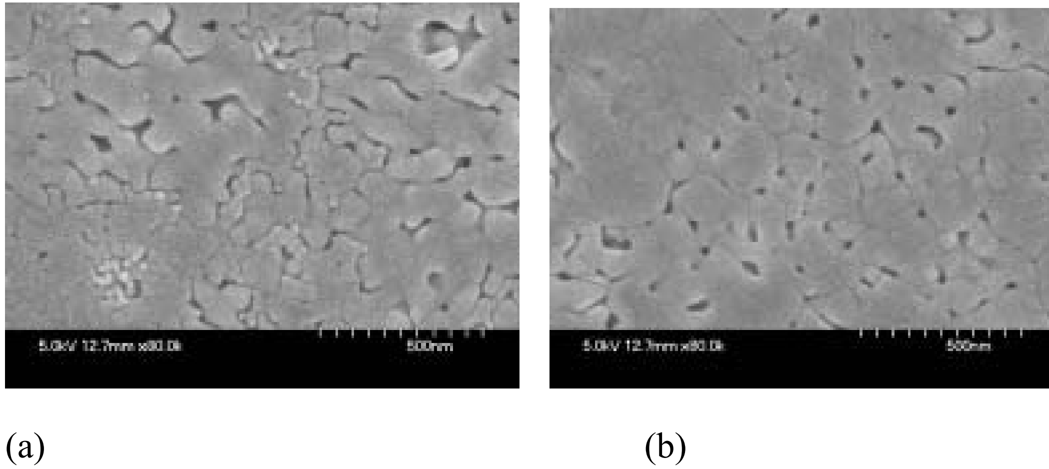


Fig. 6-3 XRD pattern of SBT thin films deposited on (a) CeO_2/Si substrate and (b) with STO seeding layer annealed at 700°C.

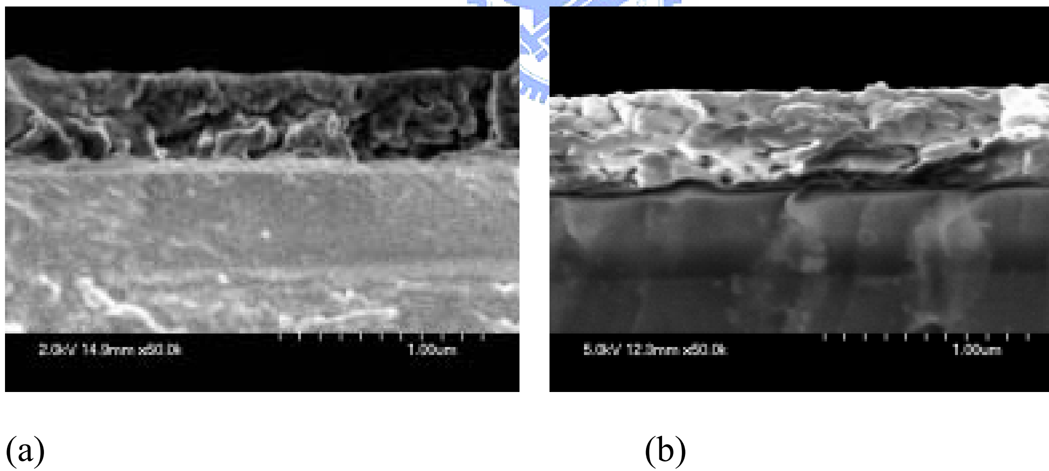
Figure 6-4 shows the SEM micrographs of the SBT thin films deposited on CeO_2/Si substrates and with STO seeding layer insertion annealed at 700°C. The surface morphology of the films shows flat and very smooth grain structure. The SBT thin film with a STO seeding layer exhibited a homogeneous microstructure and larger grains sizes. The image also shows the surface of SBT thin films deposited on CeO_2/Si substrate without STO seeding layer, which consisted of some fine grains in the films. It evident the SBT thin film with STO seeding layer can promote the grain growth of SBT during annealing. The cross section image shows the thickness of SBT thin films and with STO seeding layer. The thickness of SBT thin film and oxide

layer annealed at 700°C are about 400 nm and 20 nm, respectively (show in Fig.6-5).



(a) (b)

Fig. 6-4 SEM micrograph of SBT thin film (a) without STO seeding layer (b) with STO seeding layer on MFIS structure annealed at 700°C.



(a) (b)

Fig. 6-5 SEM cross section micrographs of SBT thin film (a) without STO seeding layer (b) with STO seeding layer on MFIS structure annealed at 700°C.

Figure 6-6 show well-saturated hysteresis loop of SBT thin film

annealed at 700°C for 10 min in MIM structure. Figure 6-7 shows the P-E hysteresis loop of SBT thin films deposited on STO seeding layer with various annealed temperature from 600 to 700°C for 10 min in oxygen ambient. The SBT capacitors showed well-saturated hysteresis loop annealed at 700 °C for 10 min. However, the SBT films annealed at 700°C with seeding layer exhibited lower ferroelectric properties than without STO seeding layer. The reason is that the applied field would be divided among SBT thin film and STO seeding layer; the applied field on the SBT thin film with STO seeding layer would be lower than without seeding layer. Then the ferroelectric properties of SBT thin film with STO seeding layer would be lower than without STO seeding layer. Another reason of the degradation of ferroelectric properties may be due to the formation of a fluorite phase near the STO seed layer. These phenomena also appeared in the SBT thin film deposited on Pt/Ti/SiO_2/Si substrate with $SrTa_2O_6$ seeding layer, which is reported by Hayashi et al [128]. The STO seeding layer in the Pt/SBT/Ir/SiO_2/Si capacitor plays an important role in controlling the bismuth of SBT thin film diffused into the Ir/SiO_2/Si substrates, crystallinity and grain growth, which would also degrade the electronic properties of SBT thin film.

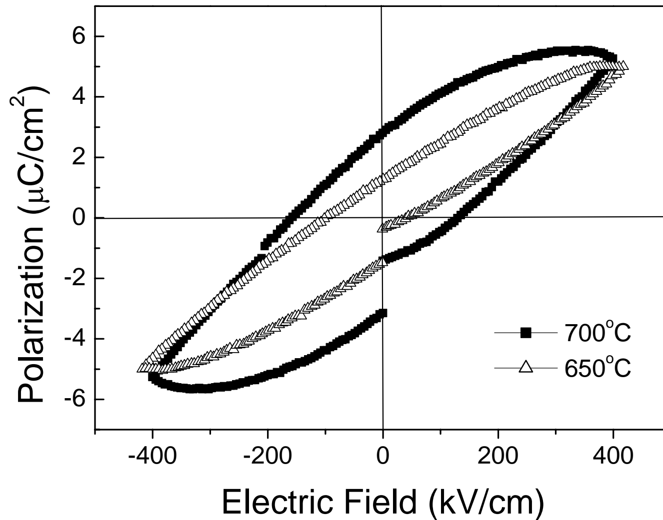


Fig. 6-6 P-E hysteresis loops of SBT thin films without STO seeding layer on MIM structure annealed at 650℃ and 700℃.

The C-V curve due to the dipole switch in the MFIS structures appears as a clockwise loop under a to-and-fro sweeping voltage for p-type substrate. Fig.6-8 illustrates a typical C-V behavior for the MFIS structure with a ferroelectric semiconductor where the gate is negative to the p-type film. As shown in Fig.6-8, clockwise hysteresis loops are clearly observed as traced by arrows, indicating that the memory effects were due to ferroelectric domain reversion and not due to charge injection. It is also found that the capacitance changes rapidly, which indicates good interface properties. The memory window of SBT films on the CeO_2 was 1.2 V at ±5 V sweep voltages. The memory window of SBT thin film with STO seeding layer was larger than SBT thin film deposited on CeO_2. There will be probably several positive

roles when STO is inserted between SBT and CeO_2/Si substrate. First, the STO seeded layer acted as a good block for bismuth diffusion which will effectively depress the loss of bismuth in SBT film and lead to non degraded electronic properties. Second, the STO seeded layer lower down the crystallization temperature of SBT, making the SBT ferroelectric phase well developed. Since the gate voltage was divided among the SBT, the CeO_2 layers, and the silicon substrates, the applied voltage of ferroelectric layer to insulator layer ratio is equated to the capacitance of insulator layer to ferroelectric layer ratio. The capacitance of insulator with STO seeding layer was larger than that without STO seeding layer. That is the higher capacitance of the ultra-thin STO seeding layer provided by thinner films and higher permittivity leads to the increase in the voltage across the SBT layer resulting in an increase in the memory window. Another reason is that the SBT thin film with STO seeding layer will easily obtain larger coercive field than without STO seeding layer as shown in Fig.6-6, 6-7, which also may contribute to the increase in the memory window, because the memory window is equal to about 2Ec (coercive field). The difference in initial capacitance of SBT thin films between two states is that the thicker STO layer makes the total capacitance smaller.

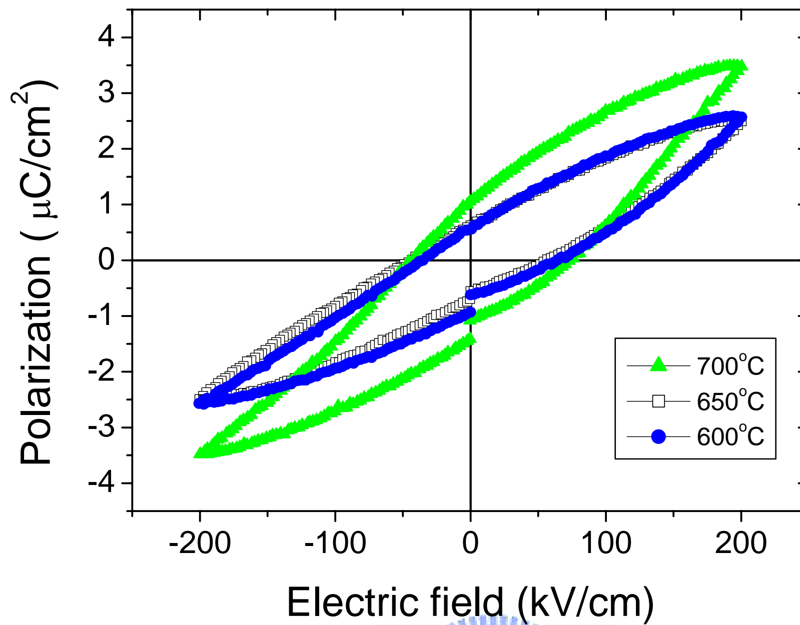


Fig. 6-7 P-E hysteresis loops of SBT thin films with STO seeding layer on MIM structure annealed at various temperatures.

Kanashima et al. [129] reported that the thickness of ferroelectric or insulator layer for the MFIS structure plays an important role in the performance. That is, the maximum memory window width can be obtained by adjusting the thickness of insulator and ferroelectric layer to a suitable range. The equivalent oxide thickness (EOT) of the STO/CeO_2 layer used in this work is about 7-8 nm. The memory window with STO seeding layer was obtained at about 2.6 V under ±5 sweep voltage, which is better than the without STO seeding film.

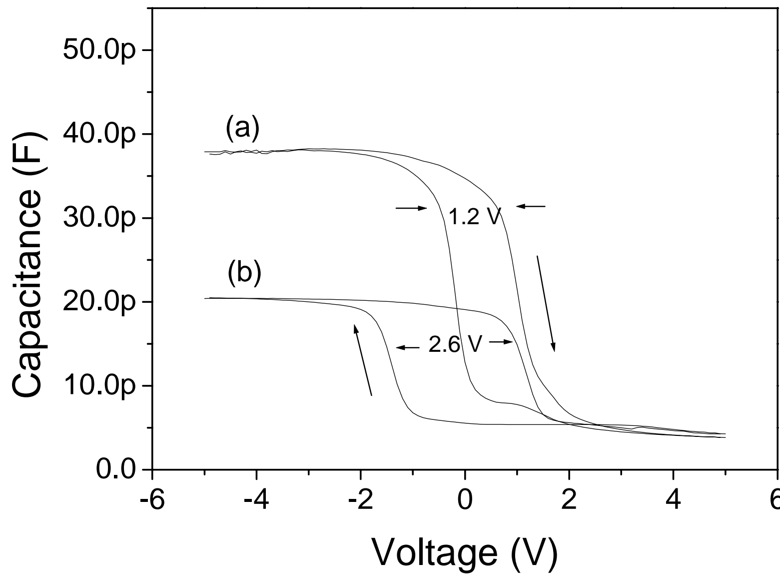


Fig. 6-8 C-V characteristic of the SBT thin films (a) without seeding layer and (b) with seeding layer on MFIS structure annealed at 700℃.

Figure 6-9 shows the leakage current densities of the SBT thin films with seeding layer and without seeding layer annealed at various temperatures on MIM structure. The leakage current of SBT thin films with STO seeding layer shows very low value of 10^{-9} A/cm^2 at 100 kV/cm electric field (Fig.6-9). The SBT thin film with STO seeding layer also shows almost same leakage current density at various annealed temperature. The film without STO seeding layer has higher leakage current density of about one order of magnitude than that with STO seeding layer. The leakage current characteristics of the thin film capacitor depend upon several factors such as the top and bottom electrode interface, surface roughness, and polarization of ferroelectric film. It means

that the SBT thin films with STO seeding layer would improve the interface state. The leakage current behavior greatly depends on the roughness of the films and increases with increasing films roughness. The homogeneous nucleation in the STO seeding layer was considered to result in the smooth morphologies of the SBT thin films as shown in Fig.6-4. Figure 6-10 show the leakage current density of SBT thin film for MFIS structure with STO seeding layer and without STO seeding layer annealed at 700℃. The leakage current density of MFIS structure with STO seeding layer is lower than that without STO seeding layer at low sweep voltage. The contribution to reduce the leakage current by the seeding STO layer is believed to be from the polarization of the ferroelectric layer.

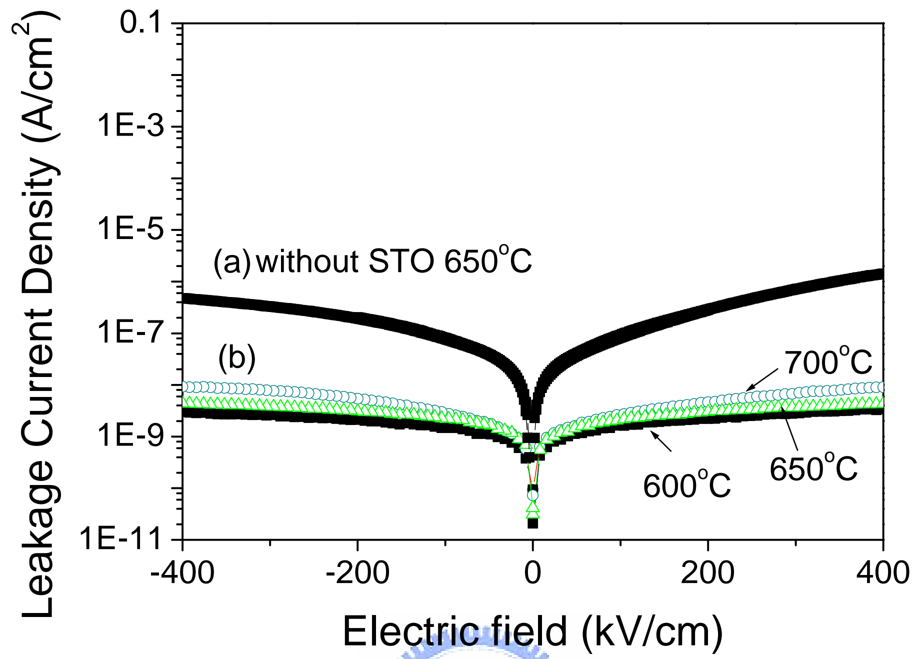


Fig. 6-9 The leakage current density of the SBT thin films on MIM structure (a) without seeding layer (b) with seeding layer annealed at various temperatures, respectively.

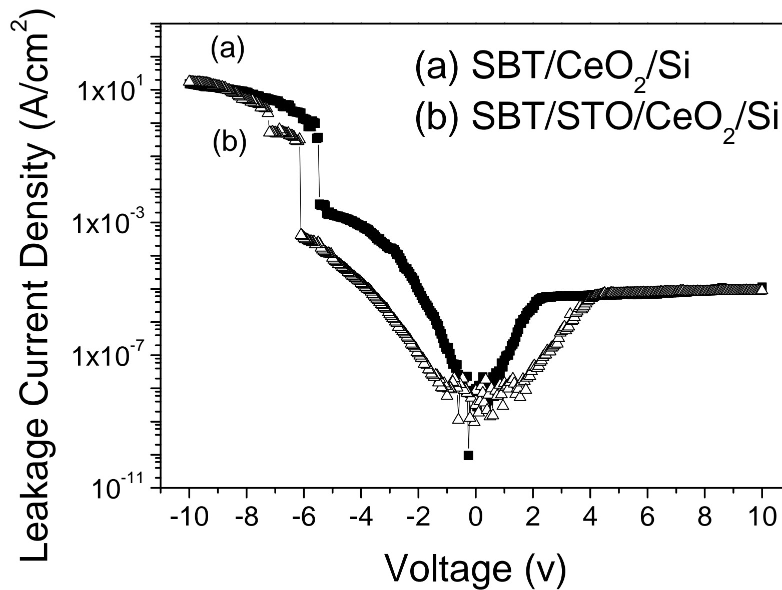


Fig. 6-10 The leakage current density of the SBT thin films on MFIS structure (a) without seeding layer (b) with seeding layer annealed at 700°C.

It is found that the ultra thin STO seeding layer significantly increased the memory window size. This is because the higher capacitance of the ultra thin seeding layer, provided by thinner films and higher permittivity, leads to the increase in the voltage across the SBT film resulting in an increase in the memory window.

The retention characteristics are also found to improve when using the ultra-thin STO seeding films in MFIS structure. After a write gate voltage large enough to saturate the memory window is applied with negative and positive polarity, the time dependence of the capacitor is measured under the hold condition of gate voltage, -1 V. The retention time is defined as the

duration required for positive bias to become equal to negative bias. Figure 6-11 shows the comparison of the measured retention characteristics between STO seeding layer and without STO seeding layer for SBT thin film in MFIS structure. The retention time of the MFIS capacitor with STO seeding layer is slightly longer than that of the MFIS capacitor without STO seeding layer. This improvement is attributed to the reduction of depolarization field due to the higher capacitance in STO seeding layer. It is concluded that SBT thin films with STO seeding layer can successfully improve the retention characteristics. But the measured retention time is still insufficient for non volatile memory application. The short retention time could be mainly to carrier injection into traps inside SBT films caused by the diffusion of SBT components into the interfacial reaction layer, leading to the decrease in the amount of the polarization.

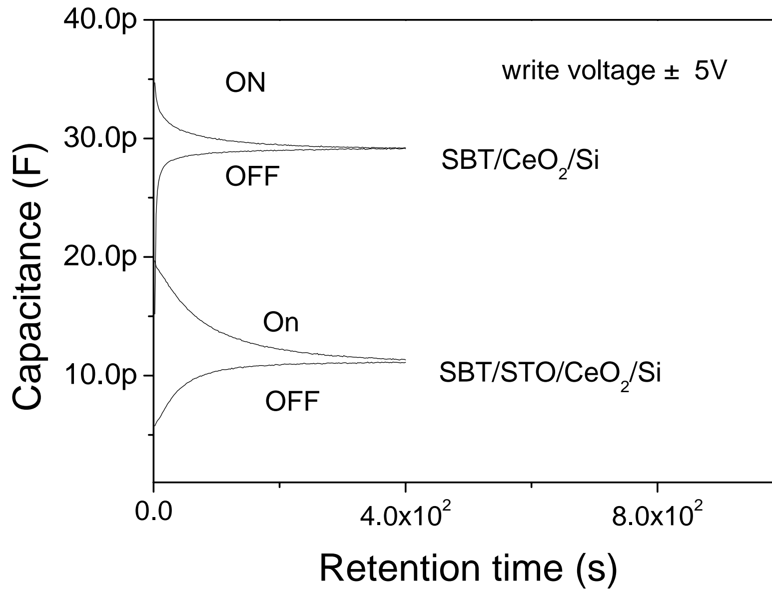


Fig.6-11 Retention characteristics of SBT thin film in the MFIS structure with STO and without STO seeding layer annealed at 700℃.

6-4. Summary

The SBT thin films were prepared by the MOD method with STO seeding layer and without seeding layer on MFIS and MIM structures. Their microstructure, crystal phase and ferroelectric property were investigated. The SBT thin film with STO seeding layer could be obtained in well crystallized SBT phase annealed at 600℃ on MIM structure. The SBT thin film with STO seeding layer can decrease the crystallization temperature and leading to the formation of single-phase SBT thin films with a relatively high (115) diffraction intensity on MIM structure. The SBT thin film with STO seeding layer also can be obtained in well crystallized single-phase SBT thin films

with a relatively high (008) and (115) diffraction intensity on MFIS structure. The memory window of the SBT thin film for MFIS structure deposited on CeO_2 is about 1.2 V at ±5 V sweep voltage. The memory window of the SBT thin film with seeding STO layer is 2.6 V. The leakage current of SBT thin film with STO seeding layer is about 1×10^{-9} A/cm^2 at 100 kV/cm. The leakage current of SBT thin film have the same value at various annealing temperatures. The leakage current density for MFIS structure of SBT thin film deposited on $STO/CeO_2/Si$ is lower than that deposited on CeO_2/SiO_2 substrate. The retention time of the MFIS capacitor with STO seeding layer is slightly longer than that of the MFIS capacitor without STO seeding layer.