Chapter 8

Dielectric and Electrical properties of $SrTiSi_xO_{3\pm2y}$ thin film-based MIM capacitors

8-1. Introduction

As the microelectronics industry continues to decrease the dimensions of integrated circuits, high dielectric constant materials is needed to replace SiO_2 for charge storage application in 1-4 Gb dynamic random access memory (DRAM) devices and to accommodate the increasing complexity of ultralarge scale integrated circuits. Silicon oxide and silicon nitride are commonly used in conventional MIM capacitors which can provide good-voltage linearity and low temperature coefficients, but their capacitance density will be limited due to low dielectric constants. Further reduced dielectric thickness can increase the capacitance density, but it will result in large leakage current and poor voltage linearity. Therefore, to adopt high-k dielectric materials seems to be an alternative way to provide good electrical performances, increase the circuit density, and reduce the cost as well. The high-k materials should satisfy various requirements such as low leakage current, thermodynamic stability on substrate, low interface defect density, and so on. There are many metal oxides such as Ta_2O_5 [138], Al_2O_3 [139], $SrTiO_3$ [140], ZrO_2 [141], and HfO_2 [142-143] that have been proposed with high dielectric constants that range from 10 to 80. Among those

materials, $SrTiO_3$ has emerged as an alternative high dielectric material for high-density dynamic random access memories (DRAM) replacing a conventional SiO_2 or Si-O-N dielectric material.

In order to obtain low leakage currents, it is important to find a dielectric material which remains amorphous during post-processing treatments, since large crystalline grain may serve as high leakage paths. More recently, investigations of amorphous ZrO_2-SiO_2 and HfO_2-SiO_2 alloys have been reported. An analysis of the phase diagram for the Zr-Si-O system, predicts that the metal oxide ZrO_2 as well as the compound silicate $ZrSiO_4$ will be stable in direct contact with Si. A value of ε=12.6 for $ZrSiO_4$ is reported by Blumenthal [144], which is reasonable considering that this structure is comprised of SiO_2 (ε=3.9) and ZrO_2 (ε=25) components. Similarly, $HfSiO_4$ compound is expected to have a dielectric constant in the range of ε=15-25. Considering all of the desired properties, $HfSi_xO_y$ and $ZrSi_xO_y$ should be excellent materials candidates for advanced gate dielectrics.

Strontium titanate (STO) is a cubic perovskite type crystal with a lattice constant of 3.905 Å. It is electrically an insulator and its dielectric constant is as high as 300 at room temperature. It is worth to investigate the STO with SiO_2 content in order to better understand the electrical and physical properties. In this letter, the electrical and physical properties of The $SrTiSi_xO_{3\pm2y}$ thin films which were synthesized by CSD method in MIM structure were investigated. It shows that the leakage current density and dielectric constant of $SrTiO_3$ thin films were strongly affected by SiO_2 content.

8-2. Experimental

The $SrTiSi_xO_{3\pm2y}$ thin film with SiO_2 content x=0-0.45 was prepared on Pt/Ti/SiO_2/Si substrate by a chemical solution deposition method. The precursor solution was made by alkoxide-carboxylate complexes. Strontium acetate [$Sr(CH_3COO)_2$], Silicon ethoxide [$Si(OC_2H_5)_4$] and titanium ethoxide [$Ti(OC_2H_5)_5$] were selected as starting materials, and acetic acid and ethylene glycol were selected as solvent. Strontium acetate was initially dissolved into dehydrated acetic acid and ethylene glycol solution which was sealed in a reflux flask under nitrogen gas. The solution was heated to 120℃ for 1 hour, and then titanium ethoxide and Silicon ethoxide were added to the solution to form a clear and stable precursor solution at 70℃ for 1 hour.

The precursor solution with a concentration of 0.25mol/L was spin-coated on Pt/Ti/SiO_2/Si substrates. The coated thin film was dried at 150℃ for 10 min, and then 400℃ for 60 min in conventional furnace to remove organic complex. This step was repeated several times until the desired thickness was obtained. The films with various Si contents were annealed at temperatures ranging from 600 to 900℃ in an oxygen atmosphere for 1 min. The thickness of $SrTiSi_xO_{3+2y}$ films is about 110±10 nm which was observed on the basis of scanning electron microscopy (SEM) analysis (show Fig. 8-6(c)). The 50 nm thick Pt top electrodes were then deposited on the films by sputtering through a shadow mask of an area of 9.6×10^{-4} cm^2.

The capacitance was measured at 100 kHz as a function of voltage

from negative to positive on the films in a metal-insulator-metal capacitor configuration with a HP 4284A impedance analyzer. The dielectric constant of $SrTiSi_xO_{3\pm2y}$ thin films was calculated from the capacitance measured at 100 kHz at zero bias voltage. The leakage current characteristics of $SrTiSi_xO_{3\pm2y}$ thin films were measured with a voltage step of 0.01 V and elapsed time of 30 s by using a HP 4146C semiconductor parameter analyzer. The cross section and surface morphology of the thin films annealed at various temperatures were measured by a field emission scanning electron microscope (FESEM, Hitach S4700) and transmission electron microscopy (TEM). The X-ray diffraction (XRD) patterns were recorded using a Hitachi X-ray diffractmeter with Cu Kα radiation and Cu filter operating at power levels of 30 kV, 20 mA to investigate the crystallinity and the phases of $SrTiSi_xO_{3\pm2y}$ thin films. The x-ray photoelectron spectroscopy (XPS) measurements were carried out in a Physical Electronics ESCA PHI 1600 spectrometer at constant pass energy of 23.5 eV. An Ar^+ ion beam was used to etch the films for 1 min to obtain the depth profiles of the films.

8-3. Results and Discussion

Figure 8-1 shows the x-ray diffraction (XRD) patterns of $SrTiO_3$ thin films as deposited at 400℃ and annealed at various temperatures in an oxygen atmosphere. It showed the typical diffraction peaks of STO phase as (110) and (200), when STO thin film was annealed above 800℃. Although the peak intensity of the diffraction pattern didn't appear to be dependent on temperature in Fig.8-1, the grain growth of $SrTiO_3$ thin film

could be observed with increasing temperature as derived from SEM micrograph of Fig.8-5. The crystallinity of the perovskite-type $SrTiO_3$ phase seemed to increase with increasing annealing temperature. Figure 8-2 shows the x-ray diffraction analysis (XRD) patterns of $SrTiSi_xO_{3\pm2y}$ thin films with various Si content as deposited at 400℃ in air. It indicated that were no the appearance of the diffraction peaks of STO phase with exception of those due to the substrate Si and Pt. Figure 8-3 shows the x-ray diffraction patterns of $SrTiSi_xO_{3\pm2y}$ thin films with x=0.25 and 0.45 at various annealing temperatures. The crystallinity of perovskite-type phase increased with increasing annealing temperature of $SrTiSi_xO_{3\pm2y}$ thin film up to about 800℃. The corresponding SEM analysis of the film confirmed the improving in crystallinity (shown in Fig.8-6). That means the Si content did not decrease the crystallization temperature, but depressed the grain growth as shown in Fig.8-6.

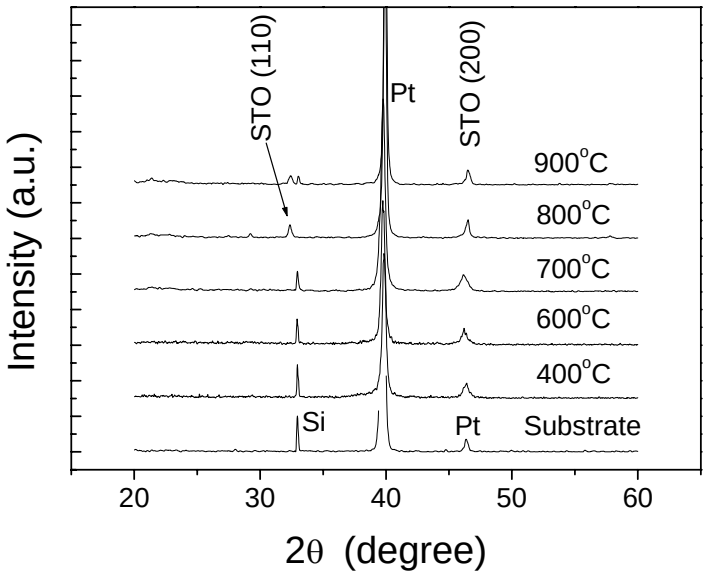


Fig. 8-1 XRD pattern of $SrTiO_3$ thin films annealed at various temperatures.

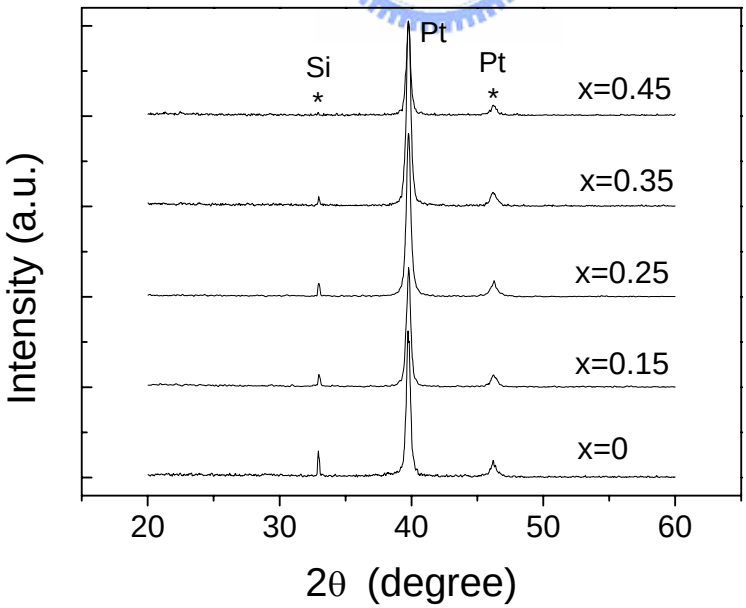
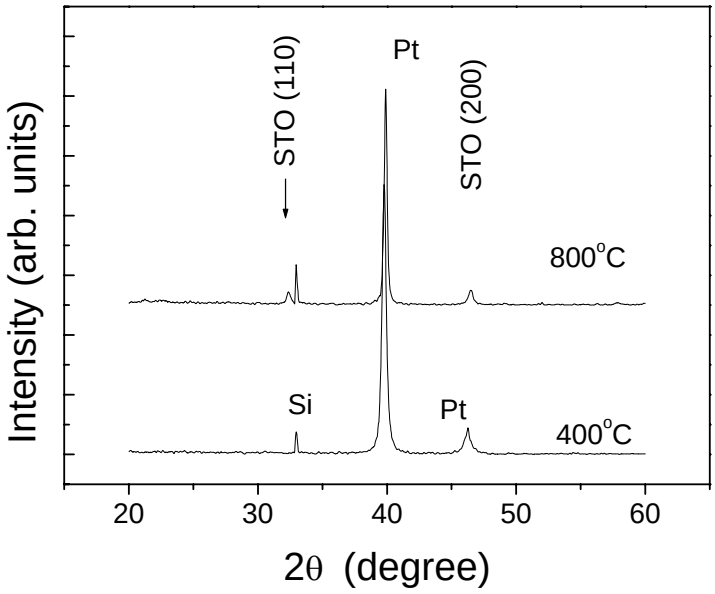
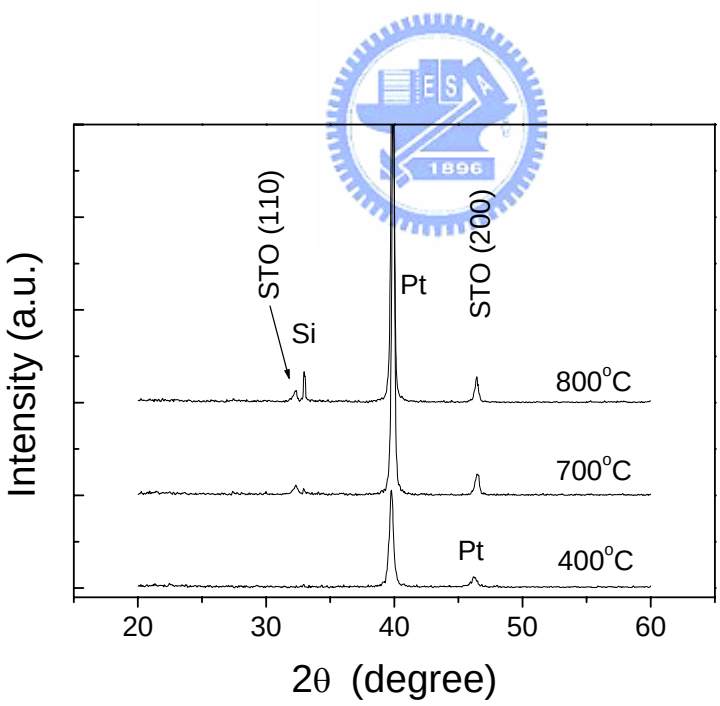


Fig. 8-2 XRD patterns of $SrTiSi_xO_{3\pm2y}$ thin films with various mole ratios of SiO_2 as deposited at 400℃.



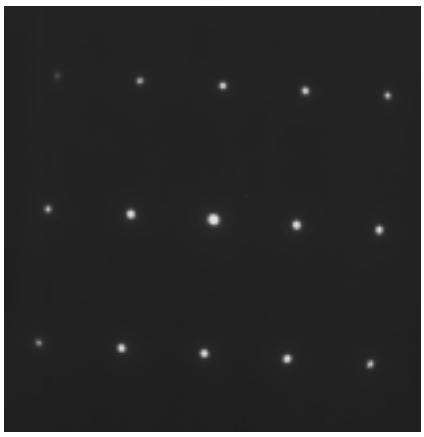
(a)



(b)

Fig. 8-3 XRD patterns of $SrTiSi_xO_{3\pm2y}$ thin films with (a) x=0.25 and (b) x=0.45 as deposited at 400℃ and annealed various temperatures.

Figure 8-4(b) shows the TEM micrograph of $SrTiO_3$ thin films annealed at 800℃, the electron diffraction pattern in figure 8-4(a) also shows the crystalline diffraction spot which is coincident with x-ray diffraction pattern. The TEM micrograph of $SrTiSi_xO_{3\pm2y}$ thin films were shown in Fig.8-4(d). The $SrTiSi_xO_{3\pm2y}$ thin film also obviously exist the perovskite phase at 800℃ annealed temperature. Figure 8-4(c) is the electron diffraction pattern of $SrTiSi_xO_{3\pm2y}$ thin films annealed at 800℃, which also showed the similar as the crystalline diffraction spot of $SrTiO_3$ thin film. From the Fig. 8-4(a) and Fig. 8-4(b), it also can be found that the grain size of STO phase is larger than that of $SrTiSi_xO_{3\pm2y}$ at the same annealed temperature.



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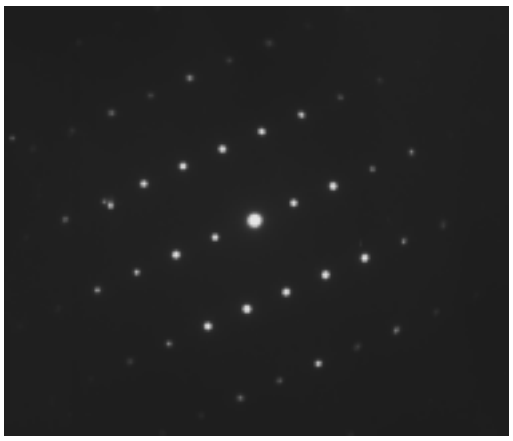
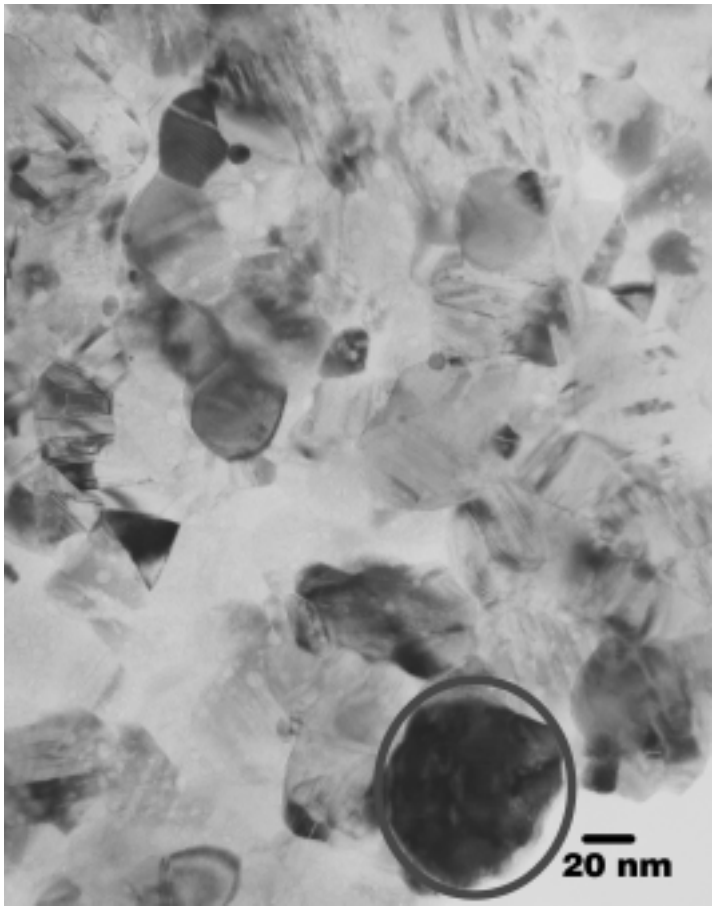
(a)

(b)

Fig.8-4 (a) TEM micrograph and (b) the electron diffraction pattern of $SrTiO_3$ thin films annealed at 800℃.



(c)

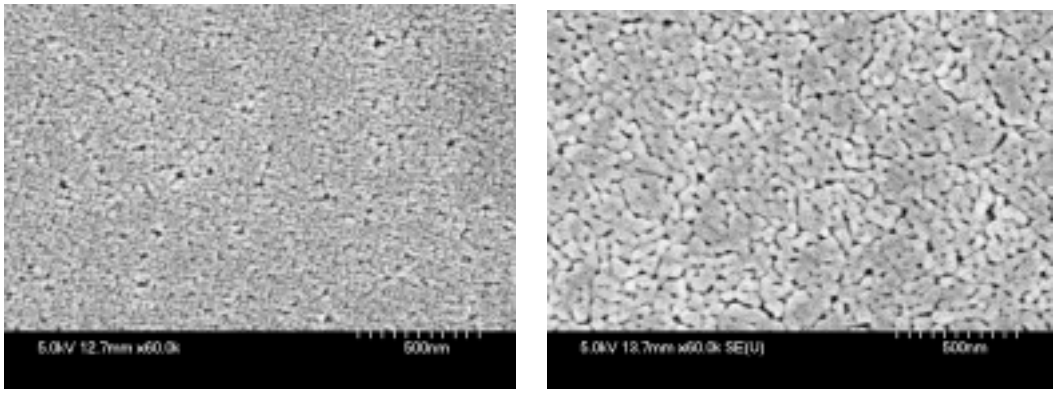


(d)

Fig.8-4 (c) TEM micrograph and (c) the electron diffraction pattern of $SrTiSi_xO_{3\pm2y}$ thin film with x=0.25 annealed at 800℃.

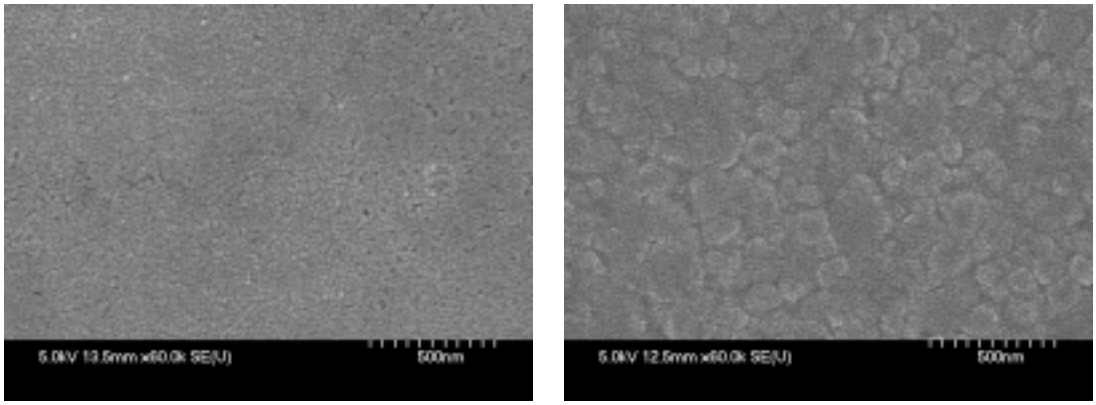
Figure 8-5 shows the SEM surface images of $SrTiO_3$ thin films as

deposited at 400℃ and annealed at 800℃, respectively. Surface morphology is important physical property which may affect the electrical properties of dielectric thin films. The $SrTiO_3$ thin films show the smooth and crack-free surface. It also showed that the grain size was increased with increasing annealing temperature. Figure 8-5 shows the cross section and surface micrograph of $SrTiSi_xO_{3\pm2y}$ thin film with x=0.25 deposited at 400 ℃ and annealed at 800℃. From the SEM image of Fig.8-5(a) and 8-6(a), it can be seen that the Si content would minimize the grain size and improve the density of $SrTiSi_xO_{3\pm2y}$ thin film. That means the Si could depress the STO grain growth and increase the total grain boundary which act as an amorphous phase and lead to a lower leakage current. The thin film with Si content seems to improve the micrograph. It is believed that the thin film prepared at an elevated temperature could enhance the crystal growth during annealing and thus improve the crystallinity of $SrTiSi_xO_{3\pm2y}$ thin film.



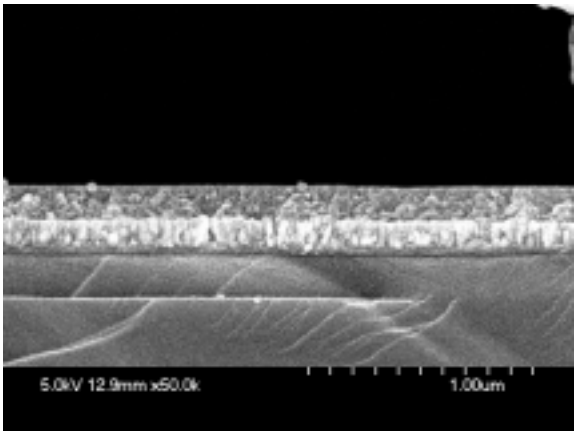
(a) (b)

Fig. 8-5 SEM micrographs of surface morphology of $SrTiO_3$ thin films (a) deposited at 400℃ and (b) annealed at 800℃.



(a) (b)

Fig. 8-6 SEM micrographs of $SrTiSi_xO_{3\pm2y}$ thin film with x=0.25 (a) deposited at 400℃ and (b) annealed at 800℃.



(c)

Fig. 8-6 SEM micrographs of $SrTiSi_xO_{3\pm2y}$ thin film with x=0.25 (a) deposited at 400℃and (b), (c) annealed at 800℃.

Figure 8-7 shows the plot of dielectric constant versus Si content for the $SrTiSi_xO_{3+2y}$ thin films at various annealing temperatures. The dielectric constants of the $SrTiSi_xO_{3\pm2y}$ thin films decreased with an increase in Si content at same annealing temperatures and increased with

increasing annealing temperature. The dielectric constant of the $SrTiSi_xO_{3\pm2y}$ thin films increased with increasing annealing temperature which was owing to the crystalline growth and crystallinity of STO phase.

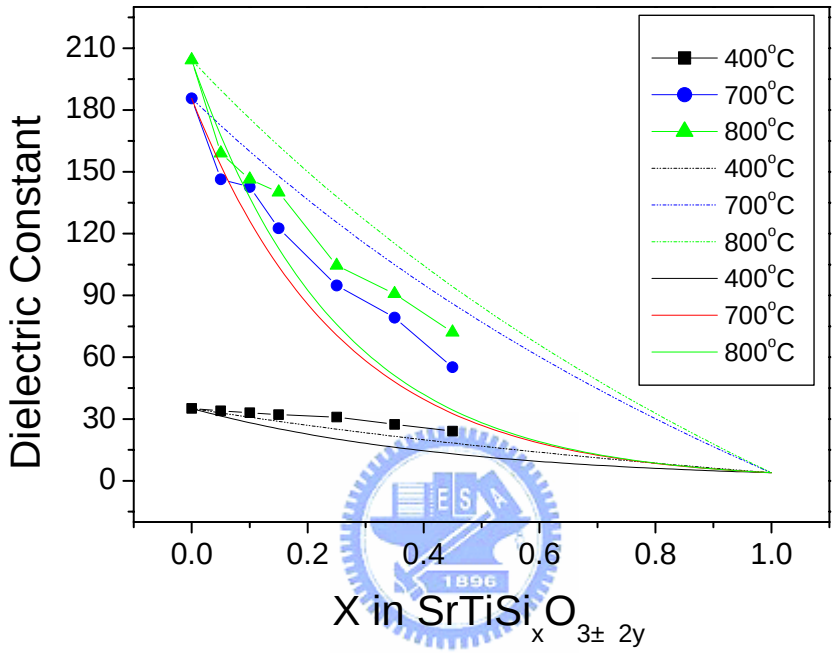


Fig.8-7 Dielectric constant at zero bias versus SiO_2 mole ratio of $SrTiSi_xO_{3+\delta}$ thin film annealed at various temperatures indicated, the dash line and solid line was fitted with SiO_2 as dispersion phase by equation (1) and (2) , respectively.

The better the crystallinity of STO phase in thin films, the higher the dielectric constant of $SrTiSi_xO_{3\pm2y}$ thin films. It has been reported [147] that higher temperature will increase the crystalline quality of the growing STO films. The dielectric constant would increase with the improvement of crystallinity of the STO phase or with increasing

annealing temperature. The high dielectric constant is the result of the displacement of the Ti ion and asymmetry of the Ti-O bond lengths in the oxygen octahedron. Kingon [145] has investigated (1-x)HfO_2-(x)SiO_2 and (1-x)La2O3-(x)SiO2 systems which showed that the more the mole ratio of SiO_2 content in thin films, the higher the crystallization temperature. The dielectric constants of $SrTiSi_xO_{3\pm2y}$ thin films are depended on crystallization temperature and Si content. The dielectric constant of the $SrTiSi_xO_{3\pm2y}$ thin films decreased with increasing Si content, which may be due to the mixing of two materials. The relationship between dielectric constant and Si content was very similar to the dispersion of lower dielectric constant materials into higher dielectric constant matrix materials. The dielectric constant of the $SrTiSi_xO_{3\pm2y}$ thin films decreased with increasing Si mole ratio, which may be due to the mixing of two phases or formation of a lower dielectric constant phase. The curve in Fig.8-7 was close to the mixing rule of logarithmic expression derived from Maxwell equation as shown by Kingery [9]. The logarithmic equation is

$$\log k=\Sigma v_i \log k_i, \qquad (1)$$

where v_i is the volume fraction of phase *i* and k_i is the dielectric constant of phase *i*. The Maxwell derived equation is

$$k=\frac{v_m k_m\left(\frac{2}{3}+\frac{k_d}{3k_m}\right)+v_d k_d}{v_m\left(\frac{2}{3}+\frac{k_d}{3k_m}\right)+v_d} \qquad (2)$$

where v_m, v_d is the volume fraction of the matrix and dispersed phase and k_m and k_d are the dielectric constants of matrix and dispersed phase,

respectively.

We chose the STO (ε=experiment value) and SiO_2 (ε=3.9) as two mixing phases, respectively. By using the above equation, the derived dash and solid lines are shown in Fig.6. The experimental values of $SrTiSi_xO_{3\pm2y}$ the thin films with various Si content annealed at 700℃ and 800℃ lie just between those fitted lines. The logarithmic rule considered the two mixing phases based on layered material and Maxwell equation was derived from the assumption of the dispersed spherical particles in a matrix material. In the present study, the $SrTiSi_xO_{3\pm2y}$ thin films with two phases can be considered as between this mode of layered and spherical particle dispersion in matrix.

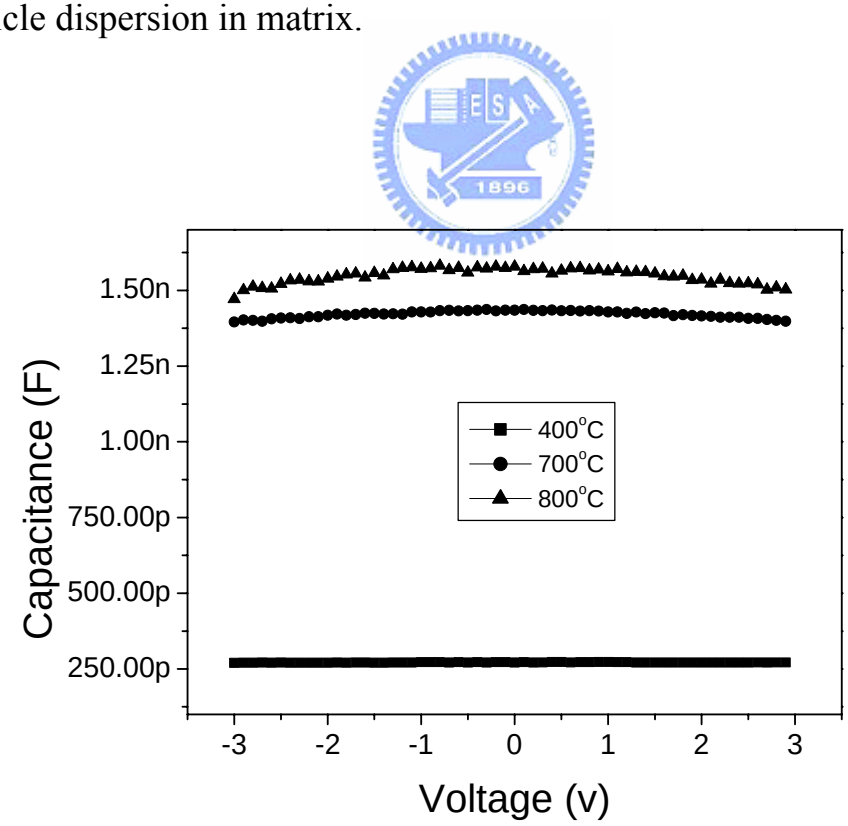


Fig. 8-8 Capacitance vs. applied voltage for $SrTiO_3$ thin film as deposited at 400℃ and annealed at various temperatures indicated.

The C-V characteristics of the $SrTiO_3$ thin films deposited at 400℃ and annealed at various annealing temperatures are shown in Fig.8-8. The capacitance value is constant with various sweep bias voltage which is a paraelectric property. The $SrTiO_3$ thin films show the nonhysteresis effect for films at various annealing temperature. It can be seen that the capacitance value was not affected by the electric field within the region of ± 3V bias and no hysteresis was observed with the increasing and decreasing bias voltage. This indicates that the dielectric films contain no mobile ions and no interface between dielectric layer and metal. It also showed that the capacitance value of the $SrTiO_3$ thin films increased with increasing annealing temperature. That is coincident with the crystallinity of the $SrTiO_3$ thin film. The capacitance value or dielectric constant of the $SrTiO_3$ thin films depended on the crystallinity of the thin film. There seems to appear a non-linear polarization property of the film annealed at 800℃. The $SrTiSi_xO_{3\pm2y}$ thin films with x=0.25 deposited at 400℃ and annealed at various temperatures are shown in Fig.8-9. The $SrTiSi_xO_{3\pm2y}$ thin films with x=0.25 also showed the constant capacitance value at various annealing temperatures and increased with increasing annealing temperature (shown in Fig.8-9).

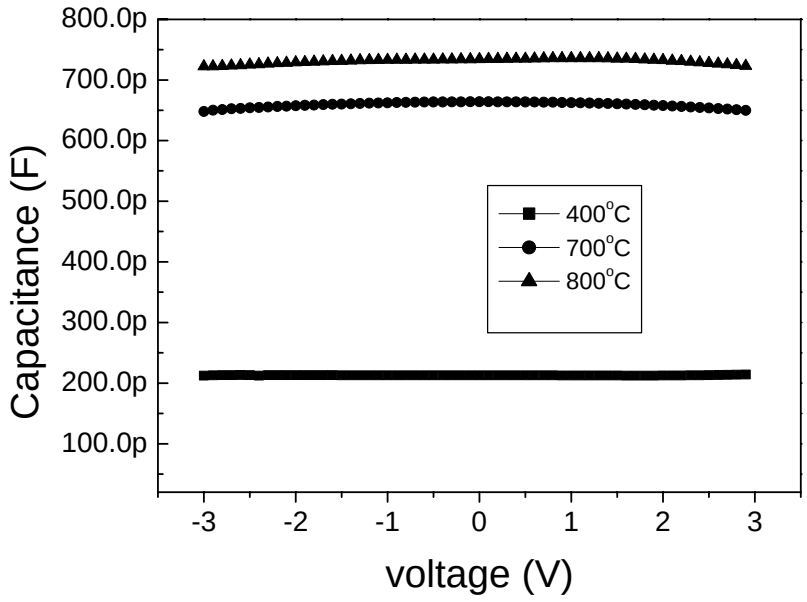


Fig. 8-9 Capacitance with applied voltage for $SrTiSi_xO_{3\pm2y}$ thin film with x=0.25 annealed at various temperatures indicated.

Figure 8-10 shows the leakage current density of 100kV/cm as a function of Si content in the $SrTiSi_xO_{3\pm2y}$ thin film at various annealing temperatures. The leakage current density of $SrTiSi_xO_{3\pm2y}$ thin film decreased with increasing Si content. The leakage current density of $SrTiSi_xO_{3\pm y}$ thin film decreased with increasing x at same annealed temperature. The grain size of $SrTiSi_xO_{3\pm y}$ thin film depressed with Si content. The smaller grain size produces more grain boundaries and contains more resistive than bulk which would lead to lower leakage current in $SrTiSi_xO_{3\pm y}$ thin film. The $SrTiSi_xO_{3\pm y}$ thin film shows the leakage current increased with increasing annealed temperature at same Si content. The higher leakage current property is believed to the

crystallinity of STO phase and increased grain size in $SrTiSi_xO_{3\pm y}$ thin film. The larger grain size would obtain higher leakage current. The films with large grain size also have short conduction paths along the highly resistive grain boundary. The leakage current of thin film with over x=0.25 at same annealed temperature was not deceased with increased Si content but instead of slightly increased, that could be due to the segregation of the highly conductive Si. The result shown in Fig.11 is the XPS spectrum of the Si 2p peak obtained from $SrTiSi_xO_{3\pm y}$ thin film with x=0.45 deposited at 400℃ and annealed at 800℃. The spectrum clearly indicates the coexistence of Si^{+4}, Si^0. The peak at a binding energy of about 101.7 eV corresponds to Si^{4+} of Si-O bonding and the binding energy of about 98.6 eV corresponds to Si^0. The XPS spectrum of $SrTiSi_xO_{3\pm 2y}$ thin film annealed at 800℃ shows the two ionic types simultaneously. The $SrTiSi_xO_{3\pm 2y}$ thin film annealed at 800℃ show Si^{+4} peak represent the Si-O bonding, but the Si^0 peak mainly come from segregation. The segregation of highly conductive Si leads to the leakage current density increase. That was the reason why the leakage current of $SrTiSi_xO_{3\pm y}$ thin film with x higher than 0.45 did not further decrease but instead of slightly increased. The area ratio of Si^0/Si^{4+} annealed at 400℃ is larger than annealed at 800℃ in the XPS spectrum of thin film. This is the reason why the film annealed at 400℃ have higher leakage current density than annealed at 800℃ (shown in Fig.8-12). The relationship

between leakage current density with x content was similar to the dielectric constant to the x content. They show both of that decreased with the reduction x of the $SrTiSi_xO_{3\pm y}$, are mainly decided by the grain size, crystallinity and Si content. It indicated that the leakage current density and dielectric constant of $SrTiSi_xO_{3\pm y}$ thin films strongly depended on the crystallization temperature or annealing temperature and x content.

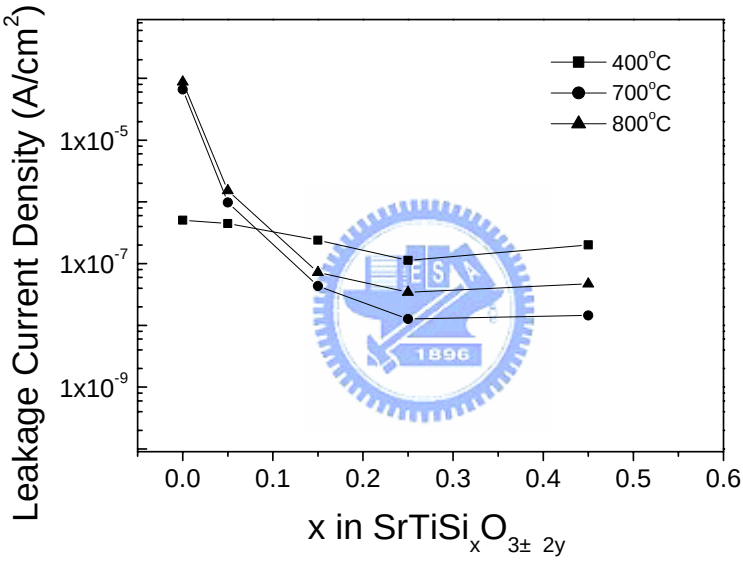


Fig. 8-10 Leakage current density of 100 kV/cm electric field vs. Si content of $SrTiSi_xO_{3\pm 2y}$ thin films annealed at various temperatures indicated.

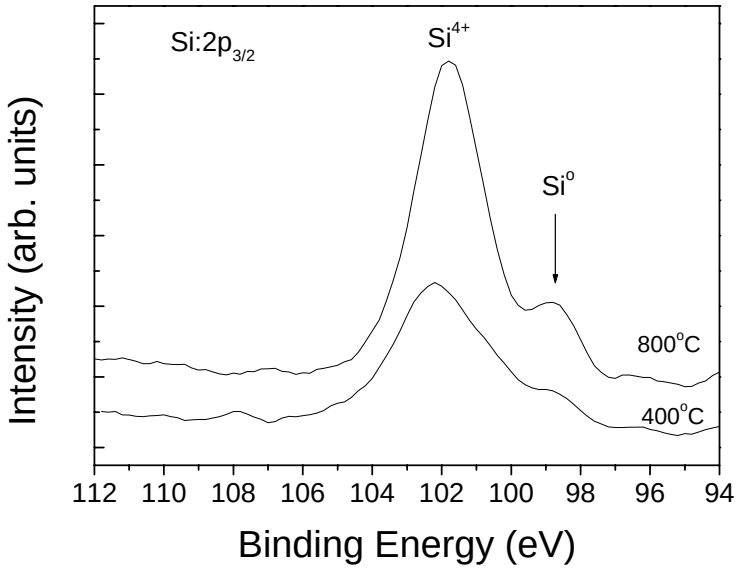


Fig. 8-11 XPS spectrum of the Si 2p 3/2 for the $SrTiO_3$ thin film with x=0.25 deposited at 400℃ and annealed at 800℃.

From Fig.8-7,8-10, the optimal condition of $SrTiSi_xO_{3\pm2y}$ thin films was the $SrTiSi_xO_{3\pm2y}$ with x=0.25 which had a suitable dielectric constant and lower leakage current densitly. The $SrTiSi_xO_{3\pm2y}$ thin film with x=0.25 as deposited at 400℃ and annealed at various temperatures are shown in Fig.8-12. The leakage current density of $SrTiSi_xO_{3\pm y}$ thin films with x=0.25 annealed at higher temperature showed lower than 10^{-7} A/cm^2 at 100 kV/cm. The 400℃ film has high leakage current, which is due to Si segregation and the residual carbon in the film. The leakage current density of the thin film annealed at 700℃ is lower than annealed at 800℃ which is correspondent to crystallinilty or annealed temperature

and $SrTiSi_xO_{3\pm y}$ content. The film annealed at higher temperature produced higher crystallinity, larger grain and has a short leakage path way which leads to a higher dielectric constant and has a higher leakage current.

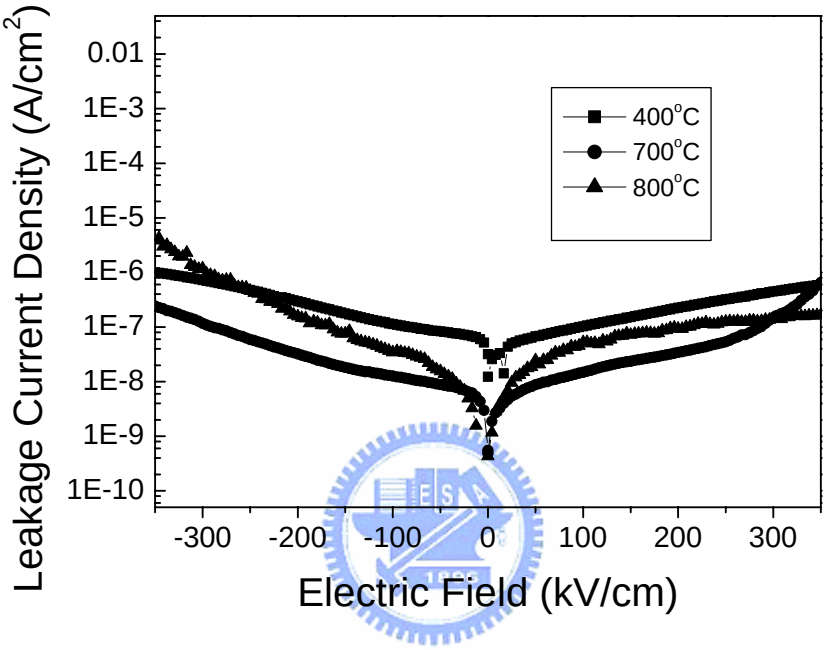


Fig. 8-12 Curves of leakage current density vs. applied voltage for $SrTiSi_xO_{3\pm 2y}$ thin film with x=0.25 annealed at various temperatures indicated.

Figure 8-13 shows the lifetime extrapolation of the $SrTiSi_xO_{3\pm 2y}$ thin films annealed at various temperatures from the dependence of cumulative failure on time-dependent dielectric breakdown (TDDB) stress time. The TDDB curve indicated that all the films operated at an electric field of above 0.6 MV/cm have a lifetime over 10 years. This reliability test indicated that the lower the annealing temperature of the

$SrTiSi_xO_{3\pm2y}$ thin films, the higher the breakdown fields in the films. That is owing to the lower leakage current density of $SrTiSi_xO_{3\pm2y}$ thin film.

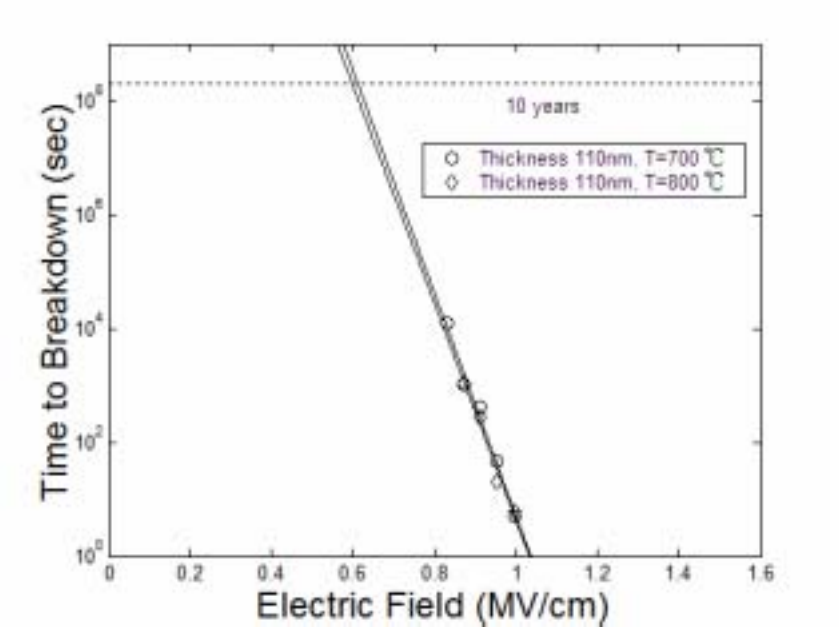


Fig. 8-13 Time-dependent dielectric breakdown for $SrTiSi_xO_{3\pm2y}$ thin film with x=0.25 annealed at 700 and 800°C.

8-4. Summary

The 110 nm $SrTiSi_xO_{3\pm2y}$ thin films were successfully prepared on $Pt/Ti/SiO_2/Si$ substrate by using chemical solution deposition method at various annealing temperature. The x-ray diffraction patterns of $SrTiSi_xO_{3\pm2y}$ thin film annealed at over 800°C exhibit peaks corresponding to the STO crystalline phase. The crystallinity of STO phase for the $SrTiSi_xO_{3\pm2y}$ thin films was not decreased with increased Si content but suppressed the grain growth of STO phase and led to an increase of total grain boundary which acted as highly resistive grain boundary and obtained lower leakage current density. The capacitance or

dielectric constant of $SrTiSi_xO_{3\pm2y}$ thin films showed obvious dependence on crystallinity, annealing temperature and Si content. The crystalline phase, capacitance and dielectric constant of $SrTiO_3$ thin film all gradually increased with annealing temperature. The leakage current density of $SrTiSi_xO_{3\pm2y}$ thin films decreased with an increase in mole ratio of Si content. The dielectric constant of $SrTiSi_xO_{3\pm2y}$ thin films showed the similar trend as leakage current density behavior as, it decreased with increasing mole ratio of Si content. The value of dielectric constant and leakage current density of $SrTiSi_xO_{3\pm2y}$ thin films with x=0.25 annealed at 700℃ have suitable dielectric constant and low leakage current of 94.8 and 1.27×10^{-8} A/cm^2, respectively. The Si content of $SrTiSi_xO_{3\pm2y}$ thin films plays an important role in determining the state of crystallinity and electric properties. The TDDB curve indicated that the $SrTiSi_xO_{3\pm2y}$ films with x=0.25 annealed at 700 and 800℃ operated at an electric field of 0.6 Mv/cm have a lifetime over 10 years.