

Chapter 9

Conclusion and future work

9-1. Conclusion

This chapter will summarize the major contributions of this work as following:

The $\text{Sr}_{0.8}\text{Bi}_{2+x}\text{Ta}_2\text{O}_{9+\delta}$ thin films were synthesized on Ir(50nm)/ SiO_2 (100nm)/Si substrates using MOD method. The $x = 0.4$ films showed a good ferroelectric property, while the $x=0.6$ films had a low leakage current density of 10^{-7} A/cm² at 100 kV/cm. The excess bismuth substituted the Sr site in the Sr-deficient and Bi-excess SBT thin films. There is a possibility of compensation due to the change in Bi ion valency (+3-x) at the Sr site as the substitution occurs.

A single SBT phase of $\text{Sr}_{0.8}\text{Bi}_{2.6}\text{Ta}_2\text{O}_{9+\delta}$ thin film was obtained at a low temperature of 450 °C. The dielectric constant and the polarization versus electric-field hysteresis loop of the SBT films increased with increasing annealing temperature due to the consistent increase in grain size and crystallinity. The leakage current density of SBT thin films decreased as annealing temperature decreased. The thin film annealed at 450 °C has a low leakage current value of 10^{-9} A/cm² at 100 kV/cm applied field.

The memory window of the SBT thin film for MFIS structure deposited on CeO_2 is about 1.2 V at ± 5 V sweep voltage, while the SBT thin film with seeding STO layer is 2.6 V. The leakage current of SBT

thin film with STO seeding layer is about 1×10^{-9} A/cm² at 100 kV/cm and have the same value at various annealing temperatures. The retention time of the MFIS capacitor with STO seeding layer is slightly longer than that of the MFIS capacitor without STO seeding layer.

A higher remanent polarization of BNT ($\text{Bi}_{3.25}\text{Nd}_{0.75}\text{Ti}_3\text{O}_{12}$) thin film successfully obtained on SRO/STO/Si substrate by MOD method. The remanent polarization (Pr) and coercive field (Ec) of the BNT ($\text{Bi}_{3.25}\text{Nd}_{0.75}\text{Ti}_3\text{O}_{12}$) thin film were 58 $\mu\text{C}/\text{cm}^2$ and 104 kV/cm, respectively. The memory window of BNT film was widely than SBT and increased with increasing capacitor area ratios. The retention time of BNT thin film in Pt/BNT/CeO₂/Pt/Ti/SiO₂/Si (MFMIS) structure with capacitor area ratio 16 is about 3200s.

The high dielectric constant $\text{SrTiSi}_x\text{O}_{3+\delta}$ thin films were successfully prepared on Pt/Ti/SiO₂/Si substrate by using chemical solution deposition method. The value of dielectric constant and leakage current density of $\text{SrTiSi}_x\text{O}_{3+\delta}$ thin films with $x=0.25$ annealed at 700 have suitable dielectric constant and low leakage current of 94.8 and 1.27×10^{-8} A/cm², respectively. The TDDB curve indicated that the $\text{SrTiSi}_x\text{O}_{3+\delta}$ films with $x=0.25$ annealed at 700 and 800 operated at an electric field of 0.6 Mv/cm have a lifetime over 10 years.

9-2. Future work

The ferroelectric memory field-effect-transistor (FEMFET) technology has many desirable features, including small cell size,

low-voltage operation, fast programming/erase speed and nonvolatility, making it an attractive alternative to flash and other existing nonvolatile semiconductor memory technologies. However, there also exhibit a short retention time problem to be resolved in ferroelectric memory. Most researchers attribute the relatively short retention time to two major causes: (1) depolarization field, (2) gate leakage current and (3) interface reaction.

Based on the above, a possible solution may arise from the growth of a single crystal, single domain ferroelectric on Si. A single crystal film eliminates the grain boundaries which are believed to be the sources of trapping centers. The trapping center can produce the depolarization and reduce the retention time. A single crystal ferroelectric also affords the possibility of a “square” P-E hysteresis loop. If this can be achieved, the ferroelectric memory will have longer retention time. Because any depolarization field will not affect the remnant polarization of square P-E hysteresis loops, unless it exceeds the coercive field.

A systematic dielectric selection process in an attempt to address gate dielectric for FRAM or capacitor for DRAM, the factors that have been considered include the following: chemical compatibility of candidate dielectrics with the silicon of the FET channel; chemical compatibility of gate dielectric and the gate contact; dielectric properties of candidate materials; electronic structure of the semiconductor-dielectric interface; likely bulk defect structure of candidate dielectrics; and likely transport characteristics of the dielectric.