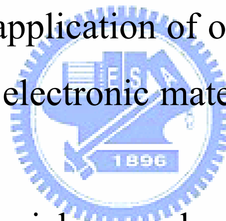
Chapter 1
Introduction

1-1. Introduction

Recently, oxide thin films of materials have been investigated for several areas, such as infrared sensor, superconductivity and ferroelectric memory. They are worth investigating for several reasons. First, the integration of two different materials in the form of thin films produces a multilayer with properties different from bulk. Second, it is challenging to produce a novel material in thin film form on a suitable substrate. Third, thin films are natural constituents for the implementation in devices based on nano-structures [1]. The application of oxide thin films in ferroelectric memory is a frontier area in electronic materials and will be concerned in this research.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Ferroelectric oxide materials were born in the early 1940s with the discovery of the phenomenon of ferroelectricity as the source of the unusually high dielectric constant in ceramic barium titanate capacitors. The ferroelectric material is a dielectric material that exhibits hysteresis loops for polarization as a function of applied field. Ferroelectric oxides with perovskite (e.g. $BaTiO_3$, $KNbO_3$) and layer-type Niobate (e.g. $PbBi_2Nb_2O_9$) [2] structures are the economically most important categories. A lot of work with those two structures has been reported in recent years.

There are two types of memory devices, ROM (Read only memory) and RAM (Random access memory) , the former is useful because the data are maintained in case of power off, but its read and write cycle

speed is very slow. The latter is converse. On the other hand, the FERAM (Non-volatile ferroelectric random access memories) is featured by large rewrite cycle as 10^{10}-10^{12} and its writing speed is very fast. FERAM possess of low writing voltage, faster writing speed, better endurance, and have the potential to replace many current materials that lack all these properties. This indicates that FERAM has a feasibility of mass storage memory as well as non-volatile RAM. In other words, FERAM is expected to open a new era of semiconductor memory. The comparison of memory IC is shown in Table 1-1 [3].

Table 1-1. Comparion of memory IC. [3]

	FFRAM	FRAM	FLASH	EEPROM	EPROM	MaskROM	DRAM	SRAM
Access Time	60ns	200ns	120ns	150ns	120ns	120ns	70ns	70ns
Progaming Time	100ns	40ns	10 μ s	10ns	10ns	N/A	70ns	70ns
Programing Voltage	5V	3-5V	12V	12.5V	12.5V	N/A	5V	5V
Erase Time	0ns	0ns	10ms	0ns	(15ws/cm^2)	N/A	0ns	0ns
Endurance	10^{12}	10^{12}	10^4	10^4	10^3	N/A	∞	∞
Retention	10Year	10Year	10Year	10Year	10Year	∞	0	0
Operation Cruuent	1mA	5mA	10mA	80mA	10mA	35mA	70mA	10mA
Cell Area	50 μ A	200 μ A	50 μ A	300 μ A	1 μ A	100 μ A	100 μ A	2 μ A
Condition	16MHz	5MHz	6MHz	6MHz	1MHz	8MHz	14MHz	14MHz

Nonvolatile ferroelectric memory is categorized into two generic types: one is the pass-gate array in which the ferroelectric nonlinear capacitors are arranged and each capacitor is isolated by one or more transistor (FRAM); and the other is the ferroelectric film gate field-effect transistor (FET), in which the ferroelectric film is deposited on the gate region (having the metal-ferroelectric-(insulator)-silicon-FET (MFS-FET or MFIS-FET) structure). The third type is a metal layer inserted into the ferroelectric layer and dielectric layer to improve device, called MFMIS (see Fig.1-1).

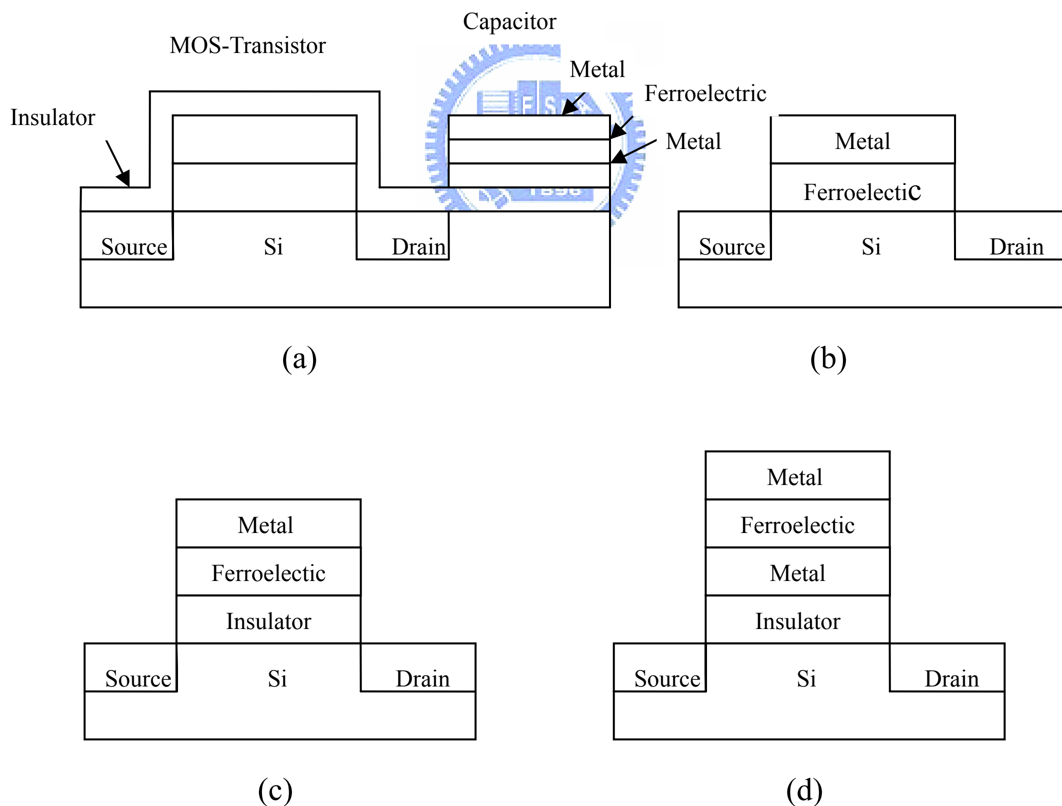

Fig.1-1 Simple model of various FeRAM (a) 1T-1C type FeRAM (b) MFS (c) MFIS (d) MFMIS in FET-type FeRAM, respectively.

During the past several decades the ferroelectric field effect has been exploited to modulate the surface potential of a semiconductor by using the spontaneous polarization of ferroelectric in contact with the semiconductor. The increasing attention has been focused on the development of ferroelectric non-volatile memories for metal-ferroelectric-semiconductor (MFS) and metal-ferroelectric-insulator-semiconductor (MFIS) structure. MFS-FET devices was the first thin film field-effect transistor with a ferroelectric gate insulator reported by Moll and Tarui [4], but the interface reactions between ferroelectric materials and Si substrates (generation of mobile ions and low retention) make it difficult to be obtained as a good device. However, the MFS structures have serious problems such as poor interface, high leakage current, retention, and fatigue. On the other hand, MFIS-FET with a relative low dielectric constant such as SiO_2 (k=3.9) as an insulator can maintain only at 3.4 $\mu C/cm^2$, which is much smaller than the remanent polarization of ferroelectric films. In other words, we cannot fully use the saturated P-E hystersis loop of ferroelectric film to control the channel conductivity of MOSFET. For example, inducing a charge of 50 C/cm^2 of PZT film means that a voltage as high as 145 V must be applied to a 10 nm SiO_2 gate insulator. This corresponds to an electric field of 145 Mv/cm, which is much larger than the breakdown field of SiO_2. So far,In order to overcome this issure, a metal ferroelectric metal insulator semiconductor (MFMIS) structure with a small MFM capacitor on a large MIS diode has been developed [5,6]. By reducing the ferroelectric MFM capacitor size, S_F, we can equivalently reduce the polarization of the ferroelectric film so that the polarization can match the induced charge of the MIS capacitor. If the area ratio between the MIS and ferroelectric MFM capacitors,

S_M/S_F, is correctly adjusted, we can utilize the saturated loop and large memory window, which agrees with $2V_c$ of the saturated P-E loop. Since the MFMIS structure is a series connection of MFM and MIS capacitors, the applied voltage is divided to the capacitance of each layer. Since the well-known ferroelectric materials have large dielectric constants, the capacitance of insulator layer must be large to apply a sufficiently high voltage to the ferroelectric layer. Furthermore, using a large capacitance insulator layer is necessary to improve the data retention characteristics. Improving the data retention character is one of the major issues of ferroelectric-gate FET research. When the gate is grounded after the "write" process, the ferroelectric MFM capacitor is reversely biased, an electric field called "depolarization field" is generated in the ferroelectric layer during the retention time. The depolarization field can reduce the ferroelectric polarization and hence reduce the data retention time. In order to improve the data retention characteristics, the depolarization field must be as small as possible, which means that the insulator layer capacitance must be as large as possible. In addition, the leakage current of both ferroelectric and insulator layers must be as low as possible.

Those dielectrics materials are used as core components of the two device types that represent the heart of the silicon semiconductor industry: as the capacitor dielectrics used for information storage in dynamic random-access memories (DRAM), and as the transistor gate dielectric in MOSFET devices. In both cases, the thickness of the present dielectric with oxide/nitride system is becoming sufficiently thin that leakage currents arising from electron tunneling through the dielectrics are posing a problem, and are viewed as a major technical barrier. As an alternative to oxide/nitride systems, much work has been done on high-k metal

oxides as a mean to provide a substantially thicker (physical thickness) dielectric for reducing leakage and improving gate capacitance.

Among the groupⅢ candidate dielectrics, alumina (Al_2O_3) is a very stable and robust material, and has been extensively studied for many applications. A substantial amount of investigation has gone into the group ⅣB metal oxides, specifically TiO_2 [8-10], ZrO_2 [11-13], and HfO_2[14-16], as these systems have shown much promise in overall materials properties as candidates to replace SiO_2. An encouraging system of materials to replace oxide are pseudobinaries, such as $(ZrO_2)_x(SiO_2)_{1-x}$ [17-18] and $(HfO_2)_x(SiO_2)_{1-x}$ [19-20], which for this purpose combine two oxides, typically in nonstoichiometric compositions. It is possible to combine the desirable properties from two different oxides with the elimination of the undesirable properties of each individual material.

In FERAM it is important to select which of the ferroelectric materials, perovskite ABO_3 like PZT or Bi layer structured ferroelectric material (that is Aurivillius Family), is suitable. The former ABO_3 structure is advantageous because of its large residual polarization (P_r value); however, its aging effect or fatigue property might be worse due to large atomic motion. The property of Bi Aurivillius Family has not been fully grasped because large single crystal was not obtained. Ferroelectric $SrBi_2Ta_2O_9$ (SBT) has been widely noted from a viewpoint of non-volatile random access memory applications. It belongs to the niobate layer-structured ferroelectrics discovered by Aurivillius and exhibits large spontaneous polarization in the a-b plane [7]. In recent years, layer-structured bismuth-based niobate ferroelectric thin films of $SrBi_2Ta_2O_9$ (SBT) and $SrBi_2Nb_2O_9$ (SBN) have become candidates for applications in nonvolatile random access memories due to their low

coercive field, low relative dielectric constant and low leakage current density. The commercial applications of ferroelectric memories include many portable electronic devices such as pagers, cellular phones and smart cards.

1-2. Motivation for the study

Ferroelectric memory technology brings many features to us, but still many of the process technology problems should be solved before making FERAM a universal memory. The first problem is ferroelectric film deposition. The second problem is the retention problem. The major deposition requirements are (1) low deposition temperature, (2) excellent uniformity over silicon wafers, and (3) conformal coverage. Although SBT thin films have been used in FERAMs, but SBT thin films still have many problems to be solved for practical applications, high crystallization temperature, relatively low polarization, high leakage current, and diffusion of bismuth. High temperature processes give rise to the inter-diffusion and interaction between constituents, resulting in a change of the interface state. Previous researchers have found out considerable deficiency in Bi content may change the interface properties and show an effect on the electrical properties of SBT/metal and SBT/Si thin film devices. SBT thin films sintered at higher temperature not only could cause bismuth volatility and diffusion, but also the change of composition. So, excess Bi-based fluxes are required to ensure proper composition, proper phase formation and good electrical properties in thin film growth of SBT.

Therefore, the aim of this research is described as followings:

(1) To obtain an SBT thin film which can crystallize at lower temperature.

(2) To obtain an SBT thin film with a proper remanent polarization or a wide memory window at lower coercive field.

(3) To obtain an SBT thin film with a very low leakage current.

(4) To control the bismuth diffusion in SBT thin films.

(5) To search another ferroelectric films which possess higher remanent polarization.

(6) To search another higher dielectric constant material to improve memory window between ferroelectric film and insulator of the capacitors stack.

1-3.Thesis Organization

This dissertation is divided into seven chapters.

Chapter 1 introduces the general background

Chapter 2 is the literature review; include the structure, composition, preparation condition, chemical reaction, physical properties and electrical characteristics of ferroelectric and dielectric materials.

Chapter 3 presents the experimental details of deposition method for ferroelectric film, dielectric film and the analyzed method of physical and electric characteristics.

Chapter 4 presents the effect of various bismuth contents on electrical properties of $Sr_{0.8}Bi_{2+x}Ta_2O_{9+\delta}$ (SBT) thin films.

Chapter 5 demonstrates electrical and dielectric properties of $Sr_{0.8}Bi_{2.6}Ta_2O_{9+x}$ thin films crystallized at low-temperature on Ir/SiO_2/Si substrates.

Chapter 6 presents the effects of the STO seeding layer and substrate configurations on the electric and physical properties of $Sr_{0.8}Bi_{2.6}Ta_2O_{9+x}$ thin films.

Chapter 7 presents the electrical properties for the polarization enhancement of polycrystalline $Bi_{3.25}Nd_{0.75}Ti_3O_{12}$ (BNT) thin film is grown on platinum-coated (SRO/STO/Si) substrate.

Chapter 8 presents the higher dielectric and electrical properties of $SrTiSi_xO_{3+\delta}$ thin film-based on MIM capacitors.

Chapter 9 is the final to make the conclusions for this thesis, along with suggestion for future work.