國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

奈米金屬鎳/鎳矽化物晶粒之非揮發性記憶體製程與研究

Study on the Fabrication of Nickel/Nickel-Silicide Nanocrystals Embedded in SiO₂ for Nonvolatile Memory

研 究 生： 許 雁 雅
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張 鼎 張 博士

中 華 民 國 九 十 四 年 九 月

本論文獻給我敬愛的父母

許明淨先生 許李桂芬女士

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Study on the Fabrication of Nickel/Nickel-Silicide Nanocrystals Embedded in SiO$_2$ for Nonvolatile Memory

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中 華 民 國 九 十 四 年 九 月

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摘要

　　在非揮發性金屬記憶體的研究方面，本論文所選取的金屬量子點材料為鎳及鎳矽化物。然而金屬的量子點記憶體在近年來受到矚目，其相對於傳統半導體材料用於量子點記憶體上，有諸多的優勢，其優勢包含低功率耗損、高密度的能階、沒有明顯的量子侷限效應(carrier confinement)、有效降低元件尺度、且可調變的空間大，因為隨不同的金屬有不同的功函數。除此之外，我們在選擇金屬的材料上，在線上製程中有其他的應用及良好的熱穩定度，是我們選擇鎳及鎳矽化物的一個主要的原因。

　　然而，我們在實驗中發現一些鎳量子點記憶體所存在的機制，我們合理的獲得一些結論去解釋我們的記憶體特性，發現其中存在兩種重要的機制，就是鎳金屬的擴散問題及其有機會與我們的介電質材料(氧化矽)作反應。此機制在高溫時

便成不可忽略的問題，也是造成高溫時記憶體特性不佳的主要原因。

　　但在同時，我們也發現矗矽化物的量子點記憶體卻可以改善在高溫時鎳量子點的問題，因為鎳層偏愛與矽反應成矽化物，所以並沒有殘存的鎳可以造成上述的問題，因此成功的獲得高溫的鎳矽化物量子點記憶體。此外，我們發現層積薄的矽(僅提供反應成矽化物)，可以較有效的控制量子點的大小及均勻性。最後，我們透過矽/鎳/矽的結構，去反應成鎳矽化物的量子點及上下的絕緣層，發現在氧化溫度 800 度時，獲得兩位元(two-bit)的記憶體特性。

Study on the Fabrication of Nickel/Nickel-Silicide Nanocrystals Embedded in SiO$_2$ for Nonvolatile Memory

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Abstract

We have studied experimentally and theoretically two kinds of nonvolatile metal nanocrystal memories: nickel nanocrystal memories and nickel-silicide nanocrystal memories. The metal nanocrystals memories come into notice as so many advantages. The advantages of metal nanocrystals over their semiconductor counterparts include low power consumption, higher density of states, smaller energy perturbation due to carrier confinement, stronger coupling with the channel, better size scalability, and the design freedom of engineering the work functions to optimize device characteristics. The reasons why nickel/nickel-silicide is chosen as the materials for the nanocrystals are the compatibility with current manufacturing technology of semiconductor industry and thermal stability of the nickel silicide.

In our experiments, we would discuss some mechanisms about the nickel

nanocrystals as memory storage medium. We obtained some conclusions to explain the memory effects for the different annealing temperatures. The two important mechanisms were nickel diffusion problem and the reaction between nickel and silicon dioxide. So these would be become the terrible problems as the high temperature processes.

At the same time, we observed the nickel-silicide nanocrystal memories to improve the disadvantages of the nickel nanocrystal memories. The nickel film was only prepared to silicidation, so the high temperature processes were suitable for nickel silicide formation. The thin nickel/silicon film was exact to be controlled the dot size and observed good uniformity at the same time. However, another good result was obtained the one cell two bit memory from the silicon/nickel/silicon structure at 800℃ annealing.

誌 謝

　　論文寫到這裡也差不多告一個段落了,雖然感覺花了很多的時間來寫這篇論文,但在接近尾聲的這一刻,才真正體會豐收的喜悅,及一切努力過程是那麼樣的得來不易,雖然只是一篇為數不多的文章,但從下筆到完成時真的是很令人感動。因為努力過了,所以才証明自己真的做得到。感謝這一切的成果並非由我一個人就可以獨自完成的,感謝上天能夠給我這次成長及學習的機會,雖然駑鈍的我總無法在過程中,好好體察這一切學習的用意,有時不免不懂得珍惜及感恩。但在這兩年的學習期間,是多少的人在背後幫助著我及陪伴著我,我為我所擁有的一切感恩,也許我無法一一詳盡這些貴人,但願這份心意能夠長存在心中,有一天這感謝能夠傳達給對方。

　　然而,先要感謝的是我的 爸爸(許明淨) 及 媽媽(許李桂芬),謝謝您們的支持及教養,才有今天的我。此外,幸運的我遇到兩位好的指導教授,一位是永遠支持我的選擇及給我空間發揮的 羅正忠 博士,另一位則是在實驗上給了我許多實質的建議及引導我方向的 張鼎張 博士,感謝兩位認真又負責的老師,否則我無法學習到這麼多的知識。再來要感謝這位幕後的推手炳宏學長,因為所有實驗上大大小小的問題,感謝學長不吝惜的幫助我克服,及感謝我最佳的實驗夥伴彥宇,謝謝你包容我急躁的個性,幫助我一同完成許多的實驗結果。此外,還要感謝實驗室的諸多學長們:永裕、碩廷、紀文、小鳴、永俊、世璋、大山、土撥、敏全、國王、致宏、志偉、興華、元均、浤宏、泓緯、家榮、炳麟、文斌、世仰...。謝謝您們在實驗上及理論學習上的幫助及指導,因太多無法詳列,但都非常謝謝您們。還有要感謝的是那些一起同甘共苦的同學及實驗夥伴們,真的很開心能夠認識你們,讓實驗過程添增許多趣味,且很懷念在 NDL 辛苦實驗時,大家互吐苦水、互相加油的那段日子,那將會是我的一段珍貴且甜美的回憶。感謝家人、師長、朋友、同學們,如今,太多的感謝只能放在心裡了,只有一句話能貼切的說出那份感動,就是:『有您們真好!』

這一刻，是該劃下休止符了，但心中那份感恩的旋律，將不隨這段樂章的停止而停止。

　　謹此致上我最真誠的感謝！

<div align="right">雁雅　敬上</div>

<div align="right">2005/08/19</div>

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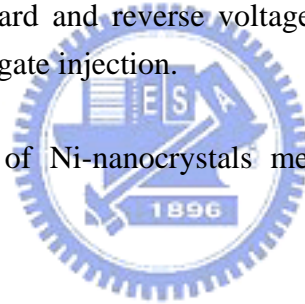Fig. 2-2   The leakage current of Ni-nanocrystals memory with Metal RTA 400℃ process.

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Chapter 1

Introduction

1.1 General Background

In recent years, the portable electronic product have widely applied, such as digit camera, notebook computer, mp3 walkman, intelligent IC card, USB Flash personal disc ,etc., and play an important role in the market. These products all are based on flash memory. The demand for the flash memory device grows with each passing day, the density and operation speed of flash memory and its reliability become the popular research theme. The operation principal of conventional Flash memory is using the polycrystalline silicon as floating gate to be the charge stored units. After electrons which injected from the channel stored in floating gate, the threshold voltage of devices will be changed. The logical "§"¡¨ an¡" " definition of nonvolatile memory devices are used for the difference between threshold voltages.

In 1960"¦s, due t ot he hi gh cost, l ar ge vd u nc, and hi gh po wer consu mpti on of t he magnetic-core memory, the electronic industries urgently needed a new kind of memory device to replace the magnetic-core memory. In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1.1]. A standard Conventional Flash device is similar to the Intel ETOX (EPROM Tunnel Oxide) structure as shown in Figure 1-1. The basic device is a Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) with a modified gate stack structure that has a control gate (CG) and a floating gate (FG) embedded in a dielectric material such as silicon dioxide (SiO2). The first SiO2 energy barrier

between the floating gate and the channel prevents electrons from leaking into the channel. A second barrier between the floating gate and the control gate prevents electrons from escaping to the control gate .The invention of FG memory impacts more than the replacement of magnetic-core memory, and creates a huge industry of portable electronic systems. The stacked-gate FG device structure continues to be the most important position for the nonvolatile-memory, and is widely used in both standalone and embedded memories up to today.

Although the conventional FG devices still come to be in face of their limitations. The conventional FG devices are much slower to program and erase. Reliable data retention is largely determined with good control and suppression of leakages from the floating gate. Since the SiO_2 barrier between the floating gate and the MOSFET channel is very thin, its quality is critical to ensure good floating gate isolation. Unfortunately, defects due to the structural imperfections and atomic bonding are unavoidable in realistic materials. These defects allow for leakage paths that are detrimental to charge storage in the floating gate. The most apparent way to avoid an over-leaky barrier is to increase the barrier thickness. However, thicker barriers slow down electron transport in and out of the floating gate. This, in turn, results in slower program and erase times.

In order to improve the write/erase speed of a floating-gate device, the thickness of the tunnel oxide must be reduced. The tunnel oxide must be less than 2.5 nm in order to achieve 100 ns write/erase time for a reasonable programming voltage (<10V). On the other hand, the tunnel oxide needs to provide superior isolation under retention, endurance, and disturbed conditions in order to maintain information integrity over periods of up to a decade. When the tunnel oxide is thinner for the first consideration, the retention characteristics may be degraded. And when the tunnel oxide is made

thicker to take the isolation into account, the speed of the operation will be slower. Therefore, there is a tradeoff between speed and reliability and the thickness of the tunnel oxide is compromised to about 8-11 nm, which is barely reduced over more than five successive generations of the industry [1.2]. Furthermore, if the tunneling oxide can not be thinned any more, both the operation voltage and speed of memory can not be improved.

To overcome the scaling limits of the conventional FG structure, two candidates are mostly mentioned, SONOS [1.3-1.5] and nanocrystal nonvolatile memory devices [1.6-1.8]. As for SONOS in Fig. 1-2, the nitride layer is used as the charge-trapping element. The intrinsic distributed storage takes an advantage of the SONOS device over the FG device, its improved endurance, since a single defect will not cause the discharge of the memory [1.5]. Tiwari et al. [1.6] for the first time demonstrated the Si nanocrystal floating gate memory device in the early nineties. As shown in Fig. 1-3, the local leaky path will not cause the entire loss of information for the nanocrystal nonvolatile memory device. Also, the nanocrystal memory device can maintain good retention characteristics when tunnel oxide is thinner and lower the power consumption [1.6-1.8]. The term "endurance" refers to the ability of the NVSM to withstand repeated program cycles and still meet the specification in the data sheet. The term "retention" describes the ability of the NVSM to store and recover information after a number of program cycles at a specified temperature.

1.1.1 SONOS nonvolatile memory devices

The triple-dielectric polysilicon-blocking oxidesilicon nitride-tunnel oxide-silicon (SONOS) structure is an attractive candidate for high density EEPROM's suitable for semiconductor disks and as a replacement for high-density

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dynamic random access memories (DRAM'¦s). Low program voltages (5 V) and high endurance (greater than 10^7 cycles) are possible in this multidielectric technology as the intermediate Si_3N_4 layer is scaled to thicknesses of 50 A. Oxide thickness in this range is necessary to minimize the undesirable effects of gate disturb while still enabling a low-voltage operation to maximize the cost benefit of SONOS memories. The thin gate insulator and low programming voltage enable the scaling of the basic memory cell and associated complementary metal-oxide-semiconductor (CMOS) peripheral circuitry on the memory chip.

Advancements in ultra-thin tunnel oxides during the 1990s have opened the path to improve performance and reliability for NVSMs based on SONOS technology [1.9]. The optimization of nitride and oxide films has been the main focus in recent years. Initial device structures in the early 1970s were p-channel metal-nitride-oxide-silicon (MNOS) structures with aluminum gate electrodes and thick (45 nm) silicon nitride charge storage layers. Write/erase voltages were typically 25-30 V. In the late 1970s and early 1980s, scaling moved to n-channel SNOS devices with write/erase voltages of 14-18 V. In the late 1980s and early 1990s, n- and p-channel SONOS devices emerged with write/erase voltages of 5-12 V. Figure 1-5 illustrates the write/erase operation using an energy-band diagram. The electrons injected from the channel are trapped in the forbidden gap of the silicon nitride film. The electrons, which are not trapped in the nitride film, tunnel through the blocking oxide into the gate electrode. If the poly-Si gate is doped p^+, then holes may tunnel from the gate to the silicon nitride valence band, thereby compensating the trapped electrons and reducing the threshold voltage shift. During the erase operation, holes are injected from the substrate into the silicon nitride valence band where they are trapped in a manner similar to electrons. The free holes pile up at the blocking oxide interface because of the larger barrier height (5 eV). Electrons may tunnel from the gate electrode into the nitride

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compensating the injected holes. A larger barrier for holes (4.7 eV) requires tunnel oxides to be less than 2.5 nm for efficient tunneling and, therefore, "hole tunneling" depends strongly on the tunnel oxide thickness. Additionally, electrons may tunnel from the valence band of the gate electrode; however, the barrier height for this process is increased by the silicon bandgap (1 eV) as compared with the tunneling from the conduction band. Thus, in summary, for SONOS device operation both carrier types are involved in the transport process.

Low-voltage (5-10 V) SONOS NVSMs may be scaled in cell size to $6F^2$ (F=feature size) and perhaps even smaller in the years to come. The simplified ONO gate stack in SONOS memory transistors lends itself to the economics of scaled CMOS circuits. The compatibility of SONOS technology with advanced CMOS logic technology permits economical integration of NVSMs as embedded EEPROMs in ASIC chips. Finally, radiation hardness provides a unique and important feature for advanced military and space systems.
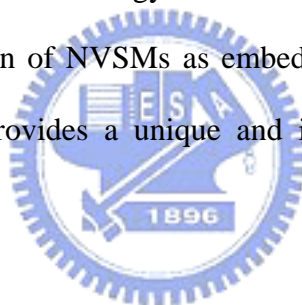
1.1.2 Nanocrystal nonvolatile memory devices (semiconductor nanocrystals)

The charge storage property of semiconductor nanocrystals embedded in a silicon oxide matrix is currently under intense investigation due to its potential application in future nonvolatile memories. The continuous down scaling of device dimensions requires more stringent and better controlled fabrication processes. One way to conveniently achieve nanometer range structures without sophisticated nanolithography techniques is through the synthesis of nanocrystals. However, the charges loss through lateral paths in nanocrystal-based memory devices can be suppressed by the oxide isolation between nanocrystals, these devices exhibited

superior charge storage characteristics compared with conventional floating-gate memory devices. All stored charges can't be lost through the few leaky paths since the charges are stored in distributed nano-dots. One way to alleviate the scaling limitation of the conventional FG device, while still preserving the fundamental operating principle of the memory, is to rely on distributed charge storage instead. The typically investigations are used semiconductors (Si or Ge) as nano dot to reduce the tunneling oxide of thickness without losing its reliability and further to reduce operation voltage.

Nanocrystal nonvolatile memories first introduced in the early 1990s. In a nanocrystal NVSM device, charge is not stored on a continuous FG poly-Si layer, but instead of a layer of discrete, mutually isolated, crystalline nanocrystals or dots. Each dot will typically store only a handful of electrons; collectively the charges stored in these dots control the channel conductivity of the memory transistor. Figure 1-4 illustrates the progression of device cross section, which has led to the present nanocrystal NVSM device structure.

As compared to conventional stacked gate NVSM devices, nanocrystal charge storage offers several advantages, the main one being the potential to use thinner tunnel oxide without sacrificing nonvolatility. This is a quite attractive proposition since reducing the tunnel oxide thickness is a key to lowering operating voltages and/or increasing operating speeds. This claim of improved scalability results not only from the distributed nature of the charge storage, which makes the storage more robust and fault-tolerant, but also from the beneficial effects of Coulomb blockade [1.7]. Quantum confinement effects (bandgap widening; energy quantization) can be notable of small nanocrystal geometries (sub-3 nm dot diameter) to further enhance the memory's performance.

There still keep the other important advantages. First, the fabrication of the

nanocrystal memories is more simplified and lower cost process as compared to conventional stacked-gate Flash memories. Second, due to the absence of drain to FG coupling, nanocrystal memories suffer less from drain induced barrier lowering (DIBL) so they have intrinsically better punch through characteristics. This advantage is gained a higher drain bias during the read operation, thus improving memory access time [1.10]. Alternatively, it allows the use of shorter channel lengths and therefore smaller cell area. Third, nanocrystal memories are characterized by excellent immunity to stress induced leakage current (SILC) and oxide defects due to the isolated charge storage in the nanocrystal layer. However, the other is the low capacitive coupling between the external control gate and the nanocrystal charge storage layer. This does not only results in lower operating voltages, thus offsetting the benefits of the thinner tunnel oxide, it also removes an important design parameter (the coupling ratio) typically used to optimize the performance and reliability tradeoff.

As for the fabrication processes, a first requirement is the aerial density of the nanocrystal dots. A typical target is a density of at least 10^{12} cm^{-2}. This is equivalent to approximately 100 particles controlling the channel of a memory FET with 100 100 nm^2 active area, and requires particle size of 5-6 nm and below. Second, the fabrication process should result in a planar nanocrystal layer, i.e., the thickness of the dielectric layer separating the nanocrystal and the substrate should be well controlled. Poor control of the tunnel oxide thickness will result in wider threshold voltage distributions and will increase the number erratic bits. More generally, good process control is needed with regards to such nanocrystal features as: size and size distribution, inter-crystal interaction (lateral isolation), uniformity of aerial crystal density, and crystal doping (type and level). Recently, Lombardo *et al.* demonstrated the nucleation process is not purely random and the dots forms with partial self-ordering. The relative dispersion of R$_{dot}$ is numerically evaluated as a function of

gate size, both for random and partially self-ordered nucleation processes [1.11]. A theoretical model considering quantum confinement and Coulomb blockade in lower Si dot shows that charge retention is improved exponentially by lower dot size scaling. As the size and size distribution of the Ge nanocrystals have been considered, She *et al.* [1.12] made a conclusion on Ge nanocrystal memory device that nanocrystal size around 5 nm is preferred to achieve fast programming speed and longer retention time, and the size should not be scaled below that. The quantum confinement effect for Ge nanocrystals smaller than 5 nm is very significant so that the retention time is shorter and the programming time is longer. Finally, it is preferred that the fabrication process is simple and that it uses standard semiconductor equipments.

Several nanocrystal fabrication processes have been demonstrated. Numerous efforts have focused on obtaining a high density of nanocrystals through a variety of techniques including aerosol technique, ion implantation, MBE technique, direct chemical vapor deposition (CVD) and recrystallization anneal of amorphous-Si. Kim *et al.* used conventional LPCVD reactor to fabricate Si nanocrystals at 620 ℃. [1.13] Direct CVD of silicon is preferred over ion implantation and recrystallization anneal due to the difficulty in obtaining the required amount of Si in the stack. Further, nucleation and growth by CVD provides appropriate simpler processing controls to manipulate the size and density of nanocrystals. Si nanocrystals with number density between 10^{11} and $10^{12}/cm^2$ have been deposited on various dielectrics such as SiO_2, Si_3N_4 and Al_2O_3 using CVD. A high density of about 5 $10^{11}/cm^2$ was obtained on nitride surface, and the density was more than three times larger than that on oxide [1.14-1.15]. Fernandes *et al.* acquired the higher density Si quantum dots ($\sim 10^{12}/cm^2$) by integrating on SiO_2/ALD Al_2O_3 tunneling dielectrics [1.16]. Kanjilal *et al.* demonstrated a sheet of spherical, well-separated, crystalline Ge nanodots embedded in SiO_2 on top of p-(001) Si wafer, fabricated by molecular beam epitaxy (MBE)

combined with rapid thermal processing and characterized structurally and electrically [1.17]. To fabricate Ge nanocrystals, the oxidation of SiGe contained films has been utilized [1.18]. As the SiGe layer is oxidized, the Ge element will be downward segregated and Si will be oxidized into SiO_2 [1.19-1.20]. Ostraat *et al.* proposed an aerosol silicon nanocrystal nonvolatile memory device with large threshold voltage shift （＞3V）, sub-microsecond program times, millisecond erase times, excellent endurance （＞10^5 program/erase cycles）, and long term nonvolatility （＞10^6 sec) [1.21]. Qu *et al.* presented an approach for synthesizing Ge nanocrystals embedded in amorphous silicon nitride films [1.22]. On the basis of preferential chemical bonding formation of Si-N and Ge-Ge, thin films with Ge clusters embedded in amorphous silicon nitride matrix have been prepared by plasma enhanced chemical vapor deposition (PECVD) with reactant gases of SiH_4, GeH_4, and NH_3 mixed in hydrogen plasma at 250 ℃. Park *et al.* also utilized PECVD to form Si nanocrystals embedded in silicon nitride film [1.23]. They presented the electron charging and discharging effects of the Si nanocrystals embedded in SiN_x film. Capacitance-voltage hysteresis is used to inspect the memory effects of the nanocrystal memory devices [1.24]. Differing from the required single planar nanocrystal layer, Ohba *et al.* proposed a novel Si dot memory whose floating gate consists of self-aligned doubly stacked Si dots. A lower Si dot exists immediately below an upper dot and lies between thin tunnel oxides. It is experimentally shown that charge retention is improved compared to the usual single layer Si dot memory [1.25].

As for the tunnel dielectric for the nanocrystal nonvolatile memory devices, Baik *et al.* proposed a tunnel barrier structure that is composed of silicon dioxide and amorphous carbon (a-C) to attain enhanced charge retention without degradation in the injection efficiency. Additionally, high-k tunnel dielectrics were investigated for Si nanocrystal memory devices [1.26-1.28]. Results show that due to its unique band

asymmetry in programming and retention mode, the use of high-k dielectric on Si channel offers lower electron barrier height at dielectric/Si interface and larger physical thickness, results in a much higher $J_{g,programming}/J_{g,retention}$ ratio than that in SiO_2 and therefore faster programming and longer retention. The programming is considered as the electron injection from the channel under positive bias operation for an NMOSFET memory device. However, the programming and erasing mechanisms of p-channel nanocrystal memory devices were also investigated by Han *et al*. [1.29]. Promising device results have been presented, demonstrating low-voltage operation for comparable threshold voltage windows and operating speeds, and thin tunnel oxide retention behavior that suggests meeting long-term nonvolatility requirements. In spite of these promising results, it is unclear whether nanocrystal memories will ever see commercialization. In order for that to happen, the uniformity of the nanocrystals needs to be improved, and the claimed benefits need to be more unambiguously substantiated.
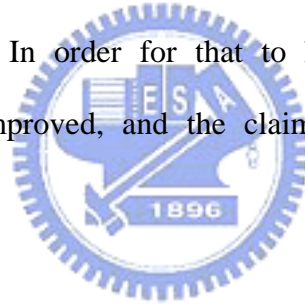
1.1.3 Nanocrystal nonvolatile memory devices (metal nanocrystals)

In optimizing the memory devices, the ideal goal is to achieve the fast write/erase of DRAM and the long retention time of Flash memories simultaneously. For this purpose we need to create an asymmetry in charge transport through the gate dielectric to maximize the $J_{g,programming}/J_{g,retention}$ ratio. Three different approaches for achieving this goal are illustrated in Fig. 1-6. By replacing the rectangular barrier with a parabolic or triangular barrier, the barrier height can be modulated by the electric field in the tunnel oxide [1.30]. Therefore, a higher tunnel–barrier is present during retention as the low electric field and a lower barrier is present during write/erase operations as the high electric field induced by external bias, thus increasing the

$J_{g,programming}/J_{g,retention}$ ratio. In practice, the parabolic or triangular barrier can be simulated by stacking multiple layers of dielectrics. Another approach is to use double-stacked storage nodes, preferably self-aligned with smaller dots at the lower stack [1.31]. In such devices, fast write/erase can still be achieved, if sufficiently thin tunnel oxides are used below and between the two stacks. However, the retention time can be significantly improved due to the Coulomb blockade effect at the lower stack, which prevents electrons in the top stack storage nodes from tunneling back into the substrate. The third approach is to engineer the depth of the potential well at the storage nodes, thus creating an asymmetrical barrier between the substrate and the storage nodes, i.e., a small barrier for writing and a large barrier for retention. This can be achieved if the storage nodes are made of metal nanocrystals. Then by engineering the metal work function, the barrier height can be adjusted by about 2 eV, giving much freedom for device optimization.

In addition to semiconductor nanocrystals, Liu et al. described the design principles and fabrication processes of metal nanocrystals [1.32-1.33]. The metal nanocrystal memory is exhibited to several advantages, such as stronger coupling with the conduction channel, better size scalability, higher density of states around the Fermi level, smaller energy perturbation due to carrier confinement, and the design freedom of engineering the work functions to optimize the device characteristics. In addition, the nanocrystals do not bear a voltage drop from gate voltage, which means all the voltages provided from control gate are dropped to tunnel oxide and control oxide and gains advantage. The higher density of states makes metal nanocrystals more immune to Fermi-level fluctuation caused by contamination. The metal nanocrystals tend to have more uniform charging characteristics, resulting in tighter V_{th} control. The wide range of available work functions provides one more degree of design freedom to engineer the tradeoff between write/erase and charge retention

because the work function of nanocrystals affects both the depth of the potential well at the storage node and the density of states available for tunneling in the substrate. By aligning the nanocrystal Fermi level to be within the Si bandgap under retention and above the conduction band edge under erase, a large $J_{g,erase}/J_{g,retention}$ ratio can be achieved even for very thin tunnel oxides. Because writing is performed by tunneling electrons from the Si substrate into the nanocrystals (thus can always find available states to tunnel into) and can have current level similar to $J_{g,erase}$, fast write/erase and long retention time can be achieved simultaneously in metal nanocrystal memories. Metal nanocrystals also provide a great degree of scalability for the nanocrystal size. To enable single-electron or few-electron memories by the Coulomb blockade effect, smaller nanocrystals are preferred. However, for semiconductor nanocrystals, the band-gap of nanocrystals is widened in comparison with that of the bulk materials due to the multidimensional carrier confinement, which reduces the effective depth of the potential well and compromises the retention time. This effect is much smaller in a metal nanocrystal because there are thousands of conduction-band electrons in a nanocrystal even in charge neutral state. As a result, the increase of Fermi level is minimal for metal nanocrystals of nanometer size.

1.2 Motivation

Recently, the memories are required by the high density, fast operation speed and good reliability. Memory-cell structures employing discrete traps as the charge storage media have attracted large of the researches as the promising candidates to replace conventional DRAM or Flash memories.

The metal nanocrystals memories come into notice as so many advantages. The advantages of metal nanocrystals over their semiconductor counterparts include low

power consumption, higher density of states, stronger coupling with the channel, better size scalability, and the design freedom of engineering the work functions to optimize device characteristics. A self-assembled nanocrystal formation process by rapid thermal annealing of ultra thin metal film deposited on top of tunnel oxide is developed and integrated with NMOSFET devices. Due to the minimization of the surface energy of the metal film under rapid thermal annealing, the driving force results in a discrete layer of metal nanodots reside on tunnel oxide.

The reasons why Nickel/Nickel Silicide are chosen as the materials for the nanocrystals are the compatibility with current manufacturing technology of semiconductor industry and thermal stability of the $NiSi_2$.

1.3 Organization of the dissertation
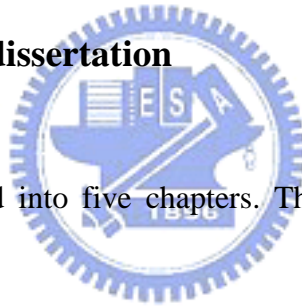
This dissertation is divided into five chapters. The contents in each chapter are described as follows.

In chapter 1, the potential memory devices about Conventional Flash, SONOS and nanocrystal memory devices is introduced.

In chapter 2, the study on Nickel nanocrystal memory technology using Dual E-Gun Evaporation System deposited Nickel thin film is investigated.

In chapter 3, the studies focus on Nickel Silicide ($NiSi_2$) nanocrystal memories by using the three different structures.

In chapter 4, we may make compare with some experimental results and make some discussions to their storage mechanisms.

In chapter 5, the final chapter is included the conclusions and the future work.

Chapter 2

A Novel Approach of Fabricating Nickel Nanocrystals for Nonvolatile Memory Application

2.1 Introduction

To overcome the scaling limits of the conventional FG structure, Tiwari et al. [2.1] for the first time demonstrated the Si nanocrystal floating gate memory device in the early nineties. Recently, considerable attention has been focused on semiconductor or metal nanocrystals embedded in the silicon dioxide of a metal-oxide-semiconductor (MOS) device for future high speed and low power consuming memory device [2.2-2.3]. The use of a floating gate composed of distributed nanocrystals reduces the problems of charge loss encountered in conventional floating-gate EEPROM memories, allowing for thinner tunnel oxide and, thereby, smaller operating voltages, better endurance and retention, and faster program/erase speed [2.4-2.6].

The self-assembling of silicon or germanium nanocrystals embedded in SiO_2 layers has been widely studied, and strong memory effects in MOS devices were reported [2.7-2.9]. There are, however, quite few reports on the memory effects of metal nanocrystals during the past years. The major advantages of metal nanocrystals over their semiconductor counterparts include (1) higher density of states around the Fermi level, (2) stronger coupling with the conduction channel, (3) a wide range of available work functions, and (4) smaller energy perturbation due to carrier confinement [2.3]. In addition, the nanocrystals do not bear a voltage drop from gate voltage, which means all the voltages provided from control gate are dropped to tunnel oxide and

control oxide and gains advantage. The higher density of states makes metal nanocrystals more immune to Fermi-level fluctuation caused by contamination. The metal nanocrystals tend to have more uniform charging characteristics, resulting in tighter V_{th} control. The wide range of available work functions provides one more degree of design freedom to engineer the tradeoff between write/erase and charge retention because the work function of nanocrystals affects both the depth of the potential well at the storage node and the density of states available for tunneling in the substrate.

The material of the nanocrystals was used by Ni and then M. Liehr et. al. was used to study the influence of interfacial SiO_2 on the reactivity of the Ni/Si(111) interface [2.10]. Iterated Ni depositions, at room temperature, on Si oxide layers of various thicknesses [grown on Si(111)] were made in ultrahigh vacuum and followed by in situ annealing up to 900 ¢XC It wa found that Ni initially agglomerates into islands at room temperature and above. Furthermore, at elevated temperatures the Ni reacts with the underlying Si through pinholes in the oxide to form $NiSi_2$. A higher temperature was required to initiate the silicide formation reaction for thicker SiO_2 layers, suggesting that the reaction is limited by mass transport through pinholes in the oxide. Direct Ni-SiO_2 interaction, in contrast, is rather limited. Some SiO_2 decomposition may take place for thicker Ni coverage ($\geqq$50A).

In this letter, we proposed a Ni nanocrystal memory device with 4.2nm-thick tunnel oxide, and studied on the memory characteristics of the metal nanocrystal. The material about Ni was suitable for the MOSFET devices as the devices scaling down.

2.2 Experimental procedures

First, the 6-in Si wafers (100) were cleaned with standard RCA recipes. The

standard RCA clean process was immersed in the HCl bench at 120℃ for 10 minutes (called SCI process). Next, the wafers were cleaned with NH_4OH at 120℃ for 10 minutes (called SCⅡ process). These steps must be carefully handled because HCl and NH_4OH will cause the reaction to produce the NH_4Cl which will hurt our bodies. The last step was dipped in HF several seconds until the backside wafer was not adhered to the DI water. This step can be observed the difference in our eyes. Second, the wafers were followed by a thermal oxidation process to form 4.2nm-thick dry SiO_2 layer as a tunnel oxide in an atmospheric pressure chemical vapor deposition (APCVD) furnace[i]. The equipment of the APCVD furnace was place at the classroom (class 10) in the National Nano Device Laboratories (NDL). As the process began, we can leave until the "§BOATⅠ"¡¨ step was complete But we must wait until the vacuum pressure was arrived for the Low pressure chemical vapor deposition (LPCVD) furnace. Before the end of the auto processes about 30 minutes ago, we must be remember come back to confirm all conditions were fine. Third, after the growth of tunnel oxide, the Nickel thin film was deposited on the oxide by Dual E-Gun Evaporation System (E-Gun)[ii]. The deposition of Nickel film was the critical process to determine the result of the size of the nanocrystals and the memory effect. The Ni was deposited about 17A with 0.1 A/sec as current range in 50-70 A. Fourth, the TEOS oxide 400 A was deposited on the Ni thin film by Plasma Enhanced Chemical Vapor Deposition (PECVD) with reactant gases of TEOS 10 sccm mixed in Nitrogen plasma at 300℃[iii]. Before the deposition process began, we always done the clean process to make chamber spotless. Finally, the N_2 rapid thermal annealing(RTA) at 400℃, 500℃, 800℃ and 900℃ for 20 sec transformed the Ni layer to liquid phase and the Ni nanocrystals formed after cooling down. This step was prepared by Metal Rapid Thermal Annealing (Metal-RTA) in the classroom (class 10). To fit the annealing temperature, we must try several times until correcting to our normal

temperature. The fitting parameters were made into list as below.

Temp.	Ramp	T-SW	Gain	D-G	I-W,I-C
900℃	90	50	-60	-6	4196
800℃	90	20	-50	-5	2997
500℃	60	20	-50	-5	1026
450℃	70	20	-50	-5	1426
400℃	70	40	-50	-5	403

Then, the samples were analyzed the micro-structure by Transmission Electron Microscope (TEM). The TEM figures can be more powerful evidence to confirm the shape of the nanocrystals. Subsequently, the Capacitance-Voltage measurement was analyzed the memory effect of the nanocrystal memories in their electrical characteristics. The Capacitance-Voltage characteristics were measured at different frequency (10kHz-1MHz) by HP4284 Precision LCR Meter. However, the Current-Voltage measurement was shown the leakage current to be verified the quality of the control oxide. The Current-Voltage characteristics were measured by HP4156C Precision Semiconductor Parameter Analyzer. The metal insulator semiconductor (MIS) structure with Ni nanocrystals embedded between tunnel and control oxide was fabricated.

2.3 Results and discussions

Our researches were focused on the forming of the Ni nanocrystals with the different annealing temperature processes. The film was annealed at elevated temperatures close to its eutectic temperature with the substrate in an inert ambient to transfer the wetting layer into nanocrystals. [2.16-17]. Before RTA, the as-deposited film came naturally with some thickness perturbation and even nanocrystals started to

form (without a clear separation in between, though). When the film was RTA treated to give the atoms enough surface mobility, the film will self-assemble into a lower-total-energy state. To reduce the elastic energy carried by the stress built into the film during the deposition process, the film tended to break into islands along the initial perturbation. However, minimization of the surface energy and the dispersion force between the top and bottom interfaces could help stabilize the film. So the final geometry would depend on the balance between these driving forces.

But our experiment results were showed some strange phenomenon. The different annealing temperature processes were prepared to analyze the Ni nanocrystal memory characteristic. The best memory effect was showed in the 400℃ annealing process. The C-V and I-V measurement results were showed in the Figure 2-1 and Figure 2-2. The nano-dots were formed from this process in the Figure 2-3. On the contrary, the C-V and I-V curves were showed in the Figure 2-4 and Figure 2-5 with 500℃ annealing process. We could find the memory effect was suppressed as the higher temperature annealing process (500℃). So the unknown reason would cause that the thermal treatment not only contributed to segregate the Ni film but some reactions were happened. The nano-dots were also preformed with the 500℃ annealing temperature process in the Figure 2-6. Both of the annealing processes were the same order of the leakage current so the broken dielectric was not the main reason to explain. The good reason was found in the M. Liehr's paper [2.10]. For thicker Ni film ($\geqq$ 50A) would cause the silicide formation with the chemical interaction between Ni and SiO_2 at 300℃. So the thermal energy would supply not only the segregation of the Ni islands but also the chemical interaction. The silicide formation would be more markedly occurred at 500℃ annealing process. That was why the imperfect geometry shapes were formed at 500℃ annealing process. Therefore, the memory effect would inhibited by the silicide interface of the nanocrystals. However

the high temperature annealing process were showed in the Figure 2-7 and Figure 2-9 at 800℃ and 900℃. The gate injection effect were showed in these annealing processes. From the M. Liehr's conclusions, we could also explain these abnormal results. The high temperature (800-900℃) $Ni/SiO_2/Si$ reactions were dominant with the Ni-Si reaction as $NiSi_2$. At high temperature annealing, the Ni was the dominant moving species in the Ni-Si reaction. In addition, the thin tunneling oxide was enhanced the Ni-Si reaction. There existed more interface traps between the tunneling oxide and the Si substrate. Because silicide formation would cause the interface traps in the Si substrate. The interface traps would inhibit the substrate injection into the nano-dots as the inversion process. So the gate injection was dominant as the high temperature annealing processes. The silicide formation would also enhance the leakage paths to lose the injection electrons especially at the higher annealing temperature (900℃). That was why the less memory effect at 900℃ annealing process. The TEM images were also showed the nanocrystal formation in Figure 2-8 and Figure 2-9 with 800℃ and 900℃ annealing processes.

2.4 Summary

In this chapter, we focused on the researches of the Ni-nanocrystal memories. The Ni nanocrystals were necessary to overcome the Ni diffusion and silicide formation problems as the thermal annealing treatment. The Ni diffusion through the tunneling oxide would cause the Ni-Si reaction at the Si substrate. The silicide formation would also react at the Ni/SiO_2 interface. So the low temperature annealing(400℃) would be possible to segregate the Ni film but not to lack the memory effect.

[i] *We chose the sixth furnace and set up the parameters about "OX50A"¨*

[ii] *The deposition rate of the E-Gun was relied on adjustment of the current magnitude by a remote control. Not the rate magnitude but the current magnitude will be more exact as we determine our film thickness. However, the current and the deposition rate may be different because the E-Gun aimed at the target position will cause the error. So we must be surely the position as the deposition beginning.*

[iii] *We chose the chamber 2 to deposited TEOS oxide by setting up the "TEOS 400"¨: As the process was started to the "§gas stabilizatio"¡¨ condtion, we can pres" ¡"E¡¨ hold this step until the TEOS flow was stable in the setting value.*

Chapter 3

Characteristics of Nickel-Silicide Nanocrystal Memory Structures with Different Fabrication Processes

3.1 Introduction

Metal nanocrystal charge storage offers several potential advantages over conventional stacked-gate nonvolatile memory devices：

(1) A simple low cost floating-gate fabrication process.

(2) These were improved retention resulting from Coulomb blockade and quantum confinement effects that enable the use of thinner tunnel oxides and lower operating voltages.

(3) These could reduce punch-through achieved by eliminating drain-to-floating-gate coupling, allowing higher drain voltages during readout, shorter channel lengths, and smaller cell area.

(4) These were excellent immunity to stress induced leakage current and defects within the floating-gate or insulating layers due to the distributed nature of the charge storage in the discontinuous nanocrystal layer.

(5) The comfortable applications were caused by high density of states around the Fermi level and wide ranges of available work functions.

The potential for improved device performance and reliability strongly depends upon the ability to control particle core size, particle size distribution, crystallinity, area particle density, oxide-passivation quality, and crystal-to-crystal insulation that prevents lateral charge conduction in the nanocrystal layer.

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As the scaling down the size of device in very large scale integrated circuits (VLSI) technology, silicides generally apply to any aspect such as lower contact resistance and fully silicide (FUSI) metal gate [3.1]. Most important of all, some reports indicate that silicide has self-passivating silicon dioxide formed under high oxidation temperature or prolonging heat treatment time [3.2]. At the same time, silicide films tended to agglomerate or form islands under such annealing condition. According to these reason, we employed this phenomenon to manufacture our metal nanocrystals embedded in the SiO_2 layer. Furthermore we verified this method could have effect of memory. And this method was one step process that we can form not only the memory storage medium but also the control silicon dioxide. This process can be so simpler low cost fabrication process than traditional nanocrystal memories processes. However, we wanted to research in the storage characteristics of the Nickel-Silicide dots so we studied on some different fabrication processes. In this letter, we proposed a $NiSi_2$ nanocrystal memory device and studied on the memory characteristics of the metal nanocrystal.

In the Ni-Si binary system, a recent bulk annealing study [3.3] has demonstrated the existence of a $NiSi + Si \leftrightarrow NiSi_2$ eutectoid reaction in the temperature range 690¢XCt o 735¢X Above this temperature, $NiSi_2$ rather than NiSi is stable in contact with Si. The existence of this reaction is evident in the present study as well. The reaction does not appear in the most widely accepted version of the Ni-Si + binary phase diagram [3.4]. From the eutectoid temperature up to the $NiSi_2 \leftrightarrow Si$ liquid peritectic temperature of 968¢C [3.5], $NiSi_2$ is stable in contact with Si. Below the eutectoid temperature, NiSi and Si are in equilibrium [3.6].

3.2 Experimental procedures

The experimental procedures were focus on the formation of the Nickel Silicide nano-dots. The fabrication processes of the tunneling and control oxide also went along with changes to be analyzed the nanocrsytals. Relying on the variable fabrications to obtain the three structures, we studied on the memory effect of the NiSi$_2$ nanocrystals memories.

3.2.1 The Oxidation of the Dry Oxide/Nickel/amorphous Silicon Structure

First, the 6-in Si wafers (100) were cleaned with standard RCA recipes. The standard RCA clean process was immersed in the HCl bench at 120℃ for 10 minutes (called SCI process). Next, the wafers were cleaned with NH$_4$OH at 120℃ for 10 minutes (called SCⅡ process). The last step was dipped in HF several seconds until the backside wafer was not adhered to the DI water. Second, the wafers were followed by a thermal oxidation process to form 45A dry SiO$_2$ layer as a tunnel oxide in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Third, after the growth of tunnel oxide, Nickel thin film and amorphous Silicon film were deposited on the oxide by Dual E-Gun Evaporation System (E-Gun) at the same run. This process was deposited Ni layer then covering a-Si layer immediately. The deposition of Nickel film was the critical process to determine the result of the memory windows so checking the frequency range is necessary before deposition. The Ni was deposited about 17A with 0.1 A/sec as current range in 50-70 A and the a-Si was deposited about 150A with 0.3 A/sec as current range in 50-60 A. Finally, the furnace oxidation processes at 900℃ ,850℃ and 800℃ for 10 minutes in the O$_2$ surrounding formed the NiSi$_2$ nanocrystals and oxidized the a-Si to become SiO$_2$ at the same time. Moreover, the oxidation process was changed by the oxidation time. This step was prepared by the "Ni silicidation" furnace of the Oxidation and Diffusion Furnaces

which belonged to the Nano Facility Center of the National Chiao Tung University in the classroom (class 10k)[i]. We can set up the auto raising temperature to arrive at the setting temperature. When the faceplate was appeared "E", we just began to calculate the oxidation time. The oxidation process was demanded for infusing into the oxygen gas so we need exchange N_2 for O_2 gas. The gas exchange sequences were list as below.

Oxidation Time	Open O_2	Close N_2	Start to Count Oxidation	Open N_2	Close O_2	Drop Temp.	Open cover of tube
15min	24:00	22:30	21:30	6:30	5:00		00:00
10min	19:00	17:30	16:30	6:30	5:00		00:00
5min	14:00	12:30	11:30	6:30	5:00		00:00

Finally, the samples were analyzed the micro-structure by Transmission Electron Microscope (TEM). Subsequently, the Capacitance-Voltage characteristics were measured at different frequency (10kHz-1MHz) by HP4284 Precision LCR Meter. The Current-Voltage characteristics were measured by HP4156C Precision Semiconductor Parameter Analyzer. The metal insulator semiconductor (MIS) structure with $NiSi_2$ nanocrystals embedded between tunnel and control oxide was fabricated.

3.2.2 The Oxidation of the Dry Oxide/Nickel/amorphous Silicon/PECVD Oxide Structure

First, the 6-in Si wafers (100) were cleaned with standard RCA recipes. The standard RCA clean process was immersed in the HCl bench at 120℃ for 10 minutes

(called SCI process). Next, the wafers were cleaned with NH_4OH at 120℃ for 10 minutes (called SCⅡ process). The last step was dipped in HF several seconds until the backside wafer was not adhered to the DI water. Second, the wafers were followed by a thermal oxidation process to form 42A dry SiO_2 layer as a tunnel oxide in an atmospheric pressure chemical vapor deposition (APCVD) furnace. Third, after the growth of tunnel oxide, Nickel thin film and amorphous Silicon film were deposited on the oxide by Dual E-Gun Evaporation System (E-Gun) at the same run. This process was deposited Ni layer then covering a-Si layer immediately. The Ni was deposited about 10A with 0.1 A/sec as current range in 50-70 A and the a-Si was deposited about 20A with 0.3 A/sec as current range about 50 A. Because $NiSi_2$ components were formed 1：2 ratio as Ni to a-Si so the thickness of a-Si layer was double of Ni layer. Forth, the TEOS oxide 200A was deposited on the Ni thin film by Plasma Enhanced Chemical Vapor Deposition (PECVD) with reactant gases of TEOS 10 sccm mixed in Nitrogen plasma at 300℃. Finally, the processes were separated into two way. One of these was prepared by Metal Rapid Thermal Annealing, the N_2 RTA process at 850℃ with several annealing time (60s, 120s, 180s, 240s and 300s). Another was prepared by Oxidation and Diffusion Furnaces. The furnace oxidation processes at 900℃ and 800℃ for 10 minutes in the O_2 surrounding formed the $NiSi_2$ nanocrystals. This process was prepared by the "Ni silicidation" furnace of the Oxidation and Diffusion Furnaces which belonged to the Nano Facility Center of the National Chiao Tung University in the classroom (class 10k). Finally, the samples were analyzed the micro-structure by Transmission Electron Microscope (TEM). Subsequently, the Capacitance-Voltage characteristics were measured at different frequency (10kHz-1MHz) by HP4284 Precision LCR Meter. The Current-Voltage characteristics were measured by HP4156C Precision Semiconductor Parameter Analyzer. The metal insulator semiconductor (MIS) structure with $NiSi_2$ nanocrystals

embedded between tunnel and control oxide was fabricated.

3.2.3 The Oxidation of the amorphous Silicon/Nickel/amorphous Silicon Structure

First, the 6-in Si wafers (100) were cleaned with standard RCA recipes. The standard RCA clean process was immersed in the HCl bench at $120℃$ for 10 minutes (called SCI process). Next, the wafers were cleaned with NH_4OH at $120℃$ for 10 minutes (called SCⅡ process). The last step was dipped in HF several seconds until the backside wafer was not adhered to the DI water. Second, amorphous Silicon, Nickel and amorphous Silicon were sequent deposition by Dual E-Gun Evaporation System (E-Gun) at the same run. The processes were deposited 15A a-Si layer then covering 3A Ni layer and lastly deposited 125A a-Si layer. The Ni was deposited about 3A with 0.1 A/sec as current range in 50-70 A and the a-Si was deposited about 15A, 125A with 0.3 A/sec as current range in 50-60 A. Finally, the furnace oxidation processes at $900℃$ and $800℃$ with some different oxidation time (5, 10, 15 minutes) in the O_2 surrounding were formed the $NiSi_2$ nanocrystals and oxidized the a-Si to become SiO_2 at the same time. In addition to these processes, $900℃$ oxidation process was added with 5minutes in N_2 then with 10 minutes in O_2. These steps were prepared by the "Ni silicidation" furnace of the Oxidation and Diffusion Furnaces which belonged to the Nano Facility Center of the National Chiao Tung University in the classroom (class 10k). Finally, the samples were analyzed the micro-structure by Transmission Electron Microscope (TEM). Subsequently, the Capacitance-Voltage characteristics were measured at different frequency (10kHz-1MHz) by HP4284 Precision LCR Meter. The Current-Voltage characteristics were measured by HP4156C Precision Semiconductor Parameter Analyzer. The metal insulator

semiconductor (MIS) structure with $NiSi_2$ nanocrystals embedded between tunnel and control oxide was fabricated.

3.3 Results and discussions

We wanted to overcome the problems of the Ni nanocrystals. The substitute was the $NiSi_2$ nanocrystals memory. The Ni would prefer to react with Si more than SiO_2 so the redundant Ni was not existed. However, the Ni diffusion and Ni-SiO_2 interaction were solved. The $NiSi_2$ material can be known by the materials science. The $NiSi_2$ sintering temperature was 600-800℃ so our researches were focused on the temperature up to 800℃. Because upper this temperature, $NiSi_2$ was very stable component and existed less unstable component of NiSi. The one major problem of NiSi was the interface leakage current. Another problem was its less thermal stability. But NiSi had lower resistivity than $NiSi_2$. These were why we chose the temperature between 800-900℃ in our experiment. And we had some information about the $NiSi_2$ material：

(1) The barrier height to n-Si is 0.66 eV

(2) 3.63nm of resulting Nickel Silicide per nm of Nickel metal

(3) 3.65nm of Si consumed per nm of metal

(4) $NiSi_2$ would not react with Al

(5) The $NiSi_2$ thin film resistivity was 40-50 μΩ-cm

3.3.1 Characteristics of the Dry Oxide/Nickel/amorphous Silicon Structure

The wafers were capping the Nickel thin film and a-Si film on the tunneling oxide

by the E-Gun. The experiments were researched by our group before [3.7]. So some conclusions were obtained as before. First, the $NiSi_2$ nanocrystals were formed completely at temperature 800-900℃. Second, the $NiSi_2$ forming rate and the oxidation rate were different from 800℃ to 900℃. The $NiSi_2$ forming rate was faster than the oxidation rate at 900℃. However, the oxidation rate was faster than the $NiSi_2$ forming rate at 800℃. This mechanism could also be proved by the a-Si/$NiSi_2$/a-Si structure later. So our study was just repeated to make sure that the $NiSi_2$ nanocrystals could be successful to be formed. The results were showed in the TEM images(Figure 3-4). The non-uniform nanocrystals(4~10nm) spread in the TEM images. Because the Ni film was not thin enough as we expected, the $NiSi_2$ nanocrystals were formed too large to isolate the storage nodes. So we added one step by capping the PECVD oxide(200 A) on these structures to isolate the storage nodes. The C-V curves were measured in Figure 3-1 to Figure 3-3. The memory characteristics were appeared in these results. Nevertheless, the unobvious memory windows (~1V) were revealed the faulty condition to be formed nanocrystals.

3.3.2 Characteristics of the Dry Oxide/Nickel/amorphous Silicon/PECVD Oxide Structure

We tried to understand the characteristic of the $NiSi_2$ nanocrystals so we did some different fabrication processes. The Ni thin film and a-Si thin film were deposited at the same time but the thickness of the a-Si film was as double as the Ni film. Therefore, the Ni/a-Si layer was prepared to form the nanocrystals only. Then, the control oxide was deposited on the $NiSi_2$ dots by PECVD system. Finally, the Ni/a-Si was annealed in N_2 with various annealing time by Metal RTA. We tried several annealing times which were 60s, 120s, 180s, 240s and 300s to analyze the

nano-dot forming. The RTA process was specially formed the $NiSi_2$ dots. Besides the film was RTA treated to give the atoms enough surface mobility, the film would self-assemble into a lower-total-energy state. The major driving forces contributed to this process so the film tended to break into islands along the initial perturbation. The Figure 3-6 to Figure 3-10 were showed the C-V measurement of the different annealing processes. The memory windows for different processes were approximately 1V after the forward and reverse 6V sweeping. But the memory window became small (~0.5V) after the forward and reverse 8V sweeping. The Ni diffusion into the Si substrate was unobvious in the $NiSi_2$ nanocrystals memory because the gate injection was not occurred. Figure 3-5 was the TEM image for the 60s annealing process. We could find that the $NiSi_2$ dots(~3nm) were formed after the RTA process. Even if annealing for the shorter time (60s), the segregation and $NiSi_2$ formation were completed at the same time by the thermal annealing treatment. Moreover, the nanocrystal distribution was uniform and each dot had the same distance to tunnel into Si substrate.

Next, the different fabrication processes were prepared to form the $NiSi_2$ dot by the furnace. The samples were made the same treatment before annealing processes then $NiSi_2$ dots were formed with different temperatures (800℃, 900℃) in O_2 ambience for 10 minutes. These processes could be compared with the first part of this chapter. Figure 3-11 and Figure 3-12 were showed the C-V measurement for 900℃, 800℃ annealing processes. The memory windows for these processes were approximately 1V after the forward and reverse 6V sweeping. But the memory window became small (<0.5V) after the forward and reverse 8V sweeping. We could find that two kind of the formation processes with metal RTA and furnace had the similar results. This meant the $NiSi_2$ dots were completely formed even if the fabrication processes changing. Due to the thin control oxide (~200A), the nanocrystal structure couldn't

bear the high voltage. Figure 3-13 was showed the large leakage current of NiSi$_2$ nanocrystals memory with furnace oxidation 900℃ 10min in O$_2$ process. This showed that the higher voltage sweeping (8V) but less memory window. The I-V curve was also showed the inverse leakage current as the small positive voltage. Because of the dots filled up with electrons, these were induced the inverse built-in field to dominate the leakage current as small gate voltage. But the mechanism of NiSi$_2$ nanocrystal was not clear and definite in the unobvious memory effect. The TEM image of furnace oxidation 900℃ as showed in Figure 3-14 was compared with TEM image of RTA process. The thick tunneling oxide (~150A) could be observed in furnace processes so the memory windows during 8V sweeping were smaller than RTA processes. The long time for thermal treatment would enhance a-Si oxidation around the NiSi$_2$ dots. For this reason, the a-Si consumed mostly to form the oxide and NiSi$_2$ dots were less to be formed about 2nm-sized. Furthermore, the small size (<3nm) and sparse dot density would make the unobvious memory effect.
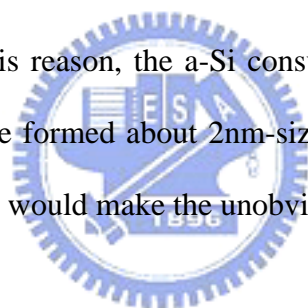
3.3.3 Characteristics of the amorphous Silicon/Nickel/amorphous Silicon Structure

The samples were only one step to deposit the three layers (a-Si~15A/ Ni~3A/ a-Si~125A) by E-Gun. Then, the furnace oxidation processes were completed the memory structures (tunneling oxide/ NiSi$_2$ nanocrystlals/ control oxide). The oxidation process was the thermal treatment to be formed the NiSi$_2$ component and segregated into low surface energy shape. Our experiments were variable with thermal treatment to make a study of forming nanocrystals. Figure 3-15 to Figure 3-18 were showed the C-V measurements for 900℃ annealing processes with variable oxidation time. The obvious memory windows could be obtained by 6V sweeping. So

these structures could success to be formed the nanocrystals and obtained good storage characteristics. Furthermore, the variable oxidation time would improve the storage characteristic to be obtained the larger memory window. The oxidation process with N_2 5minutes then O_2 10minutes was derived the largest memory window (~2.7V). In addition, Figure 3-19 and Figure 3-20 were showed the C-V measurements for 800℃ annealing processes with variable oxidation time. The memory windows were about 2.5V after the forward and reverse 6V sweeping. The variable oxidation time would not cause the memory windows changing. The C-V curve had a strange peak between inversion region and accumulation region as the forward sweeping. But this phenomenon was not found as the reverse sweeping. The TEM image as showed in Figure 3-21 could be explained this phenomenon. One dot was closed to the substrate and the other dot was longer distance to the substrate as showed in TEM image. The difference between the forming $NiSi_2$ rate and the oxidation rate were the reason for the two level dots at 800℃. Because the oxidation rate was faster than the forming $NiSi_2$ rate at 800℃, the fringes of the $NiSi_2$ dots would be capped with oxide immediately. The two level dots were formed as two bits of storage nodes. As the forward sweeping, the electrons filled in the dots began to erase from the nearby dots then erase from the remote dots lastly. Because of the delay time between two level dots erasion, the gate bias was not unique influence on C-V curve rising which meant from the inversion to the accumulation region. But the electrons were not filled in the dots inside as the beginning of the reverse sweeping. So the gate voltage was dominated the configuration of the C-V curve as the reverse sweeping. Figure 3-22 was showed the large leakage current of $NiSi_2$ nanocrystals memory with furnace oxidation 800℃ 10min in O_2 process. The I-V curve was showed the inverse leakage current as the small positive voltage. Because of the dots filled up with electrons, these were induced the inverse built-in field to dominate the

leakage current as small gate voltage. However the erasing problem as a strange peak of the C-V curve was also showed in the leakage current during the negative voltage. These electrons in the remote dots were more difficult to erase so decreasing current as increasing voltage.

3.4 Summary

The NiSi$_2$ nanocrystal memory will be a candidate for the metal nanocrystal memory in the future. Because of NiSi$_2$ material is compatible with current manufacturing technology of semiconductor industry. In addition, thermal stability of the NiSi$_2$ is another favorable quality to become nanocrystal. Moreover, the reaction between Nickel and amorphous Si had two mechanisms to be considered. Finding the optimum condition was necessary to balance the rate between oxidation and NiSi$_2$ formation. The effective control of nanocrystal sizes could be derived from the thickness of Ni/a-Si thin films. Then, rapid thermal annealing process would be suitable for fixed nano-dots position. However, the control oxide and the tunnel oxide could be obtained completely to combine with the forming of the NiSi$_2$ nanocrystal at the same time. The two-bits memory could be possible through adjustment of the thermal treatment with the a-Si/Ni/a-Si structure.

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[i] *Because we must change "Ni silicidation" furnace from medium position to below position so we need inquire for the operator and make an announcement. Until the procedures were complete, we can turn off the power switch to wait the temperature drop about six hours ago. Then, we can change the furnaces and wait the condition stability to take about six hours.*

Chapter 4

Integration with the Electrical Characteristics and the Physical Characteristics of the Nanocrystal Memory
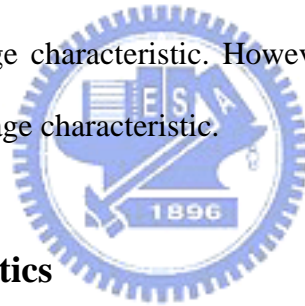
4.1 Electrical Characteristics

This part would be focus on C-V and G-V curves with the variable frequency measurements. A clear positive shift in C-V and G-V curves due to electrons trapped in nano-dots has been observed in our results. The peak in conductance around flat band condition indicated that a trap event had occurred where the electrons were stored per nano-dot. For a better understanding of the high frequency C-V results, the frequency dependent capacitance has been investigated at room temperature. In frequency dependent measurements, if we found similar clockwise C-V hysteresis and no significant change in peak position in G-V characteristics from 1 MHz to 1 KHz, which indicated that hysteresis and conductance peak had the same origin. It also suggested that the hysteresis and peak were not from interface traps, which were generally time dependence, giving rise to time or frequency dependence C-V or G-V characteristics [4.1-4.2]. So the storage mechanism inside of the nano-dots would be dominated with less frequency dependence. On the contrary, the frequency dependence of the storage mechanism would be dominated inside the interface traps.

The variable frequency C-V results of the Dry Oxide/Nickel/amorphous Silicon/ PECVD Oxide Structure were showed in Figure 4-1. Figure 4-1 was showed the furnace oxidation process to be formed the $NiSi_2$ nanocrystals at 900℃ for 10 minutes. The obvious frequency dependence was obtained by the two different

processes. So we suggested that the interface traps were dominated to be the storage nodes.

The variable frequency C-V results of the amorphous Silicon/Nickel/amorphous Silicon Structure were showed in Figure 4-4 and Figure 4-5. The furnace oxidation processes for 10minutes at 900℃ and 800℃ were corresponding with Figure 4-4 and Figure 4-5. The less frequency dependence was obtained as these results. So we suggested that the most electrons could be stored in the nanocrystals inside. The different oxidation processes with variable oxidation time and gas ambience at 900℃ and 800℃ were showed in Figure 4-2 and Figure 4-3. The largest memory window was acquired in N_2 ambience for 5minutes then in O_2 ambience for 10minutes at 900 ℃. Therefore, the $NiSi_2$ dots were formed completely in N_2 ambience and this process could be enhanced the storage characteristic. However, the increase oxidation time was less influence on the storage characteristic.

4.2 Physical Characteristics

The physical characteristics of the nanocrystals were concerned with dot size, dot shape, the distribution and the density of the nanocrystals. These physical characteristics could be caused the storage efficiency and let the nanocrystal memories to be product in the future. So we would discuss with the physical characteristics in our experiment results. The TEM images could be the most evidence for the formation of the dots. From the TEM images (Figure 3-5 and Figure 3-14), we could evidence the different rates between the oxidation and the silicidation. The obvious position difference was showed, especially the Ni moved up to form the silicide nanocrystals in Figure 3-14. So the faster silicidation rate caused the higher position of silicide nanocrystal. We could also find out that the Dry Oxide

/Nickel/amorphous Silicon/ PECVD Oxide Structures had the best uniformity in our experiment results. Because of capping oxide confined the formation of the dots, the similar dot sizes were observed. In addition, Ni was the main moving species so if we fixed the thin Si film then the position of $NiSi_2$ dots were also fixed, too. These were why the good controlled dot size was obtained.

Chapter 5

Conclusions and Suggestions for Future Work

5.1 Conclusions

Our researches were focused on the Ni and NiSi$_2$ as the metal nanocrystal memories. We chose Ni/NiSi$_2$ as our metal nanocrystals for some reasons. Most important reason was the compatibility with current manufacturing technology of semiconductor industry. However, the Ni nanocrystal memories had to face some troubles. The Ni diffusion would occur through the thin tunneling oxide to react with Si substrate. The morphology change of Ni nanocrystals would also occur as the reaction with Ni and SiO$_2$. So the best memory effect was obtained by the 400℃ annealing process. Therefore, the thermal processes were avoided to apply the Ni nanocrystal memories.

To improve the Ni nanocrystal memories, the NiSi$_2$ nanocrystal memories were studied in our experiments. The Ni film was only prepared to silicidation, so the high temperature processes were suitable for NiSi$_2$ formation. Although, the NiSi$_2$ formation and capping the control oxide could be complete together. This was another advantage for NiSi$_2$ nanocrystal memories. The uniformities of dot density and dot size were depended on the reactant of silicon, so we tried three structures as our researches. The thin Ni/Si film was exact to be controlled the dot size and observed good uniformity at the same time. However, the oxidation rate and the silicidation rate were different at 800℃ and 900℃. The oxidation rate was faster than the silicidation rate at 800℃. But the silicidation rate was faster than the oxidation rate at 900℃. In

addition, Ni was observed to be the dominant moving species in the silicidation process. Because of these mechanisms, the one cell two bit memory was obtained from the Si/Ni/Si structure at 800℃ annealing.

4.2 Suggestions of the Future Work

The mechanisms of the nanocrystal memories are not given the clear explanation until now. Sometimes we could obtain the distinct dot images but the C-V measurements were not expected in our experiment. We would try to explain our results but these explanations were still incomplete. The more complete researches will be needed in our future study of the nanocrystal memory. However, the fabrication processes of the nanocrystal formation will need to be improved in the future. The deposition of the Ni film was too thin to be controlled its quality and uniformity. But the deposition of the Ni film would determine the nanocrystal memory to be successful or not.

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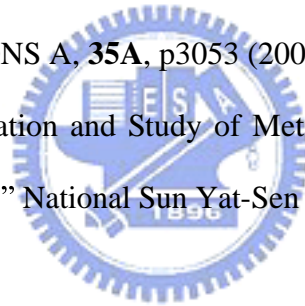
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