Analytical Settling Noise Models of Single-Loop Sigma–Delta ADCs

Fu-Chuang Chen, and Chun-Chieh Huang

***Abstract*—Switched-capacitor integrators are the basic building components for sigma–delta ($\Sigma\Delta$) modulators, and their incomplete charge transfer (settling problem) constitutes one of the dominant error sources in $\Sigma\Delta$ modulators. Due to the complexity of the settling problem, analytic models for related noises are nonexistent. In this brief, closed forms of settling error models are obtained and represented as functions of $\Sigma\Delta$ modulator system parameters. Both behavioral simulations and transistor-level circuit simulations are employed to verify these analytical models, and the results show that our analytical models are sufficiently accurate.**

***Index Terms*—Settling noise, switched capacitor (SC), sigma–delta ($\Sigma\Delta$) modulation.**

I. Introduction

SWITCHED-CAPACITOR (SC) integrators are the basic building components for the implementation of $\Sigma\Delta$ circuits. Settling problems arise from the incomplete transfer of charge in SC integrators, and they can significantly degrade the performance of $\Sigma\Delta$ modulators. Due to the complexity of settling problems, analytic models for related noises are nonexistent. Recently, some papers [1]–[3] have considered the transient transfer of charge in SC integrators and proposed several time-domain-based behavioral descriptions, which can be used in behavioral simulations. On the other hand, analytical efforts have actually been seen before. In [4]–[6], a detailed transient analysis for the charge-transfer error was carried out, but only for linear systems. It was coarsely assumed in [7] that the settling noise is white, and that the associated power spectral density (PSD) is constant in the sampling interval, but this is not close to reality.

The main purpose of this brief is to derive an analytical model for settling noises in SC $\Sigma\Delta$ modulators. The settling problems of SC integrators are mainly caused by nonidealities of operational transconductance amplifier (OTA), such as finite dc gain, GBW, and SR. Our research shows that these nonidealities create nonlinear transfer characteristics, which not only cause signal distortions (settling distortions) but also reflect high-frequency noises into the baseband (settling noises). Some analytical results about settling distortions have been provided in [7]. By employing nonlinear fitting methods and output spectrum prediction techniques, closed forms of settling error analytical models are obtained and represented as functions of $\Sigma\Delta$ modulator system parameters. Both behavioral simulations and transistor-level circuit simulations are employed to verify these analytical models, and the results show that our analytical models are sufficiently accurate.

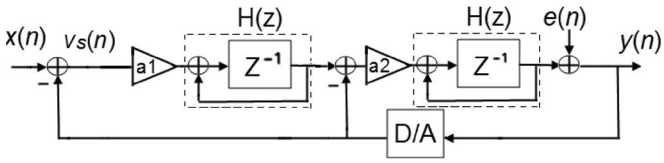

Fig. 1. Single-loop second-order $\Sigma\Delta$ modulator.

This brief is organized as follows. In Section II, the sources of $\Sigma\Delta$ modulator settling errors and the properties of the input to SC integrators are discussed. The formulation of analytical settling noise power model is presented in Section III. In Section IV, transistor-level simulations and behavioral simulations are used to validate the models presented in this brief. Conclusions appear in Section V.

II. Formulation of $\Sigma\Delta$ Modulator Settling Problems

In this brief, the discussions will be for a second-order single-loop $\Sigma\Delta$ modulator shown in Fig. 1. Settling noise models for other types of modulators can be obtained using the techniques presented in this brief. In the following discussions, $v_s(n)$ is the input to the first stage integrator of the $\Sigma\Delta$ modulator, V_S denotes the value of $v_s(n)$ at a particular time step, and $V_S(f)$ represents the frequency-domain description of $v_s(n)$.

A. Settling Noises of Sampling Phase and Integration Phase

Behavioral descriptions for settling errors are well known [2], [8]. The settling error during the sampling phase is

$$\varepsilon_1 = V_S \cdot \exp\left(-\frac{T}{2\cdot\tau_1}\right). \tag{1}$$

The settling error ε_2 during the integration phase can be divided into three cases:

1) linear settling

$$\varepsilon_2 = a_1 \cdot V_S \cdot \exp\left(-\frac{T}{2\cdot\tau_2}\right), \text{when } 0 < |V_S| < \frac{1}{a_1}\cdot SR\cdot\tau_2 \tag{2}$$

2) partial slewing

$$\varepsilon_2 = SR\cdot\tau_2\cdot\operatorname{sgn}(V_S)\cdot\exp\left(\frac{a_1\cdot|V_S|}{SR\cdot\tau_2} - \frac{T}{2\tau_2} - 1\right), \quad \text{when } \frac{1}{a_1}\cdot SR\cdot\tau_2 < |V_S| < \left(\frac{T}{2}+\tau_2\right)\frac{SR}{a_1} \tag{3}$$

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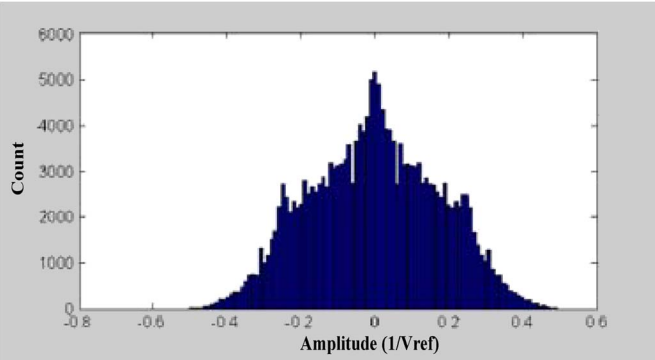

Fig. 2. Histogram distribution of $v_s(n)$.

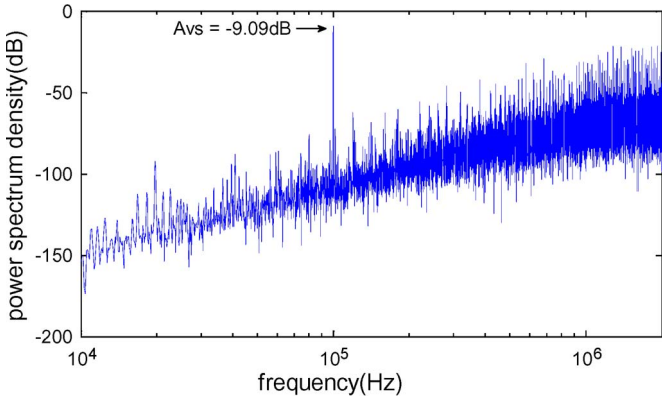

Fig. 3. PSD of $v_s(n)$.

3) Fully slewing

$$\varepsilon_2 = a_1 \cdot V_S - SR \cdot \mathrm{sgn}(V_S) \cdot \frac{T}{2}, \quad \text{when } |V_S| > \frac{SR}{a_1}\left(\frac{T}{2} + \tau_2\right) \tag{4}$$

where SR is the slew rate of OTA, a_1 is a constant before the integrator, and $\tau_2 = (1 + 2\pi \cdot GBW \cdot R_S \cdot C_S / 2\pi \cdot GBW)$ is the time constant in the integration phase, with GBW being the equivalent gain bandwidth in the integration phase.

B. Properties of $v_s(n)$

A typical time-domain histogram distribution of $v_s(n)$ is shown in Fig. 2, and the frequency-domain property of $v_s(n)$ is plotted in Fig. 3. The time-domain distribution is assumed to be Gaussian, and extensive simulations suggest that the relation between standard deviation σ_{VS} and quantizer levels 2^{B} can be approximated by

$$2^B \cdot \sigma_{vs} \approx 1.4 \cdot |V_{\mathrm{ref}}|. \tag{5}$$

Fig. 3 indicates that a small sinusoidal signal exists in $v_s(n)$. Since this small sinusoid has little influence on the settling noise to be discussed, it is ignored. Under this assumption, the height of PSD of the noise part of $v_s(n)$ is mathematically described as

$$|V_S(f)| = \left[2 \cdot \sin\left(\frac{\pi \cdot f}{f_S}\right)\right]^2 \cdot \frac{V_{\mathrm{LSB}}}{\sqrt{12 f_S}} \tag{6}$$

where V_{LSB} is the minimum step size of the quantizer.

III. Derivation of Sigma–Delta Modulator Settling Noise Power Model

In this section, models of settling noises that appear at the $\Sigma\Delta$ modulator output will be derived and expressed in noise power form. This derivation is divided into sampling phase and integration phase. Most of the complexity appears in the integration phase. Nonidealities in OTA can cause nonlinear transfer characteristics, which can increase the noise power in baseband. This nonlinearity is approximated by a nonlinear fitting that takes into account the time-domain distribution of the SC integrator input $v_s(n)$ described in (5). Then, circular convolution is employed to synthesize the PSD of settling noises at $\Sigma\Delta$ modulator output.

A. Settling Noise Power of Sampling Phase

From (1) and (6), we have

$$P_{\varepsilon_1} = \int_{-f_B}^{f_B} \varepsilon_1^2(f) df = \int_{-f_B}^{f_B} V_S^2(f) \exp^2\left(-\frac{T}{2\tau_1}\right) df$$
$$= \int_{-f_B}^{f_B} \frac{V_{\mathrm{LSB}}^2}{12 f_s}\left[4\sin^2\left(\frac{\pi \cdot f}{f_s}\right) \times \exp\left(-\frac{T}{2\tau_1}\right)\right]^2 df. \tag{7}$$

B. Settling Noise Power of Integration Phase

There are three settling conditions depending on the absolute value of V_S. The full slewing case is not considered here because it is not significant. From (2) and (3), it can be verified that the actually integrated value at the end of each integration interval can be written as

$$V_S(T) = \begin{cases} a_1 V_S(1-\beta), & |V_S| \le V_L \\ a_1 V_S\left(1 - \frac{V_L}{|V_S|}\beta e^{-1} e^{|V_S|/V_L}\right), & |V_S| > V_L \end{cases} \tag{8}$$

where $\beta = \exp(-T/2\tau_2)$, and $V_L = SR\tau_2/a_1$.

From (8), the settling error of the integration phase can be expressed as

$$\varepsilon_2(V_S) = \begin{cases} a_1 V_S \beta, & |V_S| \le V_L \\ a_1 \mathrm{sgn}(V_S) V_L \beta e^{-1} e^{|V_S|/V_L}, & |V_S| > V_L. \end{cases} \tag{9}$$

To analyze the effect of the nonlinear error [see (9)], it is approximated by the polynomial

$$p_i(V_S) = \alpha_1 V_S + \alpha_3 V_S^3 + \alpha_5 V_S^5. \tag{10}$$

Then, the least-square method is applied, and a cost function is defined to be

$$C = \int_0^{V_H} [\varepsilon_2(V_S) - p_i(V_S)]^2 \times W(V_S) dV_S \tag{11}$$

where V_H is defined as $2V_{\mathrm{ref}}$, and $W(V_S)$ is a Gaussian weighting function implementing (5). With the foregoing method, the coefficients in (10) for C to be minimum can be found to be as that in (12), shown at the bottom of the next page.

With coefficients α_1, α_3, and α_5 in (10) determined, the next step for calculating the settling noise power is to determine

$V_S^3(f)$ and $V_S^5(f)$ in (10) by using $V_S(f)$. To do this, the height of the PSD of $v_s(n)$ in (6) is modified to include angle as

$$h_e(f) = \frac{V_{\mathrm{LSB}}}{\sqrt{12 f_s}} \left[2 \sin \left(\frac{\pi \cdot f}{f_s} \right) \right]^2 \times e^{i\theta(f)} \tag{13}$$

where θ represents the angle of h_e at a particular frequency f. The angle of $V_S(f)$ should be included in the computation of $V_S^3(f)$ and $V_S^5(f)$ so that correct results can be obtained. Simulation results show that the angle of $V_S(f)$ is close to a uniform distribution. Therefore, θ is assumed to be an arbitrary value in $0 \sim 2\pi$. To find out $V_S^3(f)$, we first try to generate $h_{e2}(f)$, which is the height of PSD of the square of $v_s(n)$. When $f = 0$, $h_{e2}(0)$ denotes the sum of square of $v_s(n)$ in time domain. From Parseval's theorem, we get

$$\begin{aligned} h_{e2}(0) &= \sum v_s^2(n) \\ &= \frac{1}{f_s} \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \left\{ \frac{V_{\mathrm{LSB}}}{\sqrt{12 f_s}} \left[2 \sin \left(\frac{\pi \cdot f}{f_s} \right) \right]^2 \right\}^2 df. \end{aligned} \tag{14}$$

When $f \neq 0$, by applying circular convolution, we can express the height of PSD of the square of $v_s(n)$ as

$$\begin{aligned} h_{e2}(f) &= h_e(f) \otimes h_e(f) \\ &= \frac{V_{\mathrm{LSB}}}{\sqrt{12 f_s}} \left[2 \sin \left(\frac{\pi \cdot f}{f_s} \right) \right]^2 \times e^{i\theta(f)} \\ &\quad \otimes \frac{V_{\mathrm{LSB}}}{\sqrt{12 f_s}} \left[2 \sin \left(\frac{\pi \cdot f}{f_s} \right) \right]^2 \times e^{i\theta(f)} \\ &= \frac{1}{f_s} \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{V_{\mathrm{LSB}}^2}{12 f_s} \left[2 \sin \left(\frac{\pi \cdot f_1}{f_s} \right) \right]^2 \\ &\quad \cdot \left[2 \sin \left(\frac{\pi \cdot (f - f_1)}{f_s} \right) \right]^2 \times e^{i\theta(f_1)} \times e^{i\theta(f - f_1)} df_1. \end{aligned} \tag{15}$$

It is clear that we cannot correctly compute the magnitude of h_{e2} without taking into account the angle of h_e. Then, the

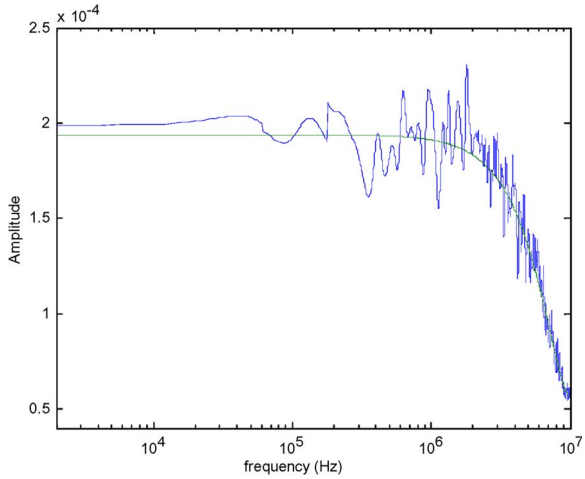

Fig. 4. Comparison of the expected value of $h_{e2}(f)$ with the behavioral simulation result.

expected value of the magnitude of h_{e2} can be expressed as

$$\begin{aligned} E\{h_{e2}(f)\} = \frac{1}{f_s} \frac{4 V_{\mathrm{LSB}}^2}{3 f_s} \Bigg[& \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \sin^4 \left(\frac{\pi \cdot f_1}{f_s} \right) \\ & \times \sin^4 \left(\frac{\pi (f - f_1)}{f_s} \right) df_1 \Bigg]^{0.5}. \end{aligned} \tag{16}$$

Fig. 4 compares the expected value of (16) and the result obtained from behavioral model simulation with $f_s = 20$ MHz and $B = 1$ bit.

Then, we can follow the foregoing technique to obtain $V_S^3(f)$ by convolving $V_S(f)$ and $V_S^2(f)$, and the expected value of $V_S^5(f)$ by convolving $V_S^2(f)$ and $V_S^3(f)$, i.e.

$$h_{e3}(f) = h_e(f) \otimes h_{e2}(f) \tag{17}$$

$$h_{e5}(f) = h_{e3}(f) \otimes h_{e2}(f). \tag{18}$$

Figs. 5 and 6 respectively compares the expected values of h_{e3} and h_{e5} with corresponding simulation results. Then, the

$$\begin{bmatrix} \alpha_1 \\ \alpha_3 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} \int_0^{V_H} W(V_S) V_S^2 dV_S & \int_0^{V_H} W(V_S) V_S^4 dV_S & \int_0^{V_H} W(V_S) V_S^6 dV_S \\ \int_0^{V_H} W(V_S) V_S^4 dV_S & \int_0^{V_H} W(V_S) V_S^6 dV_S & \int_0^{V_H} W(V_S) V_S^8 dV_S \\ \int_0^{V_H} W(V_S) V_S^6 dV_S & \int_0^{V_H} W(V_S) V_S^8 dV_S & \int_0^{V_H} W(V_S) V_S^{10} dV_S \end{bmatrix}^{-1}$$

$$\times \begin{bmatrix} \int_0^{V_L} W(V_S) \beta V_S^2 dV_S + \int_{V_L}^{V_H} W(V_S) V_L \beta e^{-1} e^{|V_S|/V_L} V_S dV_S \\ \int_0^{V_L} W(V_S) \beta \cdot V_S^4 dV_S + \int_{V_L}^{V_H} W(V_S) V_L \beta e^{-1} e^{|V_S|/V_L} V_S^3 dV_S \\ \int_0^{V_L} W(V_S) \beta \cdot V_S^6 dV_S + \int_{V_L}^{V_H} W(V_S) V_L \beta e^{-1} e^{|V_S|/V_L} V_S^5 dV_S \end{bmatrix} \tag{12}$$

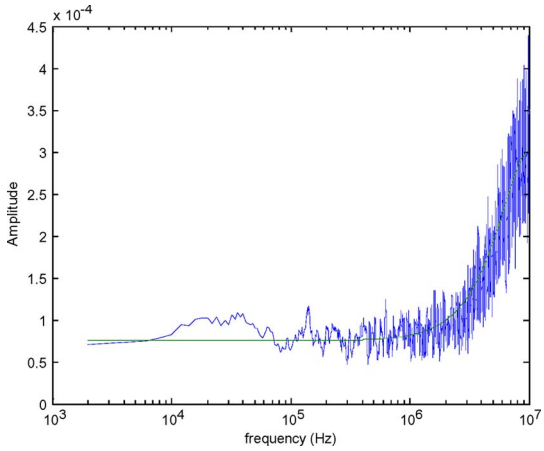

Fig. 5. Comparison of the expected value of $h_{e3}(f)$ with the simulation result by behavioral model.

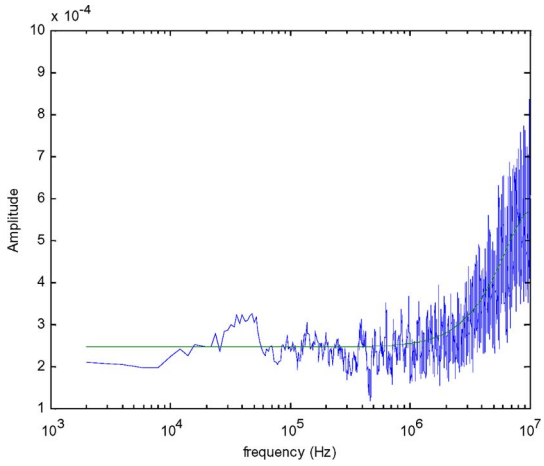

Fig. 6. Comparison of the expected value of $h_{e5}(f)$ with the behavioral simulation result.

expected value of the height of PSD of the settling noise of integration phase can be defined as

$$E\{h(f)\} = \alpha_1 E\{h_{e1}\} + \alpha_3 E\{h_{e3}\} + \alpha_5 E\{h_{e5}\}. \quad (19)$$

Therefore, the settling noise of integration phase in baseband $\pm f_B$ can be obtained by integrating (19) as

$$P_{\varepsilon 2} = \int_{-f_B}^{f_B} \left(\alpha_1 E\{h_{e1}\} + \alpha_3 E\{h_{e3}\} + \alpha_5 E\{h_{e5}\}\right)^2 df. \quad (20)$$

With the sampling-phase settling error $P_{\varepsilon 1}$ expressed in (7) and the integration-phase settling error $P_{\varepsilon 2}$ expressed in (20), the total settling noise power P_ε can be computed as

$$P_\varepsilon = P_{\varepsilon 1} + P_{\varepsilon 2}. \quad (21)$$

Discussion 1: Settling noise is mainly caused by the insufficiency in OTA SR and GBW values. In Fig. 7(a), settling noise is not obvious compared with quantization noise because SR and GBW are large enough. If SR and GBW of OTA are not large enough, the nonlinear effect becomes serious, and it can bring high-frequency noises into the baseband, which results in a large and flat noise floor in the baseband, as shown in

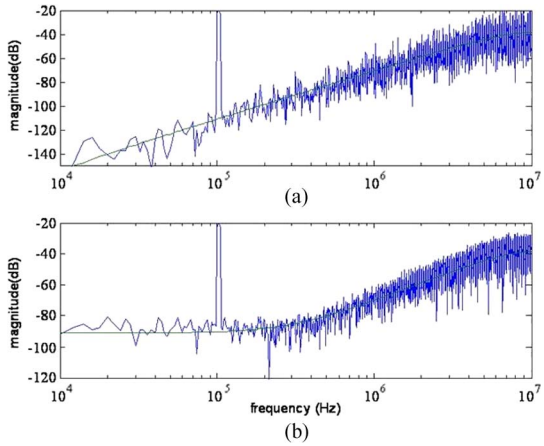

Fig. 7. Settling noise of integration phase with different parameters. (a) GBW = 80 MHz, SR = 80 V/μs. (b) GBW = 32 MHz, SR = 30 V/μs.

TABLE I
MINIMUM SR AND GBW REQUIRED W.R.T. OSR

OSR	Quantization Noise Power (dB)	Settling Noise Power(dB)	*SR* (*V*/μs)	*GBW* (MHz)
16	-58.1	$\leq$ -58.1	$\geq$ 12	$\geq$ 24
64	-88.2.	$\leq$ -88.2	$\geq$ 108	$\geq$ 64
100	-97.9	$\leq$ -97.9	$\geq$ 220	$\geq$ 90
140	-105.2	$\leq$ -105.2	$\geq$ 324	$\geq$ 113

Minimum SR and GBW required w. r. t. OSR

Fig. 7(b). Both cases in Fig. 7(a) and (b) are precisely predicted by our model. Note that α_3 and α_5 in (19) are 6.1×10^{-8} and 1.8×10^{-7} for Fig. 7(a), and they are much larger at -0.0016 and 0.0047 for Fig. 7(b). Since the low-frequency regions of $V_S^3(f)$ and $V_S^5(f)$ in Figs. 5 and 6 are flat, the $\Sigma\Delta$ modulator baseband noise would increase if α_3 and α_5 increase. Insufficient SR and GBW values quickly enlarge α_3 and α_5 so that $V_S^3(f)$ and $V_S^5(f)$ strongly impact the baseband.

Discussion 2: Our settling noise model can be used to determine OTA SR and GBW values. Among all $\Sigma\Delta$ modulator noises and distortions, the settling noise is the only one that significantly relates to OTA SR and GBW. The settling distortion [7] is also related to OTA SR and GBW, but to a less extent. Table I shows the minimum required OTA SR and GBW that double the in-band noise power w.r.t. the ideal performance.

Discussion 3: The settling noise model proposed in this brief renders the model-based $\Sigma\Delta$ modulator design optimization feasible. Behavior-simulation-based $\Sigma\Delta$ modulator design optimization has been reported in [8]. Model-based optimization can potentially be hundreds of times faster than behavior-simulation-based optimization. However, model-based optimization requires the availability of analytical models of *all* essential $\Sigma\Delta$ modulator noises and distortions. The settling noise model is the only essential analytical noise and distortion model that is not available, so it is very important that we propose a settling noise model in this brief.

IV. SIMULATION RESULTS AND VALIDATION

Spice simulation is used to verify the models presented in the previous section. The circuit-level schematic of spice

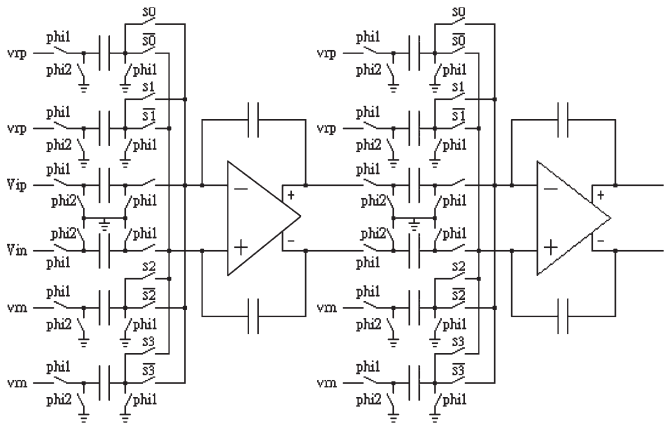

Fig. 8. Circuit-level schematic of SPICE simulation.

TABLE II
SIMULATION PARAMETERS IN FIG. 9

Parameter	Fig. 9(a)	Fig. 9(b)	Fig. 9(c)
SR $(V/\mu s)$	40	30	15
GBW(MHz)	40	32	25
P_{ε}(dB)	-85.4	-68.48	-49.2

simulation is shown in Fig. 8. The relevant parameters are $f_B = 100$ kHz, $OSR = 100$, $C_S = 0.5$ pF, $C_I = 1$ pF, and a 100-kHz sinusoidal input signal.

Three pairs of SR and GBW are employed (shown in Table II), which correspond to Fig. 9(a)–(c), respectively. In Fig. 9, three results are compared: one is from our settling noise model, and the other two are obtained from transistor-level simulation and from behavioral simulation. Since the noise observed in simulations inevitably blends together the settling noise and the quantization noise, the theoretical noise PSD shown in Fig. 9 is constructed by adding our theoretical settling noise to the theoretical quantization noise.

Fig. 9 shows good agreement in simulation and theoretical results. As OTA SR and GBW decrease from Fig. 9(a)–(c), the baseband noise floor significantly rises, and the low-frequency flat-noise-floor region also expand to about ten times as wide. The baseband settling error powers for Fig. 9(a)–(c) computed using our model are also listed in Table II.

V. CONCLUSION

This brief has presented an analytical model for settling noise in (single-loop) sigma–delta modulators. In the past, the impact of settling noise could only be revealed through time-domain behavioral simulations. This analytical model is not meant to replace behavioral simulations, but it can have many applications. For example, by inputting system parameters, such as OSR, GBW, SR, etc., this model can compute the settling noise power that appears at the $\Sigma\Delta$ modulator output. Therefore, it can integrate with other available noise and distortion models to generate a $SNDR$ to be used in $\Sigma\Delta$ modulator design optimization. This model can also reversibly be applied to compute the required OTA GBW and SR for limiting the settling noise to be under a certain level. In addition, our settling noise model can serve to reveal the mechanism about how nonlinearity transfers high-frequency noises into baseband.

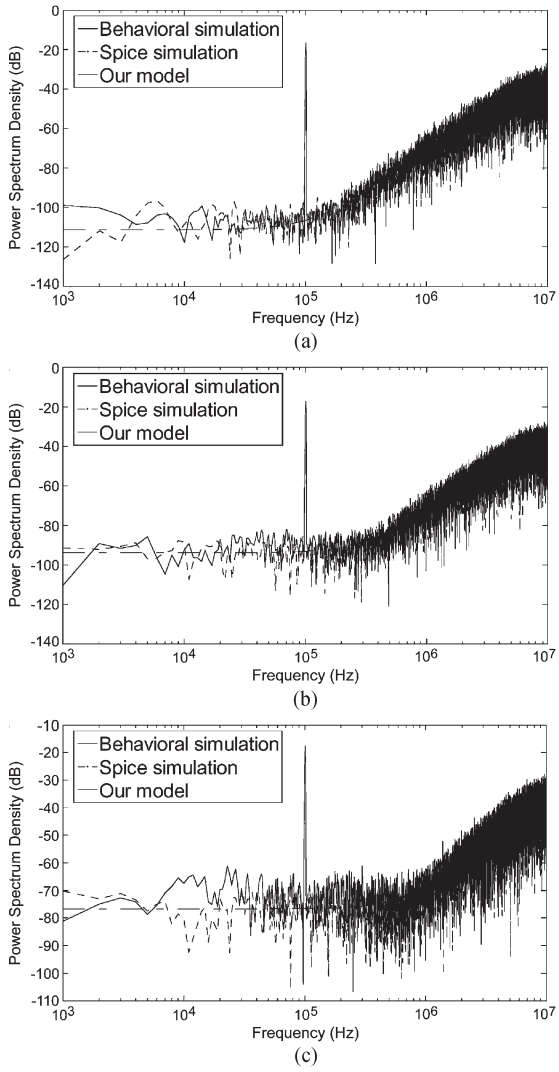

Fig. 9. Comparison of our theoretical result with transistor-level and behavioral simulation results.

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