

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

氮化矽記憶體資料保存行為之數值分
析模擬



**Numerical Analysis of the Retention Behavior in
Nitride Storage Flash Memory Cells**

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摘要

本篇論文主要探討氮化矽記憶元件內儲存電荷之保存性與穿隧氧化層厚度之關聯。利用特殊的數值方法並以多層儲存陷阱物理模型(multiple trapping model)分析，來求解 S.R.H. 方程式而更精準地提出一種記憶體資料保存行為的表示法。在求解的方程式中，我們用直接穿隧(Direct-tunneling)和透過缺陷助益穿隧(trap-assisted-tunneling)來描述電荷流失的現象，並依據一種對偶的行為 - 儲存在缺陷電子經 Frenkel-Poole 激發到傳導帶而傳導帶的自由電子可能被缺陷再捕捉回去 - 來說明電荷在氮化矽層的行為。由上述可知，我們的研究將會說明這種自由電子再被捕捉(recapture)回儲存態和穿隧現象來決定自由電子的濃度，並隨著穿隧氧化層厚度增加電荷再被陷阱捕獲行為更加明顯。利用這種再捕捉的行為可以阻擋電荷流失並增加資料保存的時間。而更深入的探討，在高溫的情況會增加電荷逃逸，還有穿隧氧化層 stress 效應都將會在這篇論文裡面討論。

Numerical Analysis of the Retention Behavior in Nitride Storage Flash Memory

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Abstract.

The bottom oxide thickness induced the charge loss blocking effect for a SONOS type flash memory is investigated. Utilizing a numerical analysis based on a multiple trapping model for solving the Shockley-Read-Hall (SRH) rate equations, the more accurate expressions for retention behavior are developed. In these equations, the classical tunneling and the stress-induced oxide trap-assisted tunneling mainly accounts for the charge loss and the trapped charge via Frenkel-Poole excitation to conduction band coupled with the conduction free carriers recapture by the traps is used to describe the charge transition within silicon-nitride (SiN) film. The free carrier concentration is governed by two competing processes, tunneling out to Si and recaptured by SiN traps. Our study shows that in an unstressed cell the recapture process starts to dominate as the bottom oxide thickness

increases. This will block the charge loss and then improve the retention time. In addition, the high temperature enhanced charge escape and the bottom oxide stress effect accelerated data loss have been considered in this thesis.



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Chapter 1

Introduction

In recent years, great efforts have been invested in nitride-based storage flash memory due to the advantages of the low power, low voltage operation [1][2], the simplicity of the process [3], the ability of continued scaling and the immunity to extrinsic charge loss as compared to the industry standard floating gate flash cell [4]. These type nitride flash cells resemble a standard MOS transistor except that the gate oxide is replaced by an oxide-nitride-oxide gate dielectric stack and can be categorized into uniform storage memory, such as SONOS (positive and negative FN program and erase illustrated in Fig. 1.1), and non-uniform storage memory, such as NROM [5]-[7] (channel hot electron program and band-to-band hot hole erase demonstrated in Fig. 1.2). In addition, SONOS differs from NROM in the bottom oxide thickness. Generally, SONOS memory has a thinner oxide to achieve a high speed of FN programming and erase. However, the data retention has been a critical concern because such thin oxide hardly barricades the charge leakage from the nitride storage node. Therefore, the optimization of the bottom oxide thickness is vital important for amelioration of SONOS technology.

Several groups have identified several kinds of charge loss mechanisms in nitride-based devices. Lundkvist et al. described that both the stored electrons direct tunneling to Si and the thermal excitation out from the nitride trap account for retention loss mechanism [8]. Lehovc et al. delivered a simple retention model based on Frenkel-Poole (F-P) release from monoenergetic traps [9][10]. White et al. considered the trap-to-band tunneling combined with the thermal excitation detrapping simultaneously to develop an analytical way to consist with the measurement data [11]. Recently, Wang et al. presented that the nitride charge escapes via F-P emission, followed by a subsequent stress-induced oxide trap assisted

tunneling [12]. Although various physical models have been derived, more conditions should be considered to emulate the retention characteristics accurately. Most models [13] assume that if the charges are emitted to the SiN conduction band, they will be completely emptied out through the ultra-thin bottom oxide ($\sim 20\text{\AA}$). This thermal emission enhances the charge decay for a device operated at an evaluated temperature environment. However, for the improvement of the data retention and the minimization of the gate disturb, the thicker bottom oxide is a great solution [14]-[17]. As we know, the tunneling probability decreases exponentially with the increasing the oxide thickness, thereby retarding the charge tunneling out. This would make the assumption that the neglect of tunneling time through the ultra-thin oxide is not applicable for a device with thick oxide.

The purpose of this study is to ascertain the bottom oxide thickness dependence on the data retention characteristics of using a numerical simulation. It is suggested that the thicker bottom oxide will block the charge loss, so that the retention behavior can not be expressed by a simple analytical form. For this reason, the multiple trapping models to solve numerically the SRH equations will be introduced. Each loss mechanism for the SONOS memory is illustrated explicitly in Chapter 2. In Chapter 3, the method for our numerical simulation will be interpreted. The implicit backward Euler coupled with Newton iteration is coded within numerical accuracy. In Chapter 4, the simulation and measurement results are compared. Some factors including the temperature dependence, oxide thickness effect, and the stress-induced oxide trap enhanced tunneling are also investigated.

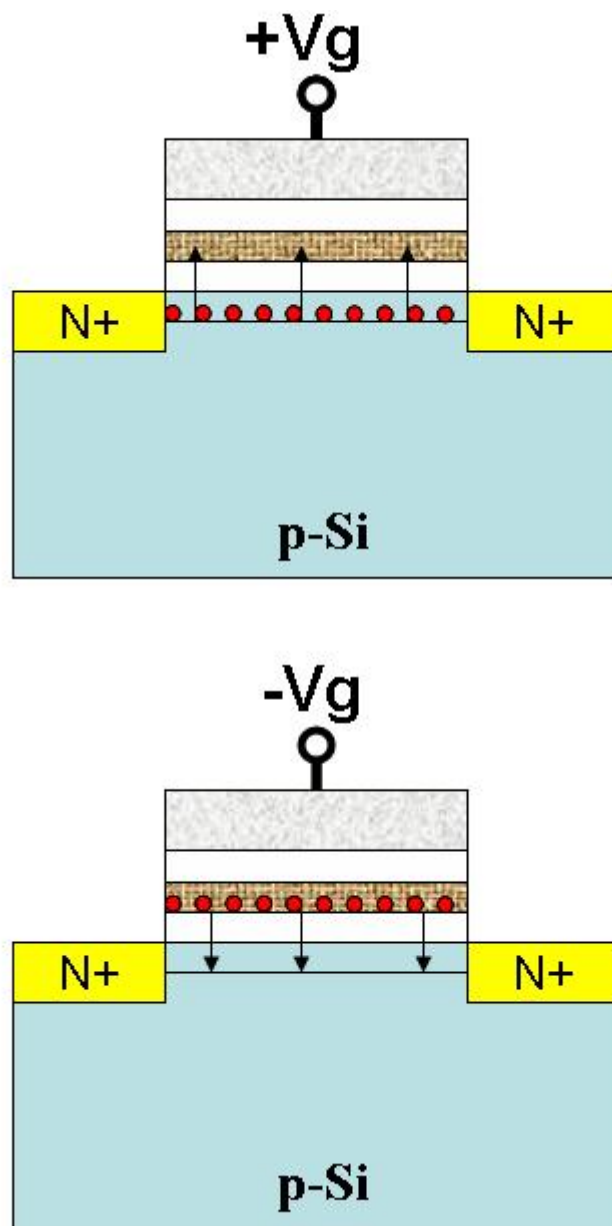


Fig. 1.1 Charge injections in SONOS device during (a) +FN write and (b) -FN erase operation

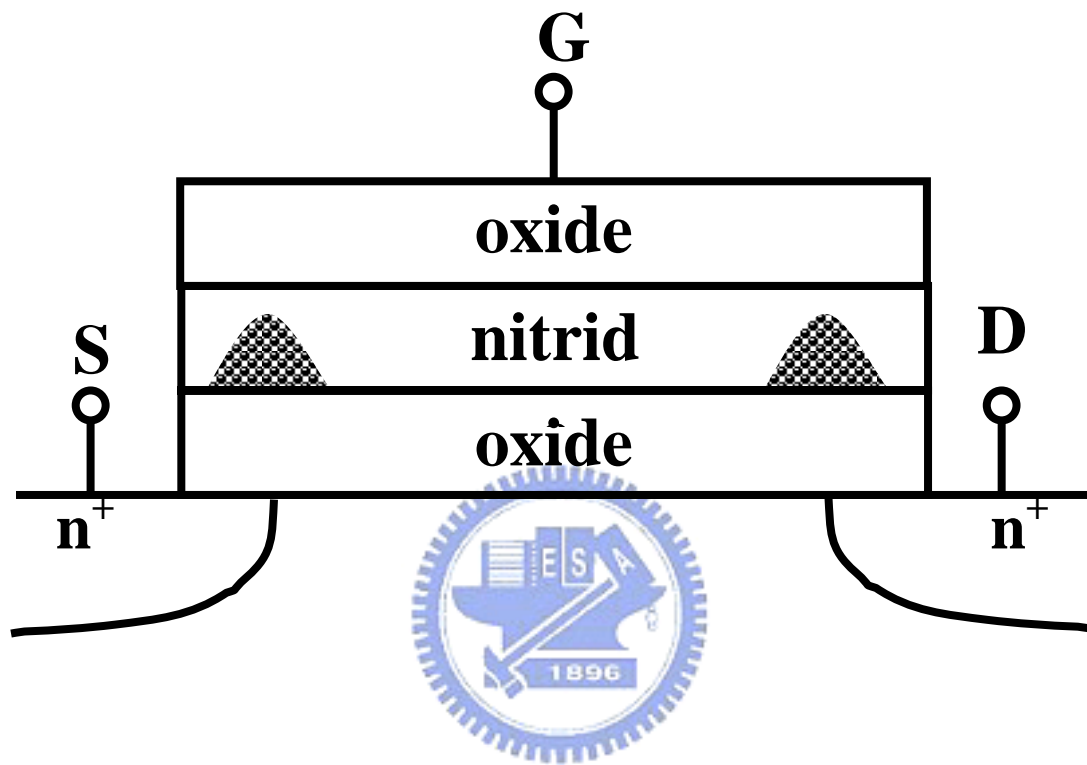


Fig. 1.2 Schematic representation of a SONOS cell and two-bit storage. The shaded area in the nitride layer represents stored charges.

Chapter 2

Theoretical model for data retention

2.1 Introduction

In this chapter, the detailed charge transport mechanisms in nitride-based memories were investigated theoretically. In previous research, many groups have proposed the retention loss models neglecting the excited carriers recapture by SiN traps [18] or merely studying the monoenergetic trap level [19][20]. To characterize the accurate decay transient, the recapture events with a multiple trapping states have been taken into account in our model.

Here, we adopt the rate equations, based on Shockley-Read-Hall (SRH) theory, describing electrons capture, release and tunneling transitions. The Wentzel-Kramer-Brillouin (WKB) approximation as well as trap-like approach depicts the tunneling feature.



2.2 Theoretical Basis

2.2.1 SRH rate equation

The complete charge decay mechanism comprising the tunneling of electrons from trapping site or from SiN conduction band to Si with a series of emission and capture processes is proposed. The four processes are depicted in Fig. 2.1 and the charge transport can be described by two sets cross-coupled SRH rate equations.

$$\frac{dn_t(x, \phi, t)}{dt} = [R_c(x, \phi, t) \cdot n_c(t) - R_e(\phi) \cdot n_t(x, \phi, t)] - R_t(x, \phi) \cdot n_t(x, \phi, t) \quad (2.1)$$

$$T_n \cdot \frac{dn_c(t)}{dt} = -(\int \int R_c(x, \phi, t) \cdot n_c(t) d\phi dx - \int \int R_e(\phi) \cdot n_t(x, \phi, t) d\phi dx) - R_{loss} \cdot T_n \cdot n_c \quad (2.2)$$

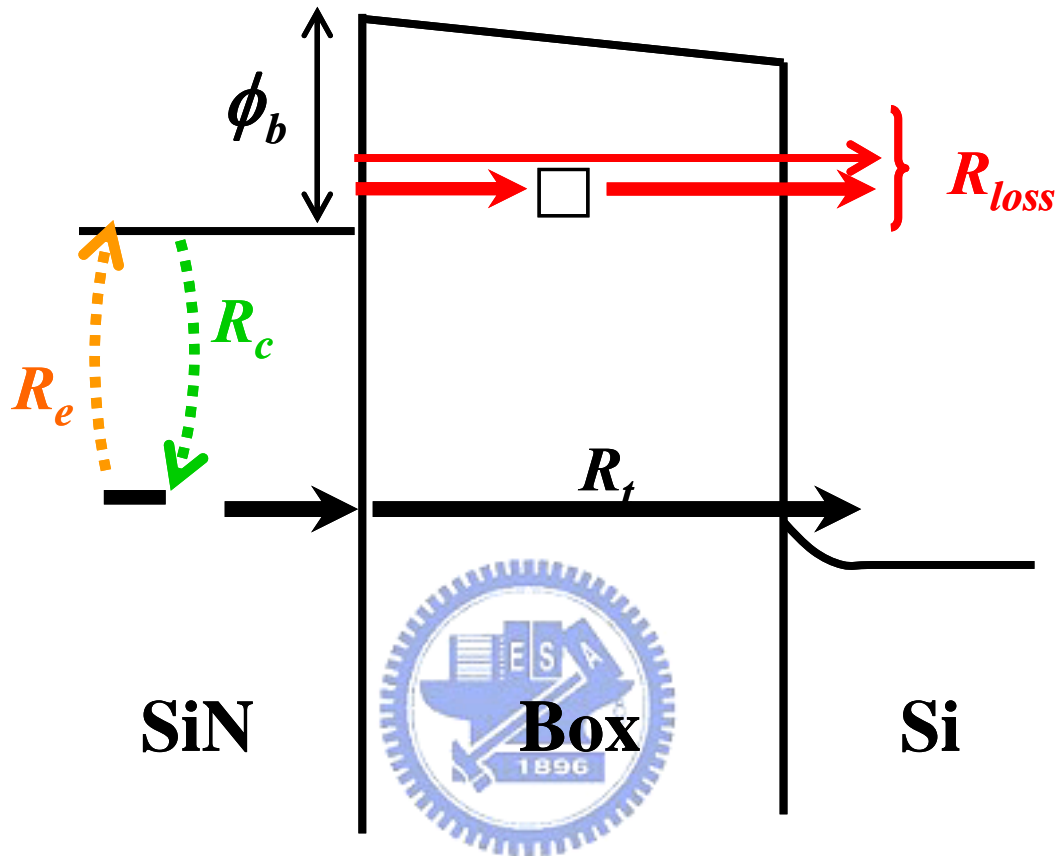


Fig. 2.1. Bandgap diagram of a SONOS device, showing retention loss mechanism: trap-to band tunneling rate (R_t), band-to-band tunneling rate (R_{loss}), Frenkel-Poole emission rate (R_e), and capture rate (R_c).

Eq. (2.1) is such a change rate for each trapping state concentration and Eq. (2.2) expresses the excess carrier transport in the SiN conduction band. Here, n_t and n_c are the concentration of occupied and free electrons, x and ϕ is the distance and energy depth from bottom oxide/SiN interface and from the nitride conduction band edge, respectively. t stands for the retention time and T_n is the thickness of SiN film. The first term on the right-hand in Eq. (2.1) states the capture of the free electrons, the second, F-P emission of the trapped electrons, and the last, direct tunneling of nitride trapped electron to Si. R_c , R_e , and R_t are the capture, emission and direct tunneling rate coefficients, separately. Additionally the total trapping states capture and emission transitions are represented at the first and second terms on the right-hand in Eq. (2.2) and R_{loss} is the loss rate coefficient from nitride conduction. The detailed descriptions for each rate coefficient term are expressed thereafter.

2.2.2 Each rate coefficient

Time constants have been employed to characterize the electron decay behavior in these discharge process, and the reciprocals of the time constants are defined as the corresponding rate coefficients. Each coefficient will be introduced and formulated.

First, the tunneling rate from nitride trap to Si substrate (trap-to-band) has been derived by a trap-like approach [21], and is described by

$$R_t = (N_{C_{Si}} \cdot v_{th} \cdot \sigma_N) \cdot P_N \cdot P_{ox} \quad (2.3)$$

where $N_{C_{Si}}$ is the Si effective density of state in conduction band, v_{th} is the thermal velocity, σ_N is the electron capture cross section of the nitride trap. The quantity of $N_{C_{Si}}$ [22] can be given by

$$N_{C_{Si}} = 2 \left(\frac{2\pi \cdot m_{Si}^* \cdot kT}{h^2} \right)^{3/2} \quad (2.4)$$

where m_{Si}^* is the electron effective mass in Si, k is the Boltzmann constant, and T is the absolute temperature. P_{ox} and P_N are the WKB tunneling probabilities through the bottom oxide and the nitride, individually, and are formulated as follows.

$$P_n = \exp \left\{ - \frac{4\sqrt{2qm_n^*}}{3\hbar E_n} \left[\phi^{3/2} - (\phi - E_n \cdot x)^{3/2} \right] \right\} \quad (2.5)$$



$$P_{ox} = \exp \left\{ - \frac{4\sqrt{2qm_{ox}^*}}{3\hbar E_{ox}} \left[(\phi_b + \phi - E_n \cdot x)^{3/2} - (\phi_b + \phi - E_n \cdot x - E_{ox} \cdot X_{BO})^{3/2} \right] \right\} \quad (2.6)$$



where ϕ_b is the conduction band offset between oxide and nitride, m_n^* and m_{ox}^* are the electron effective mass in nitride and oxide, respectively; E_n and E_{ox} are the average electric field across the nitride and oxide films.

Then, the charge loss from nitride conduction band to Si substrate is

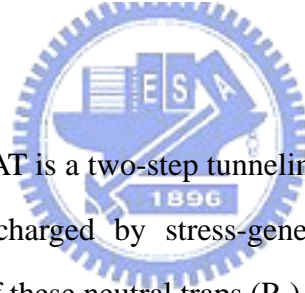
$$R_{loss} = R_{TAT} + R_{tun} \quad (2.7a)$$

R_{TAT} is the trap-assisted-tunneling rate and R_{tun} is the conventional direct tunneling rate, individually. R_{TAT} can be defined as [23]

$$R_{TAT} = v_{th} \cdot \sigma_{ox} \cdot N_{ox} \cdot P_{TAT} \quad (2.7b)$$

where N_{ox} is oxide trap density in bottom oxide, σ_{ox} is the neutral oxide trap capture cross-section and P_{TAT} presents the trap-assisted tunneling probability through the oxide trap. Here, the most favorable trap position is introduced to simplify the P_{TAT} .

$$P_{TAT} = \frac{P_1 \cdot P_2}{P_1 + P_2} \quad (2.7c)$$



It is generally believed that TAT is a two-step tunneling process, i.e. the probability of cathode electrons are first charged by stress-generated traps (P_1) and then are immediately discharged out of these neutral traps (P_2).

In Eq.(2.7a), R_{tun} expression can be obtained [24]

$$R_{tun} = \frac{v_{th}}{T_n} P_{tun} \quad (2.7d)$$

Third, the Frenkel-Poole emission rate from nitride traps to conduction band can be written as

$$R_e(\phi_n) = (N_{C_n} \cdot v_{th} \cdot \sigma_n) \cdot \exp\left(\frac{\beta \sqrt{E_n - \phi_n}}{kT}\right) \quad (2.8a)$$

where the Frenkel-Poole lowering constant β is given by

$$\beta = \sqrt{\frac{q}{\pi \epsilon_0 \epsilon_n}} \quad (2.8b)$$

ϵ_0 and ϵ_n are the permittivity of free space and nitride dielectric constant, individually. Eq. (2.8a) shows that the emission rate has a strong dependence on trap depth and applied electric field, and temperature.

Finally, the capture rate of free carriers in nitride conduction to nitride trap is defined as

$$R_c(x, \phi_n, t) = v_{th} \cdot \sigma_n \cdot N_t (1 - f) \quad (2.9)$$

N_t , is the SiN trap concentration per unit energy and f is occupation factor. It is straightforward that the capture rate is proportional to the density of unfilled traps ($N_t - n_t$).

2.2.3 The component of tunneling current

Summarized the above equations, the charge leakage current density can be described by the following formula:

$$\begin{aligned}
J = & \iint R_t(x, \phi_N) \cdot n_t(x, \phi_N, t) dx d\phi_n \\
& + q \cdot v_{th} \cdot n_c \cdot P_{tun}(\phi_b) \\
& + q \cdot v_{th} \cdot \sigma_{ox} \cdot N_{ox} \cdot P_{TAT} \cdot T_N \cdot n_c
\end{aligned} \tag{2.10}$$

In Eq. (2.10), the entire trapped charge direct tunneling components, non-trap charge tunneling, and trap-assisted tunneling through neutral oxide trap into silicon from conduction band are demonstrated respectively. In the ultra-thin oxide case, the major leakage element is direct tunneling from nitride trapping site to Si substrate. As the bottom oxide thickness and neutral oxide trap density increases, the Frenkel-Poole emission governs the charge decay instead of the direct tunneling [25]. The phenomena will be exhibited in chapter 4.



2.3 Simulation model

2.3.1 Assumption

In this section, the following assumptions are considered to make our simulation procedure simple and easy to handle.

- (a) The distribution of trapping range in energy is between SiN conduction band edge (E_c) and the corresponding Si Fermi-level (E_f). This is due to the trap state below Fermi-level is filled under the thermal equilibrium condition, as shown in Fig. 2.2.
- (b) The trap profile distributes uniformly in trap energy and in space. It is noted that this simplified assumption is sufficient to depict the precise retention behavior.
- (c) The traps inside the nitride film do not interact with each other due to the misalignment between the trap states.
- (d) The excited carriers from trapped states to the nitride conduction band are merged together. In other words, the free carrier density above conduction band is irrelevant to the spatial position.

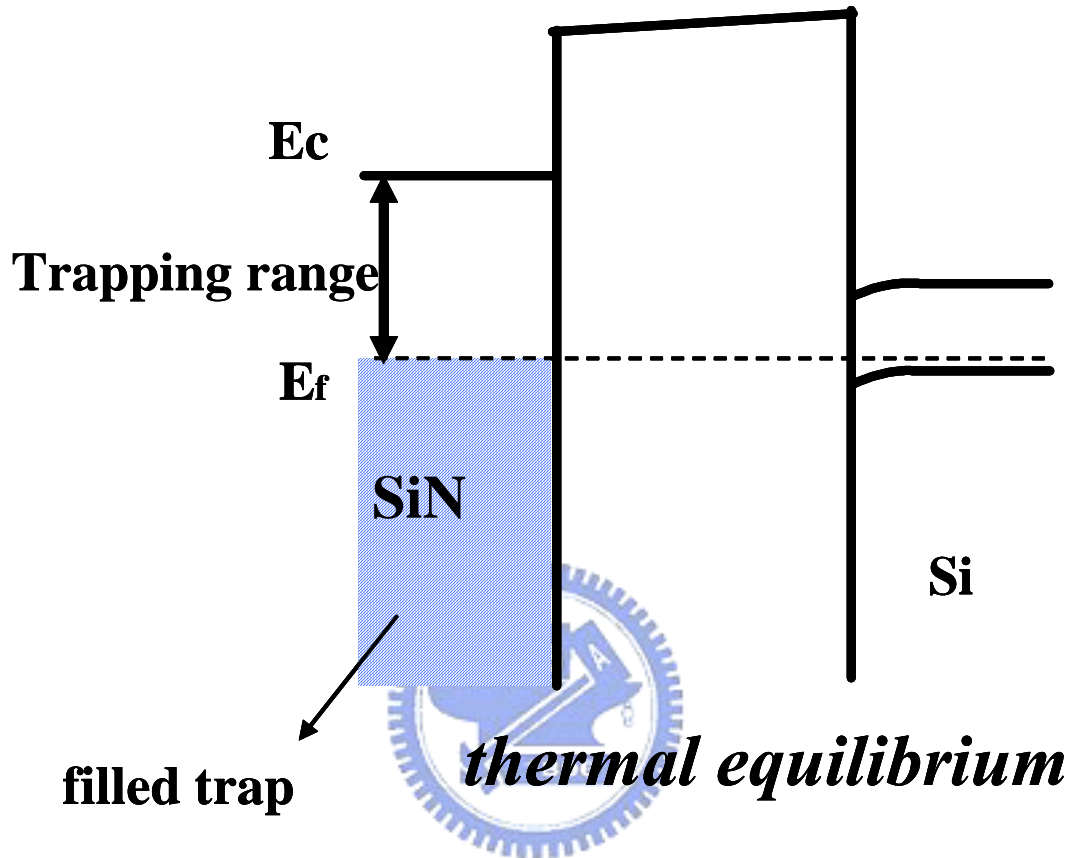


Fig. 2.2. The trapping range of a SONOS device. The shaded area below E_f represents the filled trap states.

2.3.2 Physical and Device Parameters

In this simulation, universal physical constants and band structure constants are listed together with the values in Table 2.1(a). The band structure constants encompass energy barrier heights, energy band gaps of silicon , and effective masses for electrons in the oxide and nitride, etc [26].

Device parameters pertain principally to structural parameters like dielectric constants [27] and nitride trapping parameters including capture cross-section [28]. The device parameters are tabulated with the values in Table 2.1 (b)



Table 2.1(a) Universal physical constants and band structure

Physical Constants		
Symbol	Description	Value
Universal Constant		
m_0	Rest mass of an electron	9.1E-31 (Kg)
q	Electronic charge	1.6E-19 (C)
\hbar	Reduced Planck's Constant	1.05E-34 (J-s)
k	Boltzmann's Constant	8.65E-5 (eV/ K)
ϵ_0	Permittivity of vacuum	8.85E-12(F-m ⁻¹)
Barrier Energy Parameters		
ϕ_b	Electronegativity difference between oxide and nitride	1.5eV
E_{g_si}	Band gap of silicon	1.12eV
Effective Mass Parameter		
m_{ox}	Effective mass for electrons in bottom oxide	0.5m0 kg
m_{SiN}	Effective mass in SiN for electrons	0.5m0 kg

Table 2.1(b) Device Parameters for retention simulation model

Device Parameters		
Symbol	Description	Value
Dielectric Constants		
ϵ_N	Static permittivity for Si ₃ N ₄	5.7 ϵ_0
ϵ_{ox}	Static permittivity for SiO ₂	3.9 ϵ_0
T_n	Thickness of SiN layer	9nm
T_{TOP}	Thickness of top oxide	6nm
Trap Parameters		
σ_N	Carrier capture cross-section for nitride trap	5E-13cm ²
σ_{ox}	Carrier capture cross-section for oxide trap	3E-13cm ²
Other Parameters		
v_{th}	Thermal velocity	1E7cm/s
β	Frenkel-Poole coefficient	3.17E-4

Chapter 3

Simulation Method and Numerical Techniques

3.1 Introduction

In this chapter, first, the strategy to resolve two cross coupled rate equations for the self-consistent solution is introduced. Based on the implicit and iteration numerical schemes, the two stiff and nonlinear equations in our system can be resolved. The simulation procedure is presented in detail and summarized as a flowchart to achieve convergent solutions and to ensure stability.

3.2 Numerical method

3.2.1 Explicit and implicit methods

Several distinct numerical methods have been applied to solve numerical problems. One of the most applicable methods is “explicit” forward Euler. Here, a concept of explicit is explained by a simple ordinary differential equation.

$$\frac{dy}{dt} = -\lambda y \quad (3.1)$$

Eq. (3.1) can be transferred to a first order Taylor expression.

$$\begin{aligned} \frac{y(t + \Delta t) - y(t)}{\Delta t} &= -\lambda y(t) \\ \rightarrow y(t + \Delta t) &= y(t) \cdot (1 - \lambda \Delta t) \end{aligned} \quad (3.2)$$

In the explicit method, the slope at the time t is employed to determine the increment

to the function. The advantage of explicit method is a direct computation without solving a complex iteration. However, this method always has a strict limitation on time step size for stability. If the time step, Δt , is too large, the solution of $y(t+\Delta t)$ cannot converge toward the steady solution, exhibited in Fig. 3.1(a). Therefore, another “implicit” numerical method which permits the larger time step is required. It uses the unknown information at the time $t+\Delta t$ to calculate the solution as formula following.

$$\begin{aligned} \frac{y(t + \Delta t) - y(t)}{\Delta t} &= -\lambda y(t + \Delta t) \\ \rightarrow y(t + \Delta t) &= \frac{y(t)}{(1 + \lambda \Delta t)} \end{aligned} \quad (3.3)$$



In Fig 3.1(b), the implicit concept is demonstrated and there is no divergent solution compared with Fig 3.1(a). The only concern is that to choose an appropriate time step to reach the precise solution. This will be discussed later.

3.2.2 Non-linear and Stiff system

Here, some nomenclatures for our system are given. First, the differential equations in our case are non-linear, containing products of variables. To attain the solution, the Jacobian linearization for non-linear system is essential.

In the amorphous material (SiN), one of the eigenvalues is much larger than the others. Such a system is called a “stiff” system of equations. In our case, the release time varying over many orders of magnitude is very short or long compared to the recapture as well as tunneling time. Standard ‘explicit’ scheme is not feasible because only the time steps shorter than the critical time constant are used. To realize the simulation for long-term retention, the time step should be adjustable. For this reason, implicit Euler scheme is adopted to deal with the stiff problem.

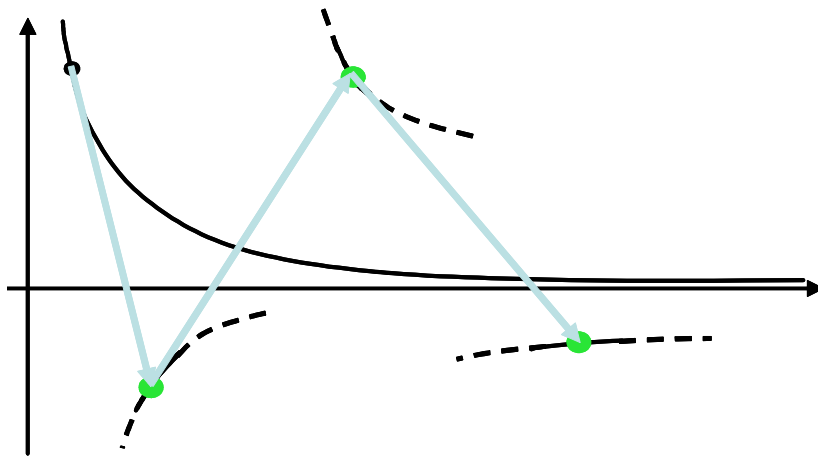


Fig.3.1(a). The “explicit” forward Euler.

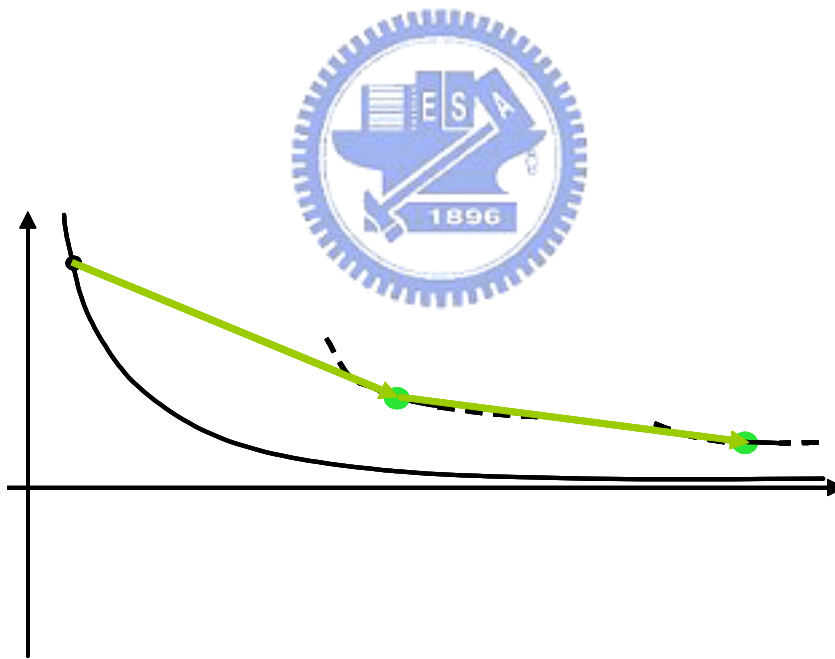


Fig.3.1(b). The “implicit “ backward method.

3.2.3 The Discrete Mesh

Expecting the use of numerical program, the continuous distribution of nitride trap in space and in energy is replaced with discrete approximation. Fig. 3.2 shows schematically the discretized meshes and transitions [29].

The finite difference method obtains an exact site for $n_i(x, \phi)$ at a finite set of x and ϕ . First, the traps are treated as a uniform spread in the interval between $0 \leq x \leq T_N$ and the distance of each spatial node from bottom oxide/SiN interface is

$$x_i = (i - 1)\Delta x \quad i = 1, 2, \dots, N \quad (3.4)$$

where T_N is thickness of SiN film and N is the total number of nodes, including those on the boundary. Given T_N and N , the each spacing is computed with

$$\Delta x = \frac{T_N}{N - 1} \quad (3.5)$$

Similarly, the traps are also assume to distribute uniformly between $0 \leq \phi \leq E_F$ and the discretized energy width is

$$\Delta \phi = \frac{E_F}{(p - 1)}, \quad p = 1, 2, \dots, P \quad (3.6)$$

where E_F is the intrinsic Fermi-level of Si substrate under thermal equilibrium and p is the number of the meshes.

3.2.4 Implement numerical implicit method by Newton iteration

After describing the discretization manner, an implicit backward Euler solution

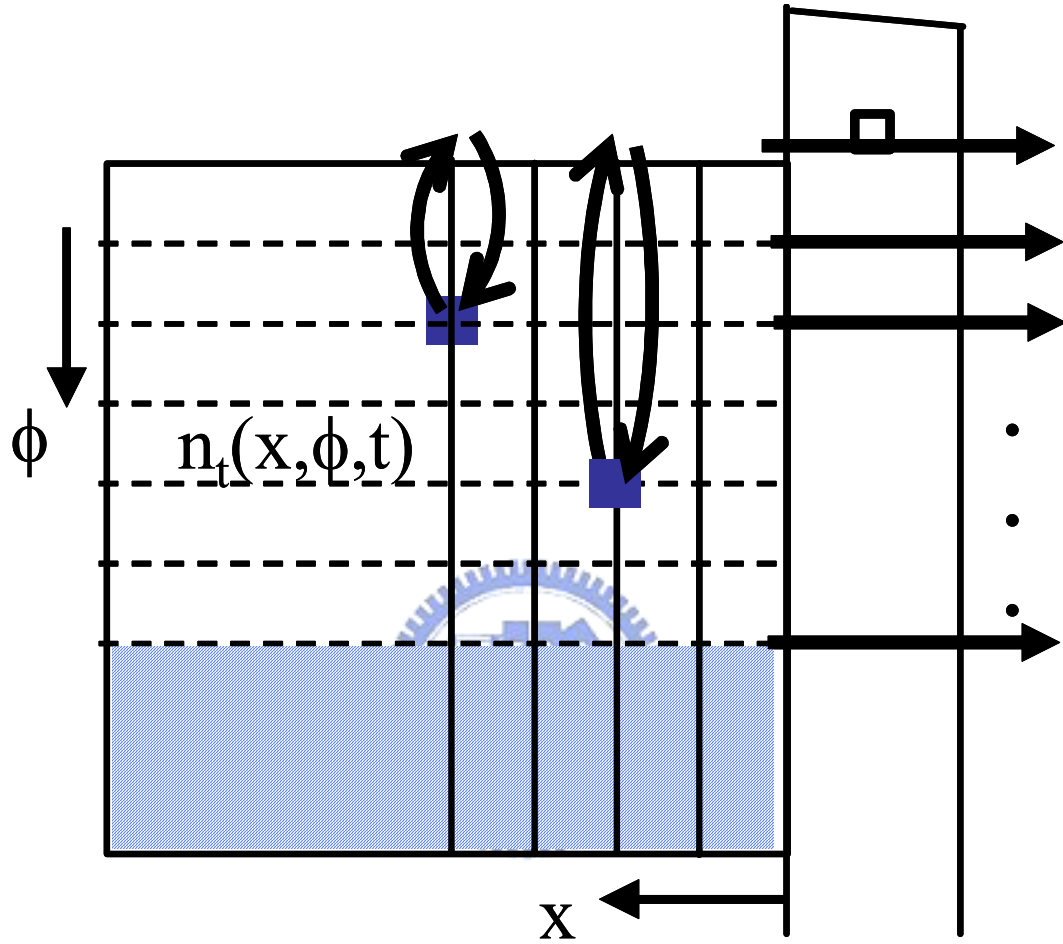


Fig.3.2. The discretized meshes and charge transitions are shown schematically.

conjoint with Newton iteration is selected to provide the required stability for large time step lengths [30], and to reach the steady state solution if the initial guess is reasonable. Prior to the introduction of the simulation procedure, the carrier density variables $y(1)$ and $y(N)$ are labeled, where

$$\begin{aligned} y(1) &= n_c, \text{ the free electron density} \\ y(n) &= \text{the trapped electron density } (2 \leq n \leq M) \end{aligned}$$

and the corresponding $M+1$ coupled equations for derivative functions $f(y)$ in vector form are listed below.

$$\frac{dy(n)}{dt} = f(y(n)) = \begin{bmatrix} f(y(1)) \\ f(y(2)) \\ \vdots \\ f(y(M)) \end{bmatrix} \quad (3.7)$$



where

$$\frac{dy(1)}{dt} = f(y(1)) = \frac{-\sum_2^{Yn} R_d(N_t - y(n)) \cdot y(1)}{T_N} dx + \frac{\sum_2^{Yn} R_e(n) \cdot y(n)}{T_N} dx - R_{loss} \cdot y(1) \quad (3.8)$$

$$\begin{aligned} f(y(2)) &= R_d(N_t - y(2)) \cdot y(1) - (R_e(2) + R_t(2)) \cdot y(2) \\ &\vdots \end{aligned} \quad (3.9)$$

$$f(y(M)) = R_d(N_t - y(M)) \cdot y(1) - (R_e(M) + R_t(M)) \cdot y(M)$$

Now, the charge density y at time step number $k+1$ is denoted by y_{k+1} , Similarly y_k is the value at time step k . The implicit first order equation is based on the Eq. (3.10),

$$\mathbf{y}_k = \mathbf{y}_{k+1} - \mathbf{f}_{k+1} \Delta t \quad (3.10)$$

where \mathbf{f}_{k+1} , denoting $\mathbf{f}(\mathbf{y}_{k+1}(n))$, the derivative function vector at the end of the time step, is unknown, but can be found by iteration. By performing a Taylor's expansion of \mathbf{f}_{k+1} , and substituting in Eq. (3.11), the iteration scheme is set up, giving for the (s+1) iterate on the (k+1) step,

$$(\mathbf{I} - \Delta t \cdot \mathbf{J}_{k+1}^s) \Delta \mathbf{y} = \Delta t \cdot \mathbf{f}_{k+1}^s - \mathbf{y}_{k+1}^s + \mathbf{y}_k \quad (3.11)$$

where



$$\Delta \mathbf{y} = \mathbf{y}_{k+1}^s - \mathbf{y}_{k+1}^s, \quad (3.12)$$

\mathbf{I} is the $(M+1) \times (M+1)$ identity matrix and \mathbf{J} is the $(M+1) \times (M+1)$ Jacobian matrix of partial derivatives with elements:

$$J_{ij}^s = \left. \frac{\partial f_i}{\partial y_j} \right|_{k+1}^s \quad (3.13)$$

The iteration proceeds by solving for $\Delta \mathbf{y}$ and updating \mathbf{y}_{k+1}^s to \mathbf{y}_{k+1}^{s+1} using

Eq.(3.12), (and hence updating f_{k+1}^s and J_{k+1}^s) repeatedly until the computed ‘correction’ Δy , is judged to be sufficiently small as the solution converges on the (k+1) time-step value, y_{k+1} .


It is useful to consider the structure of the Jacobian matrix in detail, since an effortless simulation and acceptable computer memory is allowed. Fig. 3.3 illustrates the matrix structure. J_{11} is the summation of conduction electrons loss, J_{1n} is the top row of matrix, J_{n1} is electron trapping for each mesh and J_{nn} is the diagonal term; others are zero. These zero terms mean that the communication between each localized state does not occur.

3.3 Simulation Flowchart

Fig 3.4 shows the flowchart of a simple implicit as well as Newton iteration program suited for the simulation for discharging process. At the outset, the data of the device structure condition, including the discretized mesh size, ONO stack thickness, threshold voltage window, and gate voltage bias, are read. Then, concentration of each trap state at the previous time is loaded, and then the data at next time is evaluated numerically. The output data are judged whether the self-consistent is achieved. If out of the accuracy, the iteration process will continue by decreasing the time step size until the stable results are received.

$$\begin{bmatrix} \sum_2^{Yn} R_d(N_t - y(n)_{k+1}^s) \mathbf{J}_{11} & R_d \cdot y(1)_{k+1}^s + R_e(2) \mathbf{J}_{12} & \dots & \dots & R_d \cdot y(1)_{k+1}^s + R_e(Yn) \mathbf{J}_{1Yn} \\ T_N & T_N & & & T_N \\ R_d(N_t - y(2)_{k+1}^s) \mathbf{J}_{21} & -R_d \cdot y(1)_{k+1}^s - R_e(2) - R_t(2) & 0 & 0 & 0 \\ R_d(N_t - y(3)_{k+1}^s) \mathbf{J}_{31} & 0 & \ddots & 0 & 0 \\ \vdots & 0 & 0 & \ddots & 0 \\ R_d(N_t - y(Yn)_{k+1}^s) \mathbf{J}_{Yn,1} & 0 & 0 & 0 & -R_d \cdot y(1)_{k+1}^s - R_e(Yn) - R_t(Yn) \mathbf{J}_{Yn,Yn} \end{bmatrix}$$

Fig.3.3(a). The Jacobian matrix structure



$$\begin{aligned} \text{a. } J_{11} &= - \frac{\sum_2^{Yn} R_d(N_t - y(n)_{k+1}^s)}{T_N} dx - R_{\text{loss}} \\ \text{b. } J_{1n} &= \frac{R_d \cdot y(1)_{k+1}^s + R_e(n)}{T_N} dx \\ \text{c. } J_{n1} &= R_d(N_t - y(n)_{k+1}^s) \\ \text{d. } J_{nn} &= -R_d \cdot y(1)_{k+1}^s - R_e(n) - R_t(n) \end{aligned}$$

Fig.3.3(b). Each element of Jacobian matrix. J_{11} is the summation of conduction electrons loss, J_{1n} is the top row of matrix, J_{n1} is electron trapping for each mesh and J_{nn} is the diagonal term

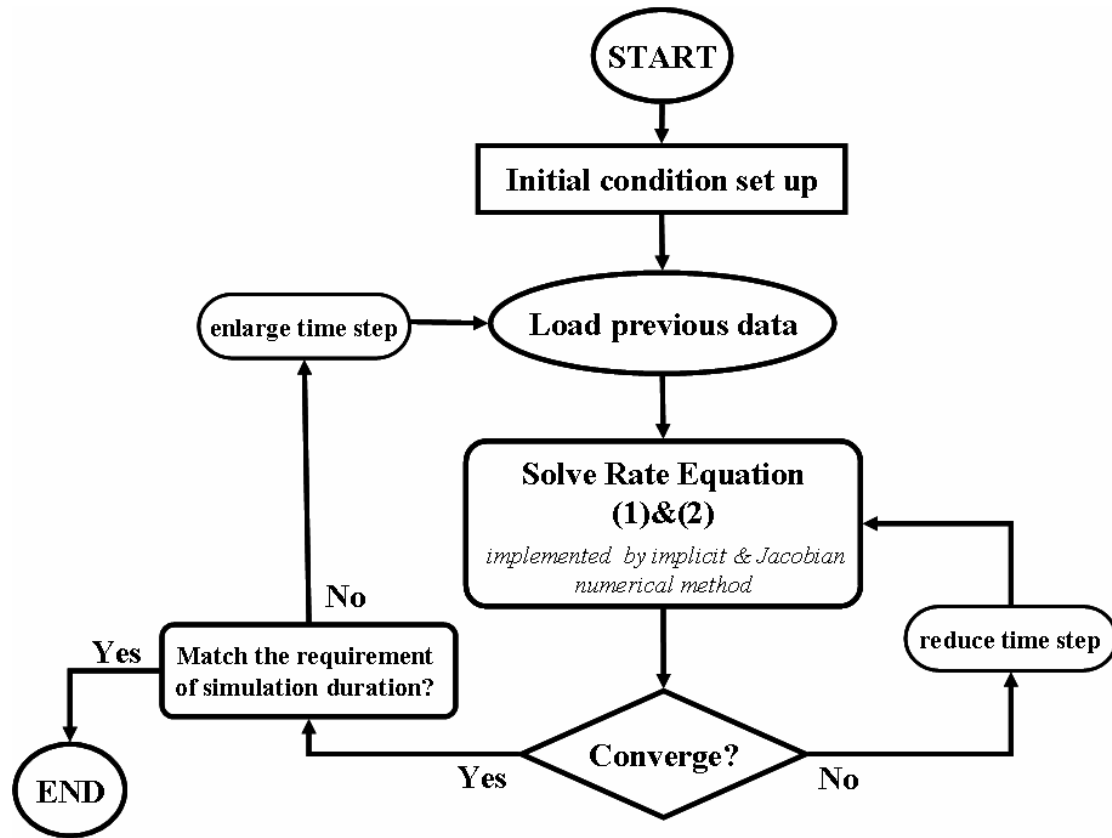


Fig.3.4. The flowchart of our simulation.

Chapter 4

Simulation Result of the Retention Behavior in SONOS Memory

4.1 Introduction

In this chapter, we will demonstrate the simulation results by utilizing the numerical analysis. First, the device structure is shown and the simulation parameters are examined. Then, the simulated and experimental results are compared and discussed. Finally, the conclusions are drawn.

4.2 Device structure and Parameter verification

4.2.1 SONOS structure

The samples used in this work are n-channel SONOS-type cells. The thickness of each ONO gate stack is 9nm (top oxide, T_{TO}), 6nm (nitride, T_N) and a variable bottom thickness, 3nm and 5nm (T_{BOT}). Devices have a gate length of 500 μ m and a gate width of 500 μ m. A uniform positive and negative bias is employed for writing and erase, individually.

4.2.2 Calibration of the simulation parameter

To ascertain whether the entire simulations are workable, the parameters listed in Table 2.1 should be calibrated. First, the bottom oxide thickness of 1.1nm and 1.8nm are utilized. The two data are consistent with Marvin White's experimental data, as shown in Fig. 4.1. In addition, the simulated data for 3nm thickness is also similar with our measurement data (Fig. 4.2). All results are gauged at 22°C and the threshold voltage window (ΔV_t) is 1.5V. When cells are operated at high temperature (225°C), the decay rate is enhanced and our simulation data can also reflect this phenomenon (Fig. 4.8). We can conclude that the parameters used in our model are reasonable because good agreements can be obtained between simulation

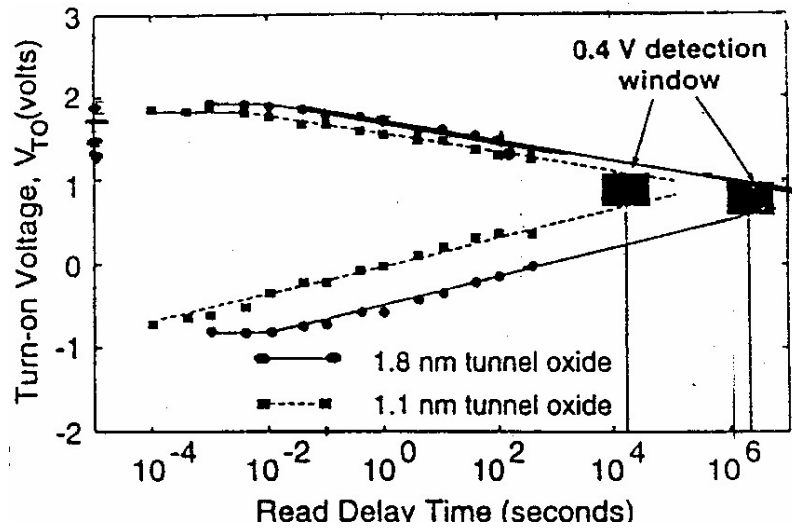


Fig.4.1(a). The retention loss of SONOS for 1.8 nm and 1.1 nm bottom oxide at room temperature in Marvin White's experiment. [31]

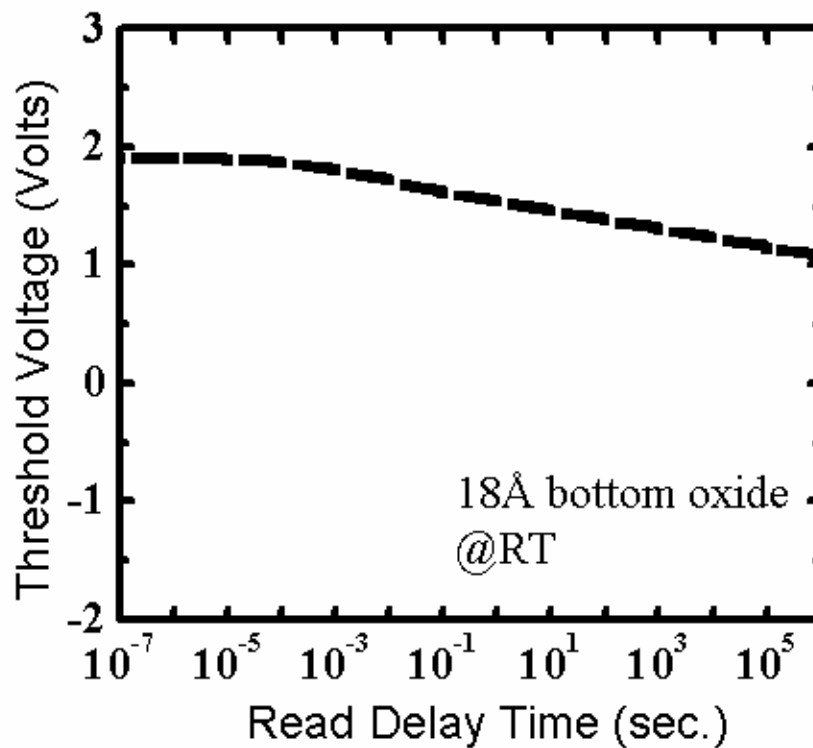


Fig.4.1(b). The retention loss of SONOS for 1.8 nm bottom oxide at room temperature in this experiment.

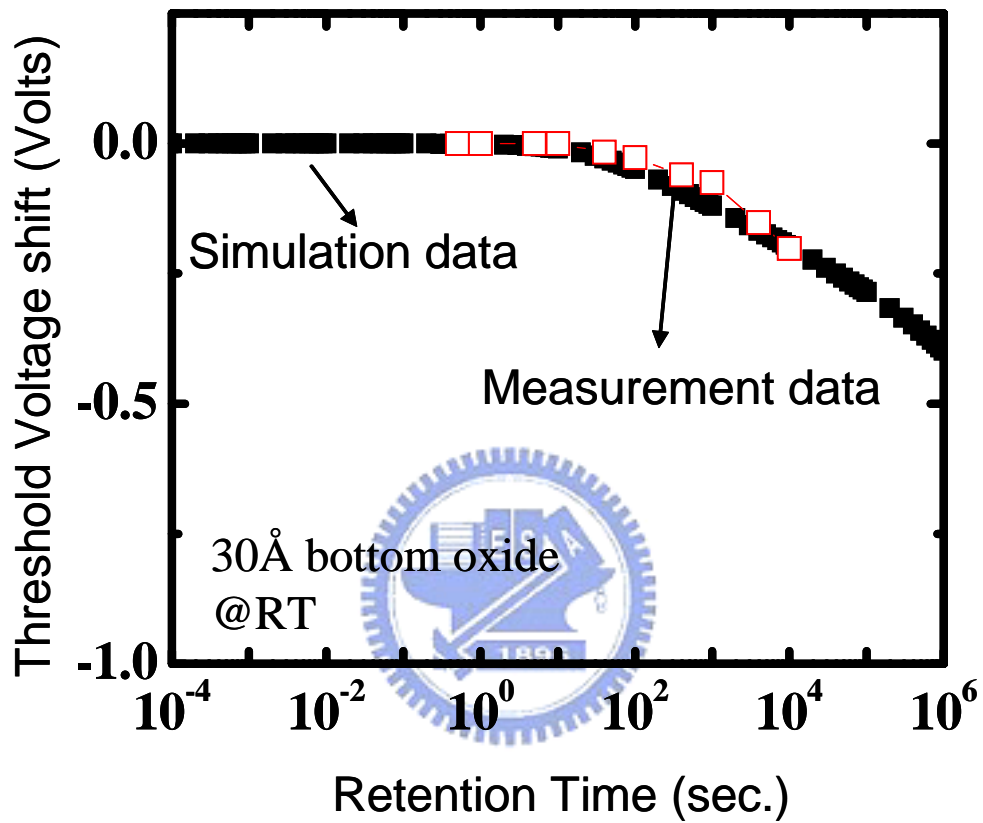


Fig.4.2. The retention loss of SONOS with simulation and measurement for 3 nm bottom oxide at room temperature. The simulated data for 3nm thickness is also similar with our measurement data.

and measurement results. The detail information will be discussed below.

4.3 Results and Discussion

4.3.1 Oxide thickness dependence on gate leakage current

It is known that thinner bottom oxide has better endurance, while it has poor data retention. Fig. 4.3 shows that as the bottom oxide thickness increases, the initial gate leakage current decreases and the corner time increases. The lower leakage current corresponds to a better charge loss due to a little tunneling transparency through a thicker bottom oxide (Fig. 4.4). Therefore, thickening the bottom oxide is a great solution to improve the data retention.

The leakage component combined with thermionic field emission and nitride trap direct tunneling is mentioned in Chapter 2. It is doubtful whether either or both parts control the charge loss simultaneously. In Fig. 4.5, the currents caused by PF emission and direct tunneling are displayed. In the beginning, the electrons excited from the shallow nitride traps dominate the leakage. After a period of time, shallow trapped charges are swept out and this will makes the direct tunneling current start to govern the gate current (Fig. 4.6). As for a thick oxide cell, the current transport in a SONOS cell is due mainly to the PF excitation current as opposed to the direct tunneling current in a thin oxide cell. The measurement is at 1sec and the ratio of the each element to total leakage is investigated as a function of bottom oxide thickness (Fig. 4.7)

4.3.2 Temperature dependence on the charge decay rate

In addition to the room temperature (22°C), the memory cells are often situated at different temperature range. According to our model, the gate currents at each temperature are simulated. Fig 4.8 shows the results between simulation and measurement, respectively. It is exhibited that the charge loss at high temperature is accelerated compared with that at a lower temperature. This high temperature will enhance the trapped charge emission rate, thereby degrading the retention behavior.

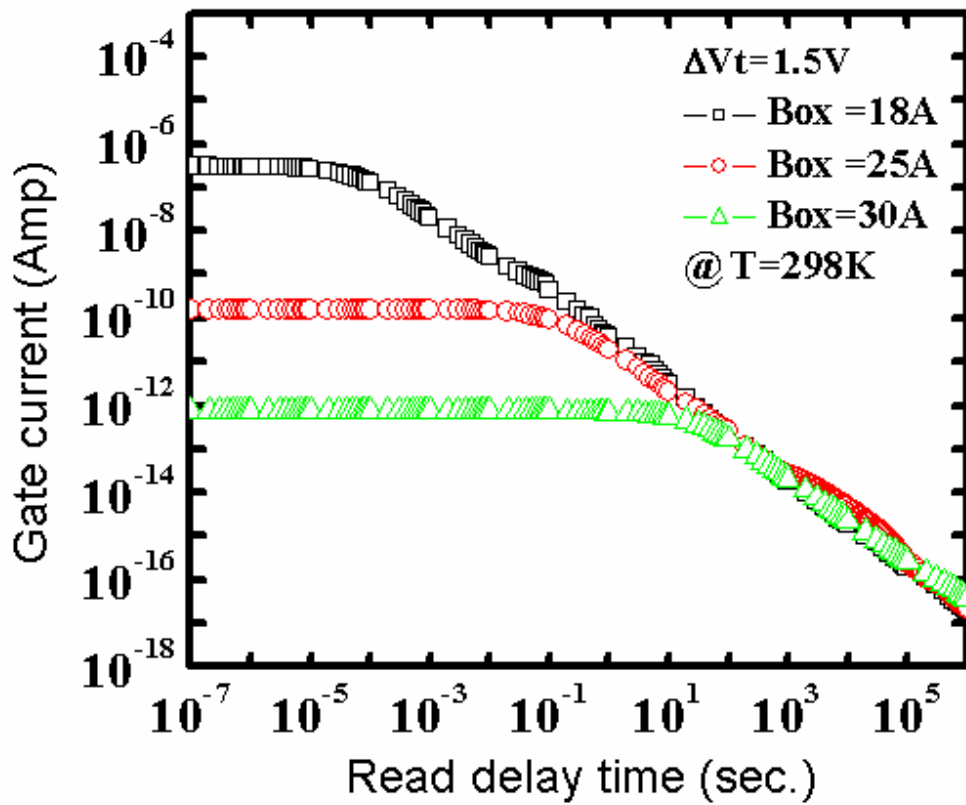


Fig.4.3. The gate current v.s. read delay time of SONOS for 3 nm, 2.5 nm and 1.8 nm bottom oxide at 298 K, respectively. While the bottom oxide thickness increases, the initial gate leakage current decreases and the corner time increases.

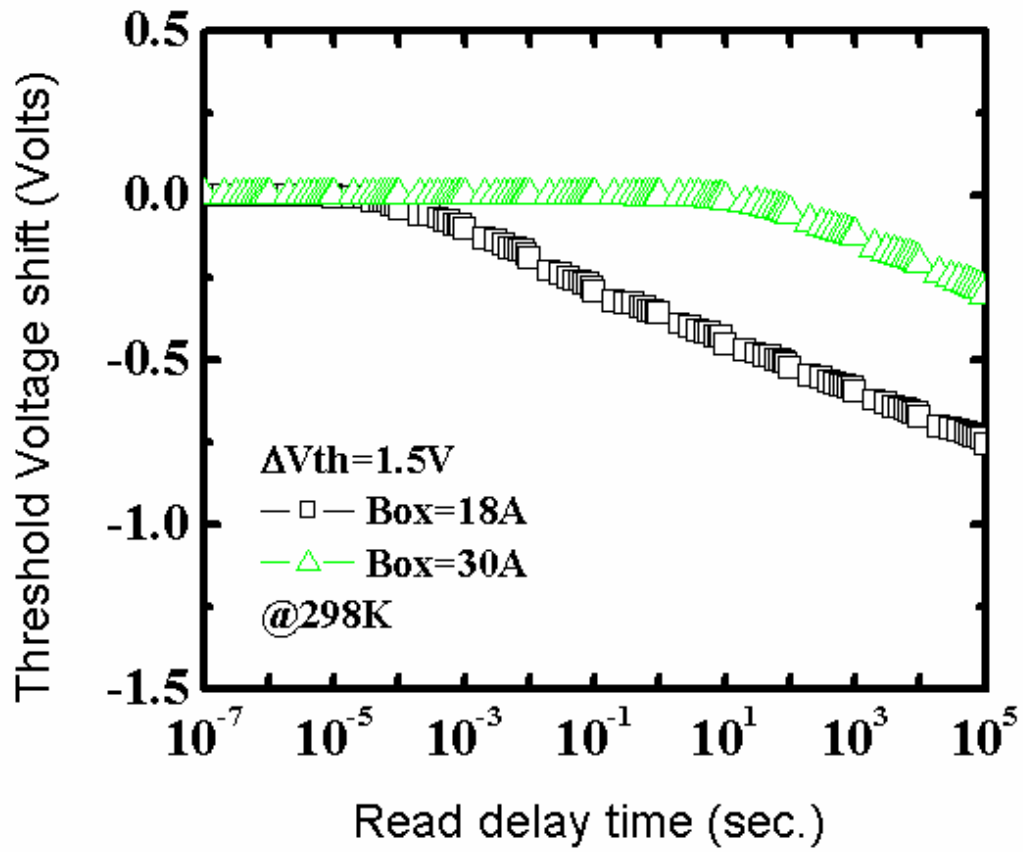


Fig.4.4. The threshold voltage shift (ΔV_{th}) v.s. read delay time of SONOS for 3 nm and 1.8 nm bottom oxide at 298 K.

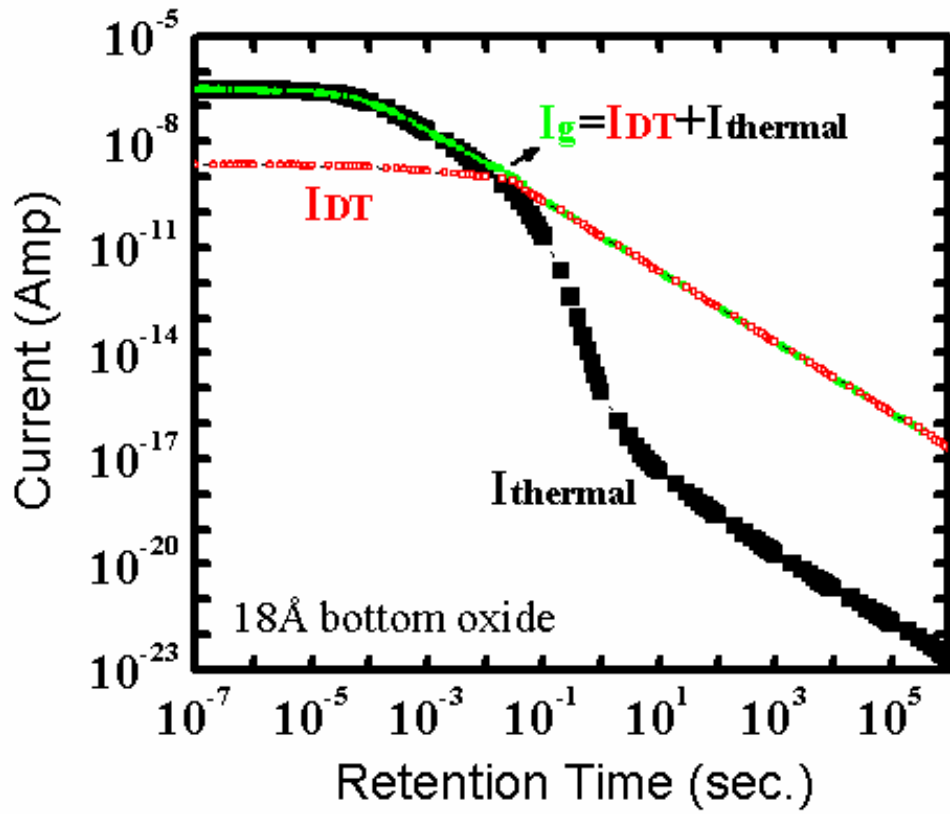


Fig.4.5. The currents caused by PF emission and direct tunneling are shown here. The gate current is equal to the combination by I_{DT} and $I_{thermal}$.

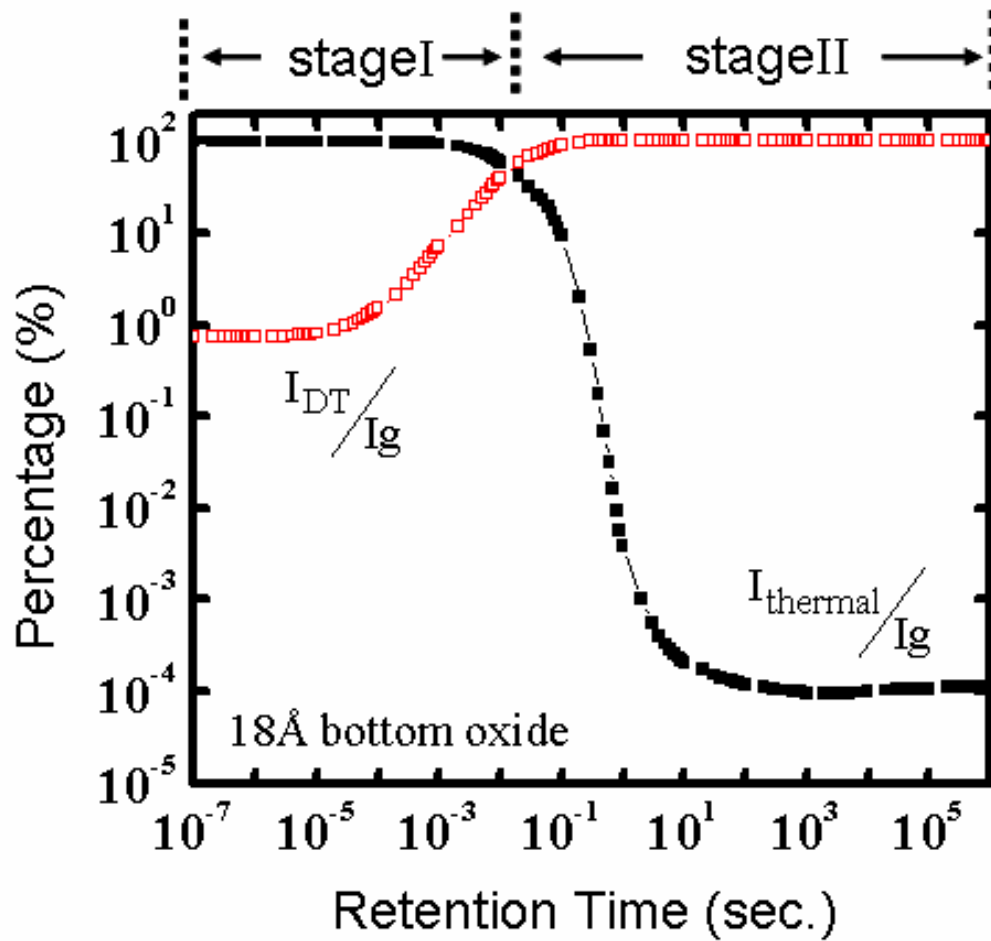


Fig.4.6. The mechanism of gate current was shown in this figure. In the beginning, the electrons excited from the shallow nitride traps dominate the leakage. After a period of time, direct tunneling current start to govern the gate current

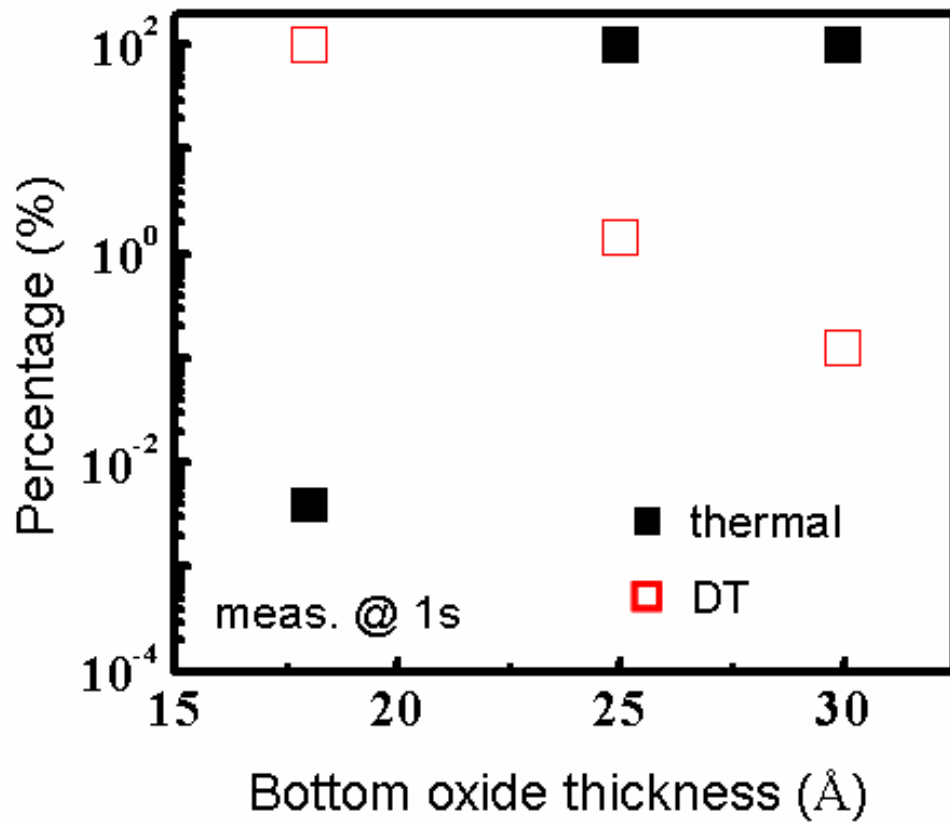


Fig.4.7. The percentage of the thermal and DT current was simulated at 1sec. The ratio of the each element to total leakage is investigated as a function of bottom oxide thickness

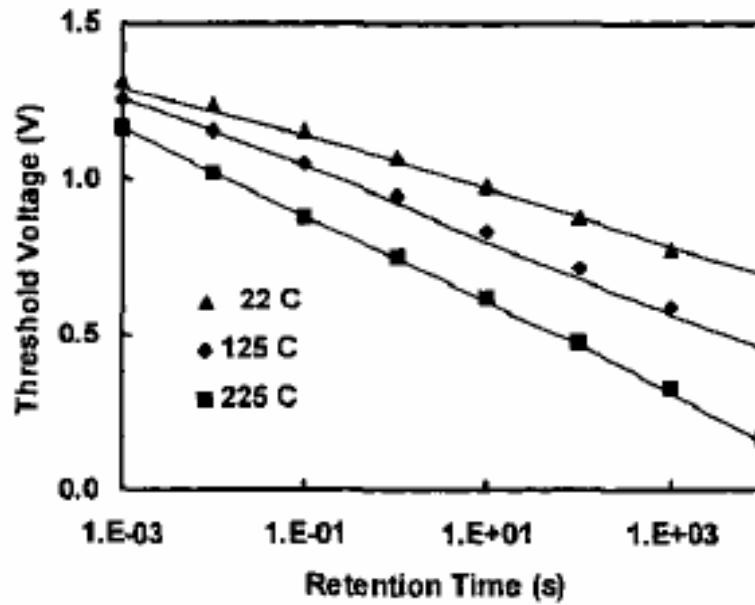


Fig.4.8(a). The measured and simulated retention characteristics of SONOS at various temperature in Marvin White's experiment. [32]

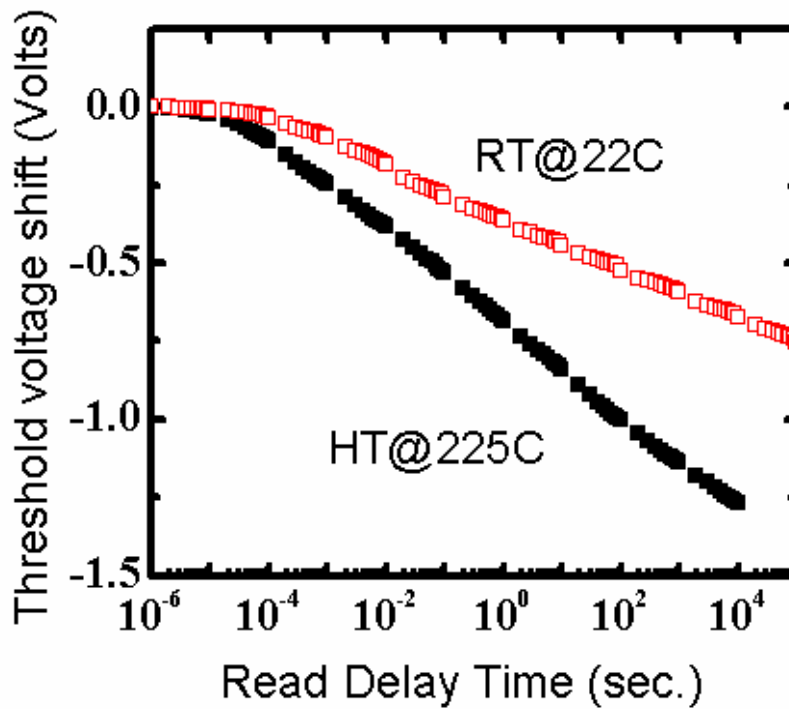


Fig.4.8(b). The simulated retention characteristics of SONOS at distinct temperature in this experiment.

The threshold voltage decay rates between 22°C and 225°C are 91mV/dec and 143mV/dec, separately. The two observations consist with our simulation results, 88mV/dec at room temperature and 140mV/dec at high temperature.

4.3.3 Nitride trapped charges distribution

The threshold voltage window decreases with the time revolution. This implies that the residual carriers within SiN film also reduce at the same time. To explore the trapped charges distribution between energy and space dimensions, each trap state concentrations at 10^{-6} , 10^{-1} and 10^4 seconds for two different temperatures are extracted through simulation process. Fig. 4.9 shows the remaining charge densities at the corresponding energy depth. As the discharge continues, electrons in shallow traps are eliminated earlier than those in deep traps. At a high temperature environment (225°C), more charges are excited due to a higher emission rate coefficient. The “empty-filled” boundary of charge concentration moves deeper compared with that at a lower temperature (22°C). In the spatial direction from bottom oxide/SiN interface toward the gate, the concentrations at different energies under room temperature are demonstrated. As expected, the lower storage density around the interface indicates that the charges near the bottom oxide tunnel out easier than those far away from the interface. Fig. 4.10 shows the result.

4.3.4 Stress effect

The aforementioned discussions are only focused on the cells without any stress. In reality, the memory cell always suffers the high electric field, i.e. P/E cycling stress. Here, the capacitor with 5nm bottom oxide thickness is employed. In this regard, the direct tunneling current can be ignored because of the sufficiently small tunneling probability. The major leakage component arises from the trap-assisted tunneling (TAT) current. The traps are neutral and increases with stress condition. At zero gate stress bias ($V_g=0V$), the simulation data for various oxide trap densities are shown in Fig. 4.11, and the threshold voltage shift is shown in Fig. 4.12. In the initial stage, the limitation of discharging process is the neutral trap density. This will fix the gate

current level at a certain level. After the corner time, the gate current turns to obey a $1/t$ time dependence. This is because that the leakage current is limited by the FP excitation and the analytical description is derived at [12].



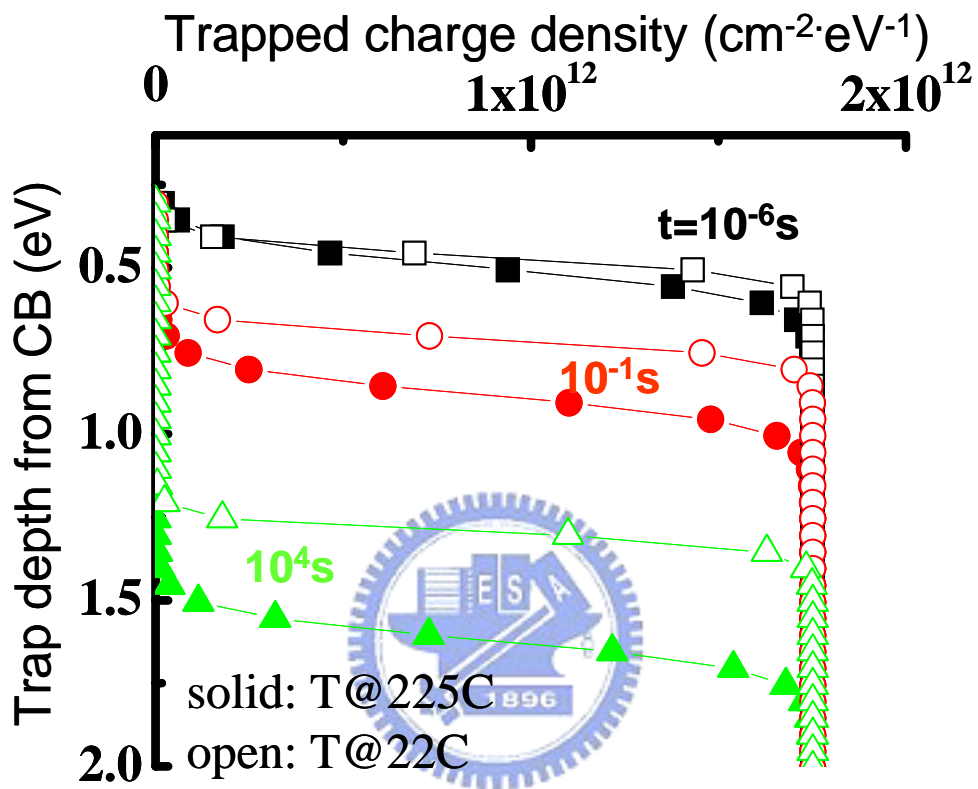


Fig.4.9. The relationship between trap depth and charge density. As the discharge continues, electrons in shallow traps are eliminated earlier than those in deep traps.

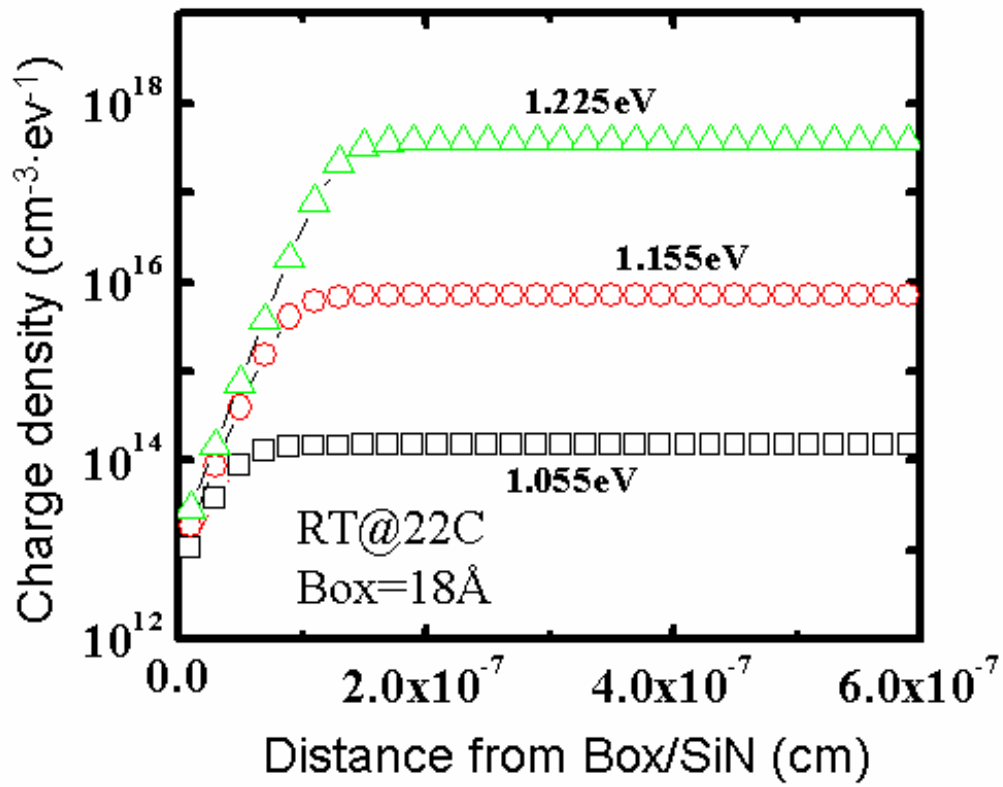


Fig.4.10. The characteristics of charge density distribution in different energy depth. The lower storage density around the interface indicates that the charges near the bottom oxide tunnel out easier than those far away from the interface.

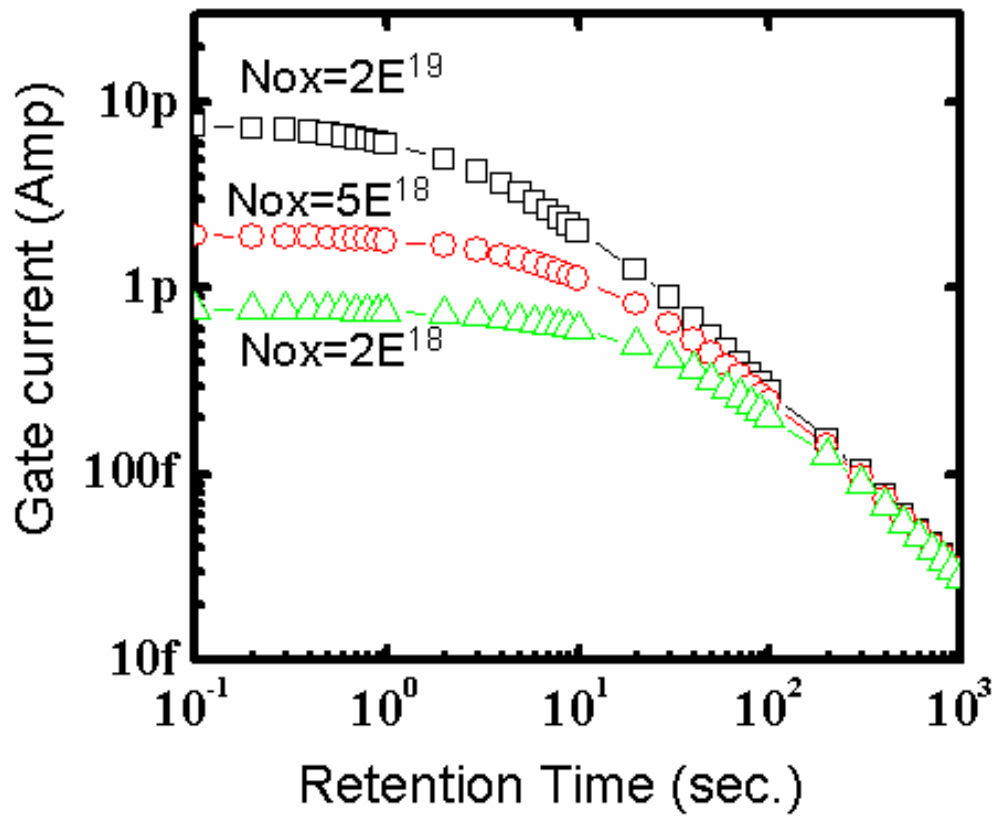


Fig.4.11. The simulation data for various oxide trap densities at zero gate stress bias ($V_g=0V$).

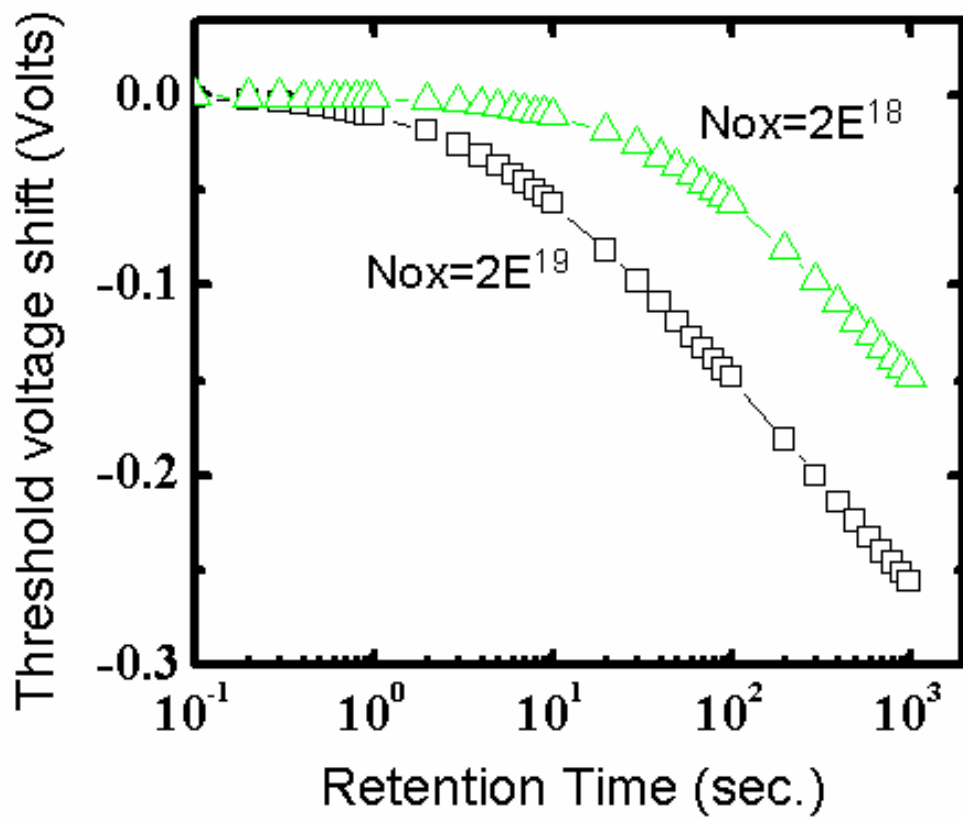


Fig.4.12. The threshold voltage shift by simulation for various oxide trap densities at zero gate stress bias ($V_g=0V$).

Chapter 5

Summary and Conclusion

The charge transient behavior in a SONOS type flash memory has been characterized. By a multiple trapping model and two sets cross-coupled SRH rate equations, the charge loss path and the associated components are identified successfully. The Frenkel-Poole emission as well as free carriers retrapping depicts the conduction inside SiN film. And the leakage current is attributed to the loss from the nitride conduction band and trap states.

Anticipating the use of numerical analysis, the discretized meshes are required. Utilizing a backward Euler implicit method with Newton's iteration, the non-linear, stiff equations are solved numerically. This method can enable us to obtain the information at each moment.

As the bottom oxide thickness increases, the leakage current is limited for a long time. This phenomenon is referred to "current blocking effect". The blocking corner time decreases after the cells suffer high field stress. This corner time can be treated as an index of bottom oxide quality. The shorter corner time corresponds to the poorer oxide quality. In addition, at a high temperature environment, the voltage decay will be enhanced due to thermionic field emission. According to simulated trapped charge distribution, the "empty-filled" boundary moves deeper with increasing temperature. It implies that more deep trapped carriers are excited and then accelerating the charge loss.

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碩士論文題目:



氮化矽記憶體資料保存行為之數值分析模擬

Numerical analysis of the retention behavior in nitride
storage flash memory