Chapter 1

Introduction

1.1 Background

1.1.1 Copper Interconnect in IC manufacture

Continuous scaling down of the transistor feature size of Si based integrated circuit is driven by faster circuit speed, chip functionality, and higher packing density [1][2]. Interconnect scaling improves interconnect density. However, this shrink strategy results in interconnect RC time delay which limits circuit performance and tends to curtail the benefits of transistor feature size scaling-down, as shown in Figure.1-1 [3][4]. The interconnect RC delay is the product of the resistance (R) of the metal line and the capacitance (C) of the interlevel dielectric (ILD) and could be expressed as:

$$RC = \rho\varepsilon\frac{l^2}{td} \quad \text{(Eq.1-1)}$$

where ρ is the resistivity of the metal, ε is the permittivity of the insulator, l and d are length and thickness of the metal line, and t is the thickness of the insulator. The dependence of ρ, ε and l in Eq.1-1 shows that RC can be reduced by choosing metals with low resistivity, insulators with low dielectric constant and/or making line lengths as short as possible. At the same time, current density increases as line cross-sectional area is reduced, leading to a degradation of electromigration endurance. Table.1-1 gave the comparison of properties of several possible interconnect metals. Owing to copper (Cu) has lower electrical resistivity (1.67μΩ-cm), better electromigration resistance [5-7] and higher melting point (1085°C) compared to Al-based alloys. Therefore, copper has been used as the interconnect material in the fabrication of advanced ultra-large scale integration circuits. However, on the application of Cu interconnect fabrication, conventional dry etching technique is difficult due to the process by-products are not volatile at the process temperature.

In order to avoid the problem in Cu etching, IBM developed a new patterning process for

Cu interconnects called a damascene process, as shown in Figure.1-2. The pattern for interconnects is first etched into the ILD. Following diffusion barrier metal (Ta) and Cu are deposited over the whole surface of the patterned wafer. Finally, Cu chemical mechanical planarization (CMP) process employs a two step polishing process.

Generally, Cu patterned polishing consists of two steps, the first step is globe planarization of protruded Cu film and the second step is to remove diffusion barrier. In first step Cu patterned polishing, the bulk of Cu is removed using acidic-pH alumina or silica slurry, and typically stops on the underlying tantalum (Ta) diffusion barrier. Since Ta has quite different hardness as well as chemical properties compared to Cu, it is necessary to switch to different polishing slurry as a second step.

Kaufman et al. [8] proposed the mechanism explaining the planarization of tungsten (W) CMP (Figure.1-3) and discussed the removal of W in terms of competition between an etching reaction that dissolves is WO_4^{-2} and a passivation reaction that oxidizes W to WO_3 on the surface which is removed by a mechanical abrasion in the slurry. This mechanism has also been applied to explain Cu CMP [9]. Complex interactions between the polishing slurry, the pad, and the wafer surface are responsible for the material removal and planarization. Figure.1-4 illustrates most of the factors that need to be considered in a CMP process.

1.1.2 Post-Cu CMP Cleaning

Cu CMP process has been used in semiconductor fabrication. However, there are several challenges remain must be overcome. For example, non-uniformity, dishing [10], erosion, scratch [11], corrosion [12-14], post-Cu CMP cleaning, etc. In the thesis, the main topic of our study is post Cu CMP cleaning. CMP is an inherently dirty process. After the process, wafer surface leaves a large amount of contaminations on the surface, which must be eliminated. There are two major contaminations. One is the abrasive from the polishing slurry, and the other is the metallic impurity contamination on the wafer surface. There

contaminations must be removed before further processing or they will cause lower yields. For example, particles deposited on the wafer surface can cause local roughness that will block the subsequent photolithography. Particles can also lead to pinholes in a subsequently deposited film. Metallic contamination in the dielectric regions or on the silicon substrate backside can easily diffuse to the gate level, where it can affect the minority carrier lifetime and cause device failure. Therefore, the availability of a post Cu CMP cleaning process that effectively removes contamination from all regions of the wafer (front, back, and edge), leaving a clean surface for the subsequent process steps, is critical to the adoption of copper technology [15][16].

1.1.2.1 Particle Contamination Cleaning

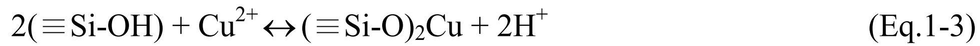
During the CMP process, copper is oxidized to form cupric/cupreous oxides (CuO or Cu_2O) and copper hydroxides ($Cu(OH)_2$) passivation on copper surface [17]. As polishing with colloidal silica based slurry, it shows the strong absorption of colloidal silica on copper surface. This maybe related to that the colloidal silica chemisorbed onto the copper oxide layer by means of oxygen bonding, as shown in (Figure.1-5) [18]. The lifting force for particles varies for different types of post CMP cleaning methods (Table.1-2) [19]. Brush scrubbing is one of the oldest and effective methods for removing particles from wafers. The mechanical force component of the material removal force is provided by the brush bristles. It is made of polyvinyl alcohol (PVA) material, the texture of which is soft when wet. The cleaning solution is typically deionized (DI) water with dilute additives that act to maximize the electrostatic repulsion between dislodged particles and the wafer surface or to mildly etch the wafer surface. Megasonic cleaning depends on acoustic streaming and the reduction of the boundary layer thickness on substrates. It has been shown to be effective in post CMP cleaning, particularly at low power, long cleaning time and high temperature. Chemicals with beneficial properties are often introduced to the cleaning process to increase the electrostatic

repulsion forces between the substrate and the contaminant deterring readhesion. Chemical cleaning is very significant in post CMP cleaning process. The liquid flow (e.g., spray and overflow) and spinning of wafers bring about a pressure gradient and exert lifting force on particles. It has the advantage of low cost of ownership and high throughput as several wafers can be cleaned simultaneously in batches, unlike brush scrubbing mechanism. In practice, buffing is commonly carrier out to remove particles [20][21]. Wafer is buffed with a HNO_3/BTA aqueous (no abrasive). HNO_3 is could dissolve copper oxide passivation on copper surface, and Cu^+ ions would be coordinated with 1H-benzotriazole (1H-BTA, $C_6H_4N_3H$) to form a mono-layer of Cu(I)-BTA on the surface to prevent the copper oxide formation [22].

1.1.2.2 Metallic Contamination Cleaning

The other problem of post Cu CMP cleaning is metallic contamination. The ITRS road map [23] suggests for 90nm technologies that critical metals have to be reduced to below 10^{10} atom/cm^2. Figure.1-6 shows the Pourbaix diagram of Cu-H_2O system [24]. It indicates that in acidic solutions with pH<5, copper oxide do not form and copper dissolves Cu^{2+} at high potentials and is immune from oxidation at low potentials. In highly alkaline solutions with pH<13, it would form CuO_2^{2-} at high potentials. For pH ranging from 7 to 13, Cu_2O formation is likely at low potentials. CuO forms on copper at higher potentials. Therefore, copper is corroded in acidic and alkaline solutions easily. In general, the CMP slurry chemistry is usually designed such that the metallic materials removed from the metal film can be dissolved. Therefore, the metallic contamination on oxide surfaces can be due to both the adsorption of dissolved metal species and the precipitation of insoluble metal compounds on the solid wafer surface. The mechanism for this copper ion-oxide surface interaction can be interpreted by using the following reactions [25]:

$$\equiv \text{Si-OH} + Cu^{2+} \leftrightarrow \equiv \text{Si-OCu}^{+} + H^{+} \quad \text{(Eq.1-2)}$$



$$2(\equiv\text{Si-OH}) + Cu^{2+} \leftrightarrow (\equiv\text{Si-O})_2Cu + 2H^{+} \qquad \text{(Eq.1-3)}$$

Metal chelators are commonly carrier out to remove Cu contamination. Because Metal chelators have one or several dentates, they would react as electron-pair acceptors to form coordination compounds or complex ions with metal ions [26][27]. However, in addition to contamination removal, corrosion control is one of important challenges for post CMP cleaning.

1.2 Motivation

Citric acid is one of the organic acids commonly used as metal chelators to remove Cu contamination in post Cu CMP cleaning. However, acetic acid also is one of metal chelators. It has never been studied so far in post Cu CMP cleaning. Therefore, we would compare their cleaning efficiency in this thesis. Furthermore, in the thesis of Kuo-Chin Hsueh [21], the post Cu CMP cleaning process involves buffing process with diluted nitric acid (HNO_3) and 1H-benzotriazole (1H-BTA, $C_6H_4N_3H$) aqueous solution for copper surface passivation and colloidal silica removal. The buffing process could effectively remove the colloidal silica abrasives and formation Cu(I)-BTA passivation on copper surface that could surely prevent copper surface be corroded and reduce surface leakage current [21]. However, Cu(I)-BTA passivation would be decomposed above 150°C. It would cause electrical property degradation. In the steel manufacturing region, they usually use Dinonylnaphthalene sulfonic acid (DNNS) and 2-Phosphonobutane-1,2,4-tricarboxlic acid (PBTC) based solution to act as prevent-rust, and they is very effectual. Therefore, we would try to use them to act as corrosion inhibitor in post CMP cleaning process. In this study, we would choose amine salt of Dinonylnaphthalene sulfonic acid and 2-Phosphonobutane-1,2,4-tricarboxlic acid tetrasodium salt (PBTC-Na_4). Their chemical structure is shown in Figure.1-7. They are water soluble corrosion inhibitors that can be used in aqueous systems and leave extremely thin hydrophobic films to protect copper.

1.3 Thesis Outline

In this investigation, novel cleaning methods are developed for post CMP cleaning in the copper damascene process. The post CMP cleaning process involves buffing process with HNO_3/DNNS or HNO_3/PBTC-Na_4 solution for copper surface passivation and colloidal silica abrasives removal. We studied the effect of novel passviation layers on electrical properties of Cu interconnect and compared with Cu(I)-BTA passivation. In addition to the removal of colloidal silica abrasives, copper contamination in the ILD surface is removed with metal chelators.

In Chapter 2, the mechanisms of the contaminations formation and removal would be described.

In Chapter 3, the cleaning efficiency and corrosion effect of metal chelators would be compared. The influences of cycle time, concentration and pH value are also studied. The wetting ability of metal chelators on oxide surface is investigated. The wetting ability of metal chelators is determined by the contact angle measurement.

In Chapter 4, we studied the effect of novel passviation layers on electrical properties of Cu interconnect and compared with Cu(I)-BTA passivation. Furthermore, the thermal stability and chemical durability of novel passivation layers would be investigated.

Finally, conclusions are given in Chapter 5.

Table.1-1 Properties of various metals.

	Al	Al alloy	**Cu**	W
Resistivity (μΩ•cm)	2.66	~ 3.5	1.67	5.65
Electromigration Resistance	Poor	Poor	Good	Very good
Corrosion Resistance	Good	Good	**Poor**	Good
Adhesion to SiO2	Good	Good	Poor	Poor
Si Deep Levels	No	No	**Yes**	No
CVD Processing	?	None	Available	Available
RIE etching	Available	Available	**No**	Available

Table.1-2 Major post CMP cleaning methods.

Method	Lifting forces
Chemical cleaning	liquid flow (e.g., spray of overflow), spinning of wafers
Megasonic	sonic wave and acoustic streaming, cavitation
Scrubbing	“wiping” with mechanical force

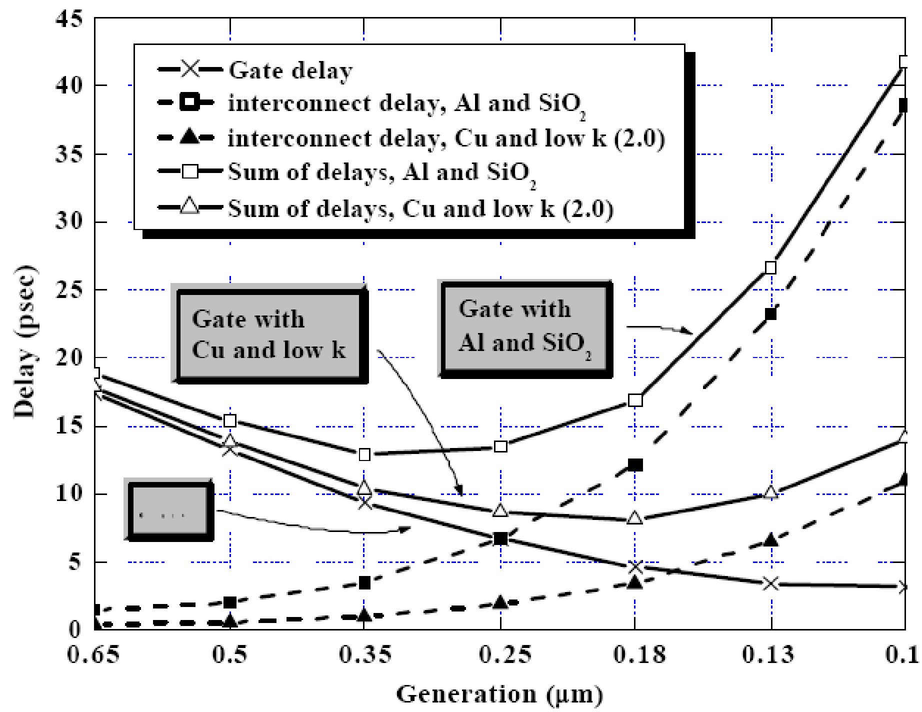


Figure.1-1 Comparison of intrinsic gate delay and interconnect delay (RC) as a function of the feature size.

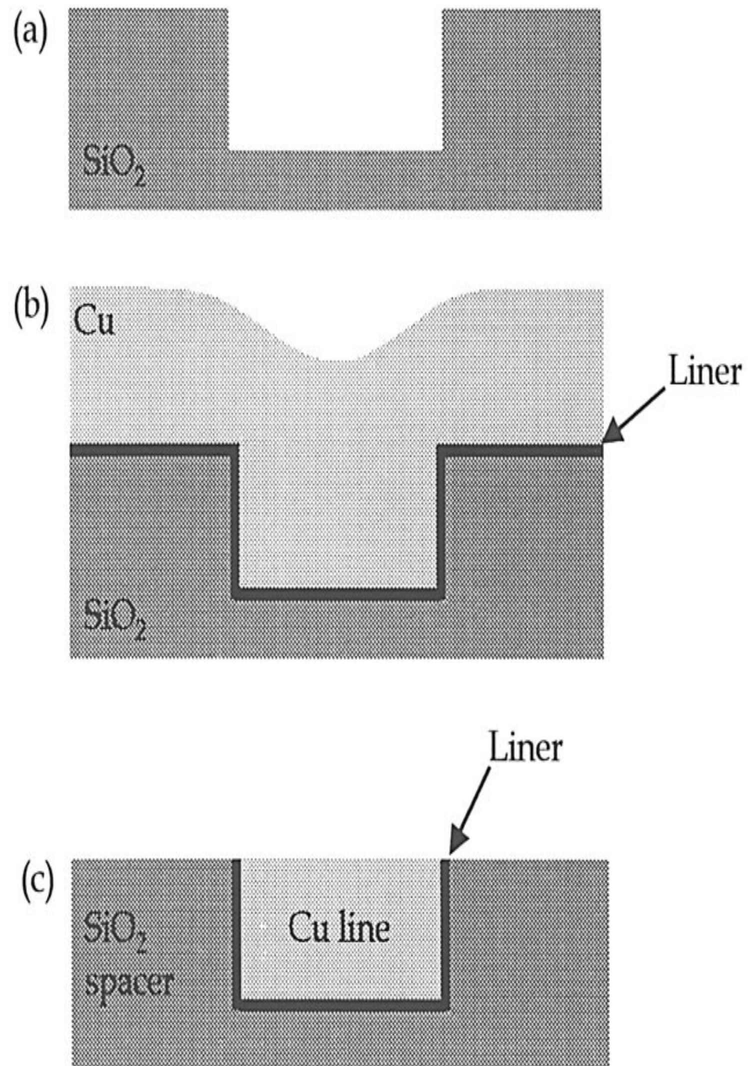


Figure.1-2 Cross-sectional view after the different process steps for the damascene technique.

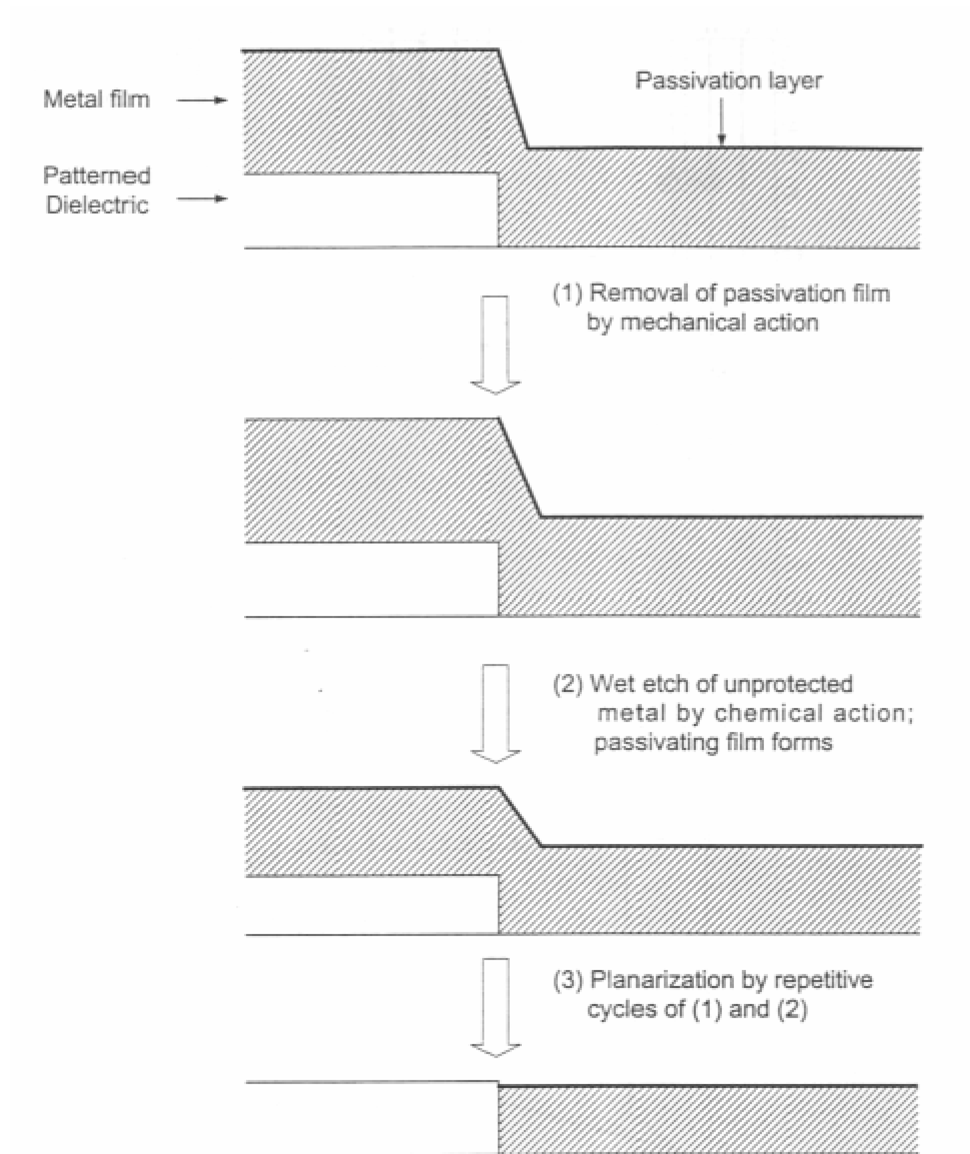


Figure.1-3 Proposed mechanism of planarization of patterned features by CMP

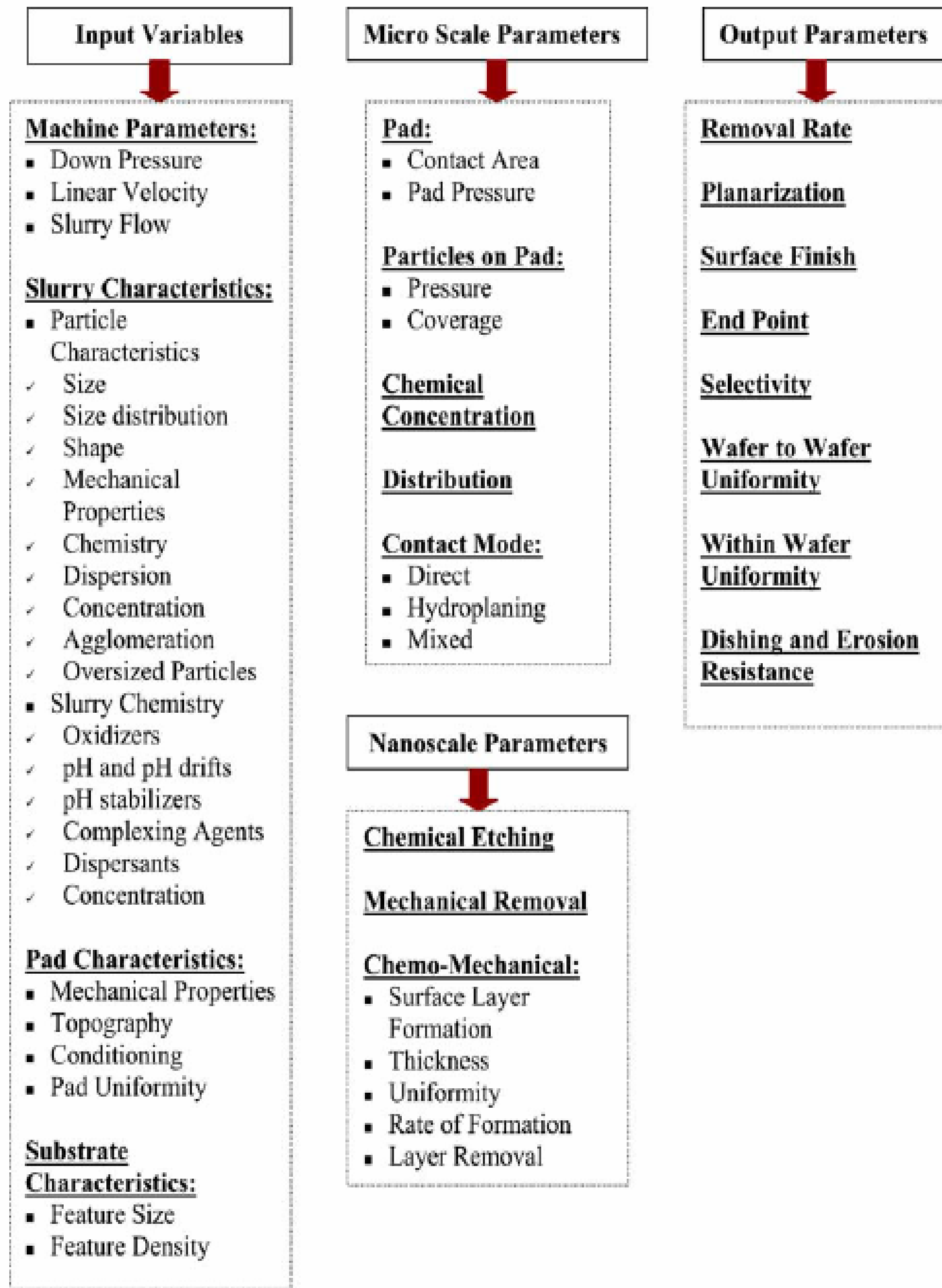


Figure.1-4 Interacting factors in a CMP process.

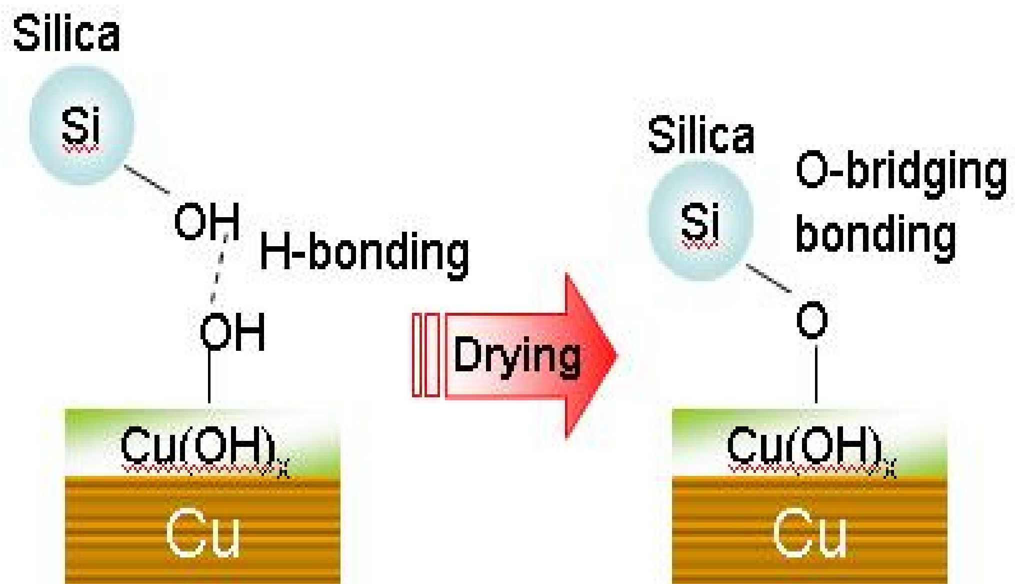
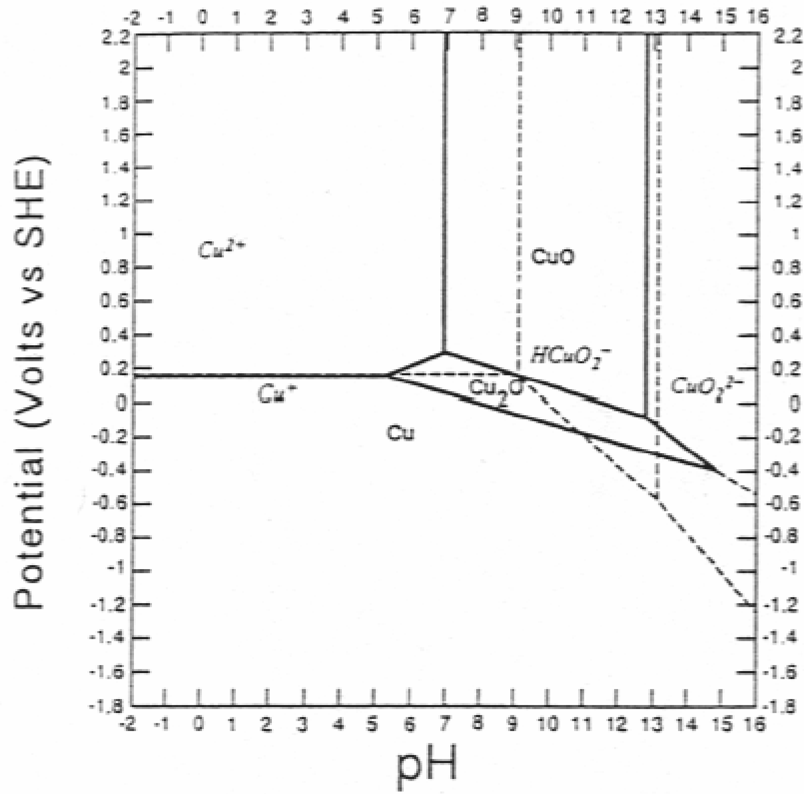
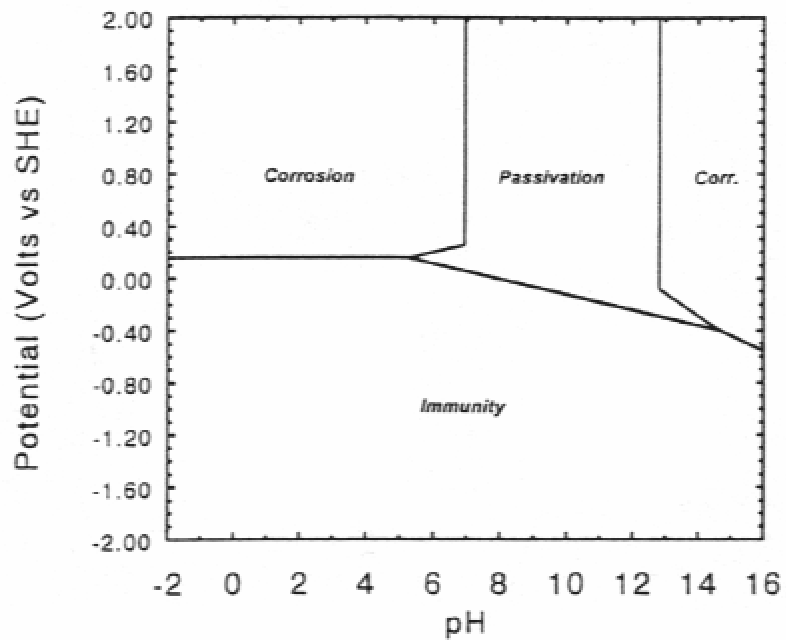


Figure.1-5 colloidal silica chemisorbed onto the copper oxide layer by means of oxygen bridging bonding.



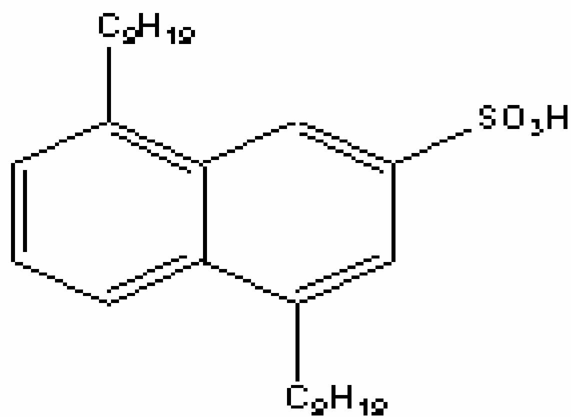
(a)

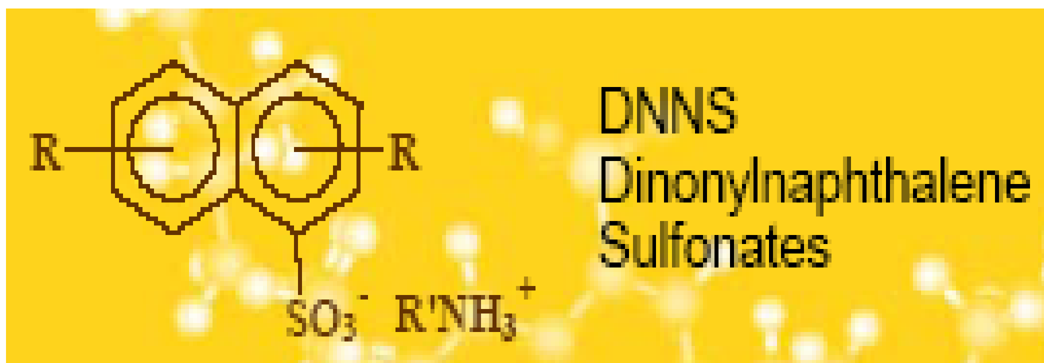


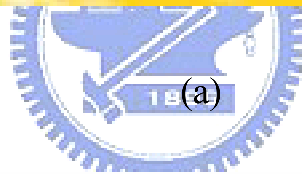
(b)

Figure.1-6 (a) Pourbaix diagram for the Cu-H_2O system

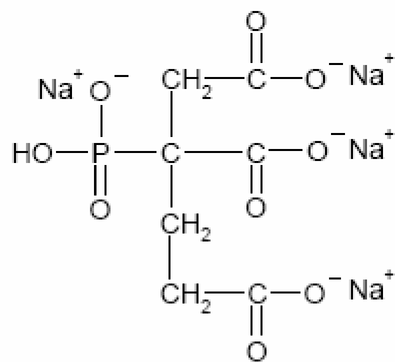
(b) Regions of corrosion, passivation, and immunity.







(a)



(b)

Figure.1-7 (a) Chemical structure of dinonylnaphthalenesulfonic acid (DNNS)
(b) Chemical structure of 2-Phosphonobutane-1,2,4 -tricarboxlic acid tetrasodium salt (PBTC-Na_4).