矽載具應用於射頻積體電路系統封裝之設計與製造

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摘　　要

此篇論文中，我們發展了一套利用低價的矽載具整合高品質因子的射頻微機電式電感器和低雜訊放大器(TSMC 0.18 製程)的系統封裝方案來實現一個擁有極寬頻(UWB)可調變的低雜訊放大器(3.1GHz~8GHz)。相較於目前的 CMOS 寬頻低雜訊放大器，由於新開發的低雜訊放大器使用擁有高品質因子和十字介電層的射頻微機電式電感器，因此擁有較寬的調頻範圍(UWB)與較低的雜訊(3.5dB)和電源消耗(10.5W)的優異特性。然而，我們為了整合矽載具和低雜訊放大器晶片，於是使用了一種最新的覆晶技術「金-金熱壓縮黏合技術」；這個新技術的優點是可免除在傳統製程中所產生的錫球及其所造成之寄生效應。此外，射頻微機電式電感器的等效模型也被推衍應用於 IC 設計上。經由統整已經發表的各種演算法，可精確地發展出一種適用於射頻微機電式電感器的等效電路模型。這些演算法包含 Greenhouse 方程式、physics-based closed-form

inductance expression 和分布式電容模型（DCM）。藉著這個模型的使用，電路設計者可以實現一個最佳化的系統封裝設計以應用於射頻積體電路領域。在這系統封裝的方案中，所有整合結構所佔用的面積幾乎等於在標準製程中所使用的面積。因此我們相信，在這片論文中所發展的矽載具和整合技術將能提供另一種替代的選擇，使積體電路設計者在未來發展出高效能的積體電路晶片。

Design and Fabrication of silicon Carrier for the SOP Application in RFICs

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Abstract

In the thesis, a System-on-Package (SOP) scheme that integrates the high-*Q* micro-machined inductors and a proposed low noise amplifier (LNA) circuit (TSMC 0.18um process) to realize a tunable wideband LNA for UWB mode-2 device (3.1GHz ~ 8GHz) is introduced and developed using a low-cost silicon carrier. Due to the use of on-carrier high-*Q* cross-membrane micro-machined RF inductors, the proposed LNA can have superior characteristics including wider tuning range, lower noise figure (3.5dB), and lower power consumption (10.5mW), and excellent reliability with environmental variation in comparison with the contemporary CMOS wideband LNA. In order to integrate the silicon carrier with the proposed LNA circuit chip, a novel flip-chip technique, Au-Au thermocompression bonding without using solder balls, is also developed and adopted to eliminate the unexpected parasitic effects resulted from the interconnect joints formed by traditional bonding technique. Moreover, the model of the micro-machined RF inductors is also developed for the following IC design. The proposed model is to synthesize the methodologies of Greenhouse's formula, physics-based closed-form inductance expression, and distributed capacitance model

(DCM) to formulate an exactly equivalent circuit model for the micro-machined inductor. Based on the model, circuit designer can achieve an optimum SOP design for RFICs application. Because the overall area of the integrated structure in the SOP scheme is almost equal to that in standard process, it is our belief that the proposed silicon carrier and developed integration technologies in this thesis can provide an alternative choice to IC designer for the future development of high performance IC chips.