Chapter 1 Introduction

1.1 Overview

With the strong development of wireless technology recently, it has great requirement and business for portable communication systems, such as mobile phone, personal digital assistant (PDA), global positioning system, digital broadcasting satellite and etc.. On the other hand, the radio-frequency (RF) chip in the wireless communication network must be provided with not only higher performance but also lower-power consumption and acceptable reliability. Thus, system-on-chip (SOC) concept is proposed to achieve the goal. The SOC means a full integration of functional circuits and passive components onto a single chip to enhance chip performance and reduce chip area, simultaneously. Unfortunately, due to the process limitation, the SOC approach still has trouble with the chip design and fabrication and several problems still have not been solved. For example, it is hard to integrate non-CMOS based devices, such as power amplifier, quartz resonator, and antenna, with a RF circuitry using the standard CMOS processes.

Recently, a new concept has been proposed to settle the process issues: that is system-on-package (SOP) [1][2]. Based on the package conception; a varieties of electronic components made by different processes, such as MEMS and CMOS techniques, are integrated on a specified carrier in which a built-in complex network is constructed for the electrical interconnects. In contrast, in the SOP approach, the built-in interconnects are fabricated using the state-of-the-arts flip chip technique to greatly reduce the parasitic effects originated from traditional wire bonding technique for the high-performance demand [3]. Since, via the carrier, all kinds of optimized devices from different processes can be fully integrated to acquire specified characteristics, such as high performance, low noise performance, low power consumption,

ultra-wide-bandwidth (UWB), and high reliability, there is no conflict between SOP and SOC and SOP, on contrary, just offers an alternative solution to realize the expected target. Therefore, it has drawn a lot of industrial attention. For example, Intel Corp. has used its 90-nm process technology as the basis for an all-CMOS wireless LAN transceiver designed as a system-on-package [4]. In addition, Philips Corp. has yielded their Bluetooth module for sale in 2004 by means of package technique, as shown in figure 1-1 [5].

In this thesis, we will demonstrate a SOP scheme that a UWB tuning low-noise amplifier (LNA) circuit (TSMC 0.18um process) is realized using a low-cost silicon carrier with the cross-membrane micro-machined RF inductors. Figure 1-2 shows the conceptive chart of fully integrated structure. The micro-machined inductor has higher quality factor (Q) value up to 40 and excellent reliability for temperature variation [6]. With the high-Q inductor, low noise figure (NF) (3.5dB) and power consumption (10.5mW), and broader bandwidth (3.1GHz ~ 8GHz) of the LNA circuit can be achieved. Furthermore, in the future, the cooling system or other high performance passive components could be included in the carrier for the transceiver fabrication with specific characteristics.

In addition, the model of the micro-machined RF inductors is also developed for IC design in the thesis. Since the RF spiral inductors have been developed for a long time, and their characteristics, including inductance, capacitance, loss mechanism, etc., have been surveyed in detail, the proposed model is to synthesize the methodologies of Greenhouse's formula [7], physics-based closed-form expression [8], and distributed capacitance model (DCM) [9] to formulate an exactly equivalent model for the micro-machined inductor. In order to further verify the electric model of the micro-machined inductor, we also utilize the contemporary simulators, Ansoft-HFSS and ADS (Advanced Design System) for comparison purpose. Finally, based on the model,

we believe circuit designer can realize an optimum RFIC design while the SOP scheme is applied.

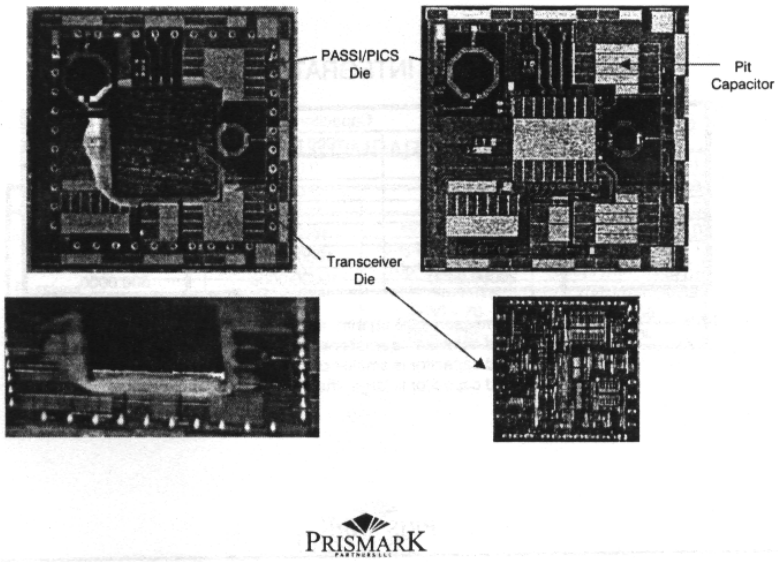

Fig. 1-1 The Bluetooth module yielded by Philips Corp in 2004 [4].

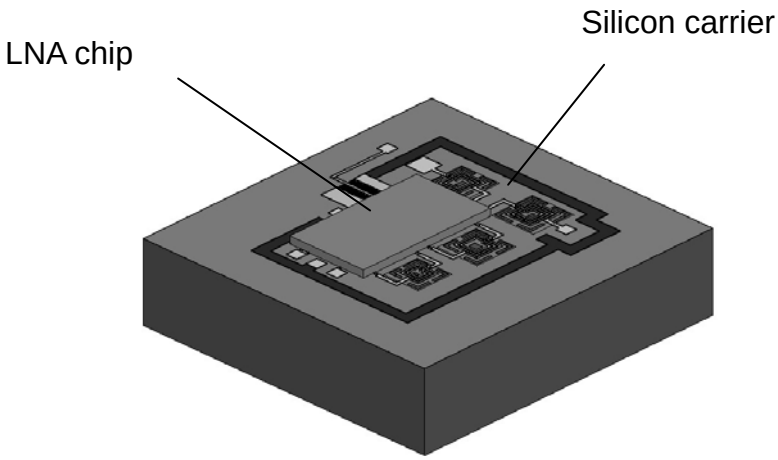

Fig. 1-2 The conceptive chart that a silicon carrier is assembled with the LNA chip made in standard process.

1.2 Thesis Organization

First, the applied components on the MEMs carrier, consisting of micro-machined inductor with cross-membrane supporting and UWB tuning LNA circuit, and flip-chip bonding technique are introduced in the chapter 2. In the chapter 3, we will synthesize the proposed methodologies in which inductance, capacitance and Series resistance expressions are derived to formulate an exactly equivalent model. Also the method of simulation will be discussed for the optimum design. Furthermore, the fabrication process of the micro-machined carrier is described in detail in the chapter 4. And the measured results of modeling are discussed in the chapter 5. Finally, the summary and future works are presented in chapter 6.