Chapter 2 Basic Concepts of Micro-Machined Carrier

2.1 Introduction

In the thesis, we will fabricate a micro-machined carrier which combines a low-power amplifier (LNA) circuit with high Q micro-machined inductors. On the carrier, there are some passive components including micro-machined inductors, bypass capacitors and measured pads. The proposed micro-machined inductor has been utilized because of its high-quality factor (Q) and excellent reliability to temperature [6]. The chip of LNA circuit is made using TSMC 0.18um CMOS process. It is designed to have the characteristics of tunable ultra-wide-bandwidth (UWB) 3.1~8GHz, low noise, and low-power performance [10]. In order to integrate the carrier and LNA circuit chip, a novel flip-chip technology [3], without using solder balls is developed to reduce the insertion loss of signal and the parasitic effect resulted from the solder balls. In this chapter, we will first discuss some basic conceptions and properties of the micro-machined inductor, LNA circuit, and flip-chip bonding as the followings.

2.2 The Micro-machined Inductor

The properties, such as loss mechanism and quality factor, are important factors to the performance of spiral inductors. Therefore, in the section, we will discuss the loss mechanism and the definition of quality factor of planar inductors in detail. After that, the proposed optimized micro-machined inductor which is superior to traditional ones in terms of high quality factor and excellent reliability with environmental variation, is introduced and adopted in the low-cost silicon carrier.

2.2.1 The Loss mechanism of Inductor

The practical inductor can not be supposed as an inductor purely at the high frequency range such as radio frequency. The imperceptible parasitic effect at the low frequency will increase with the increasing of operating frequency. Therefore, one must consider the parasitic capacitance and resistance at the high frequency. The loss mechanisms will dominate the performances of on-chip inductor, as generally resulted from two parts: the conductor loss and substrate loss. It will be discussed respectively in the following paragraphs.

(1) Conductor Loss

At DC bias, the finite conductivity of metal track will cause resistive loss significantly. The resistance of a uniform slab of metal track can be expressed as

$$R = \frac{\rho}{t} \cdot \frac{l}{w} \quad \text{(Ohms)} \qquad (2.1)$$

where ρ is the resistivity of the metal strip, and *w, t,* and *l* represent the width, the thickness, and the length of the metal strip. Moreover, the area of the conductor is the same as the product if the metal length *l* and width *w*. The expression may be denoted as

$$R = R_{sh}\left(\frac{l}{w}\right) \quad \text{(Ohms)} \qquad (2.2)$$

where R_{sh} is the sheet resistance having units of Ω/square.

At the low operation frequency, the current could be passing through the cross-section of the metal completely and the conductor can be treated as equation 2.2. Once the frequency increasing, the cross-section which the current could pass through is degraded. The phenomenon is so called the skin effect of the metal. The skin depth of the metal is inversely proportional to the square root of its driving frequency and metal

conductivity, as showed in equation 2.3.

$$\delta = \sqrt{\frac{1}{\sigma \pi \mu f}} \tag{2.3}$$

The symbol σ is the conductivity of the metal, μ is the permeability of the metal, f is the signal operation frequency. Besides, the magnetic field induced by the outer turns will go through the metal track of inner turns. The penetration of time-varied magnetic field will induce the eddy current on the metal track of inner turns. At the same time, the current flowing in the metal strip will be asymmetry due to the magnetic coupling of the adjacent metal track. The overall effect of skin depth, eddy current and adjacent effect will result in the non-uniform current distribution in the metal, as illustrated in figure 2-1. This will have a significant influence to the loss mechanism in the metal conductor at high frequencies [11].

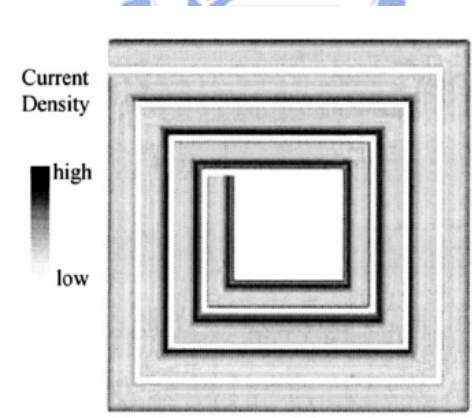


Fig. 2-1 The non-uniform current distribution of planar spiral [10].

(2) Substrate Loss

In theory, the substrate loss of planar spiral inductor can be resulted from and the losses caused by eddy current. For an on-chip inductor, the generally acknowledged

equivalent lumped circuit of substrate parasitic effect is shown in figure 2-2. C_{ox} is the parasitic capacitance of oxide layer. R_{si} and C_{si} represent the resistive and capacitive effect of substrate, respectively. Apparently, the parasitic capacitance of substrate will increase with metal length and turns of inductor. At low frequency, the capacitance of substrate can be neglected, but it will have major influence as resistive effect in the bulk at high frequency. Furthermore, the capacitive effect like a parallel capacitor will resonate with the inductor. The operation frequency region will be confined because of resonant effect.

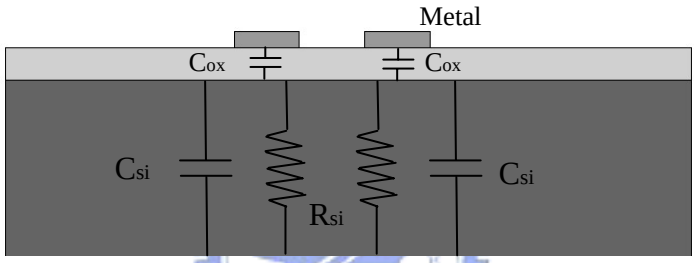


Fig. 2-2 The substrate lumped circuit model of metal track.

As the magnetic field penetrates into conductive substrate, the inductive coupling occurs and the opposite current, called “eddy current,” will be inducted. As illustrated in figure 2-6, the inductor current flows into the paper on the right (denoted as $\otimes$) and out of the paper on the left (denoted as $\odot$). According to the law of Faraday-Lenz, an electrical field is magnetically induced in an imaginary coil in the substrate underneath the inductor. Hence an induced current I_{sub} will flow in the substrate with the direction opposite to the current in the inductor. The inducted eddy current will greatly deteriorate the quality factor of inductor, especially at high frequency.

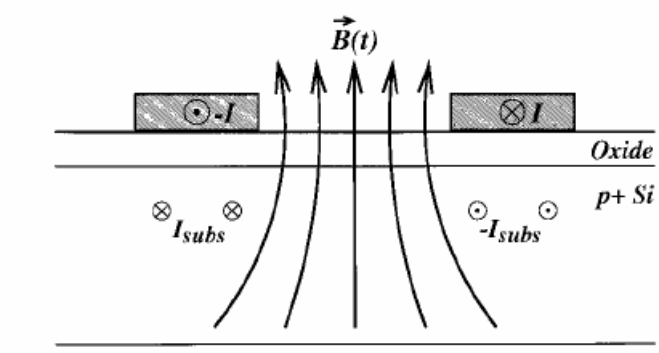


Fig. 2-3 When the magnetic field passed through substrate, the opposite-direction eddy current will be induced [6].

2.2.2 The Equivalent Circuit Model of the Inductor

According to the concept of section 2.2.1, the loss mechanism of the inductor has been described in detail. Now we can establish an equivalent circuit model including those effects of on-chip inductor in the figure 2.4 [11].

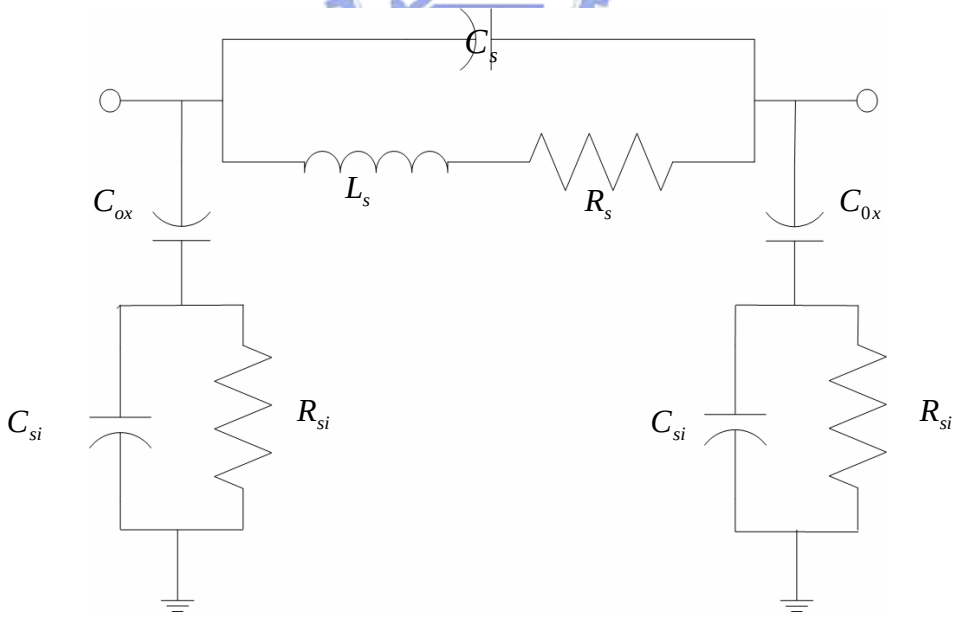


Fig. 2-4 The equivalent circuit model of inductor.

L_s represents the total inductance of the inductor. R_s is series resistance of metal track.

C_s represents the parasitic capacitance consisting of the overlap capacitance between the spiral inductor and the cross over metal, and the fringing capacitances between metal wires. The substrate effects can be modeled as a three-element network comprised of C_{ox}, R_{si}, and C_{si}. Actually, for the micro-machined inductor, the silicon substrate was removed to enhance performance. Thus, we can simplify the equivalent circuit to figure 2-6. That is, the R_{si} will be approached infinity and the C_{si} and C_{ox} will be approached zero reasonably.

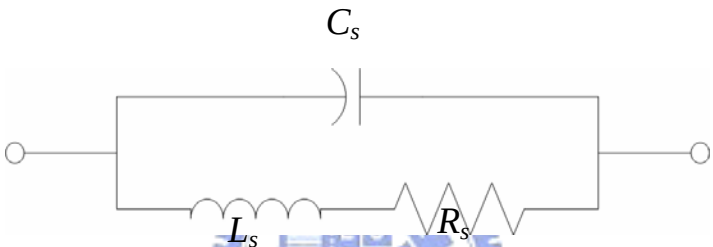


Fig. 2-5 The equivalent circuit model of the inductor with the substrate removal.

2.2.3 Definition of Inductor Quality Factor

The performance of an inductor is mainly decided by the qualify factor, Q. In general, the fundamental definition of qualify factor is

$$Q = 2\pi \cdot \frac{energy\ stored}{energy\ loss\ in\ one\ oscillation\ cycle} \tag{2.4}$$

For the figure 2-6, we make it as a single-driven RLC circuit that one terminal is excited by the source and another terminal is connected to reference port, the quality factor can be derived as [12]

$$Q = 2\pi \cdot \frac{peak\ magnetic\ energy - peak\ electric\ energy}{energy\ loss\ in\ one\ oscillation\ cycle}$$
$$= \frac{R_s}{\omega L_s} \cdot \left[1 - \left(\frac{\omega}{\omega_0}\right)^2\right] \qquad (2.5)$$
$$= \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})}$$

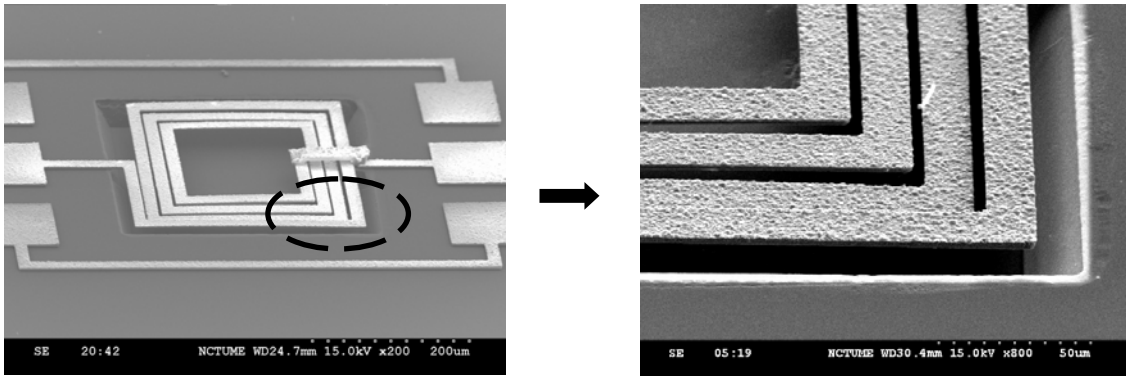
where *Zin* is the input impedance seen at source terminal. ω_0 is the resonant frequency could be treated simply as

$$\omega_0 = \frac{1}{2\pi\sqrt{L_s C_s}} \qquad (2.6)$$

So the qualify factor Q of an inductor is a frequency-dependent function. Its value will reach at zero as the inductor is at self-resonance.

2.2.4 The Optimized Micro-machined Inductor

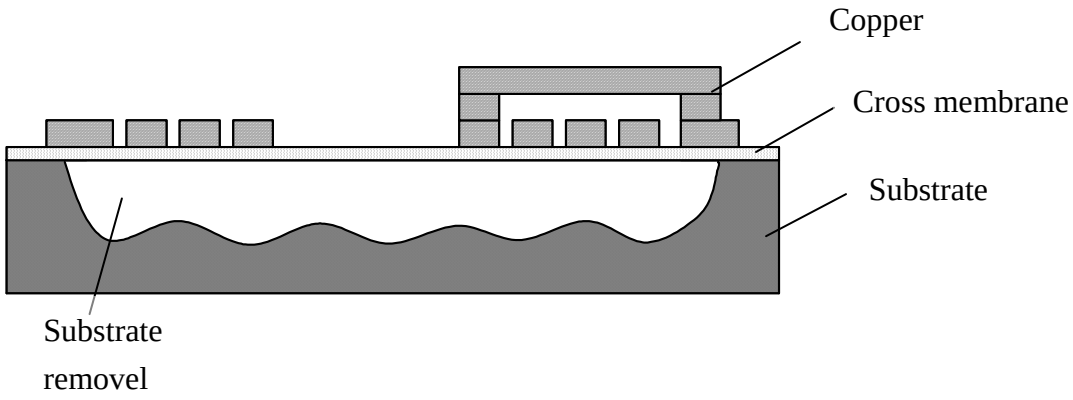
The micro-machined inductors usually have higher quality factor than the inductors in standard CMOS process. In MEMS process, the substrate under inductor is removed to reduce the parasitic effect at lowest. Without substrate loss, micro-machined inductor not only has high performance but the self-frequency of inductor can be lifted. Thus, designer can utilize MEMS inductor with broad bandwidth for the operating frequencies. However, the removal of substrate will result in reliability issues to inductors. On the other hand, the micro-machined inductors tend to be affected by the external disturbance, such as air pressure disturbance, mechanical thermal force disturbance and gravity disturbance. For example, due to the lack of machined support, the suspended inductor, showed in figure 2-7, will easily suffer the deformation in geometry. Unfortunately, as the inductor becomes deformed, the inductance and quality factor of inductor will changes. As far as the high performance circuit is concerned, the deformed inductor will not be acceptable no more.



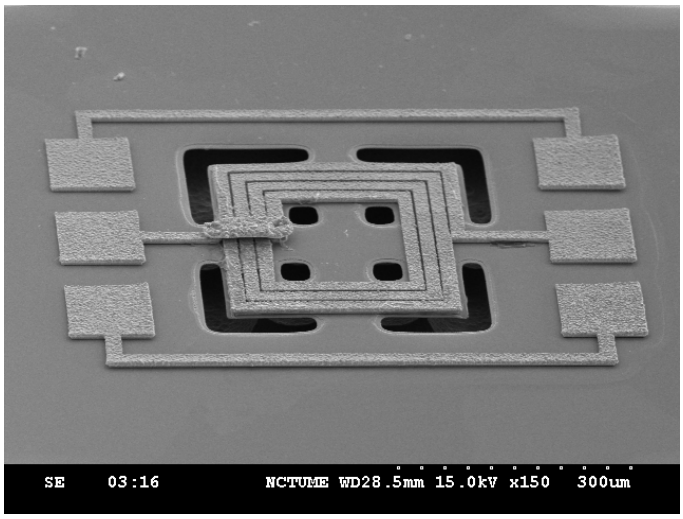
(a) (b)

Fig. 2-6 The SEM photographs of suspended inductor, (a) The oblique view of the fully suspended inductor, (b) the deformation on the corner region [5].

Recently, the optimized suspended inductor using cross membrane was proposed, as shown in figure 2-8 (a). Via the incorporation of a sandwich dielectric membrane (0.7μm SiO_2/ 0.7μm Si_3N_4/ 0.7μm TEOS) to enhance device structure rigidity, the inductor can have better signal stability. Moreover, the distinctive design of cross membrane also makes inductor insensitive to environment condition, as shown in figure 2-8 (b). The TEOS oxide underneath the corner of the inductor is removed to release the thermal stress, as shown in figure 2-8 (c) [6].



(a)



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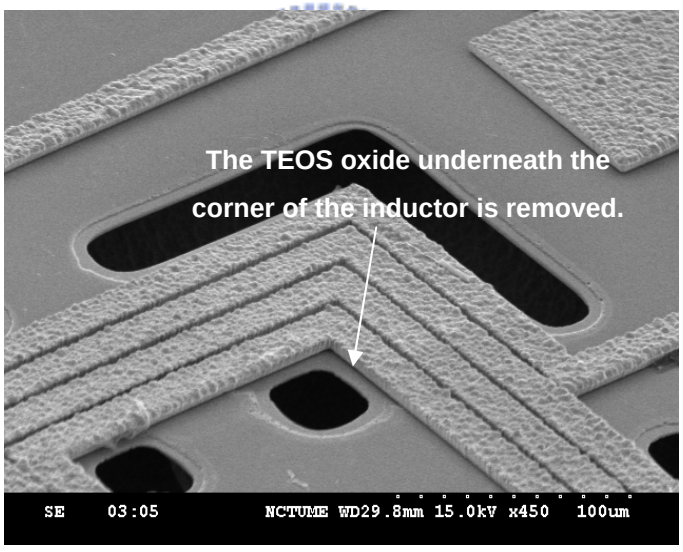
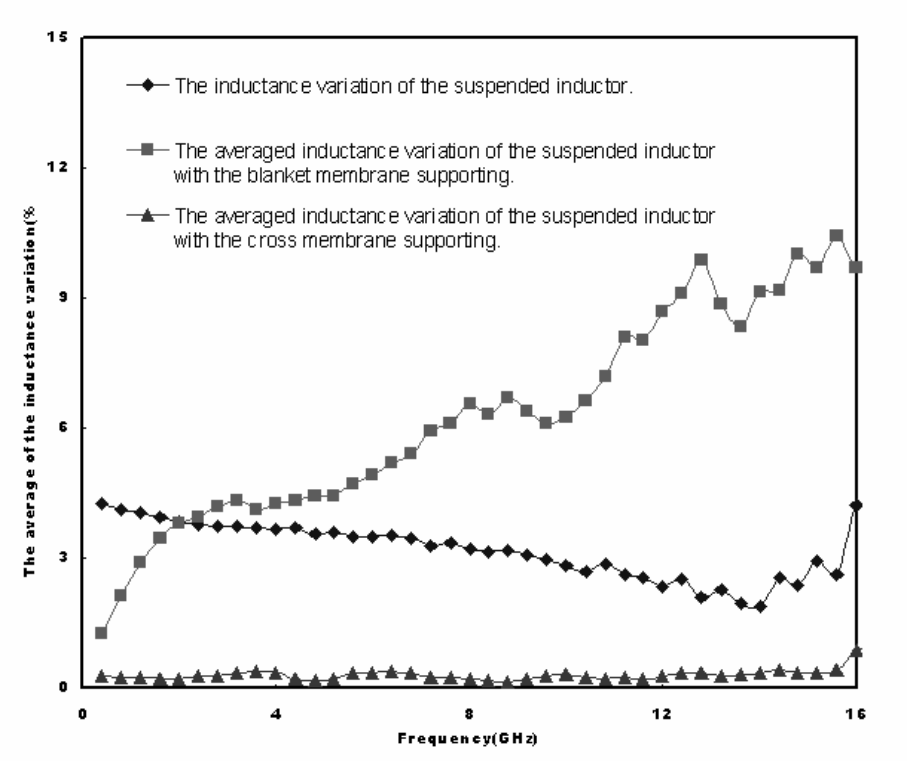


(c)

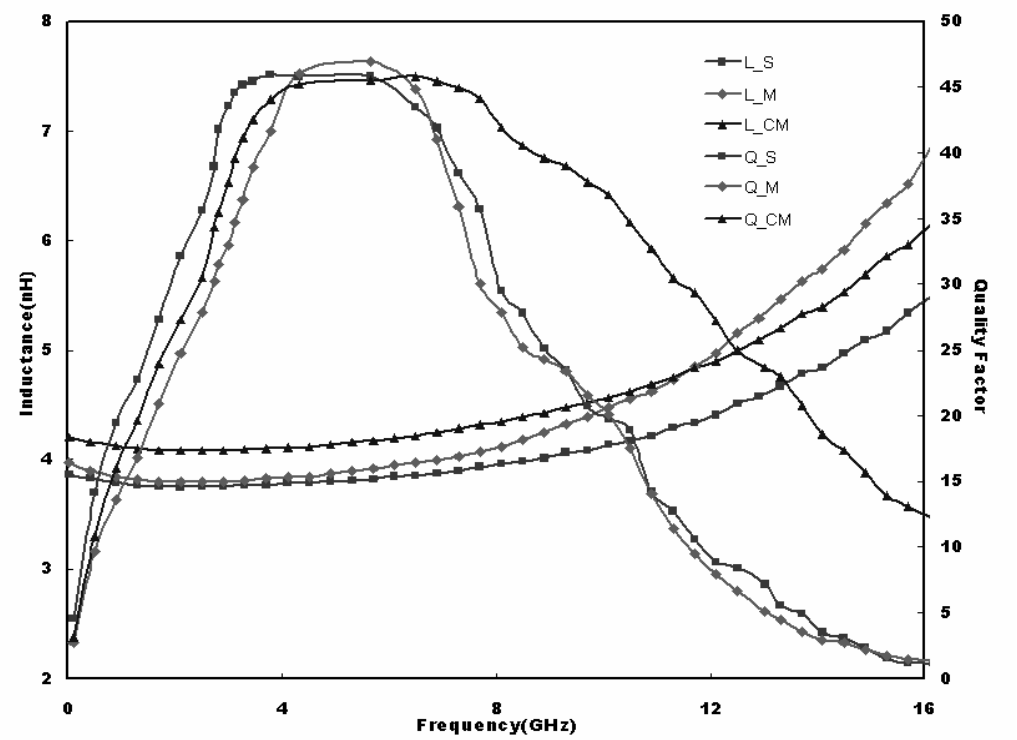
Fig. 2-7 The SEM photographs of those fabricated suspended spiral inductors with cross membrane supporting. (a) the cross-sectional view, (b) the oblique view, (c) the TEOS oxide underneath the corner of the inductor is removed [5].

In comparison with the simulation results, the proposed design of a around 4nH micro-machined inductor with a cross shaped dielectric membrane can have less 7.79% inductance variation than the traditional inductor while they are operated at 8GHz and

applied with 10 m/sec^2 acceleration. Meanwhile, the design can also effectively eliminate the inductance variation caused by the working temperature change (ΔT=55°C). In comparison with the conventional suspended inductor with a blanket membrane support and the one with the optimum design, less than 11.7% inductance variation up to 8GHz can be obtained due to the temperature change, as shown in figure 2-9(a). Most of important, the measured results shown in figure 2-9(b), present that the optimum inductor can have similar electrical performance to the as-fabricated suspended inductor, which has 4 times the quality factor enhancement than the inductor without the underneath substrate removal. That is, the new micro-machined inductors can have not only high *Q* performance but also better signal stability suitable for wide range RFIC applications.



(a)



(b)

Fig. 2-8 For the around 4nH micro-machined inductor, (a) the variation of inductance under 80℃, (b) the inductance and Q value of inductor. **S**: the suspended inductor; **M**: the suspended inductor with blanket membrane support; **CM**: the suspended inductor with cross membrane support [5].

As a whole, the high-Q micro-machined inductor indeed is a good choice for the circuit which would be operated at the high frequencies. Due to the specified design, the reliability issues of micro-machined inductor also have been promoted successfully. Furthermore, the micro-machined inductor will be modeled and optimized for actual circuit application in the chapter 3.

2.3 The LNA Circuit

The electrical advantages of micro-machined inductor have been introduced in the section 2.2. The application of high-Q and high reliability of micro-machined inductors can make functional circuit performance improvement greatly in contrast with traditional ones in standard COMS process. Figure 2-11 shows a new UWB LNA circuit published by the RFIC laboratory in NCTU R.O.C. The design target of the LNA is to achieve the ultra wideband from 3.1 GHz to 8 GHz which is the mode 2 bandwidth of UWB communication system. In general, to do the wideband frequency tuning could be achieved by switching capacitors or inductors while those components have high quality factors. Actually, it is not available for switching capacitors to extend tunable range from 3.1 GHz to 8 GHz due to the poor quality factor of large capacitance. On the other hand, the switched micro-machined inductor is a good choice for ultra wideband tunable LNA design. Consequently, the switched micro-machined inductors and MOS varactor will be utilized to make the frequency tunable capability. In the section, the conspicuous LNA is proposed with characteristics of frequency tuning range over 5 GHz, low-power consumption, and low noise finger [10].

2.3.1 Circuit Architecture

In figure 2-11, the four inductors, L_1, L_2, L_g, and L_{d1}, denoted by dot line are accomplished with micro-machined inductors. A three-section band-pass Chebyshev filter configuration, including L_1, L_2, L_g, L_s, C_1, C_2, C_{ex} and C_{gs} of M_1, is utilized as the wideband input matching. The C_{gs} is gate-to-drain capacitance of MOS and M_1. C_{ex} provides enough value of the capacitance for satisfying the filter design issue to reduce the power consumption. The benefit of adopting micro-machined inductors on L_1, L_2, and L_g is that the thermal noise can be reduced conspicuously due to the small parasitic

resistance caused by substrate loss. Switched transistor, M_{sw}, is used to switch the inductors, and a large resister R_b is employed to provide high impedance for ac open path, and thus reduce the overlap parasitic capacitance to half times then that without R_b. To provide high power gain, the Q factor of the tunable LC tank must be as large as possible, and thus the micro-machined inductor, L_{d1}, is utilized. M_3 and M_4 implement a source-follower output buffer. R_1 and R_2 are used to bias the buffer [10].

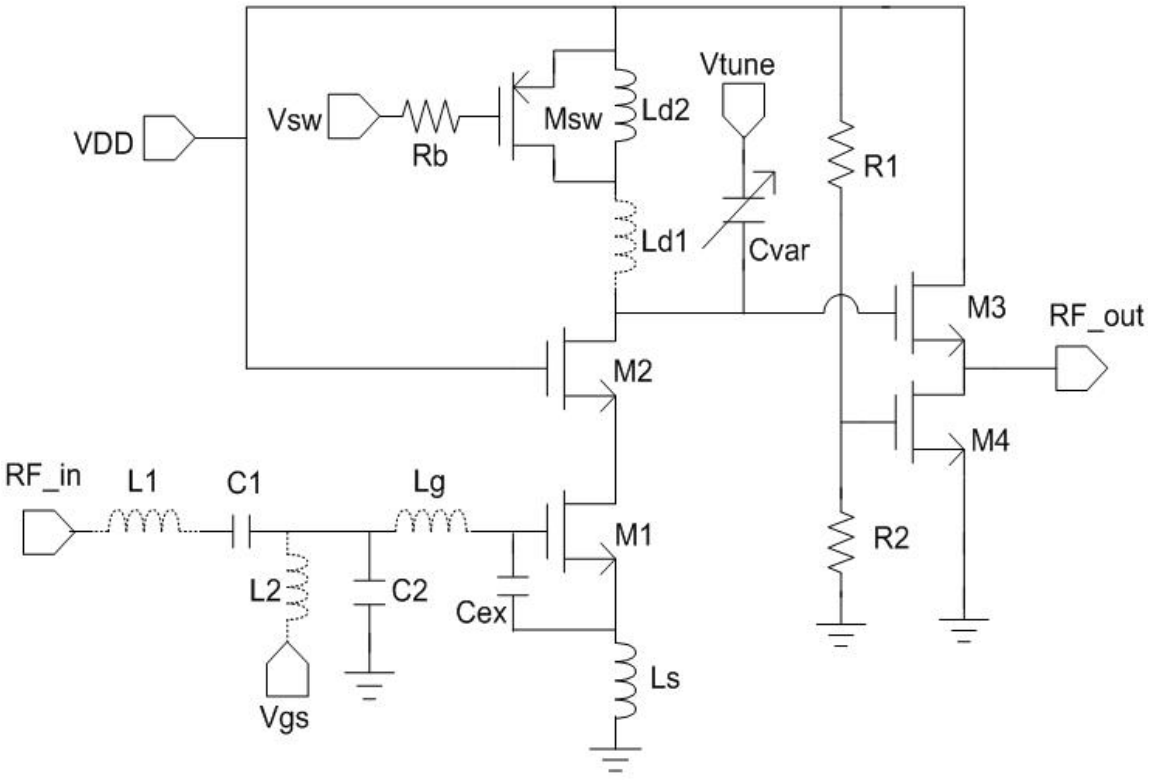


Fig. 2-9 The schematic of the tunable LNA for 3~8 GHz [9].

2.3.2 UWB Tunable Load

In the same way, we can use the high Q inductor to constitute the switch inductor load to improve the frequency tunable range and power gain rather than switched capacitor provided with low quality factor, as shown in figure 2-11 (a). R_b is attached to

reduce the overlap parasitic capacitor. When transistor Msw turned on, the impedance of parasitic resistance R_p of M_{sw} will be lower than that of L_{d2} or C_{ovp}, and the current will flow through R_p to ground. Otherwise, when M_{sw} turned off, the current will flow through the Ld2. The detail is illustrated in figure 2-11 (b) and (c) [10].

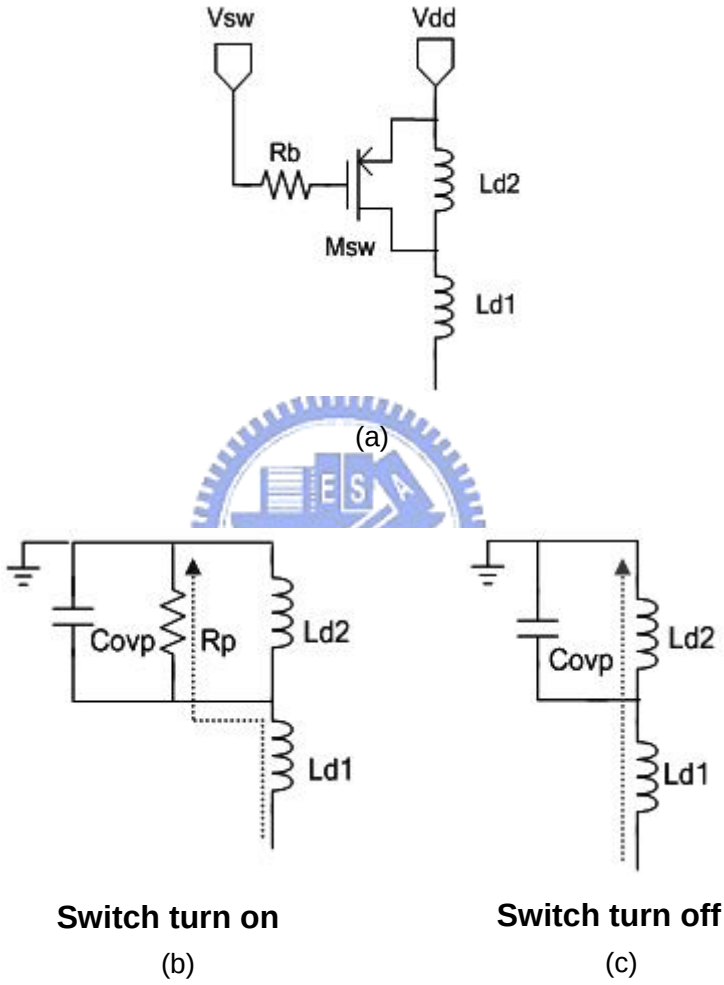


Fig. 2-10 (a) the switched inductor. The equivalent model when (b) switch turned on, (c) switch turned off [9].

2.4 Flip-Chip Bonding

We have introduced the micro-machined inductor and UWB tunable LNA in above sections. The flip-chip technology was used to integrate them on the carrier. The process

of bonding is so called IC assembly.

IC assembly is defined as the process of electrically connecting I/O bonding pads on the IC to the corresponding bonding pads on the package. It is the first processing step after wafer fabrication and singulation that enables ICs to be packaged for system using. In general, the interconnection between chip and package can be realized by using three primary interconnection technologies. These include wire-bonding, tape automated bonding (TAB), and flip chip. For wire-bonding, it is a chip-to-package interconnection technique where a fine metal wire is attached between each of the I/O pads on the chip and its associated package pin, one at a time. In this technology, a fine wire (typically gold wire 25μm in thickness) is joined using ultrasonic bonding between the IC bond pad and the matching package or substrate bond pad. The flexibility derived from this point-to-point process is one of the major advantages of wire-bonding. Tape automated bonding (TAB) is an IC assembly technique based on mounting and interconnecting ICs on metallized flexible polymer tapes. It is based on the fully automated bonding of one end of an etched copper beam lead to an IC, and the other end of the lead to a conventional package or PWB. The goal of this new technology introduction was a lower cost replacement of wirebonding technology by providing a highly automated reel-to-reel “gang bonding” technique for packaging high-volume, and low I/O devices. Moreover, to eliminate efficiently the parasitic effect of interconnection, the flip-chip technology was developed. Flip chip microelectronic assembly is the direct electrical connection of face-down (hence, "flipped") electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. Flip chip is also called Direct Chip Attach (DCA), a more descriptive term, since the chip is directly attached to the substrate, board, or carrier by the conductive bumps. The three bonding technology are summarized and illustrated in figure 2-12 [1].

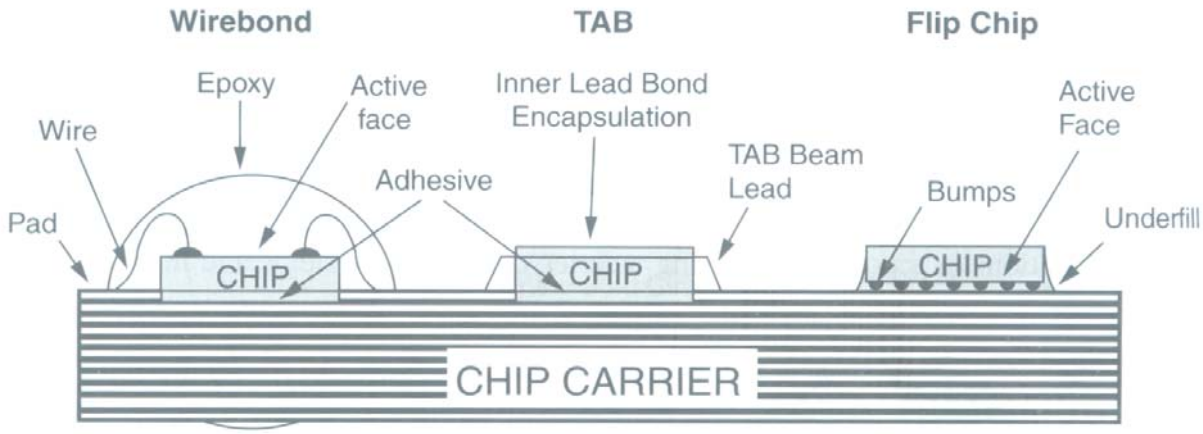


Fig. 2-11 Chip to package or substrate interconnection techniques [1].

Table 2-1 Chip-level connection parameters [1].

	Wirebonding		*TAB*	*Flip Chip*
Connection Metallurgy	Al	Au	Cu	Pb / Sn
Resistance (ohms)	0.035	0.03	0.02	0.002
Inductance (nH)	0.65	0.65	2.1	0.200
Capacitance (pF)	0.006	0.006	0.04	0.001
I/O density	400	400	400	1600
Rework	Poor	Poor	Poor	Good
Failure Rate (%/1000h)	1×10^{-5}	1×10^{-5}	N / A	$<1\times10^{-8}$

2.4.1 The Advantages

We have discussed basic concepts of bonding technique in above paragraph. The comparison of performance of wirebonding, TAB, and flip chip are shown in table 1. It summarizes the key parameters includes the electrical parameters such as resistance, capacitance, inductance, and failure rate. Apparently, flip chip clearly dominates in all of

these. Flip chip has the lowest parasitic effect of interconnection in contrast with the others. Besides, the booms in flip chip packaging results both from flip chip's advantages in size, performance, flexibility, reliability, and cost over other packaging methods and from the widening availability of flip chip materials, equipment, and services. Nowadays, the latest flip chip technique, gold-gold (Au-Au) thermo-compression (TC) bonding [3], was proposed. The most significant breakthrough of this process is the vanishment of bump. That is, the stephight of bump is equal zero nearly, so that the parasitic effects of bump vanish almost. We will chew over this technique in the chapter 4.

2.4.2 The Bumps

Until now, people have developed four kinds of flip chip bonding methods sorted by the bump category. These include solder bump, plated bump, stud bump, and adhesive bump flip chip. Figure 2-13 shows the reflowed solder bump on electroless nickel-gold UBM. Those bumps serve several functions in the flip chip assembly. Electrically, the bump provides the conductive path from chip to substrate. The bump also provides a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump provides part of the mechanical mounting of the die to the substrate. Finally, the bump provides a spacer, preventing electrical contact between the chip and substrate conductors, and acting as a short lead to relieve mechanical strain between board and substrate.

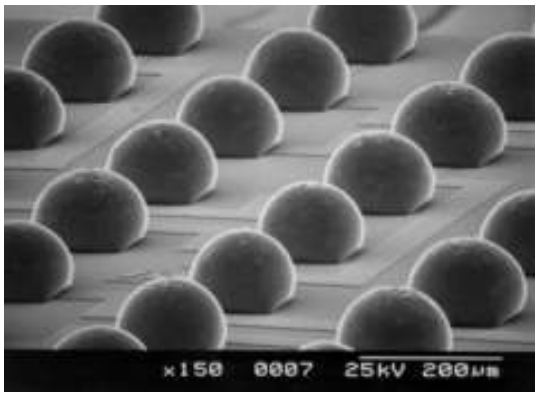


Fig. 2-12 Reflowed solder bump on electroless nickel-gold UBM.
(Source: http://www.flipchips.com)

2.4.3 The Flip Chip Process

Solder bump has the longest production history, the highest current and cumulative production volumes, and the most extensive reliability data of any flip chip technology. Therefore, we will take the solder bump for example to study the process of flip chip in the section. The solder bump flip chip process may be considered as four sequential steps: preparing the wafer for solder bumping, forming or placing the solder bumps, attaching the bumped die to the board, substrate, or carrier, and completing the assembly with an adhesive underfill. First, the solder bumping process requires that an under bump metallization (UBM) be placed on the chip bond pads, by sputtering, plating, or other means, to replace the insulating aluminum oxide layer and to define and limit the solder-wetted area. Solder is deposited over the UBM by evaporation, electroplating, screen printing solder paste, or needle-depositing [1].

After solder bumping, the wafer is sawn into bumped die. The bumped die is placed on the substrate pads, and the assembly is heated to make a solder connection. One function of the solder bump is to provide a space between the chip and the board. In the last stage of assembly, this under-chip space is usually filled with a non-conductive "underfill" adhesive joining the entire surface of the chip to the substrate [1]