Chapter 4 Fabrication Process of Silicon Carrier and Gold-Gold Thermocompression Bonding

4.1 Introduction

As mentioned in chapter 2, the MEMs carrier is designed to integrate the micro-machined inductor and LNA circuit for UWB tuning range. On the carrier, the cross-membrane micro-machined inductors, by-pass capacitors, ground pads, and measured pads will be fabricated in MEMS process. Since we have analyzed the cross-membrane micro-machined inductor theoretically in chapter 3, the inductor of specified inductance is available to realize in process utilizing the analytical model. In addition, the layout of carrier must also be considered conscientiously to avoid the unexpected parasitic effect. After the carrier is achieved, the LNA circuit made in TSMC 0.18um CMOS process will be bonded to the carrier by package. Flip chip is a common technique of IC assemble packages. Most of important, the latest flip chip technology, the Gold-Gold (Au-Au) thermocompression (TC) bonding [3], has no solder balls as conductive connectors. On the other hand, it can service as line-to-line bonding, so that the parasitic effect of solder ball vanishes and bonding area can be diminished very much. As a whole, we can integrate the micro-machined inductor and LNA circuit using low-cost MEMs process and obtain higher performance and wilder tuning bandwidth in contrast to conventions one.

4.2 Consideration of layout

The proposed layout of complete integrated circuit is shown in figure 4-1. The UWB LNA with two standard-CMOS process inductors, such as L_s and L_{d2}, is illustrated in the center of carrier. Several terminal metal lines extend to the outer edges of the LNA

die and the passivation layer above them was removed for flip-chip bonding; that is to say, the metal lines and pads where prepared for bonding are bare at air. Meanwhile, it is critical to require that these lines stretch to the edges of die certainly due to the process of thermo-compression bonding. Besides, there are four cross-membrane micro-machined inductors, i.e. L_1, L_2, L_g, and L_{d1}, used to attach the LNA. The covers above the four corners of inductors represent that it is suspend with cross membrane. The connective metal lines between micro-machined inductors and LNA also were simulated to consider their parasitic inductive effect and matching issues. According to the simulation, a metal track with length /width/thickness 160um/15um/5um has contribution on inductance around 0.1~0.2nH. Furthermore, that is not only the width of them was increased to reduce the parasitic effect, but the micro-machined inductors must be rescaled in geometry to fit with the specified inductance. All the ground pads are connected together to have the same reference for the chip die and the carrier. By the way, the metal multi-finger capacitor offers enough by-pass capacitance between V_{tune} and ground. It should be noted that the V_{gs} pad was augmented in scale to raise the by-pass capacitance. Due to the effect of transmission line at high frequencies [19], the multi-finger capacitor was not applied between V_{gs} and reference ground and was replaced with a large parallel capacitor. The I/O ports, including two GSG pads and two PGP pads (150um pitch), are fabricated on carrier for measurement. In terms of inductors on LNA chip, as the chip is flipped to assemble to carrier, they will face the silicon substrate of carrier with the distance about 2um. The unexpected substrate loss will degraded the performance of inductors on LNA chip. For this reason, we must remove the substrate of carrier under the LNA die especially.

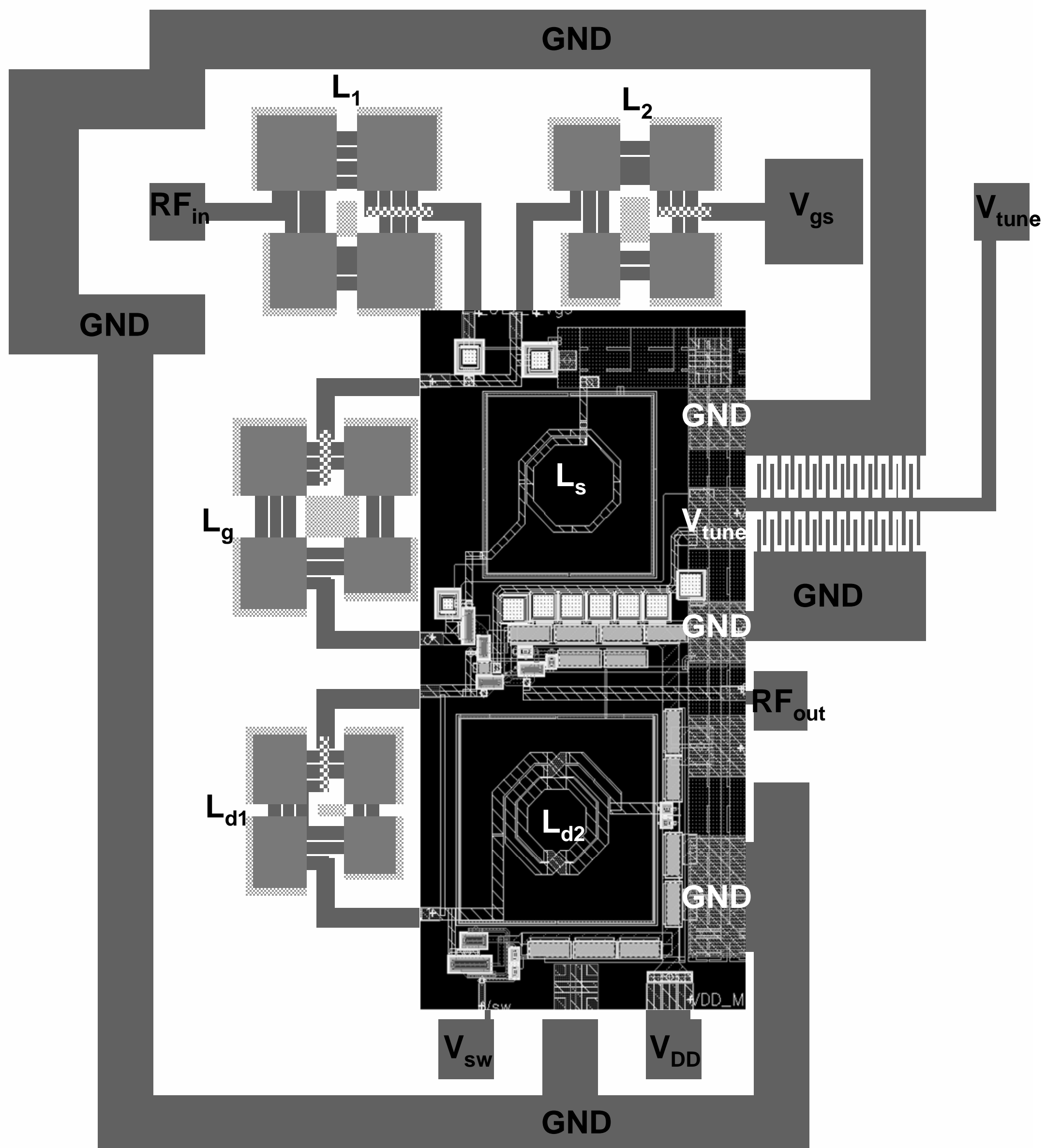
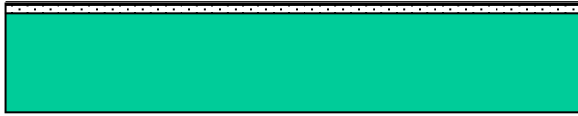


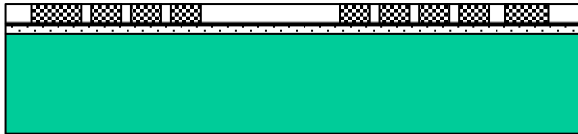
Fig. 4-1 The layout of micro-machined carrier with a LNA circuit.

4.3 Passive Components on Carrier

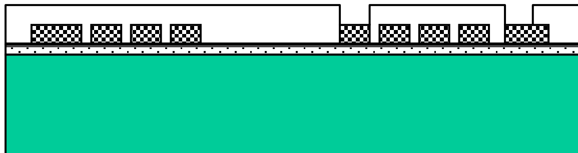
In the section, the fabrication of carrier will be carried out in MEMs process using the wafer of p-type 4 inch. The process flow of passive components on carrier, including surface micro-machined process and bulk removal process, is shown in the Figure 4-2.



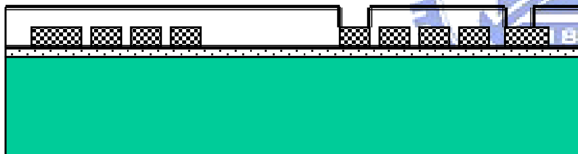
(a) Deposit sandwich membrane ($SiO_2/Si_3N_4/SiO_2$) and sputter the seed layer (Ti/Cu).



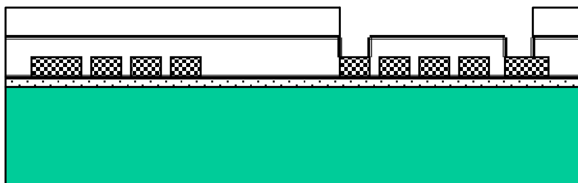
(b) The first copper electroplating for the coil part of the inductor and pads.



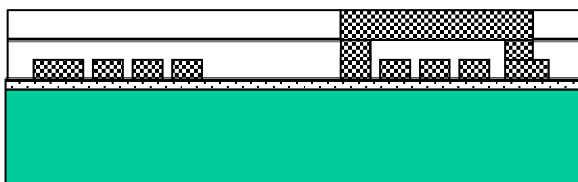
(c) The patterned photo-resist to define the via hole.



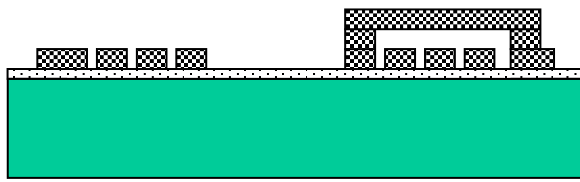
(d) Sputter the Ti/Cu seed layer of air-bridge deposition.



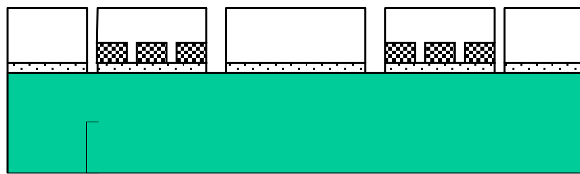
(e) The patterned photo-resist to define the air-bridge.



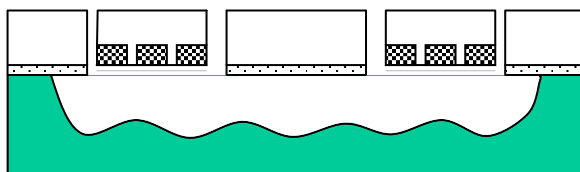
(f) The secondary copper electroplating for fabrication of air-bridge.



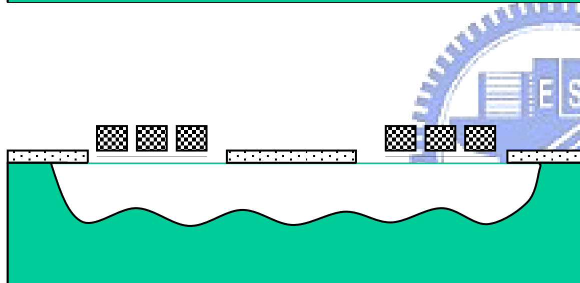
(g) All seed layers and photo-resist were released.



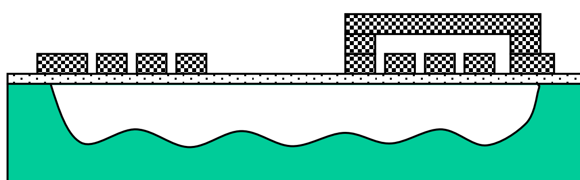
(h) Dielectric patterning using RIE.



(i) Form cross membrane using BOE etching and substrate removal using the XeF_2 gas.



(j) PR mask removal.



(k) PR mask removal.

Fig. 4-2 The process flow of passive components on the carrier [5].

In the Figure 4-2 (a), it begins with wet oxidation at 980ºC for 7000Å of thermal oxide, followed by low-stress nitride with 7000Å using LPCVD and TEOS oxide depositions with 7000Å on a p-type 4-inch silicon substrate. In addition, the thin film, consisting of 100Å Ti as an adhesion layer and 1200Å Cu as a seed layer, is sputtered

onto the silicon substrate. Figure 4-2 (b) shows that then it was patterned above the Ti/Cu thin film with the AZ 4620 photo-resist of 6μm thickness to define the region for the fabrication of the coil part of the spiral inductor and measured pads using copper electroplating. After plated the first layer of copper, a 10μm AZ4620 is spin-coated, patterned to define the via hole, as shown in figure 4-2 (c), and sputtered with another 1000Å copper seed layer on the same substrate as shown in figure 4-2 (d) for the air-bridge copper via filling. Figure 4-2 (e) illustrates that, above the seed layer of the via filling, another 10μm AZ4620 is spun onto the plated structure and patterned to define the air-bridge beam. Then it is electroplated with 5μm copper metal to fabricate the air bridge, as showed in figure 4-2 (f). Finally, the fabrication of the spiral inductor is done after lift off the underneath copper seed layer and chemically etch away the first seed/adhesion layer using CR-7T and BOE solutions as shown in figure 4-2 (g).

After the surface micro-machined process has been achieved, we will proceed with the bulk micro-machined process of micro-machined cross-membrane inductor. In other words, we will devise a way to remove the silicon substrate underneath micro-machined inductors. The underneath cross membrane is etched away to define the corner regions utilizing RIE (reactive ion etched), as illustrated with the cross-section of inductor's corner region in figure 4-2 (h). After that, the TEOS oxide is removed to make the corners of micro-machined inductors suspend at air by means of BOE solution. Since the XeF_2 gas has greatly excellent etching selectivity to silicon, the dielectric membrane or copper strips could be utilized as the mask. Furthermore, the opened area around the four corners or the adjacent region of the suspended inductor provide the paths for the XeF_2 gas to isotropically etch the underneath silicon substrate as shown in figure 4-2 (i). Finally, the photo-resist mask is removed by dipped into the Acetone solution as shown in figure 4-2 (j) and figure 4-2 (k) with cross-section of the bridge.

4.4 Gold-Gold Thermocompression Bonding

Since the MEMs carrier with passive components has been achieved, we could integrate it and the LNA chip by means of flip chip technique, Gold-Gold thermocompression bonding [3]. The detail of bonding will be discussed in the following section.

Gold-gold (Au-Au) TC bonds have been widely recognized as reliable high yield interconnects for semiconductor package applications. TC binding of compliant Au pads is widely used for connections to thin film hybrid integrated circuits. Until now, the latest development can achieve line-to-line TC bonding with misalignment distance of 1um. The basic principle of Au-Au TC bonding is that: as the gold becomes fused state at the temperature ~375ºC, we can join two objects which are coated with gold layer together under enough pressure. The key point of TC bonding comes from the thickness of gold layer, the applied pressure, and the fused degree of Au. In general, the surface roughness of Au thin film can also enhance the yield of bonds, i.e. there is larger contact area effectively.

Figure 4-3 illustrates the joining process that integrates the LNA chip and the MEMs carrier. It should be noted that the silicon substrate underneath LNA chip was etched away to diminish the parasitic substrate loss and the passivation layer mantles the metal 6 of the LNA chip was removed to enable the contact of flip chip bonding, as mentioned in section 4.2. In the beginning, in order to grow the Au layer, the surface of contact copper metal must be dipped with Pd solution and the thin Pd layer will form on the copper. Then using the electroless plating technology, the 0.5um Ni layer will be plated above the Pd layer at 80ºC. In the same way, the surface of Ni layer will be transformed as the joining Au layer using electroless plating at 90ºC. Figure 4-4 shows the process flow of plating Au layer. The equipments setup of electroless plating is

shown in figure 4-5 [20]. Finally, both the copper metals on the LNA chip and the MEMs carrier are plated with Au thin film of thickness 0.3um, as shown in figure 4-3.

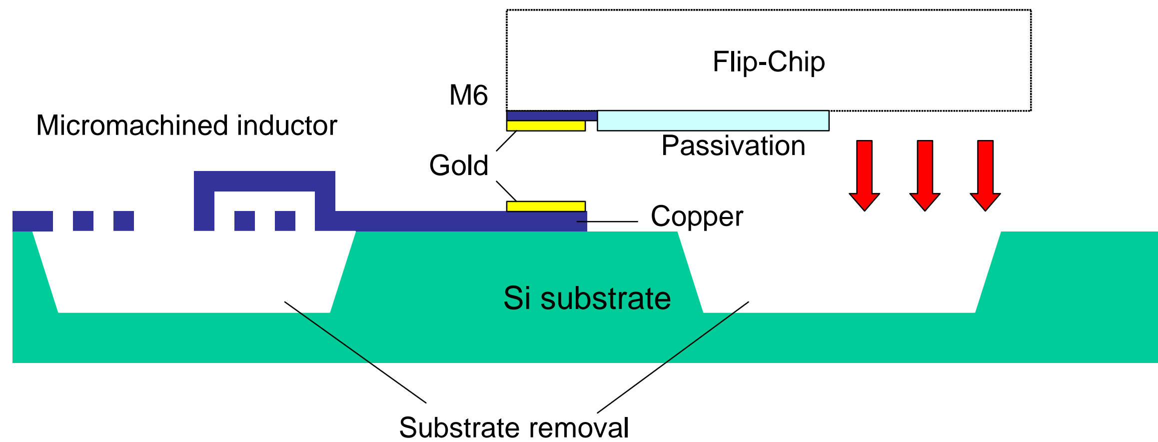


Fig. 4-3 The joining process of Au-Au TC bonding between the micro-machined carrier and UWB tunable LNA chip.

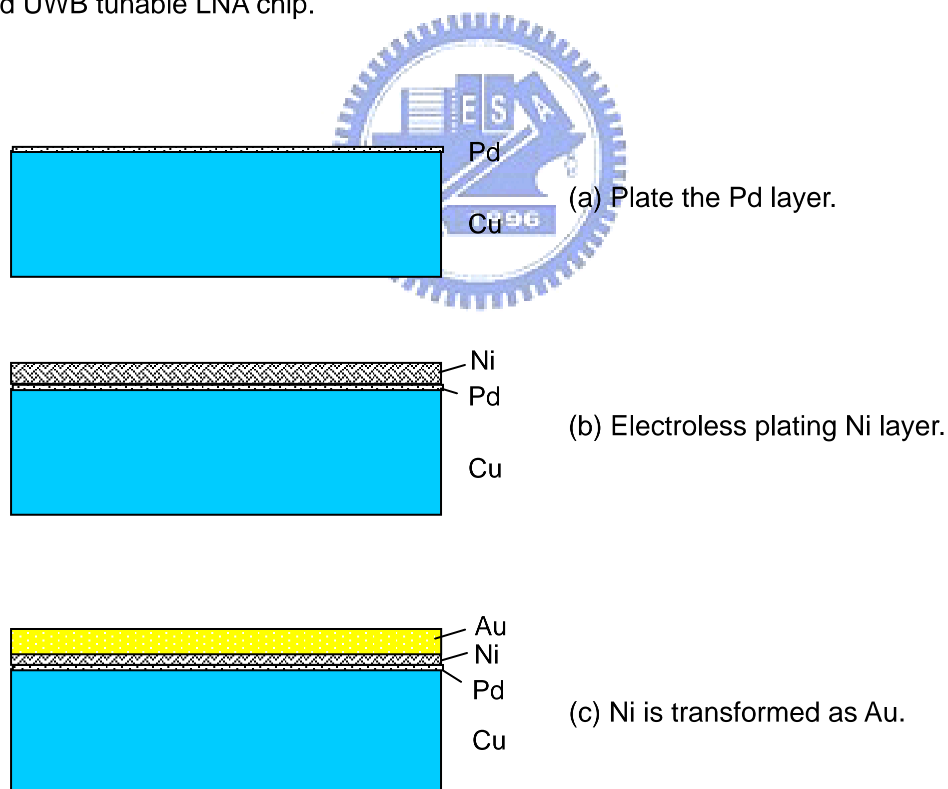


Fig. 4-4 The process flow of plating Au layer for joining.

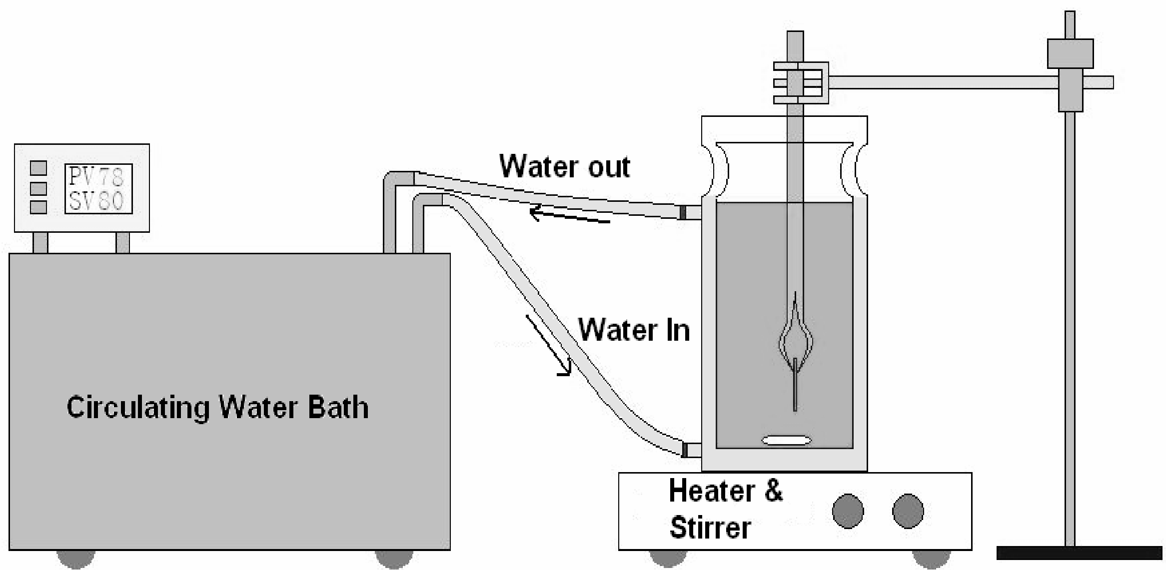


Fig. 4-5 The equipments setup of electroless plating for Ni and Au layer [20].

4.5 Joining Test

Au-Au thermocompression bonding technique is developed for electrical interconnections and mechanical joints between two chips. In order to verify the feasibility of Au-Au thermocompression bonding, two vehicles where with and without copper studs were prepared for interconnection joining test. Figure 4-6 shows that a Ti/Cu (100Å/4um) stud on **A1** is flip-bonded with another blanket Cu layer on **A2** to mimic the bonding between the contact bump of carrier and the receiving pad of circuit chip. Consequently, an excellent bond formed between the Au layers. After forcefully breaking the chips, the Cu stud has been torn away and transferred onto the other substrate. It indicates that the Au-Au bond is stronger than the adhesion force of Ti to silicon substrate and could form the electrical and mechanical interconnection. Since the joint is much thinner than conventional solder balls, low insertion loss and small parasitic effects can be achieved using the bonding technique.

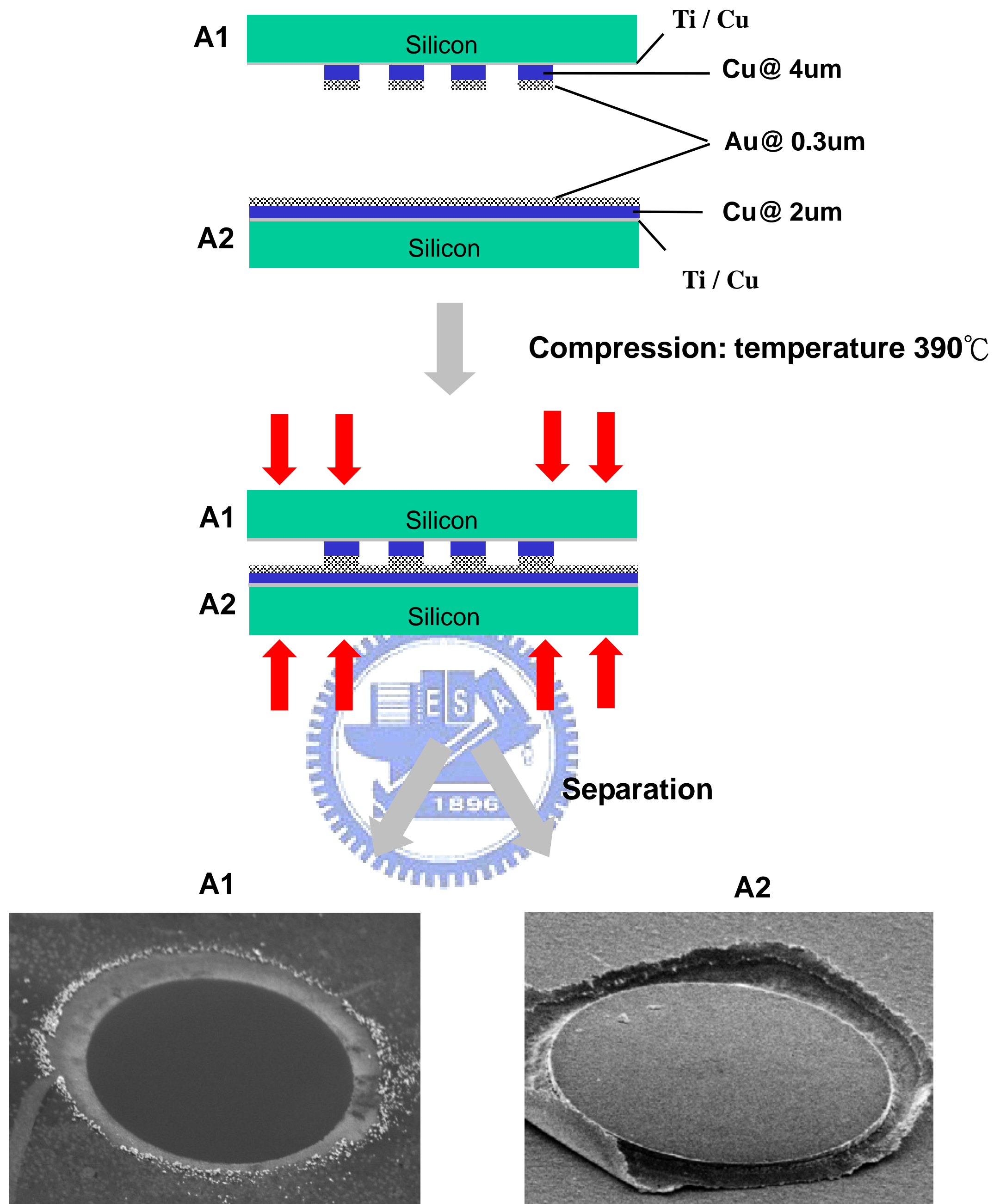


Fig. 4-6 The test vehicles with and without copper studs are both coated with electroless Au layers and bonded with each other at 390℃. After separation, the copper stud has been torn away on **A1** and transferred onto another test vehicle **A2** by means of Au-Au bond. Consequently, it shows that the strength of Au-Au bond is enough to form the electrical and mechanical interconnection.