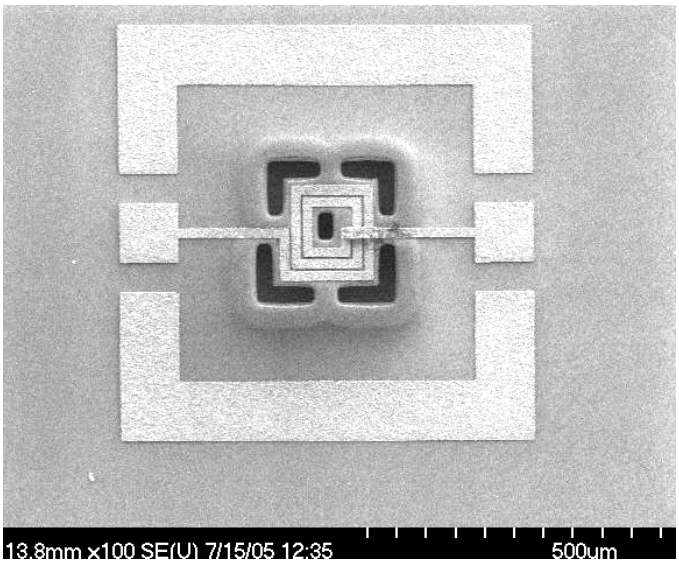
Chapter 5 Experimental Results and Discussions

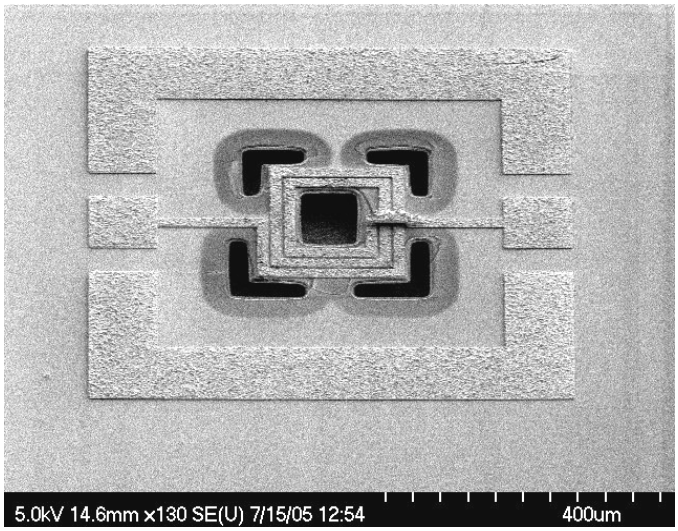
5.1 Experimental Results for Modeling

5.1.1 Fabrication of test inductors

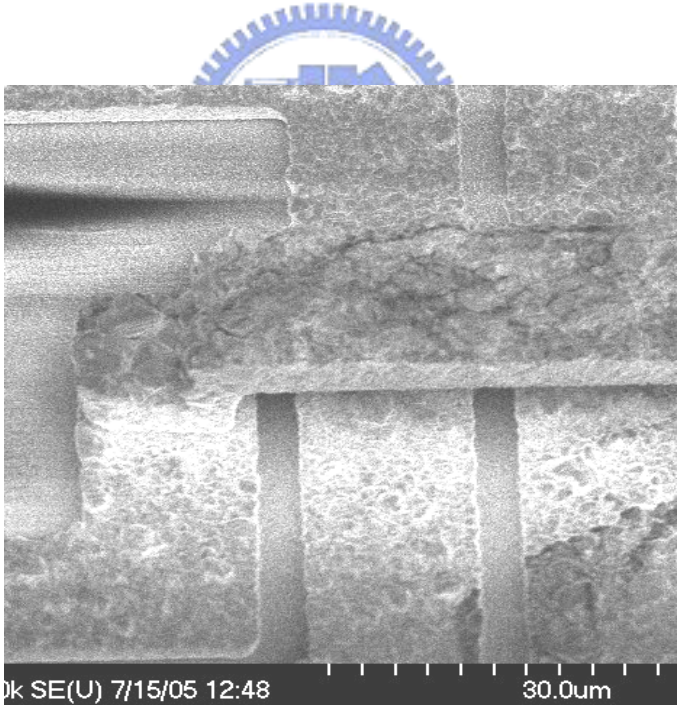
In order to verify the model mentioned in chapter 2, the test cross-membrane micro-machined inductors with different inductances consisting of the range: 0.5nH ~ 4nH, were fabricated in MEMs process and measured. Figure 5-1 shows one of the fabricated micro-machined inductors with 2.5 turn. The center of micro-machined inductor was cleared out to speed up the XeF2 etching rate of silicon substrate. Moreover, the phenomenon, that the partial membrane which surrounds inductor was caved in, occurred due to the over-etching result of RIE, as shown in figure 5-1 (a) and (b). By the way, the bridge of micro-machined inductor and the connective via were electroplated at the same time, so that the connective sections between the bridge and via are thinner than expected metal thickness of 5um, as shown in figure 5-1 (c).



(a)



(b)

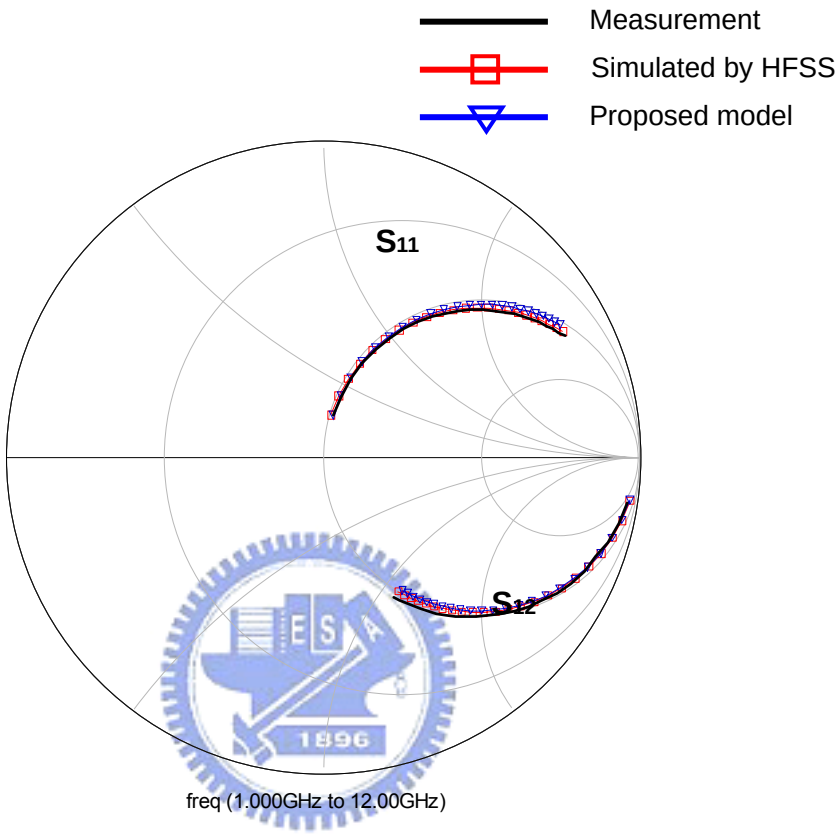


(c)

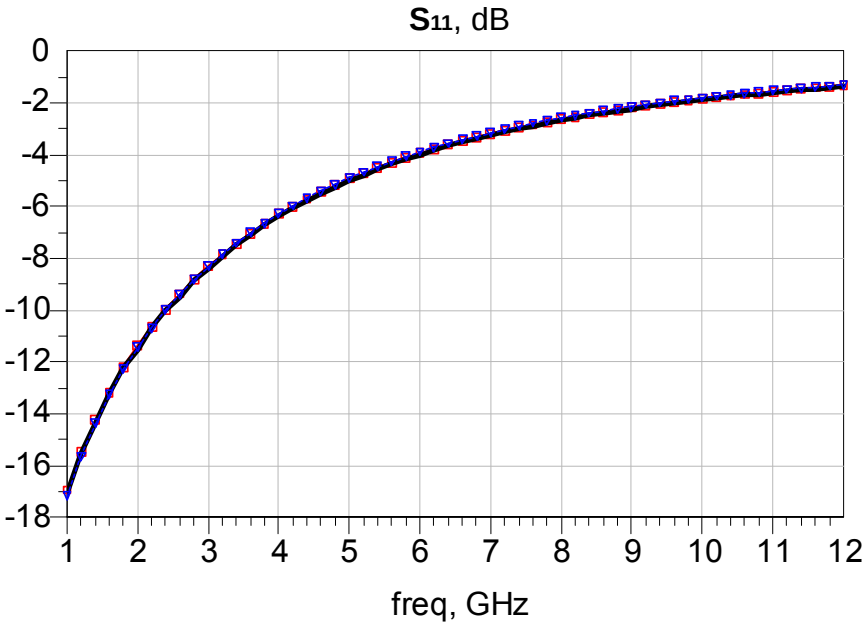
Fig. 5-1 The SEM photograph of suspended micro-machined inductor with cross membrane supporting. (a) Top view. (b) Oblique view. (c) The connected section of bridge.

5.1.2 Measurement results

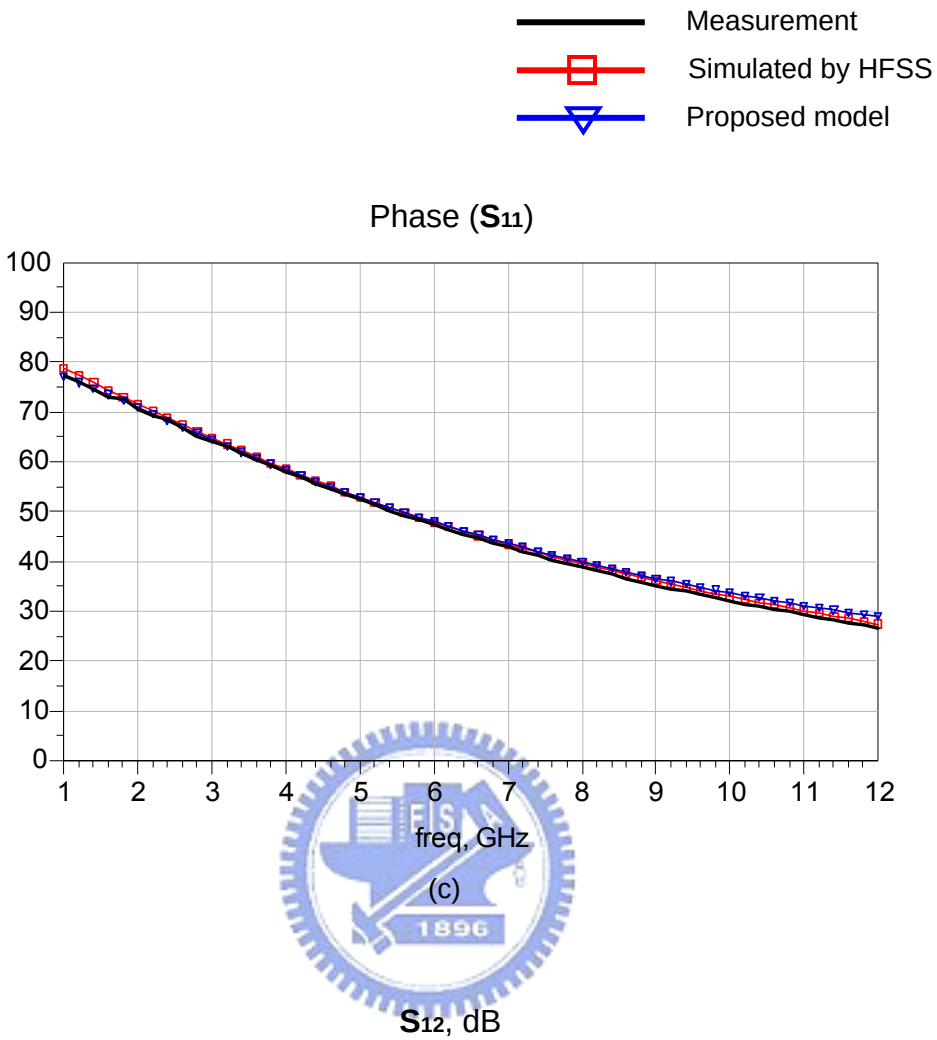
The measured results of test micro-machined inductors are in contrast to simulation and our proposed model as the followings.



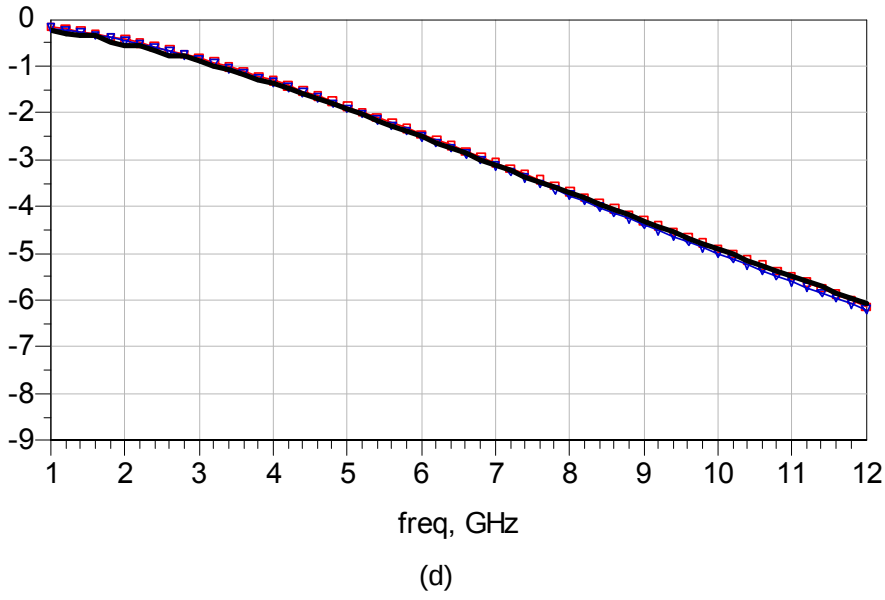
(a)



(b)


Measurement
Simulated by HFSS
Proposed model
Phase (S11)
100
90
80
70
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
11
12
freq, GHz

(c)


S12, dB
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
1
2
3
4
5
6
7
8
9
10
11
12
freq, GHz

(d)

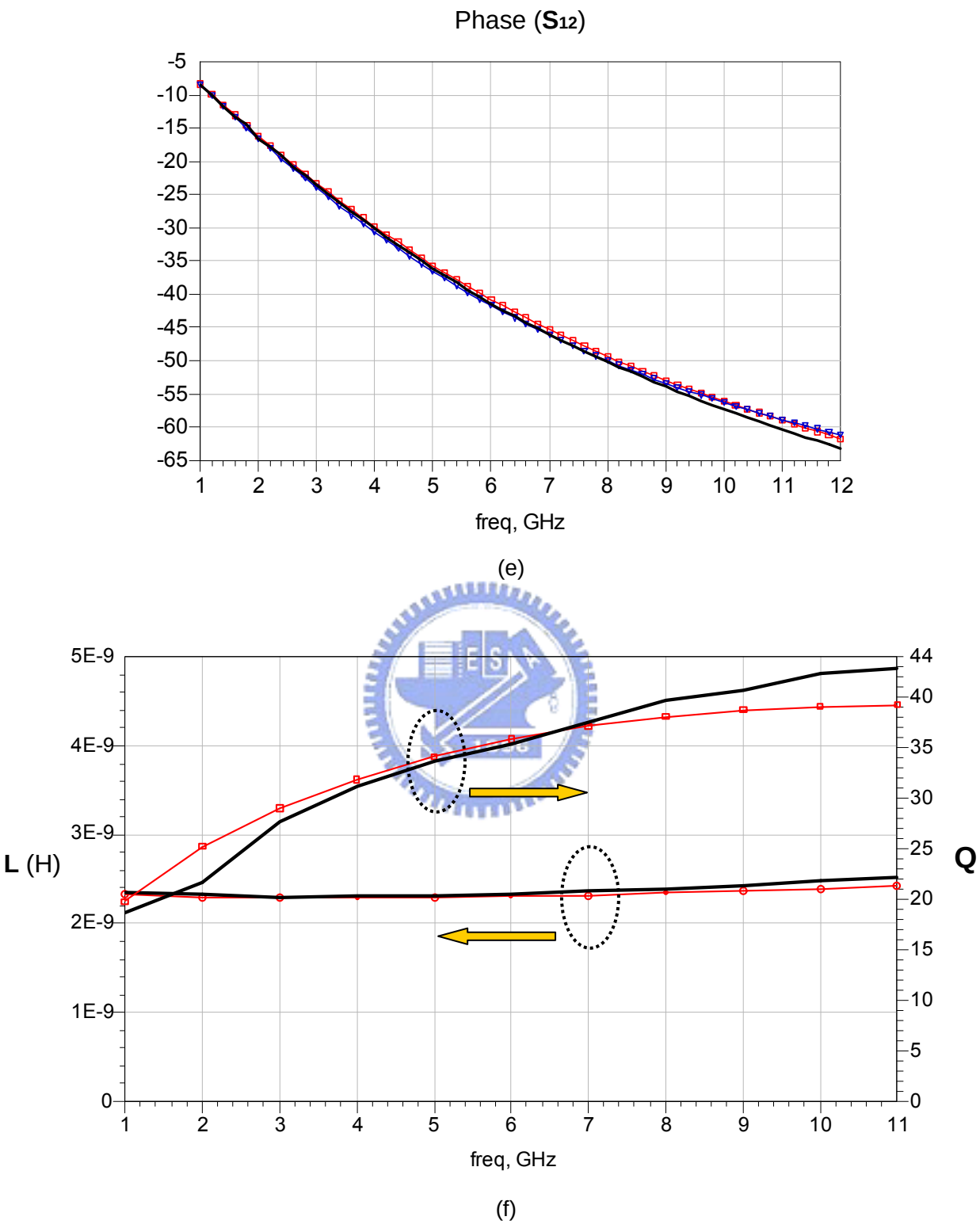
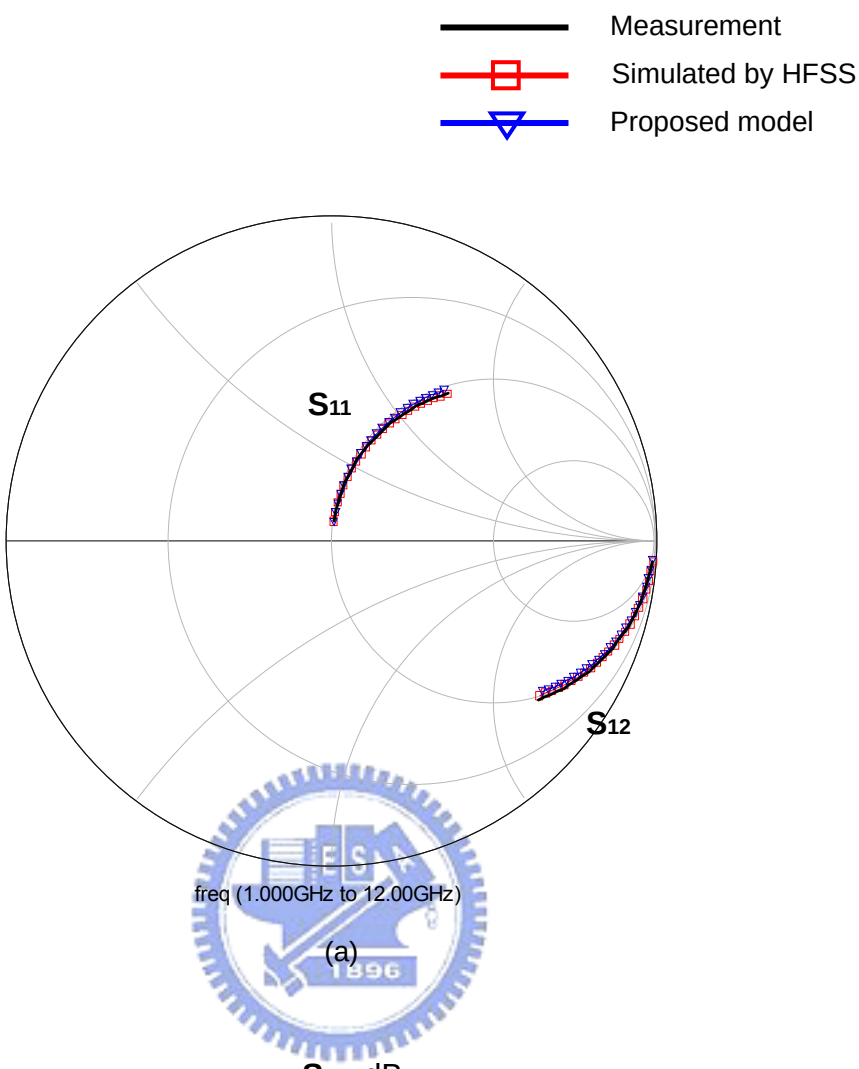
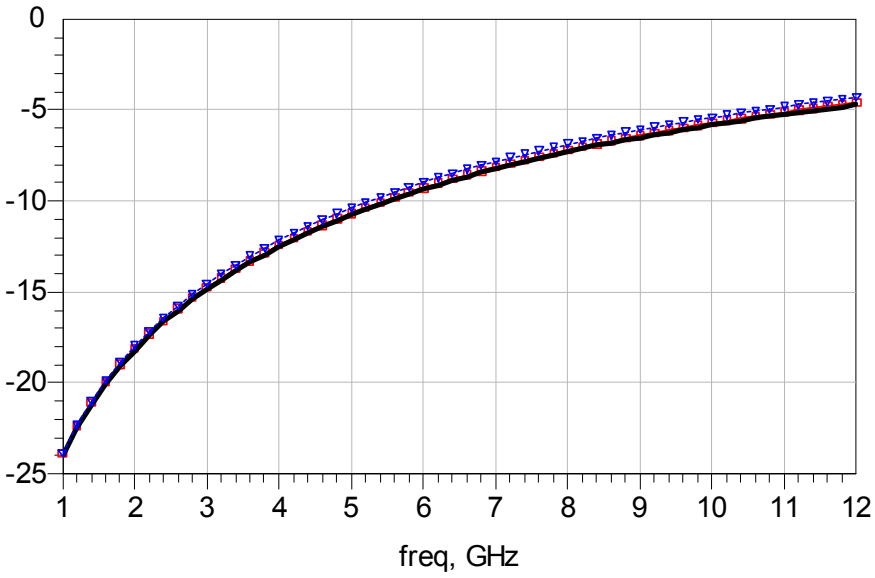


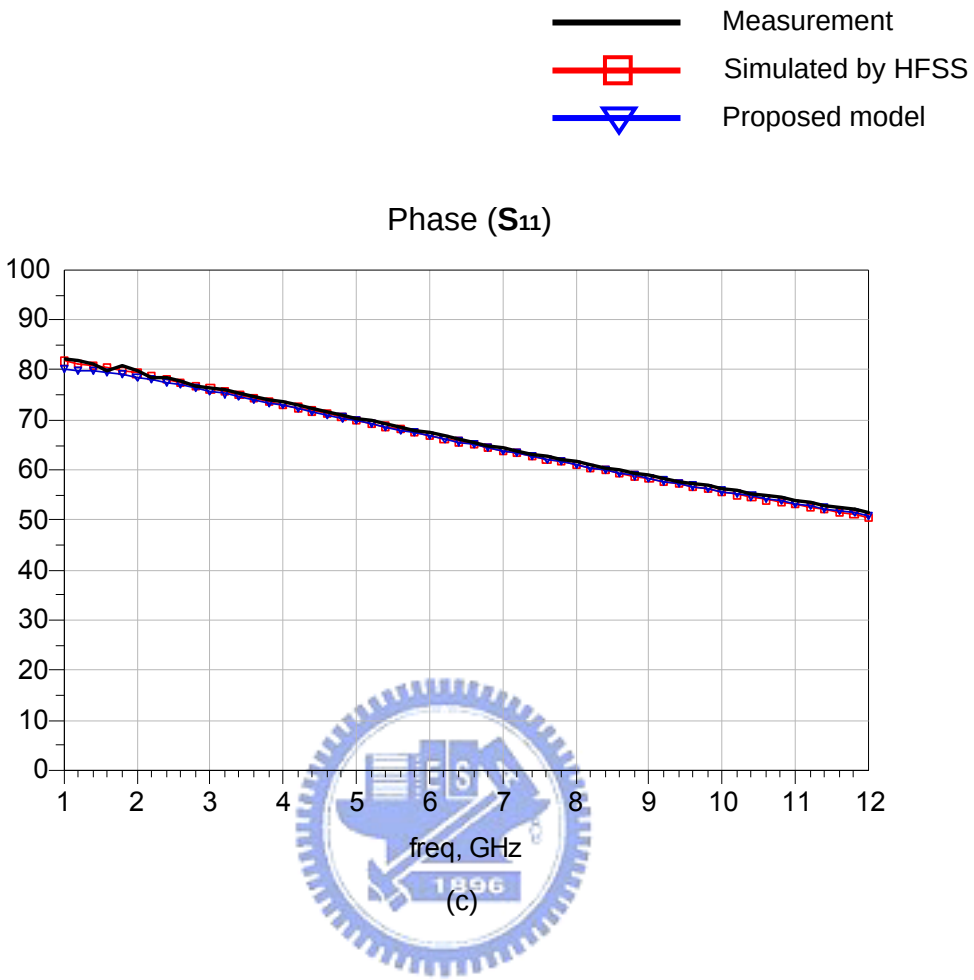
Fig. 5-2 The summary of comparison for a 2.3 nH micro-machined inductor. (a) **S11** and **S12** on Smith Chart. (b) **S11**. (c) Phase of **S11**. (d) **S12**. (e) Phase of **S12**. (f) The inductance and quality factor.


Measurement
Simulated by HFSS
Proposed model
S11
S12
freq (1.000GHz to 12.00GHz)

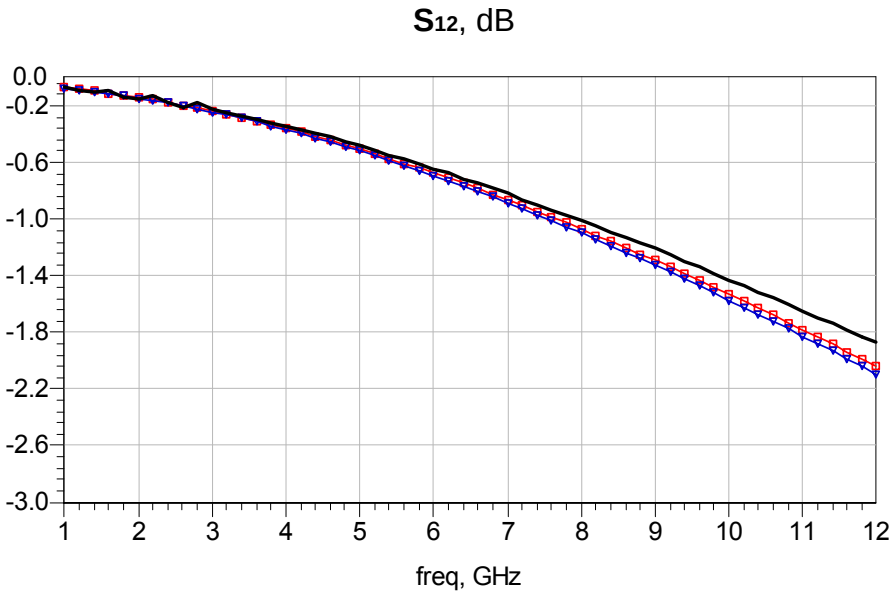
(a)


S11, dB
0
-5
-10
-15
-20
-25
1
2
3
4
5
6
7
8
9
10
11
12
freq, GHz

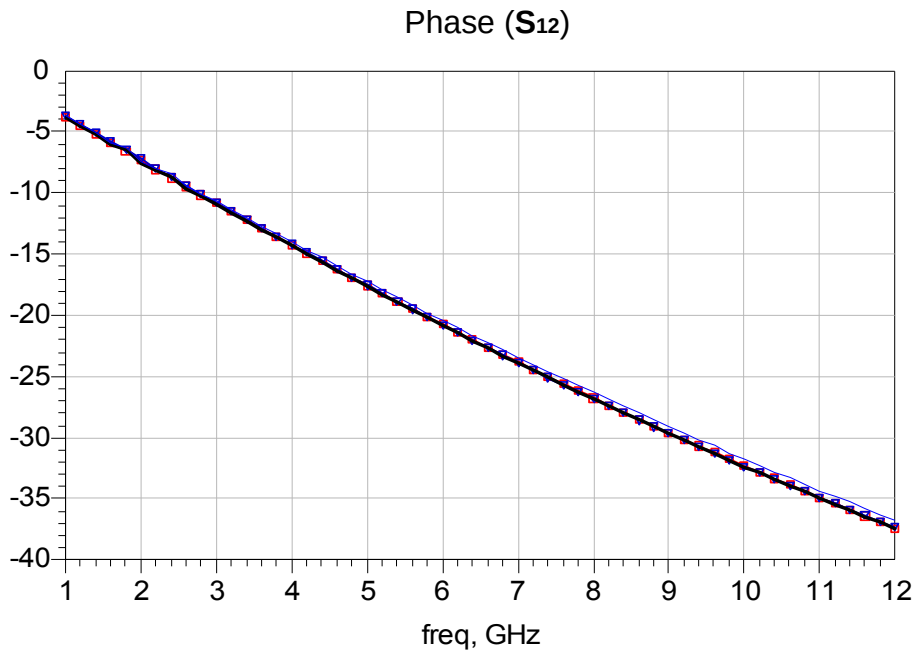
(b)


Measurement
Simulated by HFSS
Proposed model
Phase (S11)
100
90
80
70
60
50
40
30
20
10
0
1
2
3
4
5
6
7
8
9
10
11
12
freq, GHz

(c)


S12, dB
0.0
-0.2
-0.6
-1.0
-1.4
-1.8
-2.2
-2.6
-3.0
1
2
3
4
5
6
7
8
9
10
11
12
freq, GHz

(d)



(e)

Fig. 5-3 The summary of comparison for a 1.1 nH micro-machined inductor. (a) **S11** and **S12** on Smith Chart. (b) **S11**. (c) Phase of **S11**. (d) **S12**. (e) Phase of **S12**.

Figure 5-2 and 5-3 show the performances of micro-machined inductor with 2.3nH and with 1.0nH on S-parameters, respectively. Apparently, the proposed model can perform as accurately as 3-D electromagnetic simulator with less than 5% error for 1GHz to 10 GHz. However, as the operating frequency exceeds 10 GHz, the dominantly parasitic effects, such as the capacitive effect of membrane and residual substrate, must be concerned and modeled. In addition, figure 5.2 (f) represents that the quality factor of a 2.3 nH micro-machined inductor can be over 25 for 3 GHz to 8 GHz and the inductance is also stable for the range. Moreover, for the micro-machined inductors with smaller inductances (< 1nH), the accuracy of measured result will be greatly sensitive to the measurement technology and de-embedded method. Thus the calibration steps of measured process must be completed carefully.

5.2 Chip Assembly

A silicon carrier with four cross-membrane micro-machined inductors was fabricated and in addition, the silicon substrate underneath four micro-machined inductors and the corresponding location on the carrier of two inductors in standard CMOS process has been removed, as presented in figure 5-4. Apparently, the substrate under carrier was over etched and almost vanished. On the other hand, since the Au-Au TC flip-chip bonding must be applied a external stress to make Au-Au joining layers form, the lack of supporting will result in the collapse of overall structure during the bonding process.

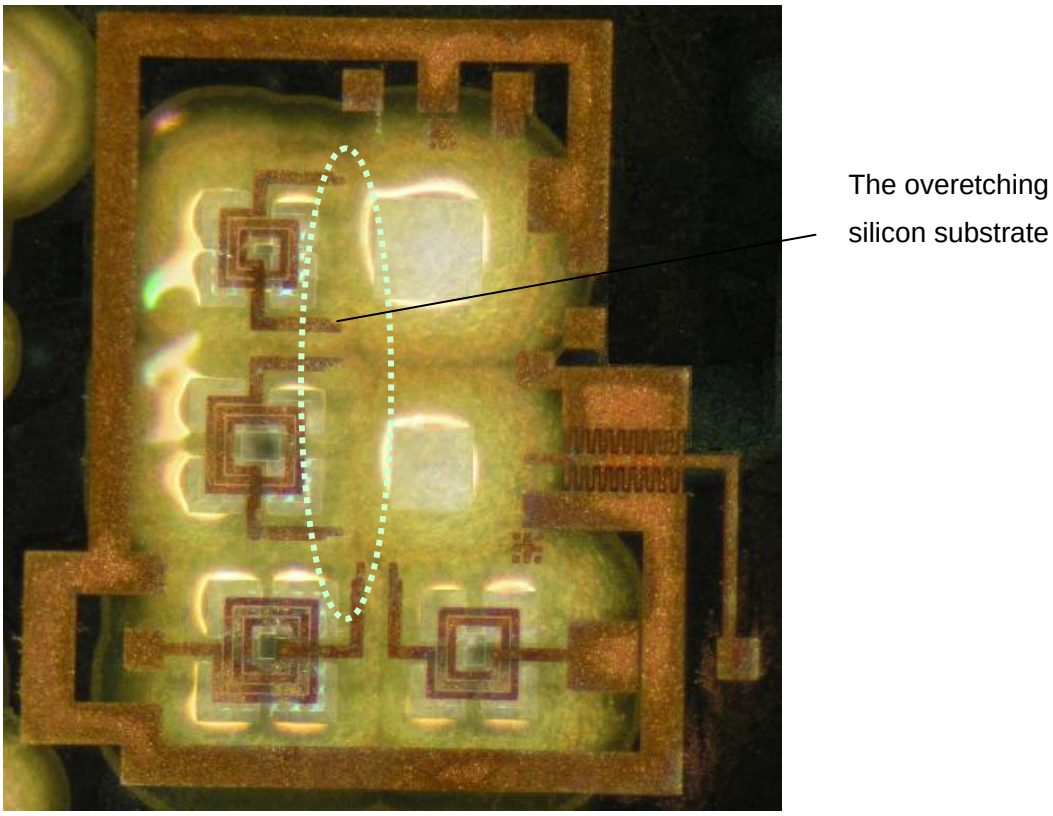


Fig. 5-4 The photograph of a silicon carrier with cross-membrane micro-machined inductors.

In order to overcome the phenomenon, the substrate etching rate which is related to the

loading factor of opening area of sandwich membrane must be thought over. Thus, the types of opening area in which the location corresponding to the inductors on LNA chip, will be redesigned to avoid the disappearance of bonding supporting. It is easy to control the substrate etching rate by making the opening area similar to that acted on micro-machined inductors, as shown in figure 5-5.

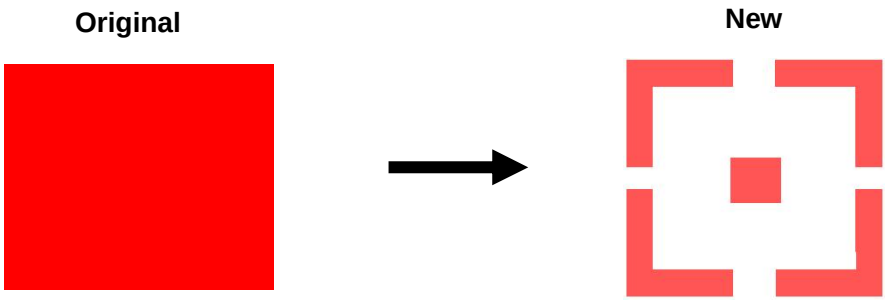


Fig. 5-5 The new type of opening area is used to control substrate etching rate well.

By means of Au-Au TC bonding, the silicon carrier will be assembled with the proposed LNA chip made in TSMC 0.18um process. Since the LNA chip is not delivered back as yet, the conceptive chart of integrated structure is temporarily shown in figure 5-5. By the chart, it is clear to know that the SOP scheme could be developed to achieve the fully-integrated UWB tunable LNA.

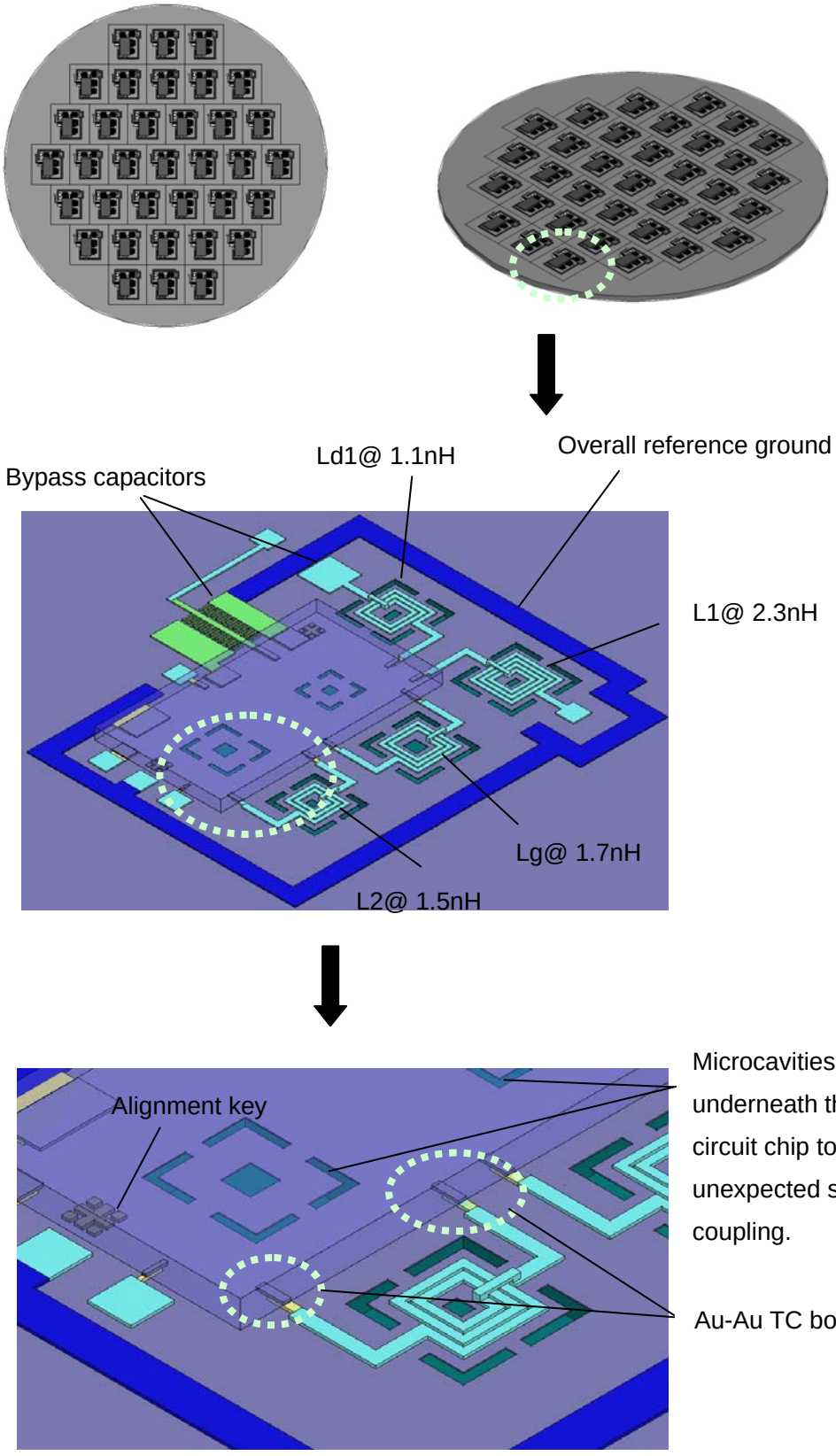


Fig. 5-6 The integration of a MEMs carrier and LNA chip using Au-Au TC bonding.