國立交通大學

電子工程學系　電子研究所碩士班

碩士論文

射頻金氧半場效電晶體於熱載子效應及氧化層崩潰時之特性化及模型化分析

Characterization and Modeling of RF MOSFETs under Hot Carrier Stress and Oxide Breakdown

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中華民國九十四年六月

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射頻金氧半場效電晶體於熱載子效應及氧化層崩潰時之特性化及模型化分析

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摘要

近年來隨著生活水準提升，無線通訊（ wireless communication）市場快速成長，無論是學術界或是工業界皆無不極力地發展無線通訊這高科技。而微波元件則是通訊系統中最重要的骨架。又由於以矽為基底的金氧半場效電晶體已經成為射頻元件的主流，所以射頻金氧半場效電晶體的可靠度分析亦變得愈益重要。

本篇論文之重點即是在研究以矽為基底的金氧半場效電晶體受到熱載子效應以及氧化層崩潰時的特性分析，此外我們也提出受到熱載子效應及氧化層崩潰時的金氧半場效電晶體小訊號模型並且討論個別小訊號參數的變化情形。

首先受到熱載子效應後的金氧半場效電晶體其高頻雜訊，功率特性以及

截止頻率受到很嚴重的破壞。這主要是因為金氧半場效電晶體的互導下降之故。另外我們可以藉著固定汲極電流來減緩熱載子效應對於金氧半場效電晶體的影響。這可以由金氧半場效電晶體在受到熱載子效應後其臨界電壓，次臨界擺幅，電子遷移率的變化來解釋。

另一方面，由於氧化層在崩潰後會產生一個漏電路徑，所以輸入端的阻抗以及反射係數會有很明顯的變化。值得注意的是金氧半場效電晶體在氧化層崩潰後會在氧化層區產生額外的散粒雜訊, 因此其最小雜訊值會劇烈地增加。

最後，透過小訊號模型的分析，我們發現金氧半場效電晶體的互導，汲極到源極的電阻以及閘極到源極的電容受到熱載子效應以及氧化層崩潰的影響較大。另外我們也確認了在氧化層崩潰後主要的漏電路徑是產生在閘極與源極或通道的重疊區域。

Characterization and Modeling of RF MOSFETs under Hot Carrier Stress and Oxide Breakdown

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Abstract

In recent years, with the improvement of living standard, the development of wireless communication has become the most important technology, not only in academic circles but also in the industries. Microwave transistors are the backbone of these modern wireless communication systems. Since the Si-based MOSFETs (metal-oxide-semiconductor field-effect transistors) have become the mainstream of RF transistors in recent years, the reliability of RF MOSFETs is more and more important.

The purpose of this thesis is to investigate the characteristics of RF MOSFETs under hot carrier stress and oxide breakdown. In addition, we proposed a small-signal model individually after hot carrier (HC) stress and oxide breakdown (OBD) and discuss the variations of each small-signal parameter.

Firstly, we found that the degradations of cut-off frequency, noise and power characteristics are very obvious after HC stress. It can be explained by the decrease of the transconductance. In addition, the degradation of linearity can be softened by biasing the transistor at constant drain currents. This experimental observation can be explained by the change of threshold voltage, transconductance, subthreshold swing, and mobility under HC stress.

Secondly, since a new leakage path is generated in the gate oxide after oxide breakdown, the input impedance and optimized input reflection coefficient suffer degradations. It is worthwhile to notice that the minimum noise figure increases dramatically after hard oxide breakdown (HBD). It can be explained by the additional shot noise source in gate oxide after HBD.

Finally, from the small-signal model, the transconductance (g_{m0}), drain-to-source resistance (R_{ds}), and gate-to-source capacitance (C_{gs}) suffer more degradation after HC stress and oxide breakdown. We also confirm that the main leakage path locates at the gate and source/channel overlap region.

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Chapter 1

Introduction

1.1 RF Transistors

Currently RF electronics is one of the fast growing parts of semiconductor industry. This is due to explosive growth in the wireless communication market in the past 10 years. However about twenty years ago, this situation was much different. During that time, RF electronics was somewhat mysterious and their applications had been mainly military (e.g. secure communication, electronic warfare system). In the 1990s, the situation changed dramatically. The new global political situation has led to considerable cuts in military budgets. Furthermore, a shift to consumer applications took place, and consumer applications clearly became dominated. Therefore, the design philosophy for many microwave systems changed from "performance at any price" to "sufficient performance at lowest cost".

Microwave transistors are used in a large number of different circuits such as low-noise amplifiers, power amplifiers, mixers, frequency converters and multipliers, attenuators, and phase shifters. Although the requirements on transistor performance differ from application to application, microwave transistors in principle can be distinguished into two groups as small-signal low-noise transistors and power transistors. For microwave electronics, on the other hand, a large variety of different semiconductor materials have been employed, such as Si, SiGe, GaAs, InP, further III-V compounds, and wide bandgap materials [1-3]. In the few years, the silicon-base MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) have become the mainstream of RF transistors.

1.2 Basic Concepts of RF MOSFETs

In the past 20 years, the silicon base MOSFETs have widely been used in VLSI (Vary Large Scale Integration) applications. However, most RF circuits and systems have been implemented either compound semiconductor transistors. It is due to that the microwave properties of silicon base MOSFETs were inferior to other high-frequency transistors. In recent years, with the fast growth in the wireless communications market, the demand for high performance and low cost RF solutions is rising. Fortunately, the continuous down-scaling CMOS technology has resulted in a strong improvement in the RF performance of MOS device [4]. The basic structure of MOSFETs, shown in Fig. 1-1, consisting of a single gate, a semiconductor substrate and a heavily doped source and drain region, has not changed in the past twenty years. Only the dimensions and other features have been scaled down continuously to meet the demands of higher speed and increased compactness. There are several criterions to determine RF MOSFETs performance such as cut-off frequency, maximum oscillation frequency, power gain, linearity, and noise figure. Table 1-1 shows the cut-off frequency, maximum oscillation frequency and minimum noise figure versus the gate length of n-channel MOSFETs. For today 50- to 100-nm gate length the cut-off frequency can achieve almost 200GHz and maximum oscillation frequency can achieve 70 GHz. The NF_{min} for 70nm gate length RF MOSFET can be reduced to 0.13 dB. In addition, very high power gain (>25dB) is possible at realistic current for the most advanced technologies [5]. The VIP3 of 70nm gate length can be lower than 0.81 V [6]. Therefore RF MOSFETs have been serious alternatively to the traditional microwave transistors. Moreover, MOSFETs offer very large scale integration and high reliability. As a result, to realize systems-on-chip, the RF operation must use RF MOSFETs to conform to the integration.

1.3 RF MOSFET Reliability Issues

1.3.1 Hot Carrier Reliability of RF MOSFETs

With the scaling MOS transistor technology, the hot-carrier (HC) reliability becomes a challenging concern while keeping a relatively high drain voltage for both the digital and analog applications. Hot carrier generation and their effects in the characteristics of MOSFETs have been known for a long time [7-9]. It is a result of the high electric fields present inside the MOSFET which naturally appear when high biasing voltages are applied to a short-channel device. The general damages from the hot-carriers on a MOS transistor include the shift of the threshold voltage, the drain current degradation and the decreasing transconductance. Because the RF circuits are sensitive to the parameters of their components [10], HC effects are also important in RF circuit design.

1.3.2 Effects of Oxide Breakdown on RF MOSFETs

Due to the scaling of the SiO_2-based gate dielectric in MOSFET, the time to the first oxide breakdown reduces hugely. The chip reliability margin shrinks significantly. Therefore, ultra thin gate-oxide reliability is an urgent issue in deep-submicron silicon CMOS integrated circuit technology. Traditionally, the occurrence of a first gate-oxide breakdown event is considered as a failure for MOSFETs. However, when the gate-oxide is ultra thin, the first breakdown event is most likely to be a soft breakdown. As long as the inversion layer is formed in the channel, the device will still work functionally. In fact, even when hard breakdown happens, MOSFETs may not fail. However, those post-breakdown will generate many defects near oxide-semiconductor interface. Moreover, there will be a small spot of breakdown path through the gate oxide after hard breakdown. These phenomenon cause device parameters shift and change the oxide conduction.

1.4 Organization of the Thesis

In Chapter 2, we will explain the physical mechanism of hot carriers and oxide breakdown. Then we will introduce different measurement methods that are use to measure s-parameters, noise characteristics and power characteristics of RF MOSFETs. In Chapter 3, we will discuss HC effects on the RF behaviors of MOS transistors. Then we will discuss the effects of oxide breakdown on FOM of RF MOSFETs in Chapter 4. In Chapter 5, we will establish the small-signal models of MOSFETs under HC stress and oxide breakdown and discuss the degradations of each model parameters. For the device model after hard breakdown, some external components will be added into the conventional model to discuss the shift of model parameters of RF MOSFETs after oxide breakdown. Finally, some conclusions will be given in Chapter 6.

Year	1995	1997	1999	2001	2003	2005	2007	2009
L(nm)	250	180	140	120	100	70	50	35
f_T (GHz)	33	49	70	84	112	145	205	420
f_{max} (GHz)	41	47	51	52	60	62	68	85
NF_{min} (dB)	0.5	0.35	0.23	0.2	0.15	0.13	0.1	0.08

Table 1-1: Performance of CMOS technology in several generations.

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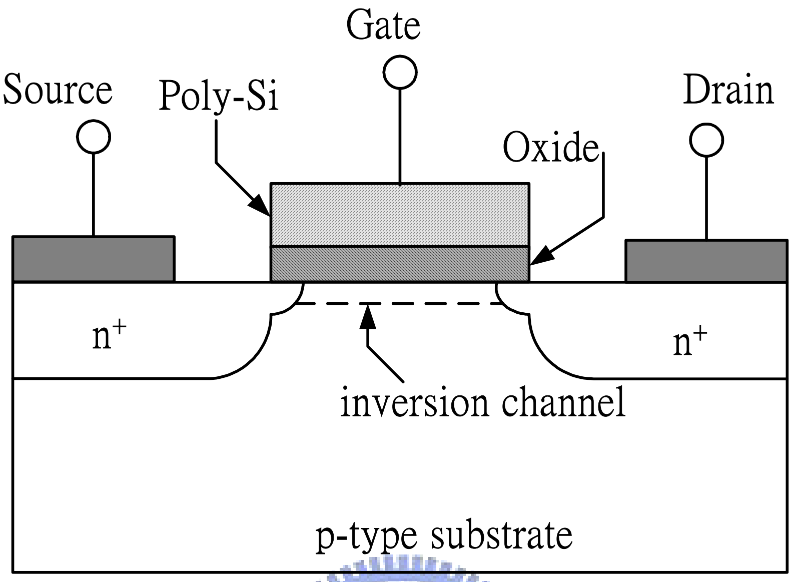


Fig. 1-1: Schematic of a typical bulk MOSFET structure.

Chapter 2

Basic Theory and Experiments

2.1 Hot Carriers Mechanism

Hot Carriers are a result of the high electric fields inside the MOSFETs when high biasing voltages are applied to a short-channel length device. Electrons in the inversion layer can get high energies in the high electric field. It is possible that carriers with high energy (i.e. hot carriers) have sufficient energy to overcome the potential barrier between the silicon and silicon dioxide and penetrate into the gate oxide. Some of them may get stuck inside the gate oxide at the defect sites or traps, denoted by N_{ox}. Hot carriers also can break the atomic bonds at the interface of the silicon substrate and the gate oxide and generate new traps which are called interface traps, denoted by N_{it}. The difference between these two types of traps is that interface traps can be in charge exchange with channel whereas the oxide traps cannot be in direct charge exchange with charges in the channel. These two types of traps will degrade the quality of gate oxide and affect the device electric parameters.

As shown in Fig. 2-1(a), when the MOSFET is operated in the saturation region, the channel electrons will gain high energy on their way from source to drain and penetrate into gate oxide. The hot carriers are called channel hot electrons (CHE). The event of a carrier gaining energy and entering the gate oxide is a statistical phenomenon. The maximum numbers of hot carriers which penetrate into gate oxide occur when $V_G \cong V_D$ [11].

Another effect that can be caused by energetic carriers in the channel is that carriers on the way toward drain collide with lattice atoms and generate new electron-hole pairs. These electron-hole pairs can also gain high energy in the electric field and produce new electron-hole pairs, similar to avalanche process in a reversed biased p-n junction. This process is called drain avalanche hot-carriers (DAHC), which is shown in Fig. 2-1(b). During the same process, the energetic carriers can impinge on the atomic bonds at the interface of the substrate and gate oxide or inside the oxide, and break them. Therefore new electronic states N_{it} are created at the interface. In an NMOSFET, the extra electrons generated in avalanche process are absorbed by drain, and the extra holes are absorbed by substrate terminal which form the substrate current component I_{sub}. It is known that generation of electron-hole pairs in an avalanche process is proportional to both strength of electric field and the number of primary carriers initially flowing in the channel. For low values of V_G above the threshold, the transistor is in deep saturation and a pinch-off region is formed near the drain which results in a strong lateral electric field in that region. Also at low values of V_G the drain current is low. As V_G increases, Id increases, but transistor comes out of saturation region gradually. This causes that a maximum value for I_{sub} appears at some particular value of V_G. It is reported that at $V_G \cong \frac{1}{2} V_D$ the maximum I_{sub} is generated in MOSFETs [12].

The third mechanism of hot carriers is called substrate hot electrons (SHE). Unlike the cases of CHE and DAHC, which were caused by lateral electric field in the channel, SHE is caused by the vertical electric field between gate and the substrate. As shown in Fig 2-2(c), the electrons which are thermally generated in the region below the gate, drift toward the silicon-silicon dioxide interface and gain kinetic energy in the electric field below the gate. Some of these electrons penetrate into oxide and cause a uniform distribution of trapped charge in the oxide. SHE is not a major problem in short channel devices as most of the electrons are absorbed into source and drain region and a smaller fraction of them reaches the device surface, compared to the long channel devices.

2.2 Oxide Breakdown Mechanism

Generally, in advanced MOS devices, there are two breakdown mechanisms observed in dielectric materials. One is called HBD (Hard-Breakdown) and has a permanently distortion in gate oxide dielectric. It results in a dramatic increase of the output currents due to the increasing gate leakage current. The other breakdown mechanism is called SBD (Soft-Breakdown), and the breakdown process shows smoothly and slightly. The physical mechanism involved in, and leading to, the dielectric breakdown process are very complex. They involve impact ionization in the oxide layer, injection of holes from the anode, creation of electron-hole pairs in the oxide, electron and hole trapping, creation of surface state at the oxide-silicon interface, and the interaction of many or all of these process.

The mechanism of tunneling into an electron trap can be explained by Fig. 2-2(a). As electrons tunnel into an oxide layer, some of the electrons can get trapped. The trapped electrons modify the oxide field so that the field near the cathode is decreased, while the filed near the anode is increased. Hence the tunneling current will reach a stable value in Soft Breakdown.

As electrons travels in the conduction band of an oxide layer, it gains energy from the oxide filed. If the voltage drop across the oxide layer is larger than the band-gap energy of silicon dioxide, the electron can get enough energy to cause impact ionization. As shown in Fig. 2-2(b), when a tunneling electron arrives to the anode, it could cause impact ionization in the anode near oxide-anode interface. Depending on the energy of the tunneling electron, the hole thus generated could be from deep down in the valence band, and thus could be “hot”, a hot hole in the silicon–oxide interface can have a high probability of been injected into oxide layer. On the other hand the injected hole can be trapped in the oxide layer as it travels towards the cathode.

The trapped holes in the oxide layer cause an increase in the oxide field near the cathode and a decrease in the oxide field near the anode. This could be illustrated in Fig. 2-2(c). According to the F-N tunneling equations:

$$J_{FN} = \frac{q^3 E_{OX}{}^2}{16\pi\hbar\phi_{OX}} \exp\left(-\frac{4\sqrt{2m^*}\phi_{OX}{}^{3/2}}{3\hbar q E_{OX}}\right) \qquad (2\text{-}1)$$

A small increase in the oxide field near the cathode can cause a large increase in the tunneling current. Thus, hole-trapping in the oxide near the cathode provides positive feedback leading to the electron tunneling process. Dielectric hard breakdown occurs when the positive feedback leads to a run away of the electron tunneling current at some local weak spots of the oxide [13]. It appears as a current prominence in current-versus-time plots.

2.3 Device under Test and Measurement Techniques

2.3.1 Device under Test

The MOSFETs are n type MOSFETs in P-well. Multi-finger MOS transistors used in this work were fabricated using a 0.13 μm baseline technology with channel L=0.12 μm and two different sizes of channel width W=3.6 μm×22(number of fingers)×2(multiplier) and 3.6 μm×4(number of fingers)×8(multiplier) . The gate oxide thickness is 20 Å.

2.3.2 I-V Measurement

The DC characterizations and stress experiments of RF MOSFETs were performed using Agilent 4156B precision semiconductor parameter analyzer. From the I_D-V_G curve, we extract the threshold voltage (V_{TH}), and transconductance (g_m=dI_D/dV_G).

2.3.3 High Frequency Characteristics Measurement

For microwave devices, the high frequency characteristics are generally obtained by the measurement of the s-parameters. In this work, on-wafer s-parameters measurement was carried out from 0.1 to 50.0 GHz using microwave coplanar probes and HP 8510C Network Analyzer. On-wafer dummy structures were used to de-embed the pad parasitics. Then, the de-embedded parameters were transformed to the H, Z or Y parameters to extract the desired parameters.

2.3.4 RF Noise Measurement

The ATN NP5 system was used for high frequency noise measurement in this study. It includes the instruments of dc measurement system, small-signal s-parameter system and noise power measurement system. The schematic and block diagram is shown as Fig. 2-3. The NP5 system consists of a mainframe controller and two remote modules suitable for mounting on a wafer probe station. The port 1 (input) module, the Mismatch Noise Source (MNS), contains the solid state electronic tuner with a built-in bias tee and switching circuitry. The port 2 (output) module, the Remote Receiver Module (RRM), contains a bias tee, switching circuitry, and a low noise amplifier.

Noise figure is often a simplified model of the actual noise in a system, where a single, theoretical noise element is assumed in each stage. Designing low-noise microwave circuits and systems involves trade-offs between the available gain of a stage and its corresponding noise figure. Making design decisions requires knowledge of how an active device's gain and noise figure change as a function of the source reflection coefficient. In general, noise parameters and gain are independent, requiring separate device characterization. Gain can be determined from S-parameters. A noise parameter characterization must vary the source reflection coefficient presented to the device by using a special tuner.

The dependence of noise factor on source impendence is shown as the following equations.

$$F = F_{\min} + \frac{4R_n}{Z_0}\left(\frac{\left|\Gamma_{opt} - \Gamma_S\right|^2}{\left|1+\Gamma_{opt}\right|^2\left(1-\Gamma_S{}^2\right)}\right) \tag{2-2}$$

F = Noise factor of the DUT

$F_{\min}$ = Minimum noise factor of the DUT that occurs at $\Gamma_{opt} = \Gamma_S$

R_n = Noise resistance (the sensitivity of noise figure to source admittance changes)

Γ_S = Source reflection coefficient that results in the noise factor F

Γ_{opt} = Optimum source reflection coefficient for minimum noise factor

The associated gain provided by a device when it is driven by a specific source impedance and can be calculated from the S-parameters of the device and the source reflection coefficient. The associated gain as a function of source impedance is:

$$G_a = \frac{(1-\left|\Gamma_S\right|^2)\left|S_{21}\right|^2}{\left|1-S_{11}\Gamma_S\right|^2(1-\left|S_{22}+\frac{S_{21}S_{12}\Gamma_S}{1-S_{11}\Gamma_S}\right|^2)} \tag{2-3}$$

2.3.5 Output Power Measurement

We used the load-pull system (ATN LP1 measurement system) to measure and discuss power characteristics and linearity in our study. The functions of this load-pull system perform power discussions on output power, power gain, power added efficiency (PAE), and inter-modulation distortion. The configuration of a load-pull system is shown in Fig. 2-4(a).

By load-pull test, the output power is measured and plotted as a function of the complex load seen by the transistor. Since a complex load requires two axes, the plot actually appears as constant power contours on a complex impedance plane, for example, a Smith chart. A variable, precisely calibrated tuner operates as a matching network, presenting various complex impedances to the transistor according to a control input. With the aid of an automated system, the real and imaginary parts of Z_1 are gradually varied such that the power meter maintains a constant reading. The result is the contour corresponding to that power level shown in Fig. 2-4(b). When Z_1 arise so does Z_{in}, necessitating the use of the tuner between the signal generator and the transistor to ensure that the impedance seen by the generator remains constant.

If the power delivered to the input is constant, the output power increases as Z_1 approaches its optimum value, Z_{opt}. This trend is accompanied by a narrower range for Z_1, resulting in the tighter contours and eventually a single impedance value, Z_{opt}, as the output reaches its maximum level, P_{max}. In other words, the load-pull test systematically narrows downs the values of Z_1 so as to obtain both the maximum output power and corresponding load impedance. The load pull system can also calculate intermodulation distortion using two-tone frequency test.

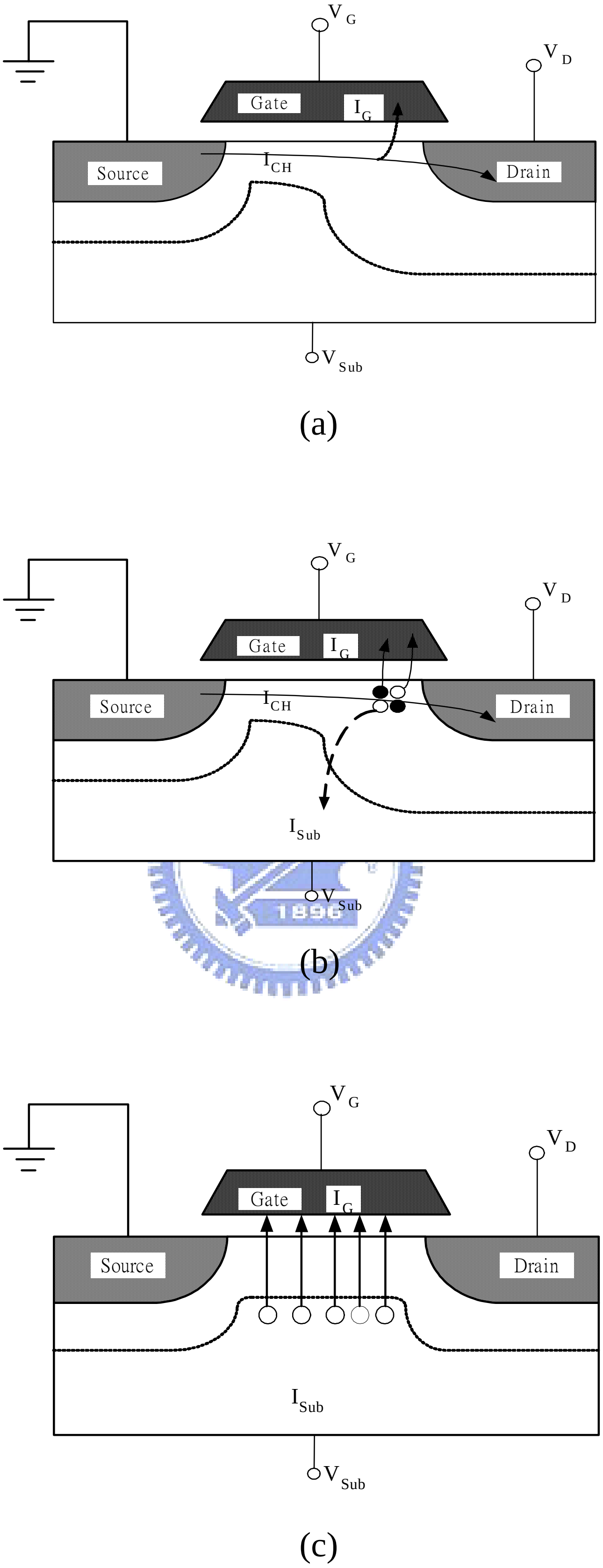


Fig. 2-1: (a) Channel hot electrons (b) Drain avalanche hot carriers
(c) Substrate hot electrons

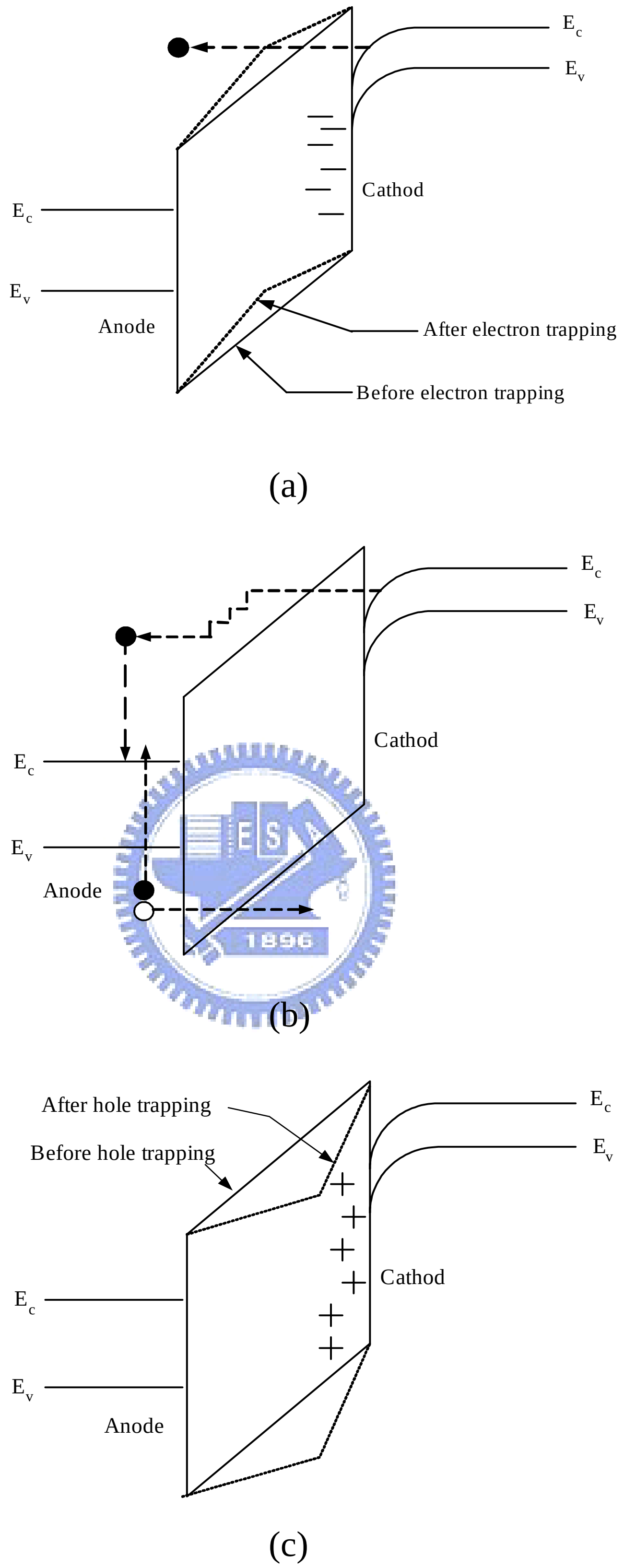
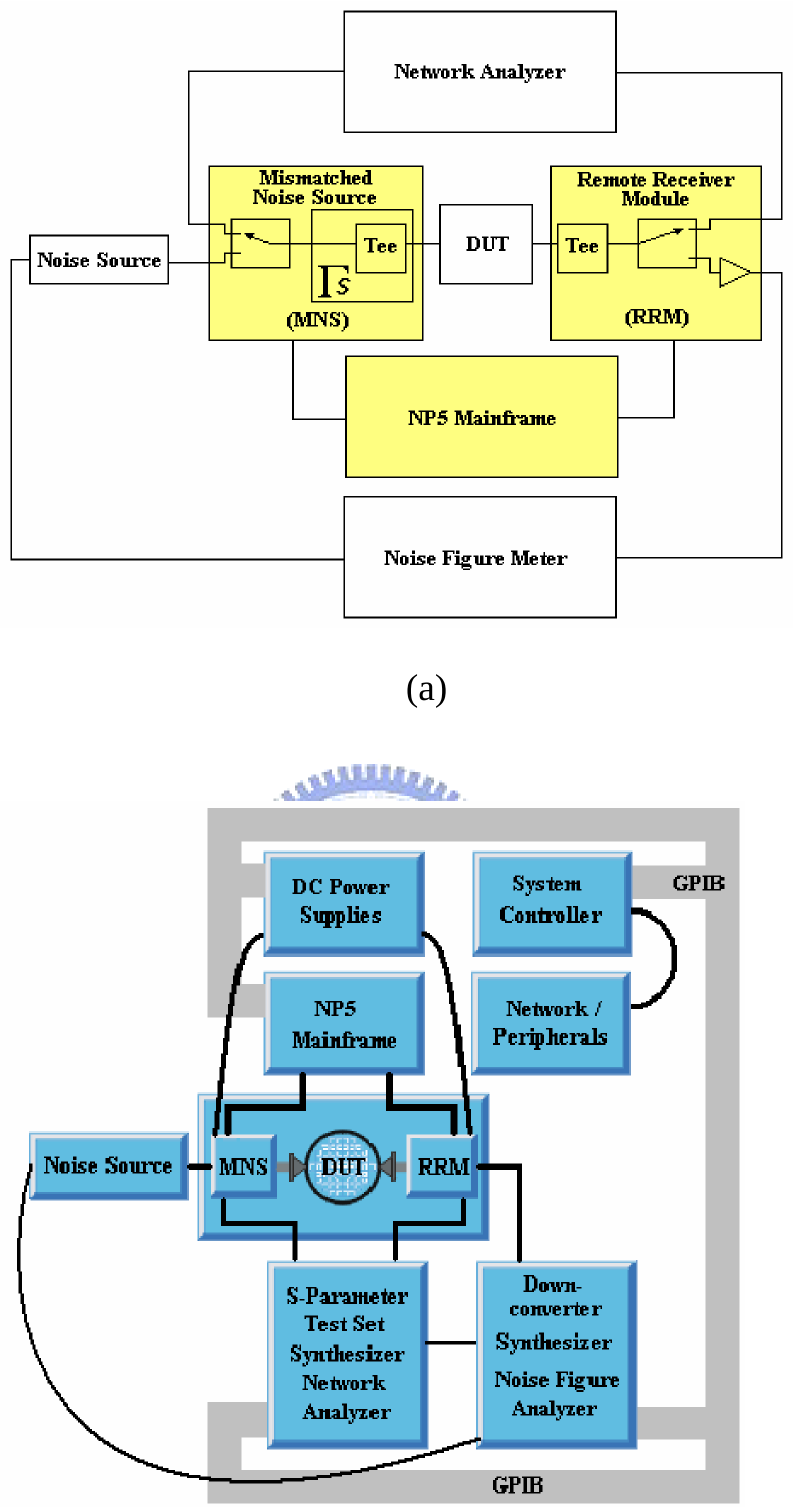


Fig. 2-2: (a) Schematic illustrating the trapping of tunneling electrons.
(b) Schematic illustrating the generation of an electron-hole pair in the anode by a tunneling electron.
(c) Schematic illustrating the trapping of holes in the oxide. layer.



(a)

(b)

Fig. 2-3: The schematic and block diagram of the RF noise measurement system.

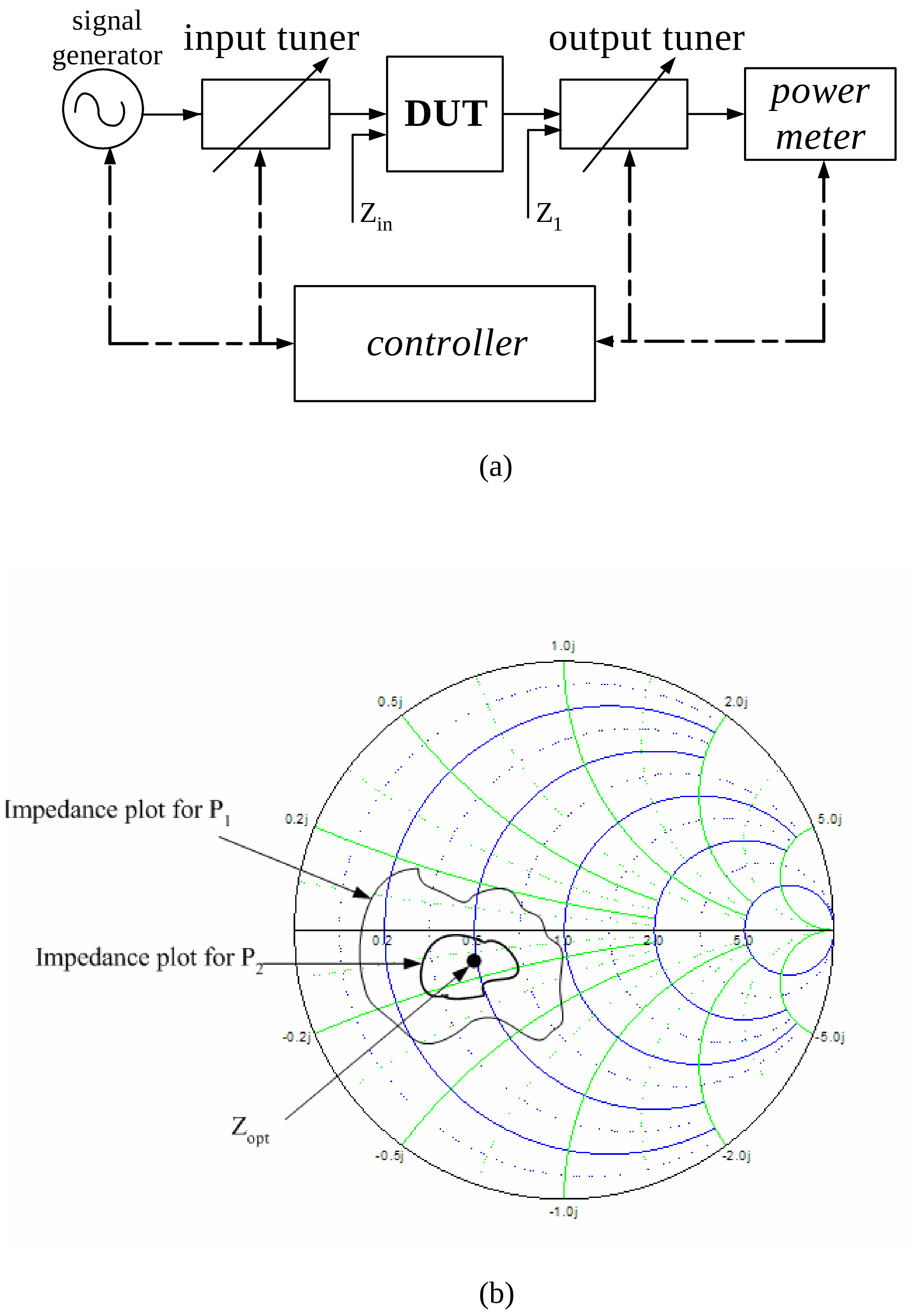


Fig. 2-4: (a) Block diagram of the load-pull measurement system.
(b) Power contours on a Smith chart.

Chapter 3

Characteristics of RF MOSFETs under Hot Carriers Stress

In this chapter, the effects of HC stress on DC characteristics of RF MOSFETs will be discussed in the beginning. In general, the degradations are quite different by using different stress method and in our experiments we found that the degradations are more serious under drain avalanche hot carrier (DAHC) stress. After then we discuss HC effects on the S-parameters, we found that the values of S_{22} and S_{21} are degraded seriously. It implies that the output impedance and voltage gain are influenced after stress. Finally, we focus on the changes of the main figures of merit (FOM) of RF MOSFETs after HC stress. It shows that the degradations of noise and power characteristics are obvious due to the HC stress effect.

3.1 HC Stress Experiments

In our experiments, the channel length and total width of MOSFETs are 0.12 μm and 158.4 μm, respectively. For DAHC stress, the gate and drain of the test transistors were biased at 1.2V and 2.4V, respectively. For channel hot electron (CHE) stress, the gate and drain of the test transistors were both biased at 2.4V. The DC characteristics and S-parameters were measured by every 1000 seconds during the stress process. The final stress time is terminated at 7000 second.

3.2 Effect of HC Stress on DC Characteristics

The general effects of the HC stress on the dc characteristics of a MOSFET are shown in

Fig. 3-1. It shows no noticeable variations for device under CHE stress as illustrated in Fig. 3-1(a). Therefore the channel hot electrons just slightly influence the DC characteristics of MOSFETs. On the contrary, it shows a large degradation for device measured after DAHC stress shown in Fig. 3-1(b). Hence the degradations caused by drain avalanche hot carriers are much larger compared to channel hot electrons. Therefore in the following discussion we will focus on the degradations of MOSFET caused by DAHC stress. After DAHC stress, the degradation of saturation drain current in our experiments is about 17%, and the threshold voltage is shifted from 0.45 V to 0.52 V. In Fig 3-1(b), the transconductance (g_m) reduces significantly, and the maximum value shifts to higher gate voltages after HC stress. We also found that g_m and drain current reduction is more serious in low gate bias region and this phenomenon is possibly due to the interface state generation and the oxide trap charge [14][15].

3.3 HC Effects on S-parameters

As shown in Fig. 3-2, the values of S_{11} and S_{12} are almost unchanged with increasing HC stress time. It implies that the input reflection coefficient and isolation of the RF MOSFETs are affected slightly by HC stress. On the other hand, S_{22} and S_{21} changed more obviously after HC stress. The degradations of S_{22} and S_{21} can be explained by the decrease of transconductance and the increase of the output drain conductance. It also implies that the output reflection coefficient and the voltage gain of the RF MOSFET are affected seriously after HC stress. It is worthwhile to pay attention to the degradation of S_{22} when biasing at lower gate voltages. With increasing stress time, the degradations of low frequency value of S_{22} have different trends. The low frequency value of S_{22} strongly depends on the output impedance. After HC stress, there are a lot of defects generated by impact ionization near the drain region and those defects provide acceptor states in NMOSFETs [16]. Therefore the electric field near the drain region will increase and the drain current is more controlled by V_D. Therefore the output impedance decreases while biasing at high V_G shown in Fig. 3-3. However while biasing at low V_G, due to the reduction of the depth of depletion region, the output impedance decrease more slightly initially. After a long period of stress time, the increase of oxide trapped charge raise the threshold voltage dramatically shown in Fig. 3-4, so the output impedance becomes to increase shown in Fig. 3-3. Therefore the degradations of low frequency value of S_{22} have different trends with increasing stress time at low V_G bias condition.

3.4 Effects of HC Stress on Cut-off Frequency and Maximum Oscillation Frequency

The cut-off frequency is defined as the transition frequency at which the small-signal current gain of a transistor with common source configuration and short-circuit load drops to unity. As shown in Fig. 3-5(a), the cut-off frequency drops off conspicuously after HC stress. By using the small-signal equivalent-circuit model, the cut-off frequency (f_T) can be approximated as:

$$f_T \cong \frac{g_m}{2\pi(C_{gs}+C_{gd})} \qquad (3\text{-}1)$$

From above equation, f_T is related with g_m and gate-to-source capacitance (C_{gs}). After HC stress, there are many interface states generated near the oxide and semiconductor interface. Therefore C_{gs} increased after stress. In addition, from discussions in Section 3-2, g_m reduced significantly after HC stress. Due to the increase of C_{gs} and the decrease of g_m, f_T reduced dramatically after HC stress. By the observation of Fig. 3-5(a), it also suggested that the degradation of cut-off frequency is more robust to HC stress when biasing at higher gate voltages which is similar to the degradation of g_m.

As shown in Fig. 3-5(b), maximum oscillation frequency (f_{max}) also decreases after HC stress. The maximum oscillation frequency is defined as the transition frequency at which the unilateral gain of a transistor with common source configuration drops to unity. It can be approximated as:

$$f_{\max} \cong \frac{f_T}{2\sqrt{2\pi f_t C_{gd} R_g + G_{ds} R_{in})}} \qquad (3\text{-}2)$$

Because the maximum oscillation frequency is approximately proportional to the cut-off frequency, the degradations are correlated to the cut-off frequency. Therefore, f_{max} decreased after HC stress and the degradation is more serious while biasing at low V_G which is similar to the degradation of f_T.

From Fig. 3-5, we compared the RF performance degradation with the DC performance degradation. The degradations of f_T and f_{max} are proportional to the g_m degradation which can be explained by equation (3-1) and (3-2). Comparing the slopes of these two lines in Fig 3-6, the degradation of f_T is much larger than of f_{max}. Since f_{max} is proportional to $g_m^{1/2}$, it is less sensitive to HC stress.

3.5 HC Effects on Power Performance

The effect of HC stress on the output power of a MOS transistor is shown in Fig 3-7. It was measured at gate voltage V_{GS}=0.8 V and drain voltage V_{DS}=1.2 V, where g_m is the maximum value in device saturation regions, and the frequency was operated at 2.4 GHz. The source and load impedances are matched for maximum output power before stress. Because the fundamental output power of a MOS transistor is basically correlated to g_m/g_{ds}, the HC-induced degradation of the dc parameters will lead to a reduction of output power and gain. After HC stress the output conductance has changed, the load impedance will deviate from the maximum output power condition, making the further reduction of output power. In Fig. 3-8, it shows the power gain as a function of gate voltage biases. The power gain reduces after HC stress. However, as the gate voltage bias increases to a higher value, the power gain which was degraded by the HC effect shows a consistent value with the fresh one. As the source and load impedances are matched for maximum output power, the available output power gain can be expressed as:

$$G_{a,\max} = \frac{f_T^{\,2}}{4f^2(2\pi \cdot f_T \cdot R_g \cdot C_{gd} + G_{ds} \cdot R_{in})} \tag{3-3}$$

We can find the maximum available power gain is proportional to f_T which is correlated to g_m. Therefore after HC stress, the power performance in Fig. 3-8 shows a consistent curve with the transconductance in Fig. 3-1. It also suggested that biasing at a higher gate voltage is more robust to HC stress. However, in order to reduce static power consumption in analog/RF applications, they are going to be biased at much lower V_{GS} than digital devices thus are more vulnerable to HC stress.

3.6 HC Effects on Linearity

To characterize the linearity, the third-order intercept point (*IP3*), at which the output power and third-order intermodulation (IM3) power are equal, is commonly used. For low distortion operation, the third-order intercept point should be as high as possible. As shown in Fig. 3-7, by the two tone test, the output *IP3* (*OIP3*) reduces from 21 dBm to 19.22 dBm after HC stress, while the input referred *IP3* (*IIP3*) reduces from -2.27 dBm to -3.55 dBm. Hence, the RF linearity degrades under HC stress when the MOSFET operates at a fixed gate bias.

The third-order point of gate voltage amplitude (VIP3), where the fundamental and IM3 output amplitude of drain current are equal, is a good indication of device linearity even at high frequency [17] and a large VIP3 is required for high linearity. In addition, it is easily obtained from the DC characteristics [17]. Therefore we use this parameter to explain the impact of HC stress on linearity of RF MOSFET. The definition of VIP3 can be given as:

$$VIP3 = \sqrt{\frac{4g_m}{3g_{m3}}} \tag{3-5}$$

where g_{m3} is the third-order Taylor expansion coefficient of drain current versus gate voltage. The parameters, g_m and g_{m3}, can be directly extracted from the dc characteristics. Actually, the equation (3-5) is obtained without considering the non-linearity of output conductance. Because the amount of output conductance non-linearity is much smaller than that of transconductance when devices operate in saturation region, it can be negligible for low load impedance condition [17], [18]. Fig. 3-9 shows the *VIP3* measured with V_{GS} -V_{TH} (V_{TH} is the threshold voltage) of a MOSFET before and after stress. With a fixed $V_{GS} - V_{TH}$ bias condition, we can ignore the shift of the threshold voltage, and observe that the *VIP3* shows a slightly change after stress with a typical analog bias conditions, i.e. 0.1V< $V_{GS} - V_{TH}$ < 0.6V. It indicates that the degradation of linearity after stress at a constant gate bias condition is mostly due to the shift of threshold voltage. The observation in Fig. 3-9 is interesting and indicates that although the hot carrier stress affects the transconductance and threshold voltage of the device, its effects on linearity of the transistor can be alleviated as $V_{GS} - V_{TH}$ is kept at a constant. That is to say, RF linearity is less affected by HC stress if biasing the MOSFET at constant drain currents as shown in Fig 3-10. We find that *OIP*3 and *IIP*3 only show a slightly change after stress for the device measured at a fixed output drain current. It is noted that *OIP3* decreases slightly on middle drain currents due to decrease of the power gain after stress.

From Fig 3-9, we observe the *VIP3* increases after HC stress at low bias condition, which can be explained by the increase of linearity at lower drain currents. Because the HC stress will affect the threshold voltage, channel mobility, subthreshold swing, and source/drain resistance, their effects on *VIP3* have to be studied. In general, the effective channel mobility in strong inversion region can be expressed as:

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{GS}-V_{TH})} \tag{3-6}$$

where μ_0 is the low field mobility and θ is the mobility degradation coefficient due to high electric field. From the simulated results of an I-V model [19], we found that the most important parameters affecting *VIP*3 at fixed $V_{GS} - V_{TH}$ are subthreshold swing (S.S.) and θ, as shown in Fig 3-11. With increasing S.S., *VIP*3 will increase in weak inversion region. With reducing θ, *VIP3* will increase at 0.05 V < $V_{GS} - V_{TH}$<0.2 V, and decrease at $V_{GS} - V_{TH}$ >0.2 V. It should be noted that μ_0 has no effects on *VIP*3. This is because μ_0 contributes equally to g_m and g_{m3}, so its effects are cancelled out in g_m/g_{m3}. The observation in Fig. 3-11 can also be predicted by Volterra series calculation as reported in [20]. For the transistor in our work, after HC stress, S.S. increases from 82.6 to 92.6 mV/decade, and θ decreases from 1.54 to 0.68 V^{-1} (see the inset of Fig. 3-9), so *VIP*3 increases in the low bias region, as shown in Fig. 3-9.

3.7 HC Effects on Noise Characteristics

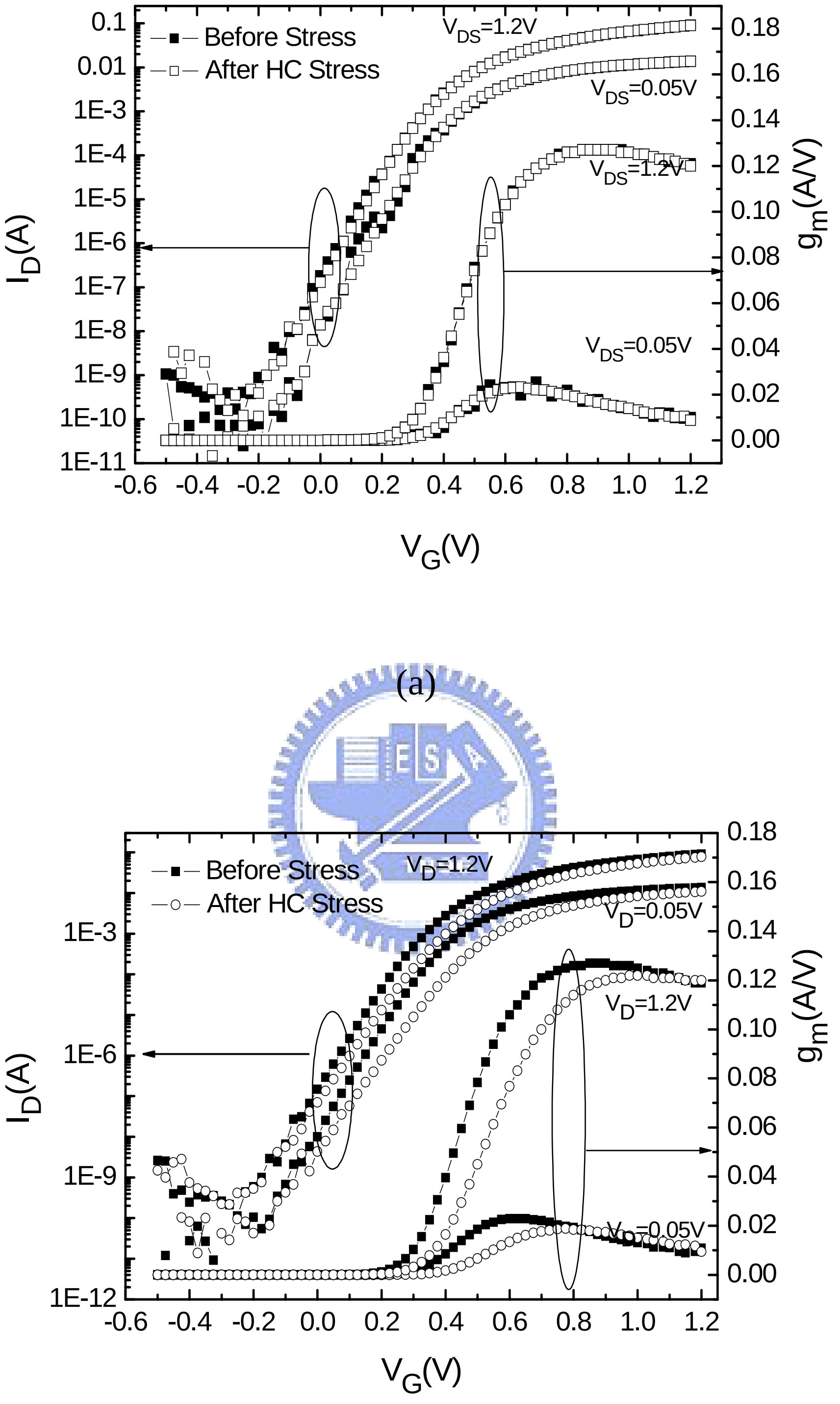
To characterize the noise characteristics, three noise parameters have been analyzed. If the noise contribution of source resistance of the MOSFET was neglected, we can use the compact model shown in Fig. 3-12 to approximate these parameters as [21]:

$$R_n \approx R_g + \frac{WC_{OX}\mu_{eff}}{2g_m{}^2} \times \frac{1}{L_C} \tag{3-7}$$

$$NF_{\min} \approx 1 + 2[(\frac{f}{f_T})^2 \frac{WC_{OX}\mu_{eff}(V_{gs}-V_{th})R_g}{2L_C} + (\frac{f}{f_T})\sqrt{\frac{WC_{OX}\mu_{eff}(V_{gs}-V_{th})R_g}{2L_C}}] \tag{3-8}$$

$$Z_{opt} \cong R_{opt} + jX_{opt} = \frac{\sqrt{35}}{7} \times \frac{1}{\omega C_{gs}} \angle 57.7^{\circ} \tag{3-9}$$

From above equations, the noise parameters strongly depend on the gate-to-source capacitance and transconductance. Due to the little change of input impedance (see the S_{11} in Fig. 3-2), the optimized input reflection coefficient almost didn’t change after HC stress, as shown in Fig. 3-13. From equation (3-9), we found that the minimum noise figure has a strong dependence on C_{gs} and g_m. Due to the degradation of g_m, minimum noise figure increases drastically after stress shown in Fig 3-14. The increase of minimum noise figure is about 88% of initial value. Therefore, HC effect is a very critical concern as designing a LNA. As shown in Fig 3-15, the locations of the valley are not the same. The degradation is also less serious in higher gate voltage region. It is possibly due to the shift of the threshold voltage and the g_m degradation shown in Fig. 3-1. Fig 3-16 shows the noise resistance increases after HC stress. It can be explained by equation (3-7) and the g_m degradations. According to equation (3-7), the noise resistance is independent of frequency. However, the noise resistance is indeed correlated with the frequency shown in Fig. 3-16. This relation may be contributed by the parasitic parts of RF MOSFETs. Fig. 3-17 shows the degradations of R_n versus different gate voltages. It is obvious that degradations are almost consistent when the MOSFET turns on.



(a)

(b)

Fig. 3-1: (a) DC characteristics of a MOSFET before and after CHE stress.
(b) DC characteristics of a MOSFET before and after DAHC stress.

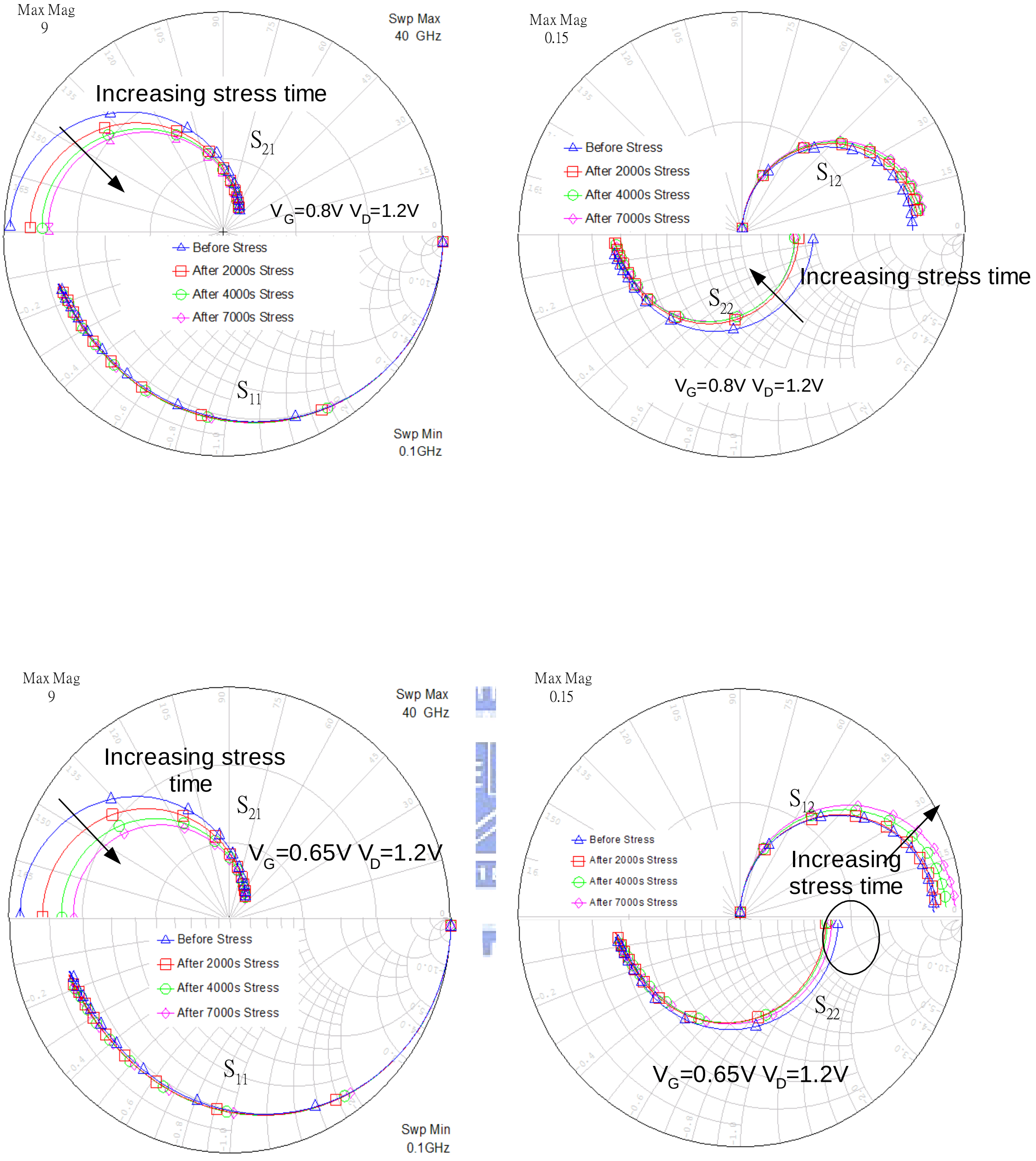


Fig. 3-2 S-parameter degradations with increasing stress time at different bias conditions.

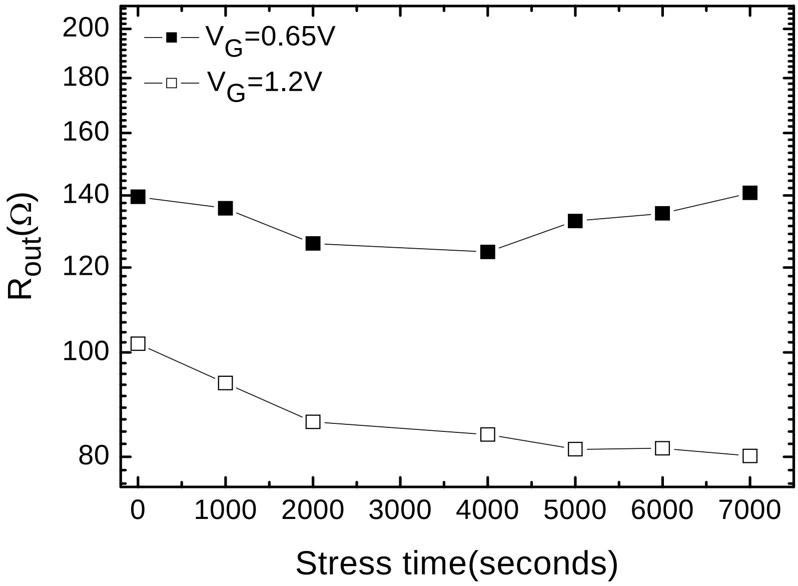


Fig. 3-3: Output impedance versus stress time at different bias condition.

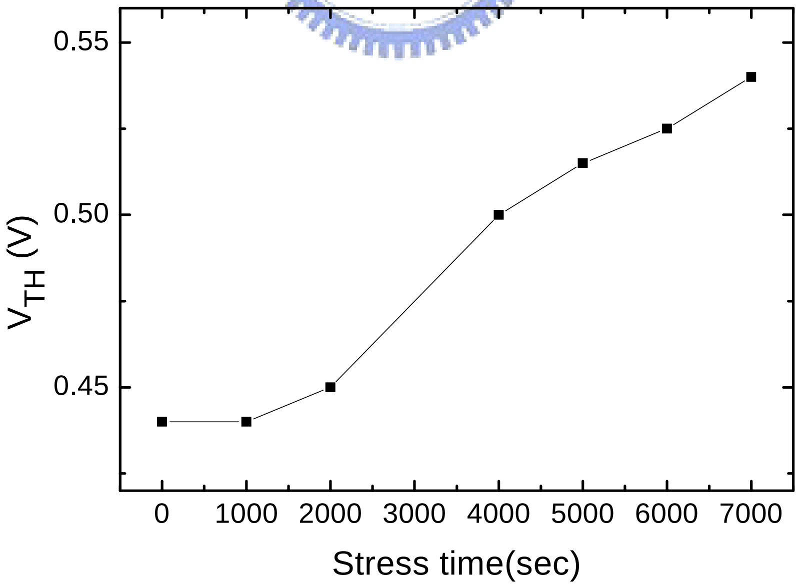
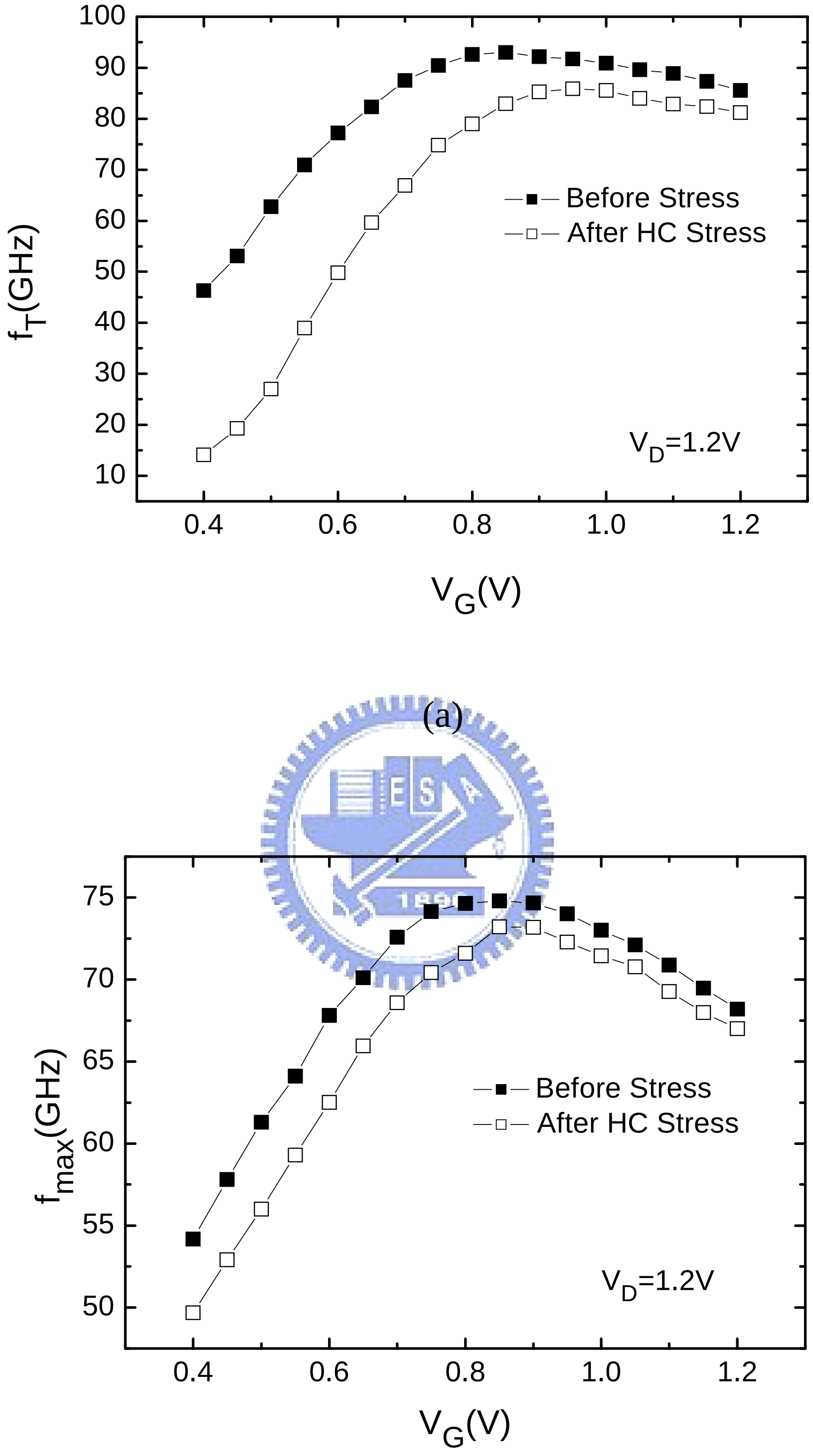


Fig. 3-4: Threshold voltage versus stress time.



(a)

(b)

Fig. 3-5: (a) Cut-off frequency before and after HC stress.
(b) Maximum oscillation frequency before and after HC stress.

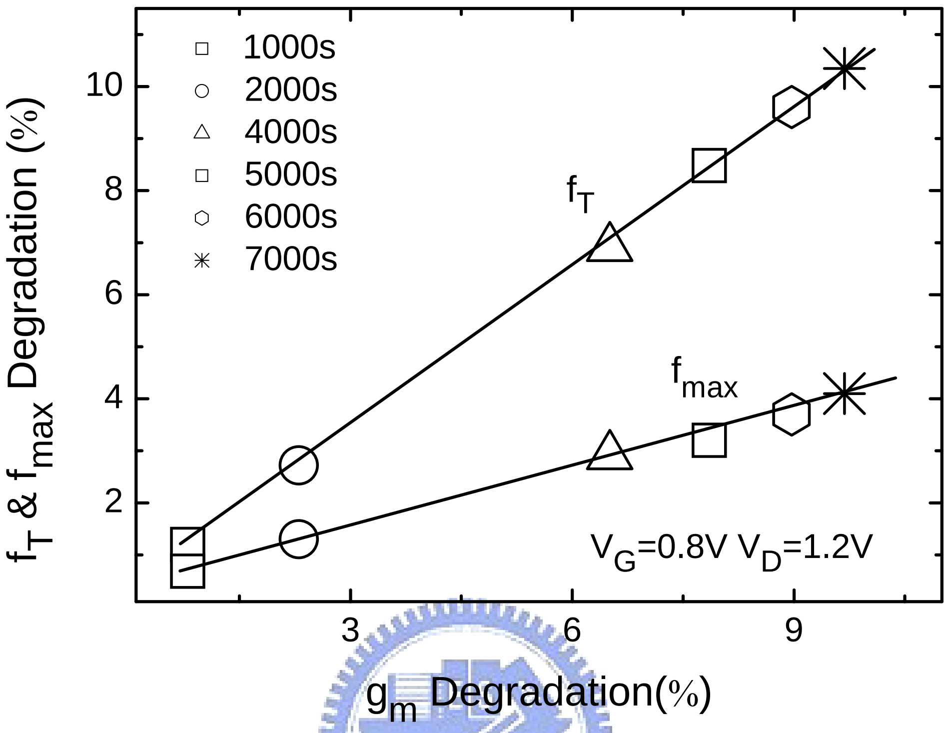


Fig. 3-6: Relation between f_T and f_{max} degradations and g_m degradation.

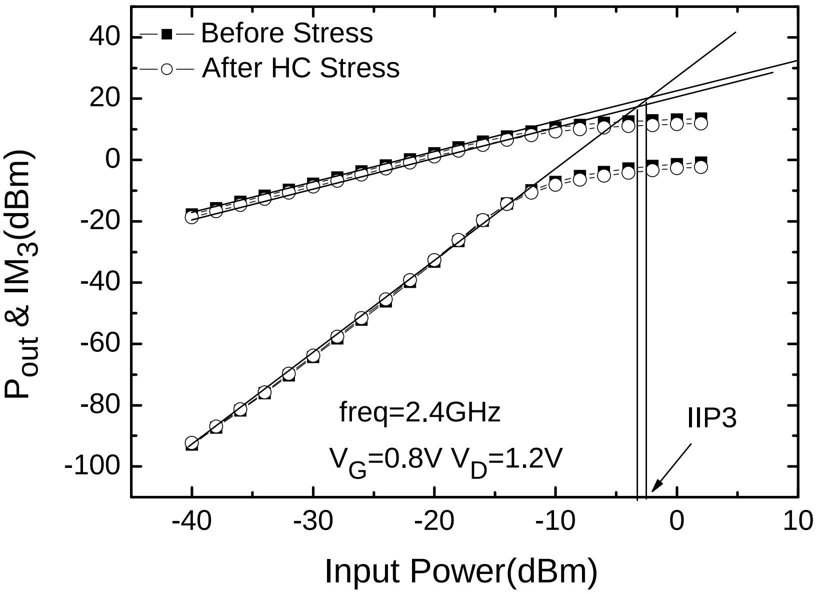


Fig. 3-7: Output power and 3rd-order intermodulation (IM3) power versus input power before and after HC stress.

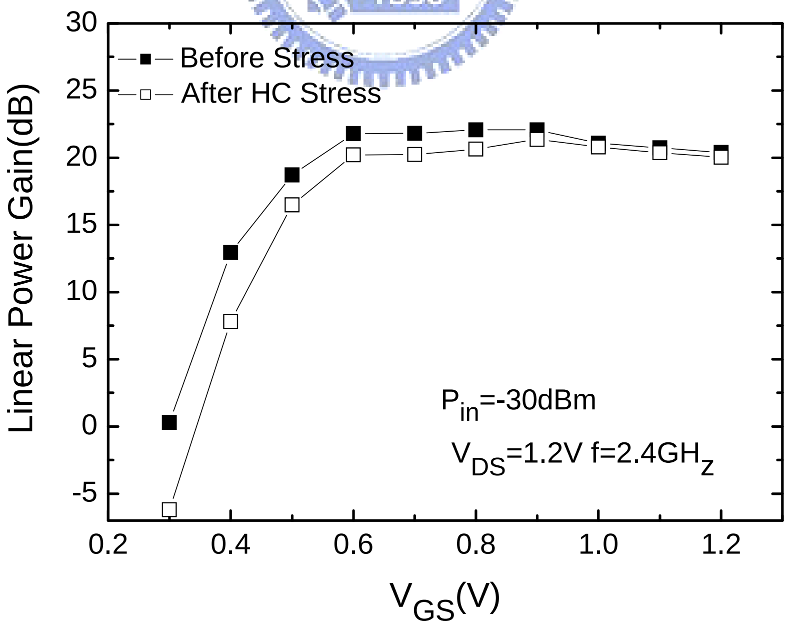


Fig. 3-8: Power gain versus gate bias voltage for a MOSFET before and after stress measured at a fixed V_{DS} = 1.2V.

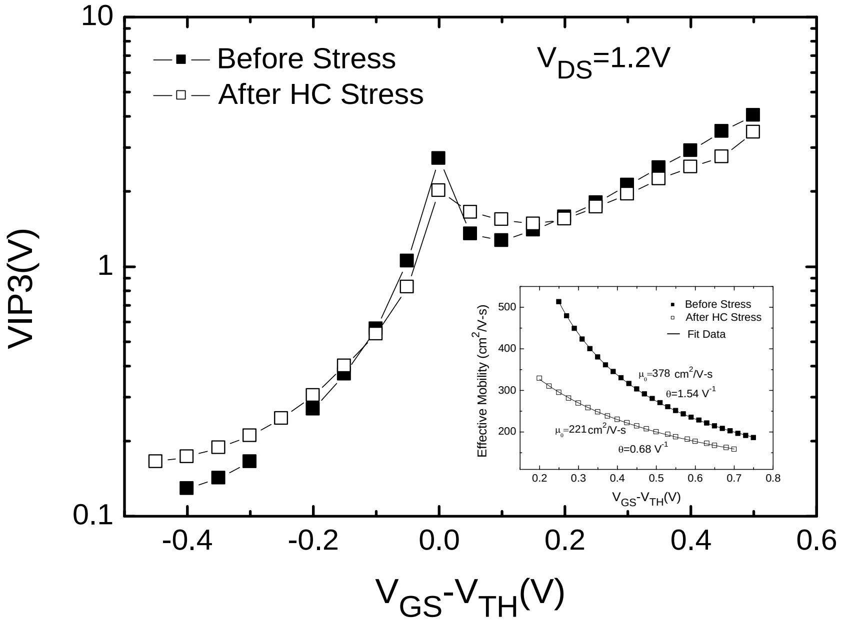


Fig. 3-9: *VIP3* versus $V_{GS} - V_{TH}$ for a MOSFET before and after stress. Inset is the effective channel mobility before and after stress.

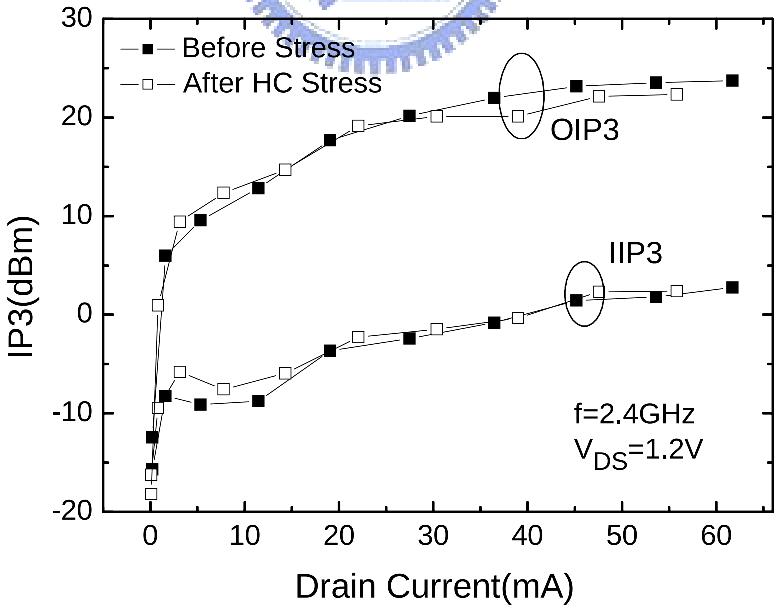


Fig. 3-10: Measured *OIP3* and *IIP3* versus drain current for a MOSFET before and after HC stress.

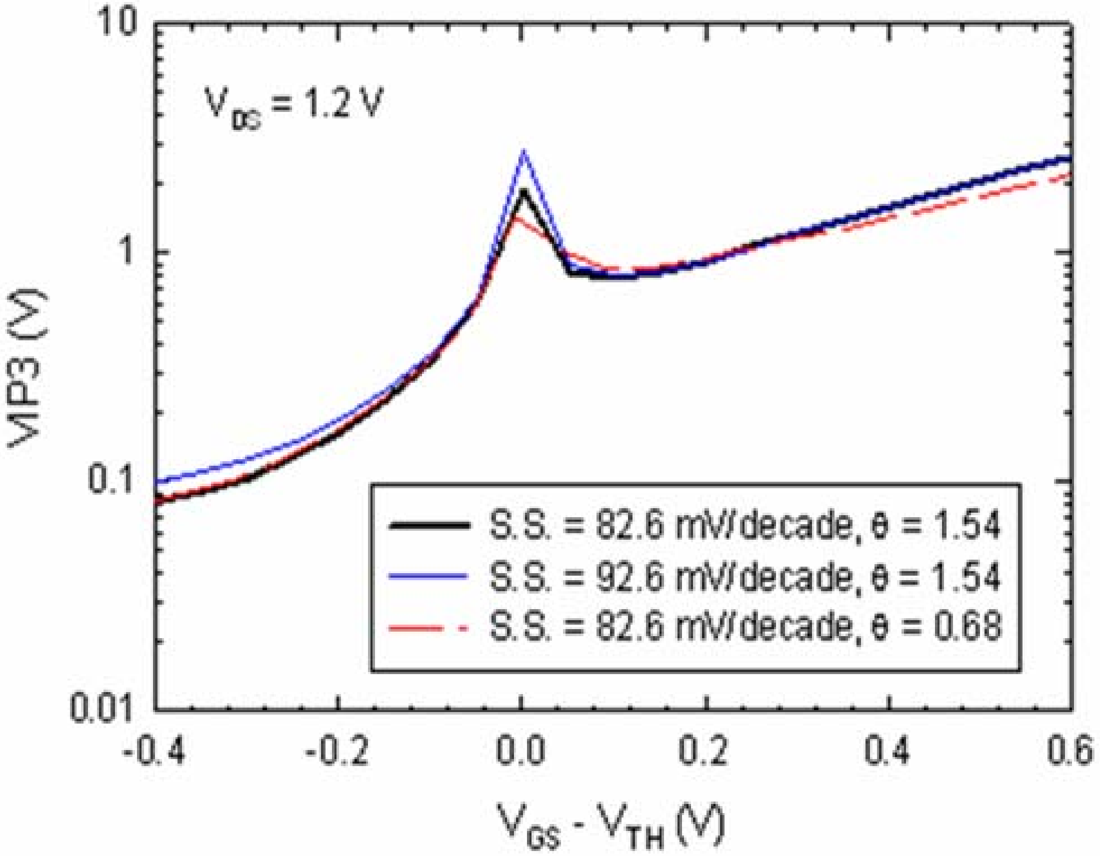


Fig. 3-11: Simulation results of *VIP3* with different subthreshold swings and mobility degradation coefficients.

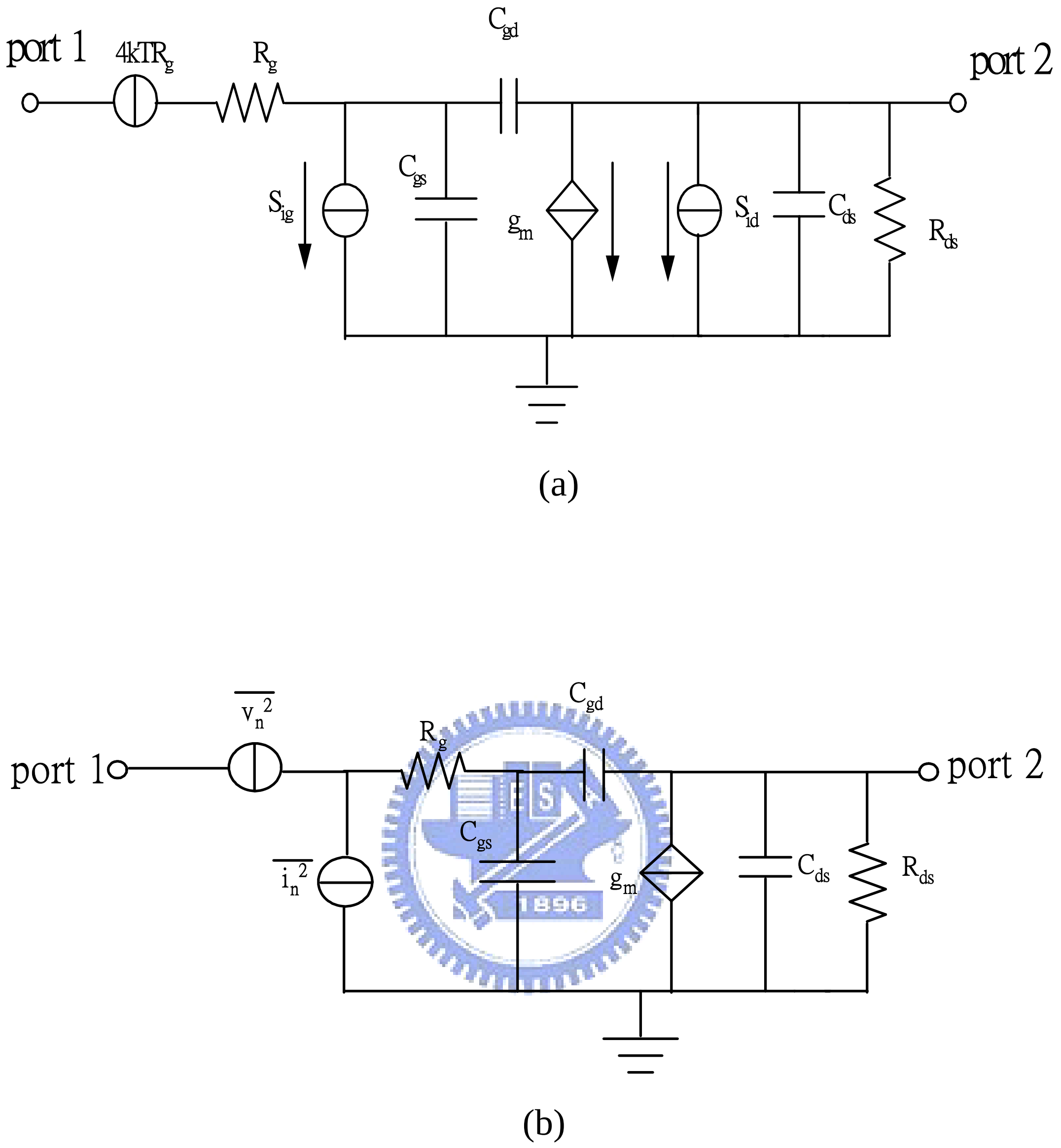


Fig. 3-12: (a) Equivalent circuit model of a MOSFET with thermal noise sources, where S_{iD} and S_{ig} are drain current and induced gate noise, respectively.
(b) Noise free MOSFET circuit model with input referred noise voltage and current.

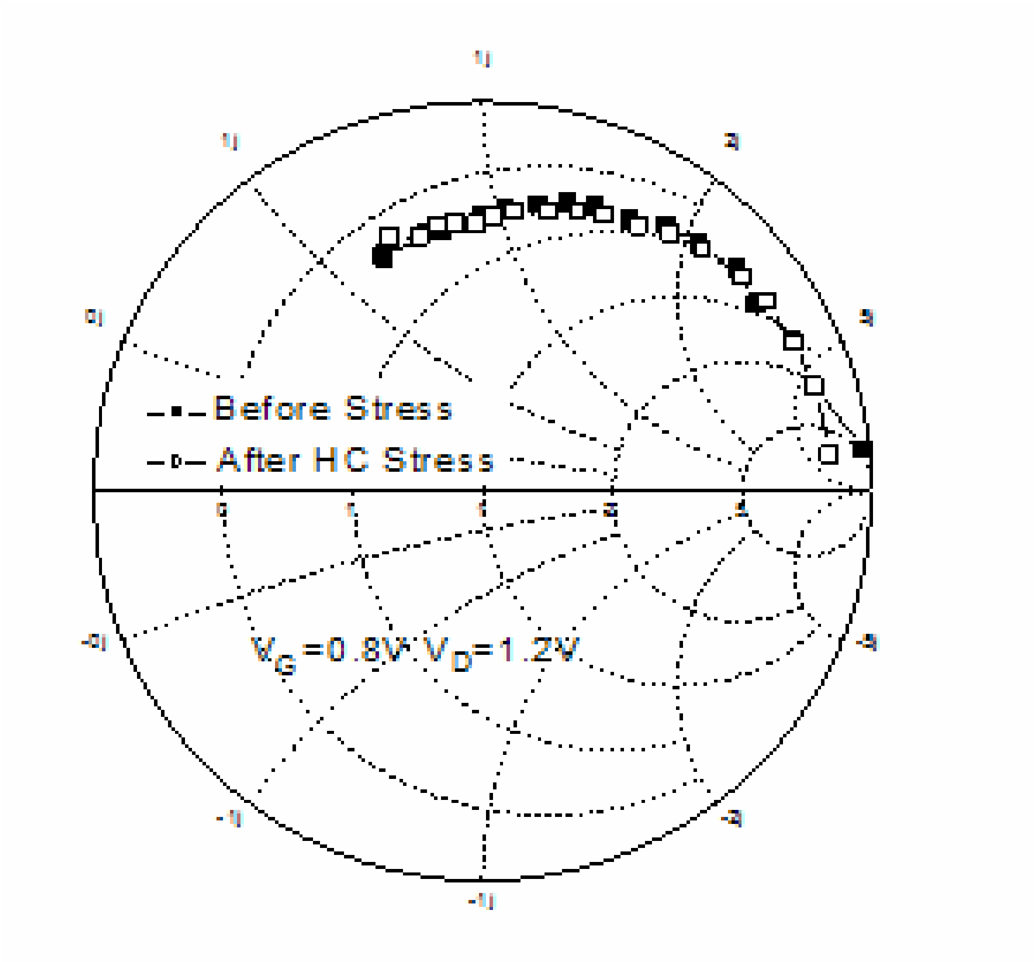


Fig. 3-13 Optimized input reflection coefficient (Γ_{opt}) before and after stress.

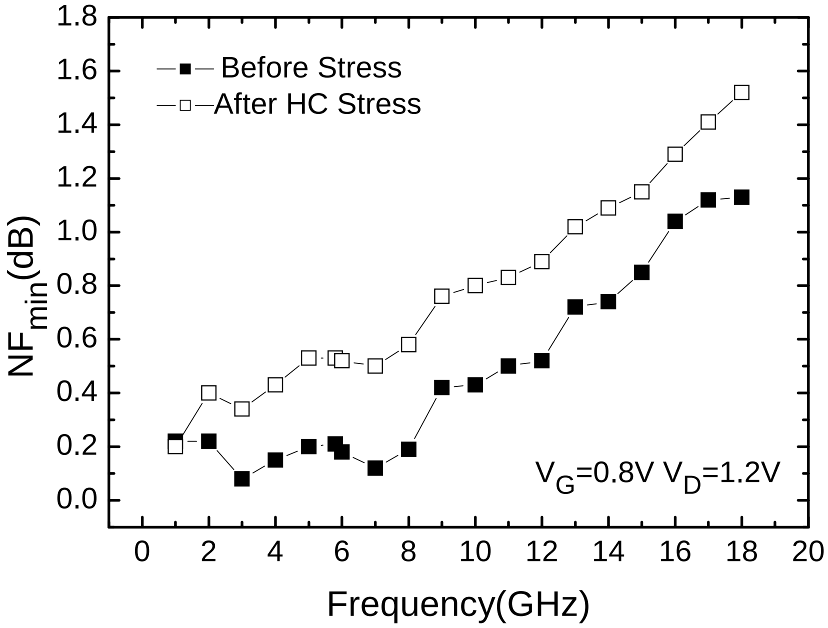


Fig. 3-14: Minimum noise figure (*NF*$_{min}$) versus frequency before and after HC stress

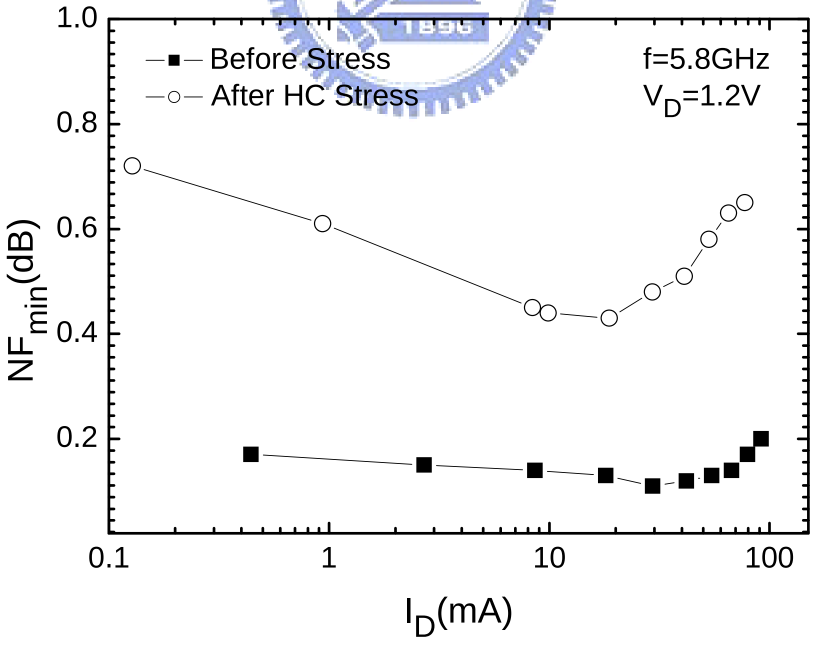


Fig. 3-15: Minimum Noise figure versus drain current before and after HC Stress.

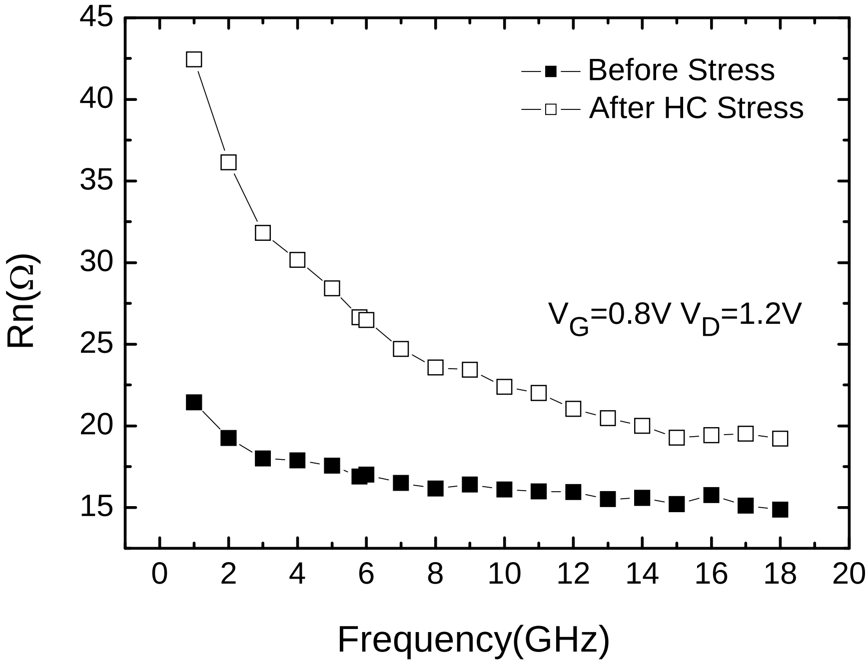


Fig. 3-16: Noise resistance (R_n) versus frequency before and after stress at fixed bias.

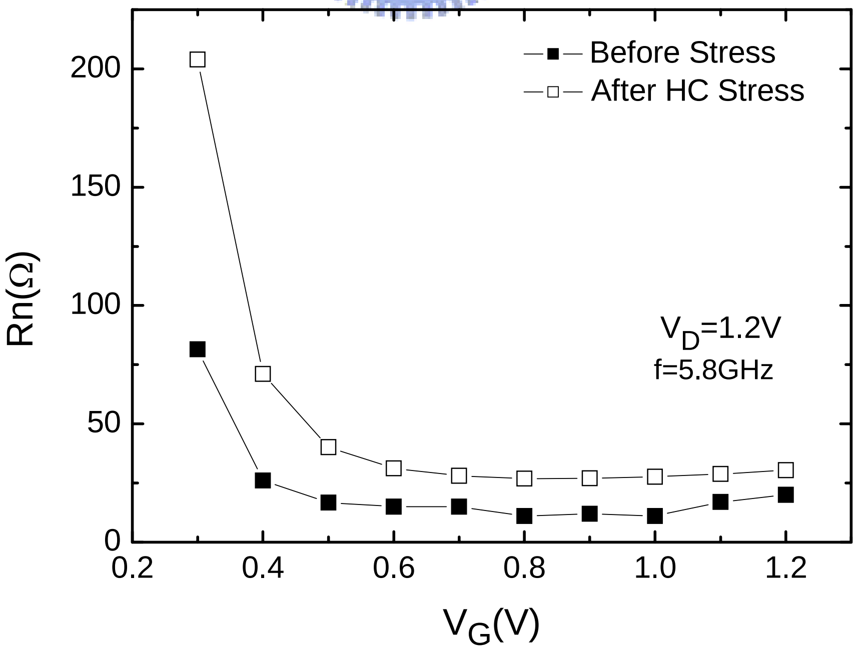


Fig. 3-17: Noise resistance versus gate voltage before and after stress.

Chapter 4

Characteristics of RF MOSFETs after Oxide Breakdown

In this chapter, we discuss the degradations of RF MOSFETs after soft breakdown (SBD) and hard breakdown (HBD). The channel length and total width of the devices under test are 0.12 μm and 158.4 μm respectively in our experiments. The gate oxide stress was subjected to a constant voltage stress under 3.9 V with the source, drain and bulk terminals shorted to ground. As shown in Fig. 4-1(a), the time to soft breakdown is defined as a time at which the gate current increases by 10 % from its initial value. From Fig. 4-1(b), the oxide hard breakdown was defined using a threshold on-stress current of 1 mA. Then we study the effects of oxide breakdown on DC, high-frequency, and power characteristics of a MOSFET.

4.1 Effects of Oxide Breakdown on DC Characteristics

In Fig. 4-2, it shows the I_G-V_G characteristics of the device before and after stress. The gate current is extremely low before HBD. After HBD, the gate current increases dramatically. It implies that a consistent leakage path in the gate oxide is formed. From the insert figure of Fig. 4-2, the resistance of this leakage path is about $7k\Omega$.

Fig. 4-3 shows the I_D-V_G characteristics of the MOSFET before and after oxide breakdown. Due to the generation of the interface states and oxide traps after oxide breakdown, the "on" drain current and transconductance all decrease. After soft breakdown, the degradation of saturation drain current in our experiments is about 3%, and the threshold voltage is shifted from 0.45 V to 0.46 V. On the other hand, the degradation of saturation drain current is about 9% and threshold voltage is shifted from 0.45V to 0.48V after hard breakdown. It is obvious that the “off” current increases dramatically after hard breakdown due to the contribution of the gate leakage current. It will increase static power consumption of a MOSFET in digital operation.

4.2 Effects of Oxide Breakdown on Cut-off frequency and Maximum Oscillation Frequency

Because a new leakage path will be generated after oxide breakdown, we add gate-to-drain and gate-to-source resistors to the small signal model of MOSFETs to derive the equation of cut-off frequency. The cut-off frequency can be approximated as:

$$f_T \cong \frac{g_m - \frac{2}{R_{gd}} - \frac{1}{R_{gs}}}{2\pi(C_{gs} + C_{gd})} \tag{4-1}$$

where R_{gd} is the gate-to-drain resistance and R_{gs} is the gate-to-source resistance. From the above discussions, the new leakage path was not formed after soft breakdown. Therefore the degradation of f_T is very slight, as shown in Fig. 4-4(a). However it is clear that the cut-off frequency reduces significantly after oxide hard breakdown. It is due to the g_m degradation and the existence of R_{gd} and R_{gs}. The f_T degradation is less significant at high gate voltage. It suggested that biasing at higher gate voltage is more robust to hard breakdown.

As shown in Fig. 4-4(b), the maximum oscillation frequency (f_{max}) is affected by SBD and HBD. From equations 3-2, the f_{max} is proportional to f_T, so f_{max} reduced after oxide breakdown. In addition, it is obvious that the degradation is more serious after HBD. Since f_{max} is directly proportional to the power gain of the MOSFET. Due to the new leakage path in the gate oxide, the power loss of the MOSFET will increase after oxide breakdown. Therefore f_{max} suffers degradations after oxide breakdown.

4.3 Effects of Oxide Breakdown on S-Parameters

The S-parameters of a MOSFET before and after oxide breakdown are shown in Fig. 4-5. We observed that the S_{12} and S_{11} are almost not affected by SBD. It implies that the input impedance and isolation of the MOSFET may not change. However, for devices after HBD, a gate-to-source leakage path is created. This leakage path would change the input impedance of MOSFETs and thus S_{11} changes obviously. We also found that the degradation of S_{12} is very slight. Therefore we can infer that the main leakage path doesn't locate at the gate-to-drain overlap region.

As shown in Fig. 4-5, the magnitude of S_{21} both decreased after SBD and HBD. However the degradations are not obvious at high frequencies. By using the small signal model shown in Fig. 4-6, the S_{21} of a MOSFET can be approximated as:

$$S_{21} = -2 \cdot \frac{Z_{in,i}}{Z_o + R_g + Z_{in,i}} \left(\frac{g_m - sC_{gd}}{1 + g_m R_s}\right) \cdot \frac{(1 + g_m R_s) Z_L}{sZ_L C_{gd} + 1 + g_m R_s} \cdot \frac{Z_o}{Z_0 + R_d} \tag{4-2}$$

$$Z_{in,i} = \left[\frac{(1 + g_m R_s)^2}{s(1 + g_m R_L)(1 + g_m R_s) C_{gd}} + \frac{(1 + g_m R_s) Z_L}{1 + g_m Z_L}\right] || \frac{(1 + g_m R_s)}{sC_{gs}} \tag{4-3}$$

At low frequency, S_{21} can be approximated by:

$$S_{21} = -2 g_m R_L \frac{Z_0}{(1 + g_m R_s)(Z_o + R_d)} \tag{4-4}$$

The S_{21} is strongly proportional to g_m. Hence the magnitude of S_{21} reduces significantly at low frequency after oxide breakdown. Since the correlation between g_m and S_{21} is smaller at high frequencies, S_{21} is less degraded by oxide breakdown. There are almost no degradations above 12 GH_Z. Finally, the degradations of low frequency value of S_{22} are due to the degradations of

g_m and output conductance

4.4 Effects of Oxide Breakdown on Power Performance and Linearity

The gate oxide breakdown is an important reliability issue for the design of power amplifiers. Fig. 4-7 shows the linear power gain measured with different gate voltages after SBD and HBD. It was found that the degradation is more significant after HBD. Moreover, it shows a slight deviation in higher gate bias regions. The degradation of power gain is corresponded to the g_m degradation in Fig. 4-3. From Fig. 4-7, it suggested that the device biasing at high gate voltages is more robust to oxide breakdown.

The degradations of output power, power gain and power-added efficiency (PAE) are shown in Fig. 4-8. The PAE can be expressed by:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}(1 - \frac{1}{G}) \tag{4-5}$$

At low input power, the PAE is less changed under stress, due to the output power and drain current, and thus power dissipation, reduce simultaneously. When input power is larger than 1dB compression point, the degradations of PAE become serious. Because a part of the ac signal of drain current will be cut off as the input power is large enough. For this reason, the average drain current will increase with increasing input power. Since the bias current of the device after oxide breakdown and HC stress is lower than that of the fresh one, the negative duty cycle of output waveform would enter the cut off region earlier. As a result, the power dissipation of stressed device is higher than that of fresh one, leading to lower PAE. Since the DC degradation is more serious after HC stress, the degradations of PAE is more serious after HC stress. As a result, hot carriers effect is a more critical concern as designing power amplifiers from above discussions.

Since the dc behaviors are changed, the linearity would be affected by the oxide breakdown. As shown in Fig. 4-9, the linearity suffers obvious degradation at a fixed voltage bias after HBD. It is due to the g_m degradations shown in Fig. 4-3. Because the g_m degradation after oxide breakdown is less serious for device biasing at constant currents, RF linearity suffers less degradation. As shown in Fig. 4-10, oxide breakdown degrades the RF linearity slightly if biasing the MOSFET at constant drain currents.

4.5 Effects of Oxide Breakdown on Noise Performance

The impact of gate shot noise is associated with the gate leakage current in MOSFETs. After oxide breakdown, the gate leakage current increases dramatically. Therefore gate shot noise plays a dominant role in determining the high frequency noise in the MOSFET after oxide breakdown. The drastic change of noise characteristics due to oxide breakdown could be qualitatively explained using established analytical expressions considering the increased contribution from gate shot noise [22]:

$$R_n = \frac{\overline{v^2{}_n}}{4kT\Delta f} = \frac{\gamma}{\alpha g_m} \qquad (4\text{-}6)$$

$$F_{\min} \cong 1 + 2R_n \omega C_{gs} \sqrt{\frac{\delta(1 - C_G{}^2)\alpha^2}{5\gamma} + \frac{2qI_G g_m \alpha}{(4kT\gamma\omega^2 C_{gs}{}^2)}} \qquad (4\text{-}7)$$

where $\alpha \triangleq g_m / g_{d0}$, with g_{d0} being the drain conductance for V_{DS}=0V, γ, δ and C_G are parameters of the models for drain noise and induced gate noise. From above equations, noise resistance is mainly dominated by the drain (channel) thermal noise and g_m. Hence R_n reduces significantly after oxide breakdown as shown in Fig. 4-11. From Fig. 4-12, we found that the R_n degradations are almost consistent when the MOSFET turns on.

From (4-7), the minimum noise figure is not only determined by R_n but also induce gate noise [term of $\frac{\delta(1-C_G{}^2)\alpha^2}{5\gamma}$] under the square root of in (4-7) and gate shot noise [term of $\frac{2qI_G g_m \alpha}{(4kT\gamma\omega^2 C_{gs}{}^2)}$] under the square root of in (4-7). When the gate leakage is low or frequency is high enough, NF_{min} is dominated by the induce gate noise, and (4-7) simplifies as:

$$NF\min \cong 1+2\omega/\omega_T\sqrt{\gamma\delta(1-C_G{}^2)/5} \tag{4-8}$$

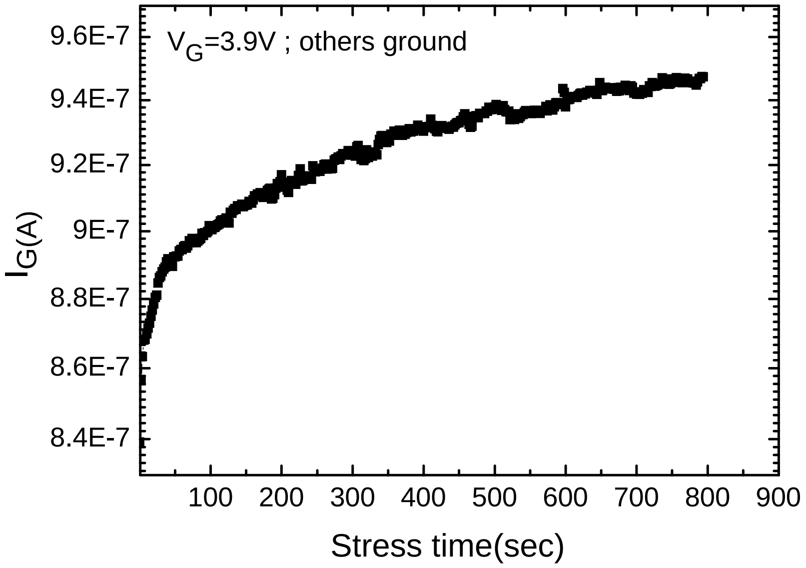
It is proportional to the frequency. On the other hand, when the gate leakage become larger or the frequency is low enough, the NF_{min} can be approximated as:

$$NF_{\min} \cong 1+\sqrt{2qI_G\gamma/(kT\alpha g_m)} \tag{4-9}$$

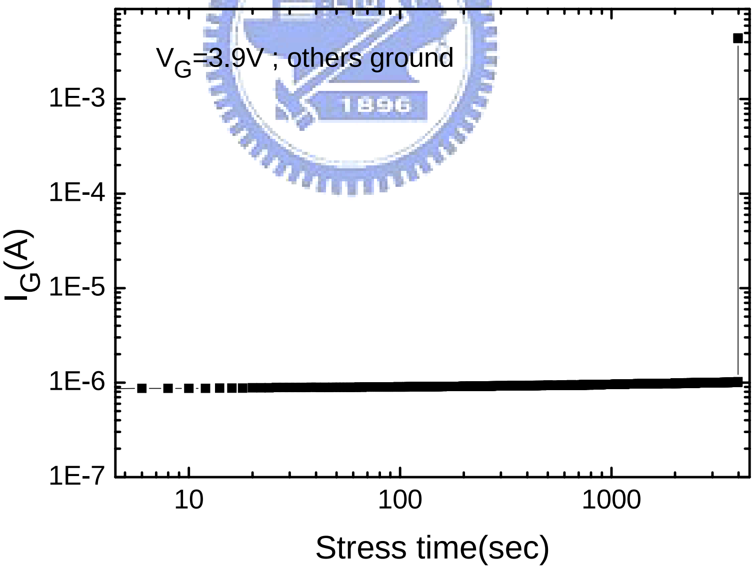
It is independent of frequency. Due to g_m degradation, NF_{min} increases after oxide breakdown shown in Fig. 4-13(a). The degradation is more serious after hard breakdown due to the additional shot noise source. Since I_G increases dramatically for device after hard breakdown, the frequency independent region is much larger than that of the fresh one. Fig. 4-13(b) compares the NF_{min} degradations after HBD and HC stress. The NF_{min} suffers less degradation after HC stress. It is quite different from the degradations of the other electric performances. As shown in Table 4-1, the DC characteristics, power performance and noise resistance are degraded more significantly for devices under HC stress. From above discussions, those characteristics depend on transconductance strongly. Since g_m suffers larger degradations after HC stress, those characteristics are degraded more dramatically. However, the NF_{min} is degraded more significantly for device after HBD than that after HC stress due to the additional shot noise source occurred in the gate region. Fig. 4-14 shows the NF_{min} as a function of drain current before and after oxide breakdown. The locations of the NF_{min} valley shift after hard breakdown. It may due to the shift of threshold voltage. Finally, Fig. 4-15 shows the degradations of optimized input reflection coefficient. For devices after oxide breakdown, an additional resistance in leakage path will be introduced between gate and source, leading to the reduction of input impedance. As a result, the magnitude of the optimized input reflection coefficient will be reduced after oxide breakdown.

	Δg_m (%)	ΔI_D (%)	ΔIIP3 (%)	ΔPower Gain(%)	ΔNF_{min} (%)	ΔR_n (%)	Δf_T (%)	Δf_{max} (%)
After HBD	-6	-10.3	-4.1	-4.2	232.1	28	-8.3	-1.5
After HC Stress	-15.3	-22.8	-8.1	-8.3	88.3	114	-17.1	-6.9

Table 4-1: The variations of DC, high-frequency, noise and power characteristics of a MOSFET after HBD and HC stress at V_G=0.8V V_D=1.2V.



(a)



(b)

Fig. 4-1: (a) Time evolution of gate current before and after soft breakdown.
(b) Time evolution of gate current before and after hard breakdown.

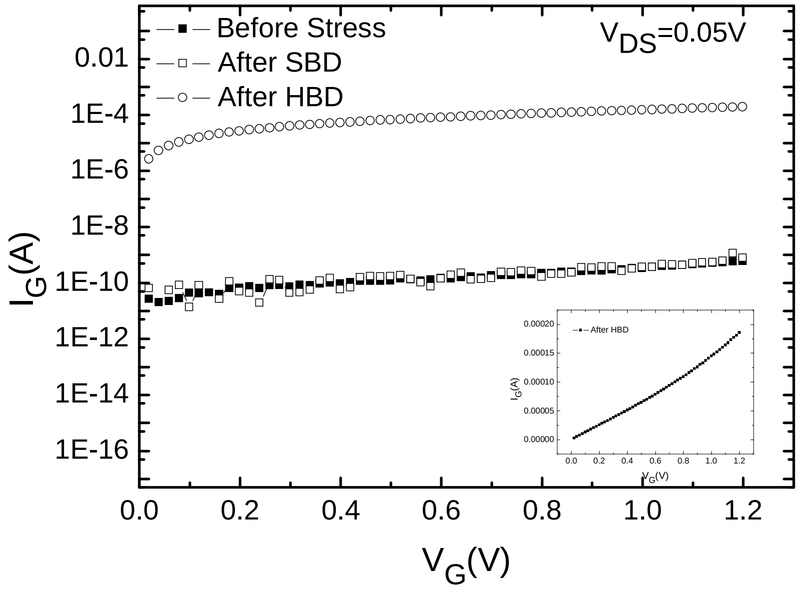


Fig. 4-2: Gate current versus gate voltage before and after oxide breakdown.

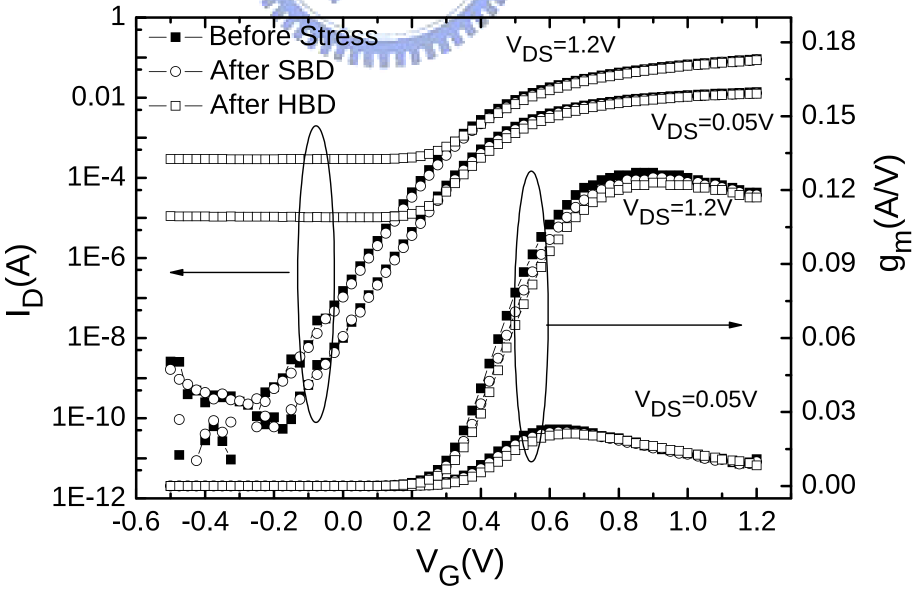
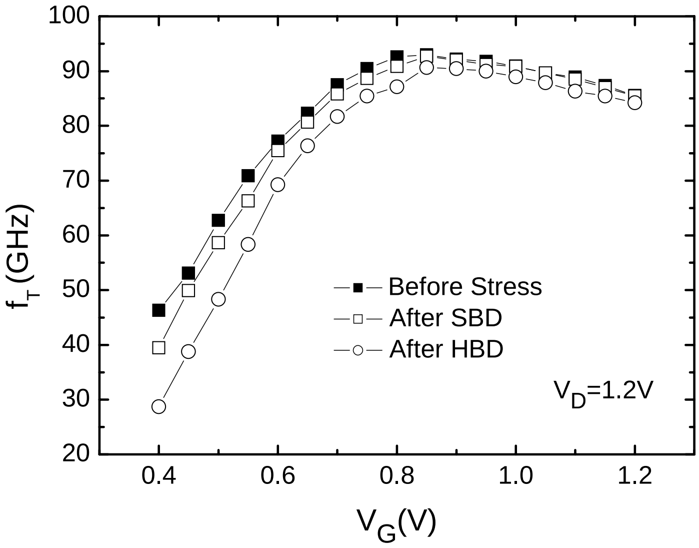
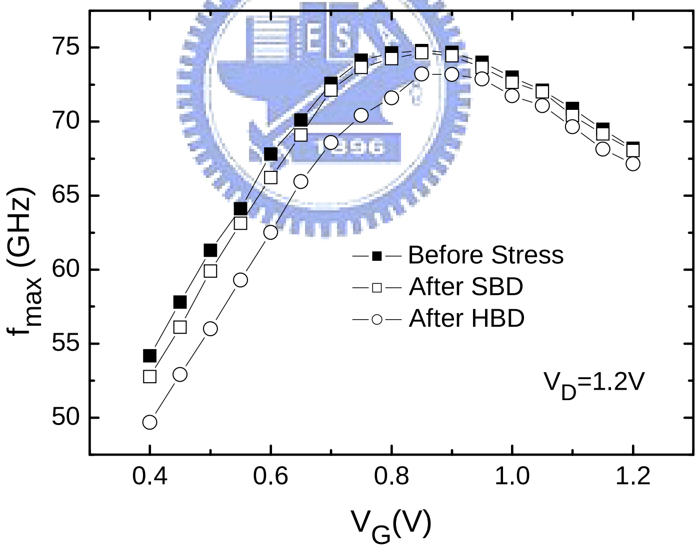


Fig. 4-3: DC characteristics of a MOSFET before and after oxide breakdown.



(a)



(b)

Fig. 4-4: (a) Cut-off frequency and (b) maximum oscillation frequency versus gate voltage before and after oxide breakdown.

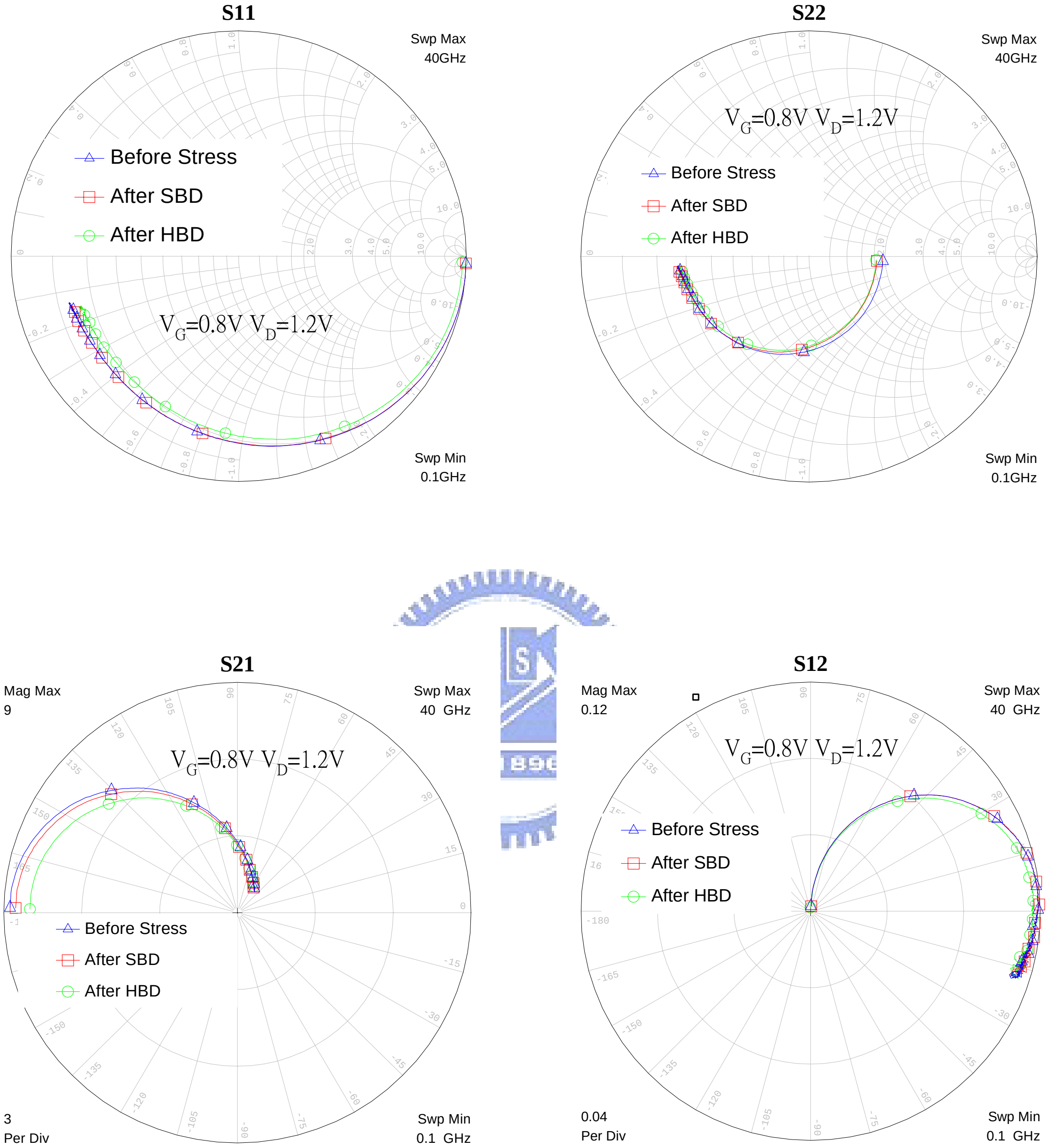


Fig. 4-5: S-parameters before and after oxide breakdown.

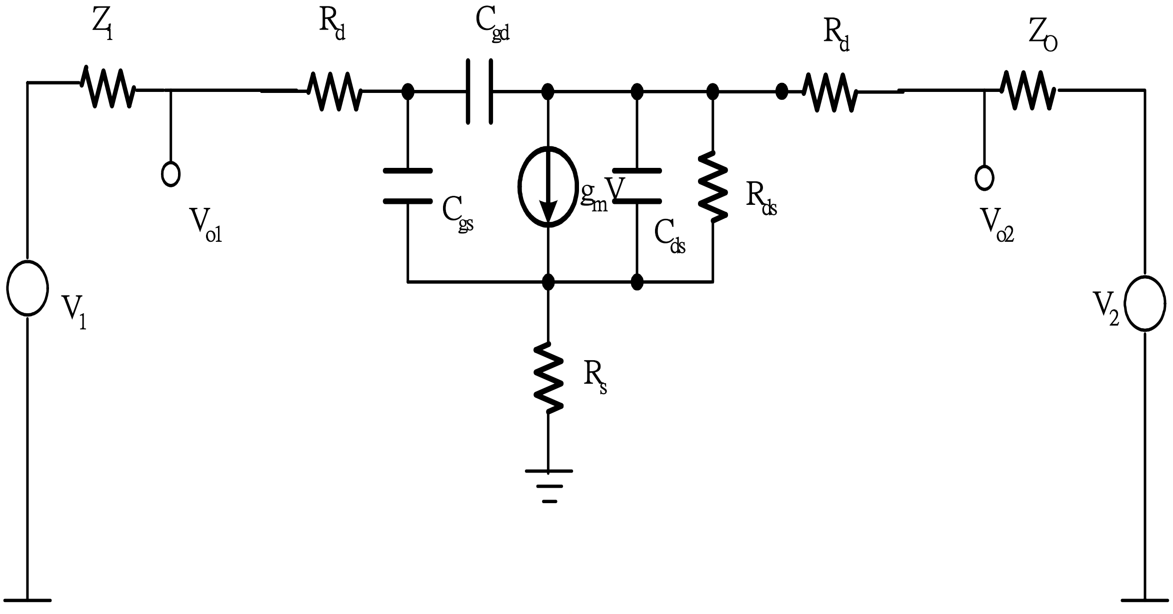


Fig. 4-6: Small signal model for the measurement of S-parameters.

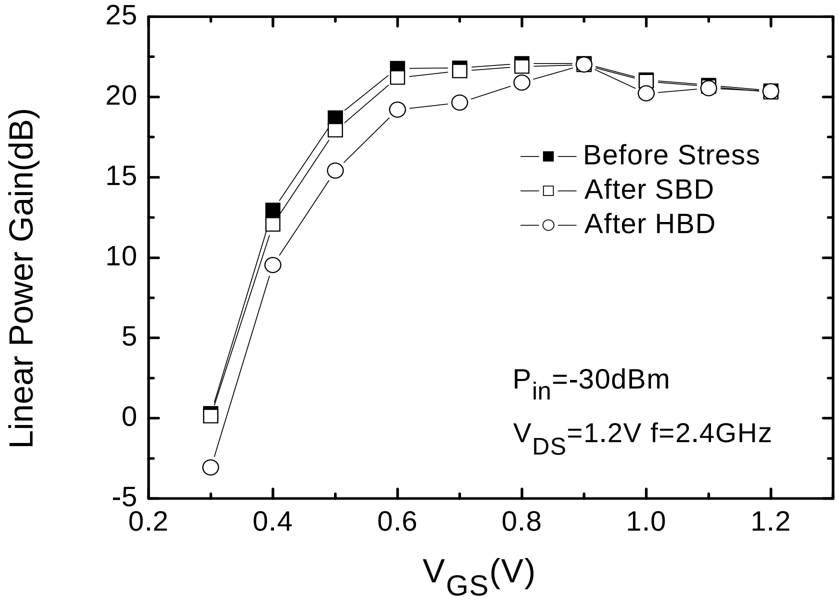


Fig. 4-7: Power gain versus gate bias voltage for a MOSFET before and after oxide breakdown at a fixed V_{DS} = 1.2V.

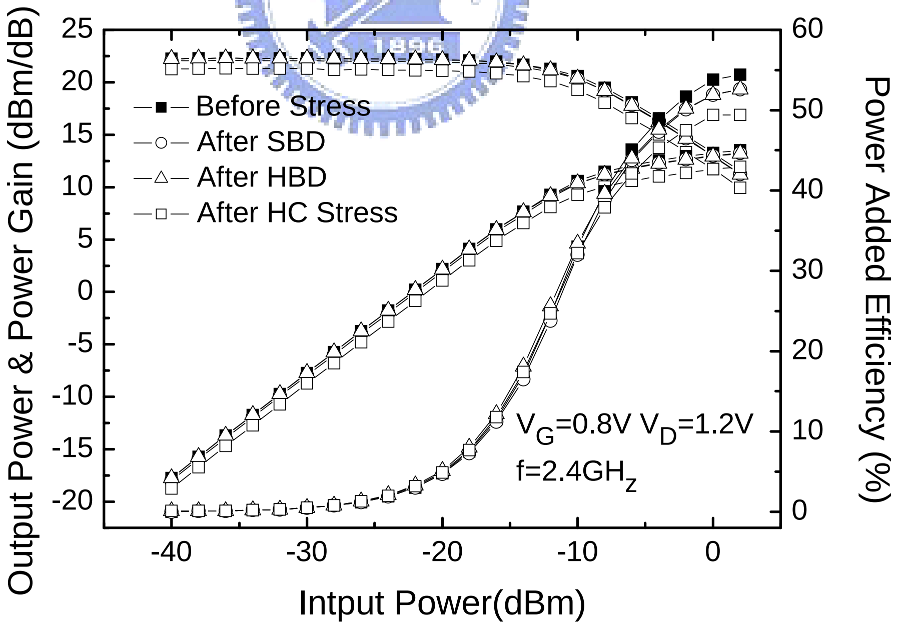
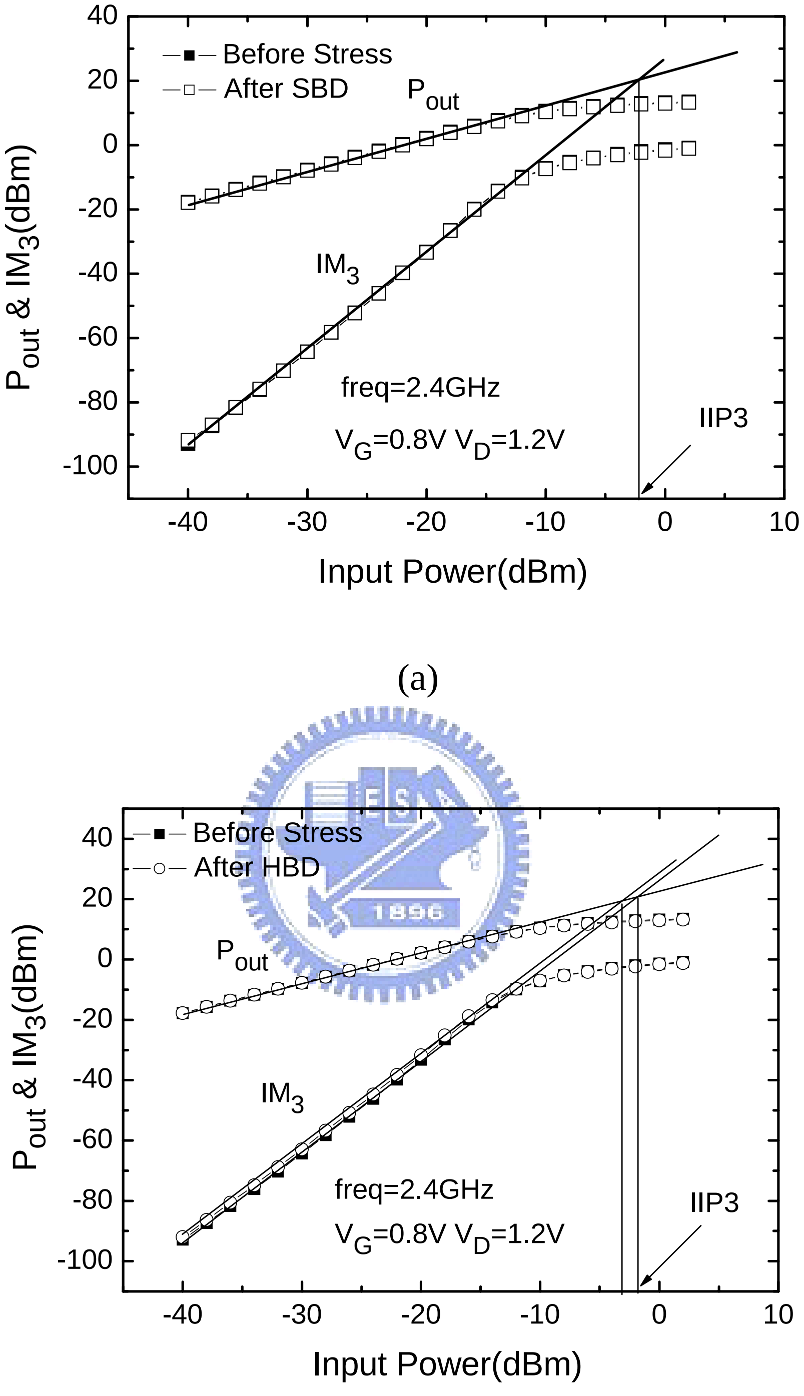


Fig. 4-8: Output power, power gain and PAE versus input power before and after oxide breakdown and HC stress.



(a)

(b)

Fig. 4-9: (a) Output power and 3rd-order intermodulation (IM3) power versus input power before and after soft breakdown.
(b) Output power and 3rd-order intermodulation (IM3) power versus input power before and after hard breakdown.

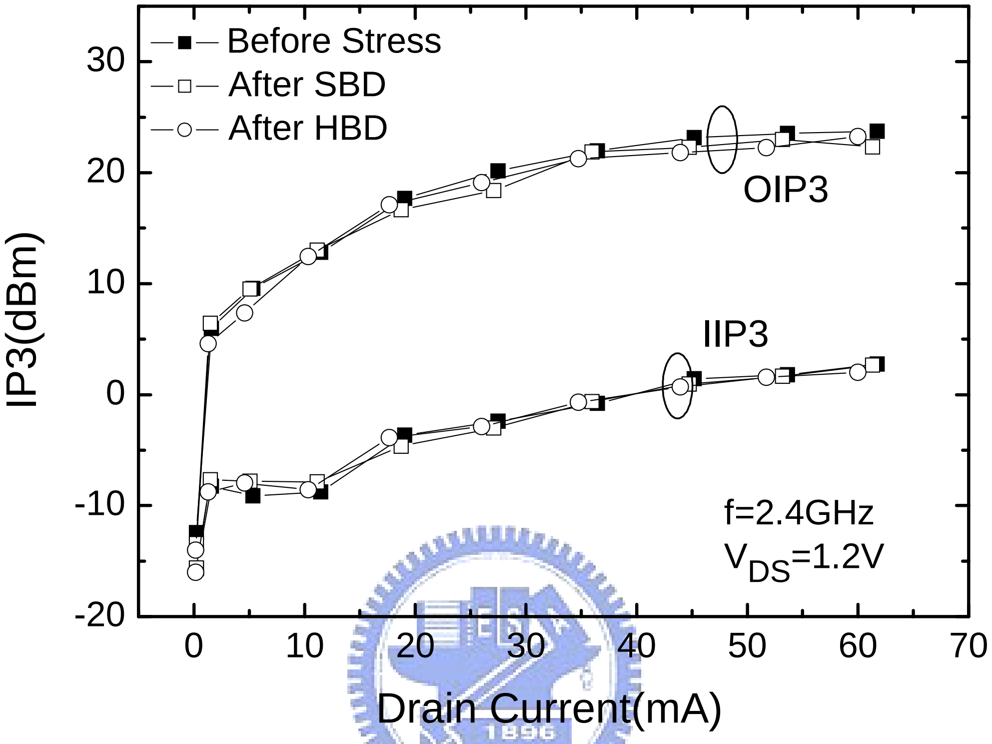


Fig. 4-10: Measured *OIP3* and *IIP3* versus drain current for a MOSFET before and after oxide breakdown

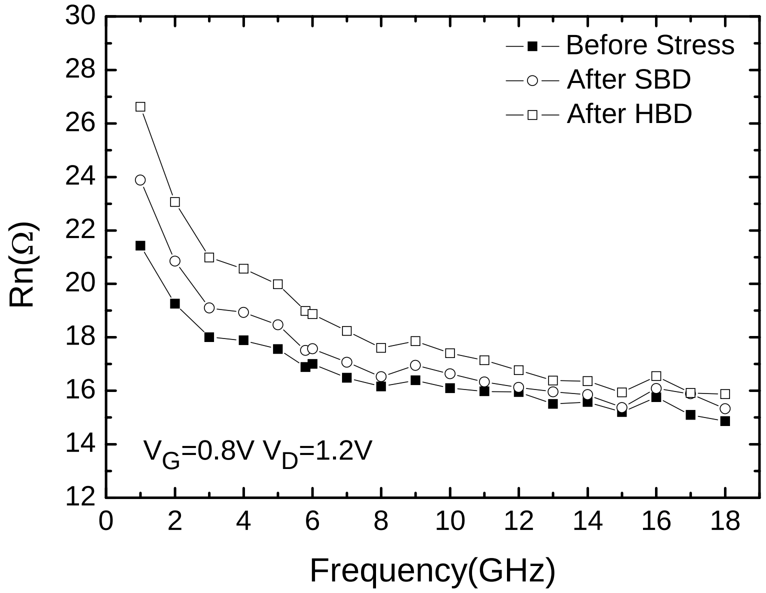


Fig. 4-11: Noise resistance (R_n) versus frequency before and after oxide breakdown at a fixed gate bias.

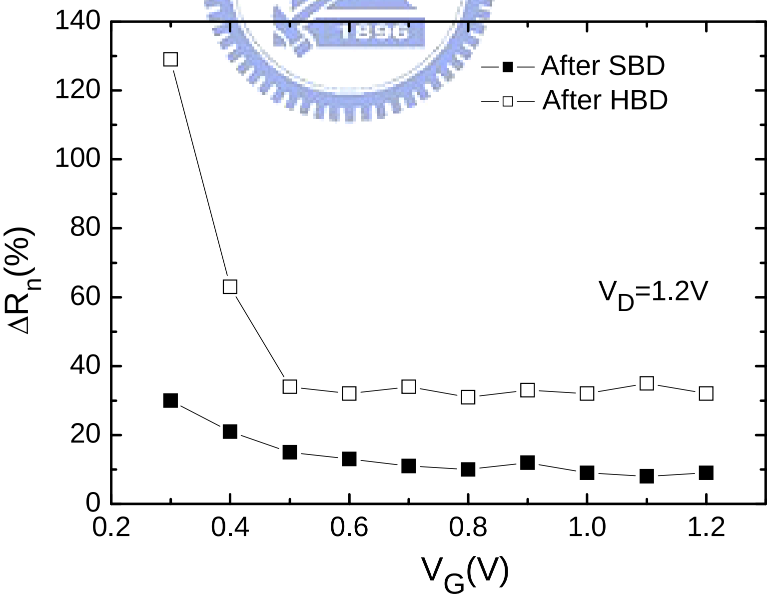
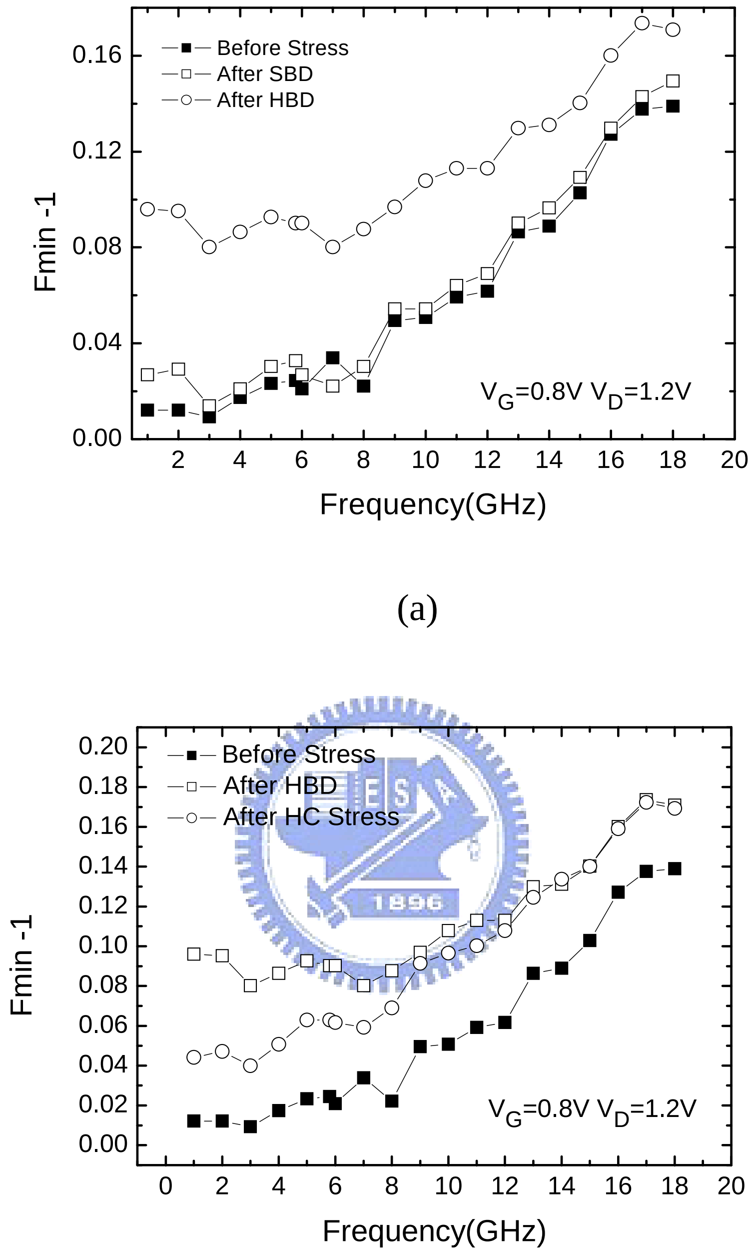


Fig. 4-12: The variations of R_n versus different V_G after HBD and SBD.



(a)

(b)

Fig. 4-13: Minimum noise figure (NF_{min}) versus frequency before and after stress.

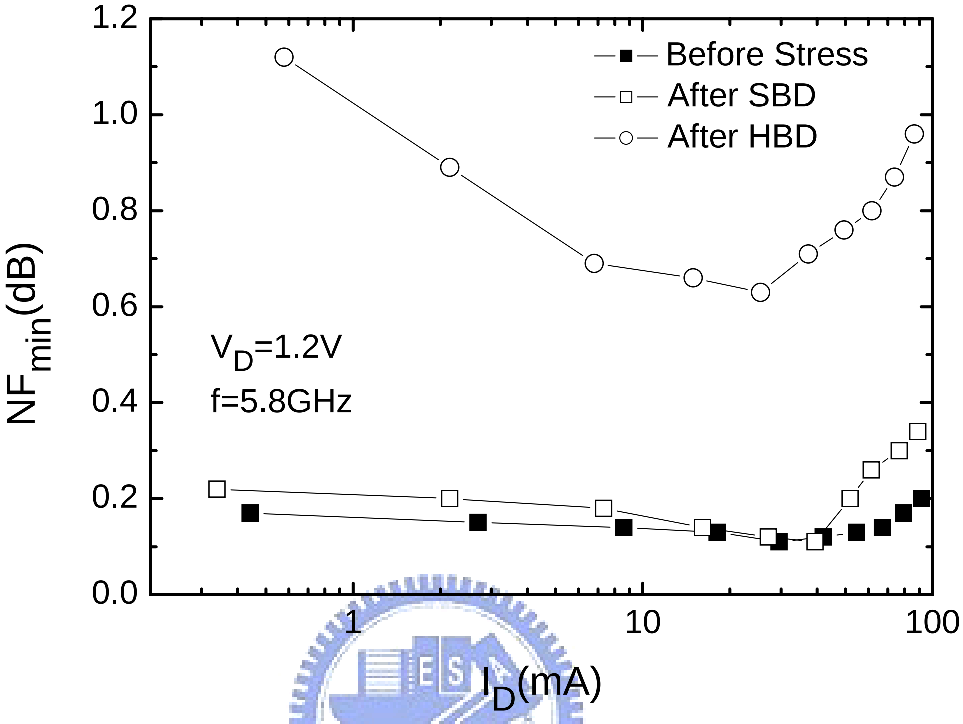
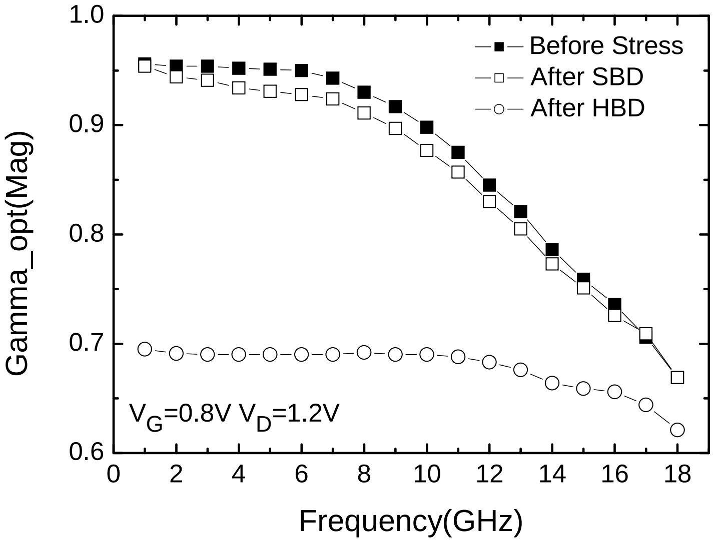
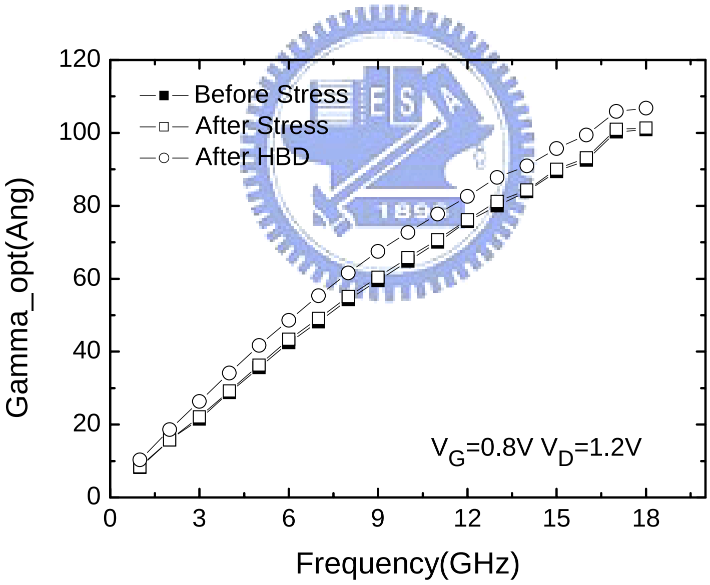


Fig. 4-14: Minimum Noise figure versus drain current before and after oxide breakdown.



(a)



(b)

Fig. 4-15: (a) Magnitude of optimized input reflection coefficient before and after oxide breakdown.

(b) Phase of optimized input reflection coefficient before and after oxide breakdown.

Chapter 5

Modeling of RF MOSFETs under HC stress and Oxide Breakdown

In this chapter, we establish a small-signal model of the RF MOSFET which is valid up to 18 GHz. The cold-FET method [24] was used in our model to extract the parasitic resistances. An extraction approach, which was proposed by S. Lee [25], was adopted to determine the intrinsic circuit parameters. For modeling devices under HC stress, we compare the variations of each parameter after stress. To model the oxide breakdown effects, we add gate-to-source and gate-to-drain resistances to the device model after oxide breakdown. The main leakage path located at the gate and source overlap region. It is quite important while considering the input network matching.

5.1 Extraction Method of Small-Signal Model Parameters

The small-signal model shown in Fig. 5-1(a) can be partitioned into three parts. The first part includes the parasitic series resistors R_g, R_d and R_s, and the second part refers to as the substrate network. The third part is the intrinsic model. We extract the parasitic resistors by using the zero-bias small-signal equivalent circuit as shown in Fig. 5-2. If the frequency is not high enough, we can ignore the substrate network. Conversion of the measured zero bias S-parameters into real components of an equivalent z-parameters network yields the parasitic resistance values. Equations for the parasitic resistances of the model shown in Fig. 5-2 are given by:

$$\mathrm{Re}(Z_{11}) = R_g + R_s \tag{5-1}$$

$$\mathrm{Re}(Z_{22}) = R_d + R_s \tag{5-2}$$

$$\mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = R_s \tag{5-3}$$

Fig. 5-3 illustrates the values of R_g, R_s and R_d extracted by this technique.

After de-embedding the parasitic parameters, we use the curve-fitting method [26] to extract the parameters associated with the substrate parasitic. After d-embedding R_g, R_s, and R_d, the resulting network would become that shown in Fig. 5-1(b) and it will produce following equations:

$$\frac{1}{R_{ds}{}^{eff}} = \mathrm{Re}\,al(Y_{22}{}^{c} + Y_{12}{}^{c}) = \frac{1}{R_{ds}} + \frac{k_1\omega^2}{1+k_2\omega^2} \tag{5-4}$$

$$C_{ds}{}^{eff} = \frac{1}{\omega}\mathrm{Im}(Y_{22}{}^{c} + Y_{12}{}^{c}) = C_{ds} + C_{jd}\left(\frac{1+m_1\omega^2}{1+m_2\omega^2}\right) \tag{5-5}$$

$$R_{bk} = \frac{k_2}{k_1}[1-\frac{m_1}{m_2}]^2 \tag{5-6}$$

$$C_{bk} = \frac{m_1 C_{jd}}{m_2 - m_1} \tag{5-7}$$

where k1, k2, m1, m2 can be considered as constants. From above equations, the parameters which are associated with substrate network can be obtained by using curve-fitting method. Finally the parameters of the intrinsic network shown in Fig. 5-1(c) can be directly extracted by following equations [26]:

$$C_{gd} = -\frac{1}{\omega}\mathrm{Im}(Y_{i,12}) \tag{5-8}$$

$$C_{gs} = \frac{1}{\omega}\mathrm{Im}(Y_{i,12} + Y_{i,11}) \tag{5-9}$$

$$C_{ds} = \frac{1}{\omega}\mathrm{Im}(Y_{i,12} + Y_{i,22}) \tag{5-10}$$

$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{i,22})} \tag{5-11}$$

$$g_{m0} = Mag(Y_{i,21} + Y_{i,12}) \tag{5-12}$$

$$\tau = -\frac{1}{\omega}Phase(Y_{i,21} - Y_{i,12}) \tag{5-13}$$

Fig. 5-4 shows the extracted values of each parameter versus frequency. The extracted parameters remained somewhat constant with frequency. Finally we show the measured and modeled S-parameters in Fig. 5-5 to verify the accuracy of this model.

5.2 Modeling of RF MOSFETs under HC Stress

From the observations of S-parameters after HC stress, we assume that there are no new components added to the equivalent circuit shown in Fig. 5-1.Therefore we directly use conventional small-signal model to establish the device model under HC stress. As shown in Fig. 5-6, this model is accurate under HC stress. Table 5-1 shows the extracted parameters before and after HC stress at different bias conditions. We found that only C_{gs}, g_{m0}, R_{ds} and R_d suffer degradations after HC stress.

First of all, we plot the extracted C_{gs} and C_{gd} with increasing stress time, as shown in Fig. 5-7. It is obvious that C_{gs} and C_{gd} increase with increasing HC stress time. The variations of C_{gd} are very slight compared with that of $C_{gs.}$ We use the definition of small-signal gate-to-source capacitance to explain this observation [27]:

$$C_{gs} = -\frac{\partial Q_g}{\partial V_s} = \frac{WC_{OX}}{v_{sig}}\int_{x=0}^{x=L} v_{ac}(x)dx \tag{5-14}$$

in which L and W are the length and width of the MOSFET, respectively, v_{ac} is the small signal potential along the channel, v_{sig} is the small signal voltage applied to the source in order to measure C_{gs}, and C_{ox} is the gate oxide capacitance per unit area. For fresh device, there are no negative trap charges near drain. Hence v_{ac} changes uniformly from source to drain terminal. After HC stress, due to the presence of negative trap charges near drain, v_{ac} near drain increases. Therefore the value of equation (5-14) increases and C_{gs} increases dramatically after HC stress. It implies that input matching has been changed at high frequency. It should be pointed out that depending on bias point, C_{gd} changes slightly, as confirmed by the data in [28]. As a result, the variation of C_{gd} is too small to have any significant effects on the RF performance of the MOSFET compared to that of C_{gs}.

Fig. 5-8 shows the degradations of g_{m0} and R_{ds} with increasing stress time. The degradations of g_{m0} are more serious when biasing at lower gate voltages. R_{ds} decreases initially and then increases with increasing stress time. They are all in agreement with the discussions in Chapter 3, Section 3-2. We also found that drain resistance increases slightly which is due to the generation of negative trap charges near drain terminal after HC stress.

5.3 Modeling of RF MOSFET after Oxide Breakdown

From Fig. 4-2, the gate leakage current almost didn’t change after SBD. Therefore we still use the equivalent circuit shown in Fig. 5-1 to establish the small-signal model of a MOSFET under SBD. On the other hand, due to the dramatic increase of gate leakage current after HBD shown in Fig. 4-2, we assume that there are two leakage paths generated in gate-to-source and gate-to-drain overlap regions. Therefore we add gate-to-source resistance (R_{gs}) and gate-to-drain resistance (R_{gd}) into the equivalent circuit shown in Fig. 5-1 to establish HBD model shown in Fig. 5-9. R_{gs} can be determined by fitting the low frequency value of S_{11} and R_{gd} can be determined by fitting the magnitude of S_{12}. Fig. 5-10 and Fig. 5-11 show the measured and modeled S-parameters to verify the accuracy of SBD and HBD models. The values of extracted parameters are shown in Table 5-2. It is obvious that the degradations of HBD are much more serious than that of SBD.

From Table 5-2, the decrease of R_{ds} is due to the non-uniform distribution of defects and channel length modulation. Since the surface mobility are degraded by interface state, g_{m0} decreased after oxide breakdown. We also found that C_{gs} and R_g increase after oxide breakdown which is due to the generation of interface state and oxide trap charge.

The extracted value of R_{gs} is equal to 6540Ω which is roughly agreement with the measured results in Chapter 4, Section 4-2 and R_{gd} is equal to 33kΩ. Therefore the main leakage path is formed in gate and source/channel overlap region after HBD. It also implies that the input impedance has been changed after HBD which is roughly in agreement with the discussions in Section 4-3.

Finally, we compare the degradations of extracted model parameters after HBD and HC stress listed in Table 5-3. It is clear that the degradations of HC stress are more serious than that of HBD. It is possibly because that the amounts of interface state and oxide trap charge are larger after HC stress as compared to that after HBD.

	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	τ (psec)
Before Stress	1.7	7.71	3.51	28.8	1400	0.057	0.210	0.38	0.358	3	288	2.8
After HCS	1.7	7.89	3.52	28	1400	0.058	0.231	0.38	0.358	3	282	2.8

(a)

	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	τ (psec)
Before Stress	1.7	7.71	3.51	45.2	1400	0.057	0.212	0.38	0.358	3	310	2.8
After HCS	1.7	7.89	3.52	41	1400	0.058	0.237	0.38	0.358	3	278	2.8

(b)

	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	τ (psec)
Before Stress	1.7	7.71	3.51	75	1400	0.0574	0.215	0.38	0.358	3	270	2.8
After HCS	1.7	7.89	3.52	76.2	1400	0.0578	0.239	0.38	0.358	3	209	2.8

(c)

Table 5-1: Extracted parameters before and after HC stress at (a) V_G=1.2V, V_D=1.2V, (b)V_G=0.8V, V_D=1.2V, and (c)V_G=0.65V V_D=1.2V.

	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	τ (psec)	R_{gs} (Ω)	R_{gd} (Ω)
Before Stress	1.7	7.71	3.51	45.2	1400	0.0574	0.212	0.38	0.358	3	310	2.8		
After SBD	1.73	7.71	3.51	43.4	1400	0.0574	0.212	0.38	0.358	3	303	2.8		
After HBD	1.84	7.76	3.51	40	1400	0.058	0.219	0.38	0.358	3	290	2.8	6540	33k

(a)

	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	τ (psec)	R_{gs} (Ω)	R_{gd} (Ω)
Before Stress	1.7	7.71	3.51	75	1400	0.0574	0.215	0.38	0.358	3	270	2.8		
After SBD	1.73	7.71	3.51	73.1	1400	0.0574	0.215	0.38	0.358	3	262	2.8		
After HBD	1.84	7.76	3.51	68.7	1400	0.0578	0.221	0.38	0.358	3	240	2.8	6540	33k

(b)

Table 5-2: Extracted parameters before and after HBD and SBD at (a) V_G=0.8V, V_D=1.2V, and (b) V_G=0.65V, V_D=1.2V.

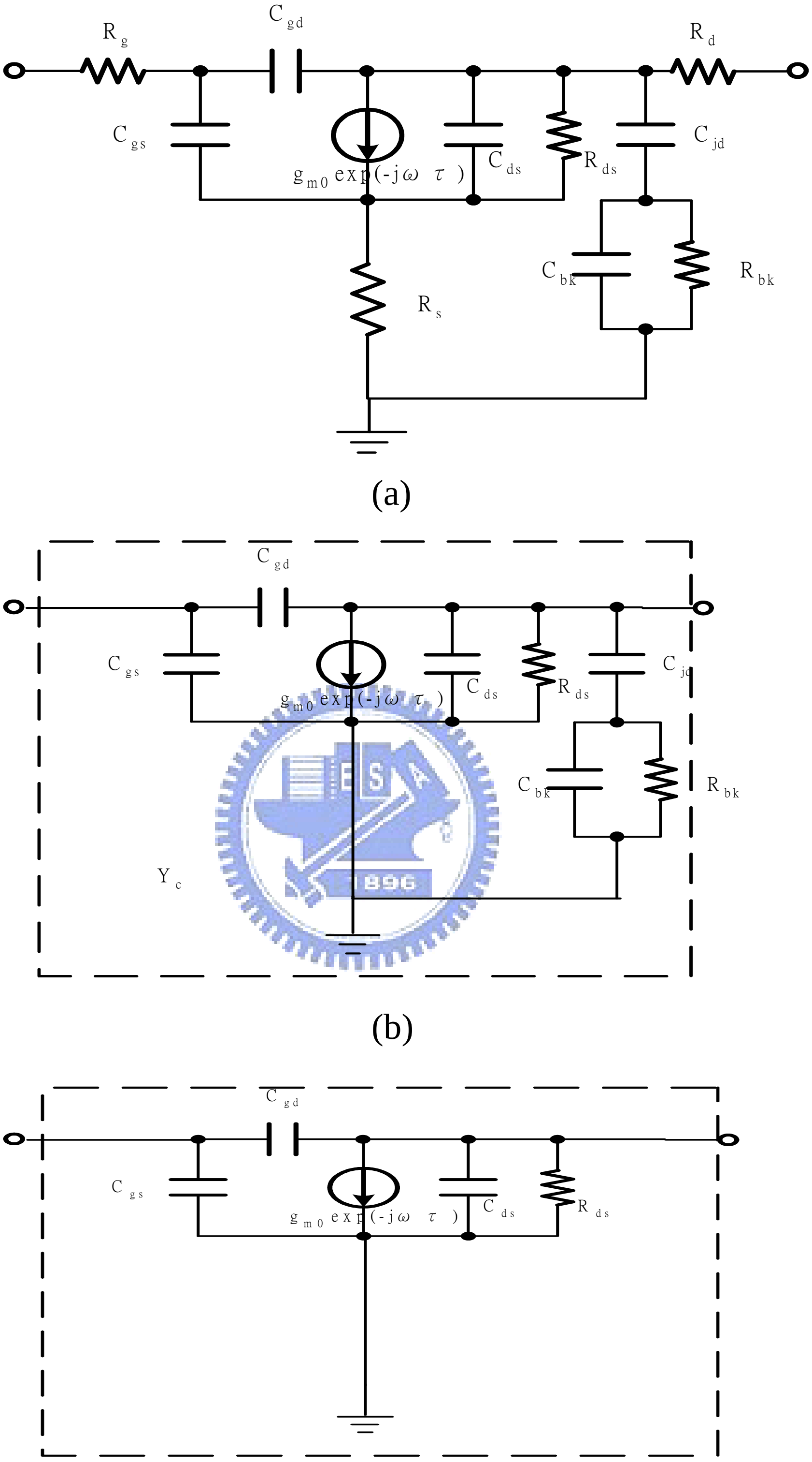
	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	τ (psec)	R_{gs} (Ω)	R_{gd} (Ω)
Before Stress	1.7	7.71	3.51	45.2	1400	0.0574	0.212	0.38	0.358	3	310	2.8		
After HCS	1.7	7.89	3.52	41	1400	0.0578	0.237	0.38	0.358	3	278	2.8		
After HBD	1.84	7.76	3.51	40	1400	0.058	0.219	0.38	0.358	3	290	2.8	6540	33k

(a)

	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	τ (psec)	R_{gs} (Ω)	R_{gd} (Ω)
Before Stress	1.7	7.71	3.51	75	1400	0.0574	0.215	0.38	0.358	3	270	2.8		
After HCS	1.7	7.89	3.52	76.2	1400	0.0578	0.239	0.38	0.358	3	209	2.8		
After HBD	1.84	7.76	3.51	68.7	1400	0.0578	0.221	0.38	0.358	3	240	2.8	6540	33k

(b)

Table 5-3: Extracted parameters before and after HC stress and HBD at (a) V_G=0.8V, V_D=1.2V, and (b) V_G=0.65V, V_D=1.2V.



(a)

(b)

(c)

Fig. 5-1: (a) Conventional small-signal model of a MOSFET. (b) Equivalent circuit after de-embedding parasitic components. (c) Small-signal model for the intrinsic part of a MOSFET.

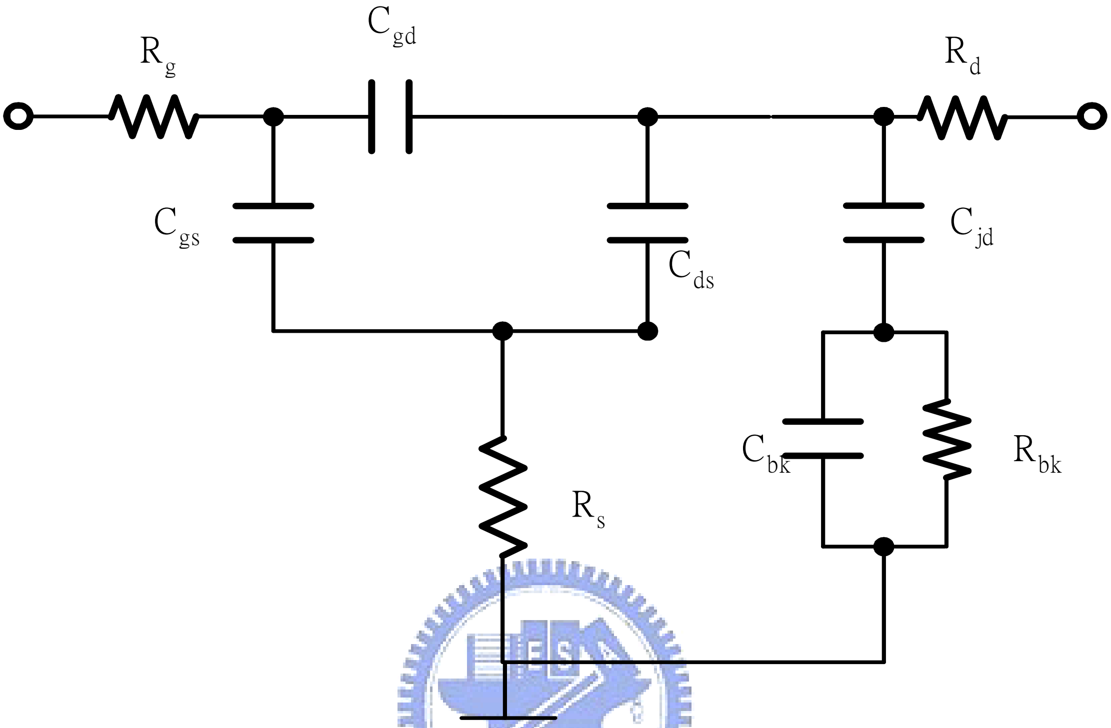


Fig. 5-2: Small-signal model of the MOSFET at the zero bias condition.

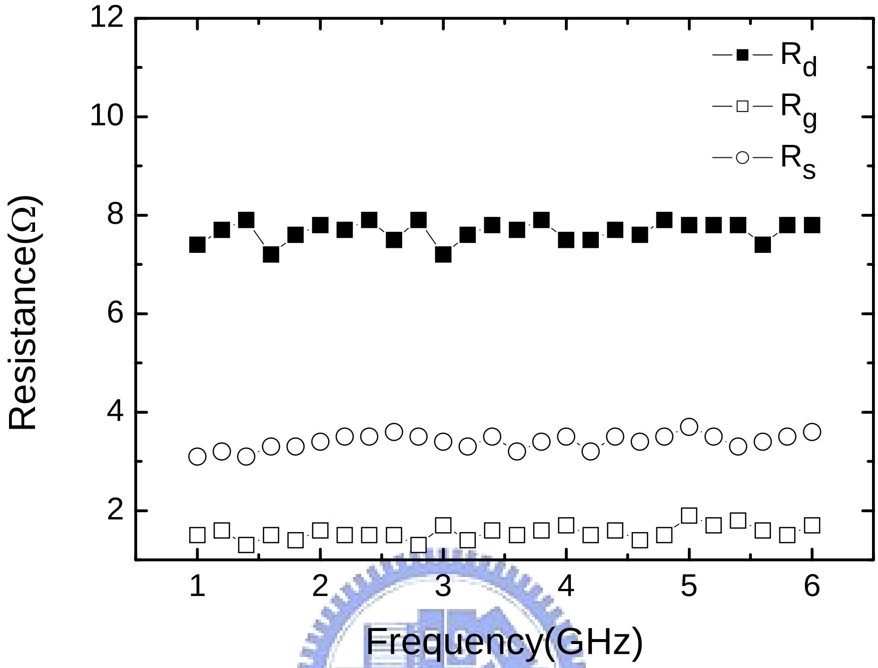
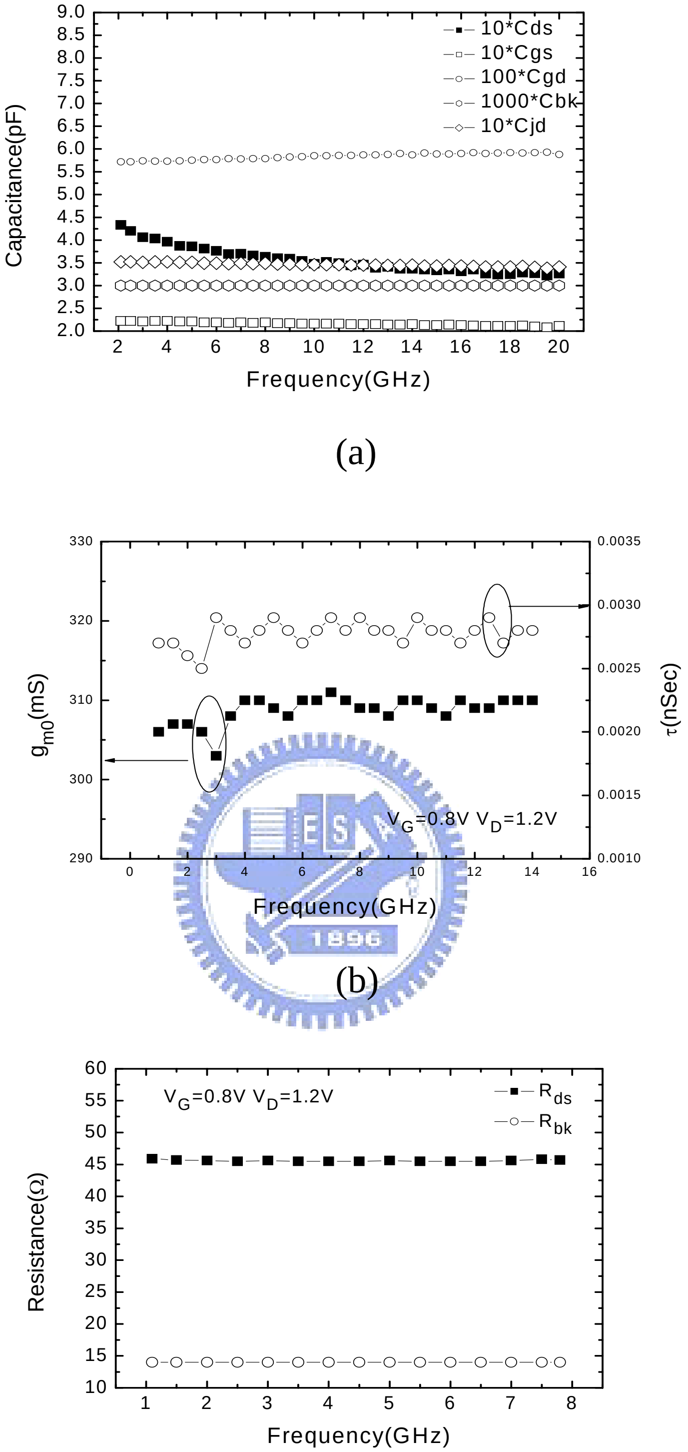


Fig. 5-3: Extracted values of R_s, R_g and R_d versus frequency.



(a)

(b)

(c)

Fig. 5-4: (a) Extracted capacitance versus frequency. (b) Extracted g_{m0} and τ versus frequency. (c) Extracted R_{ds} and R_{bk} versus frequency.

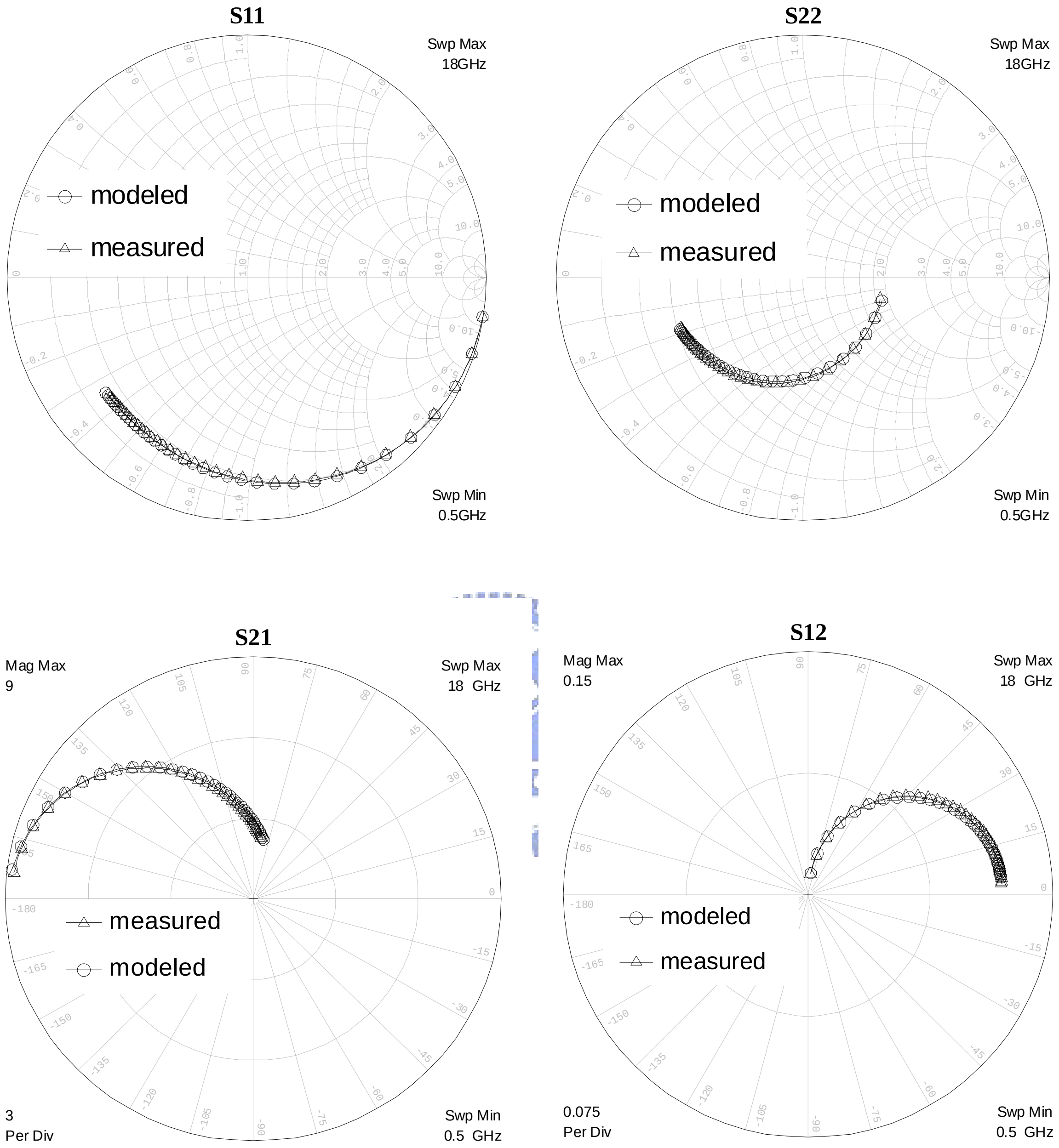


Fig. 5-5: Measured and modeled S-parameters of a MOSFET before stress at V_G=0.8V V_D=1.2V.

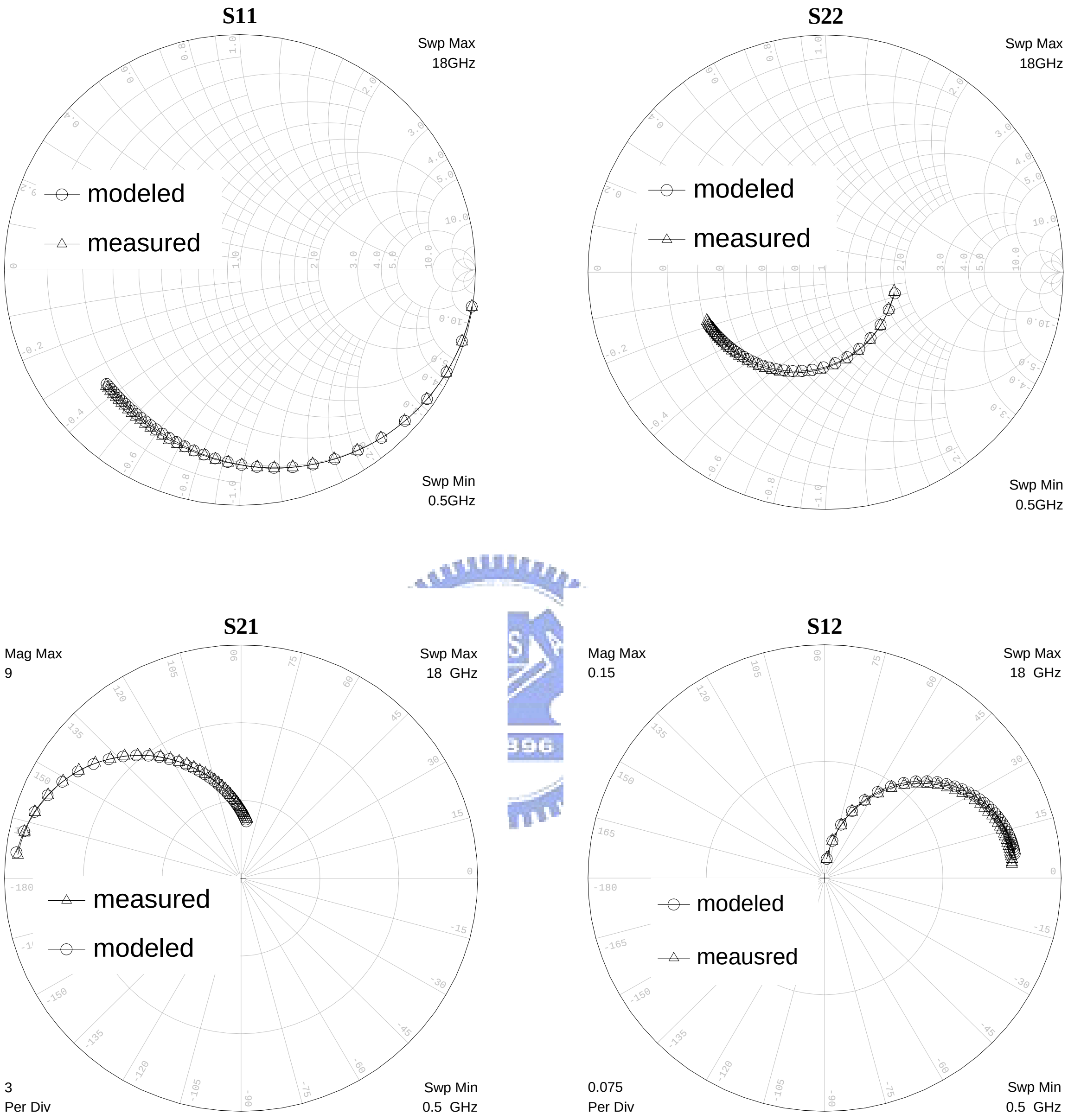
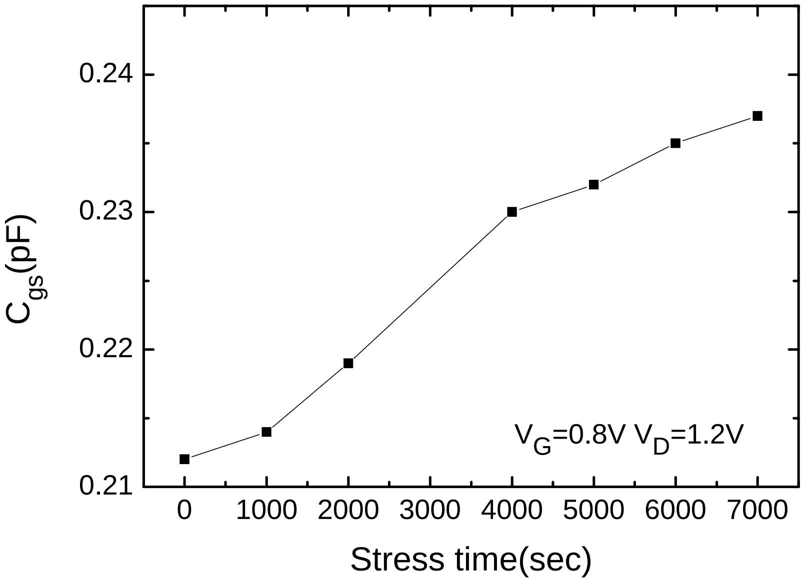
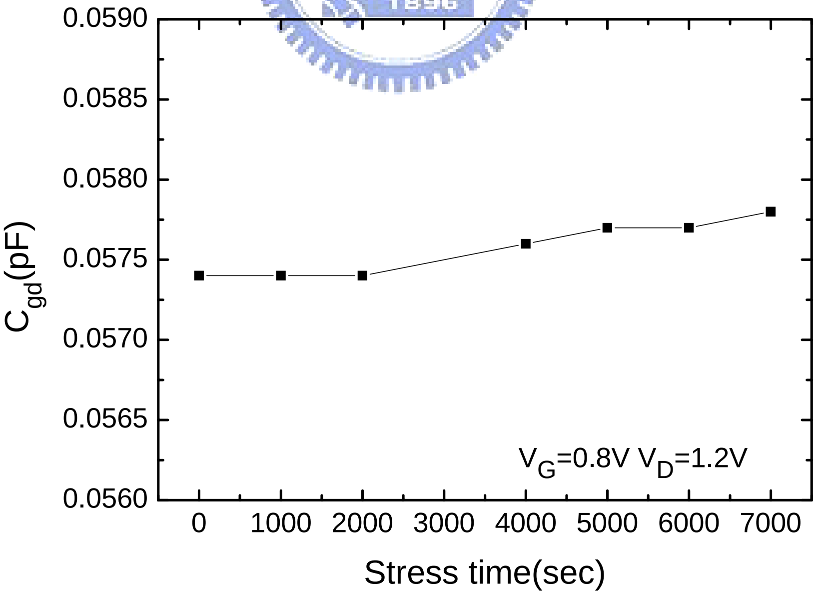


Fig. 5-6: Measured and Simulated S-parameters of a MOSFET after 7000s HC stress.

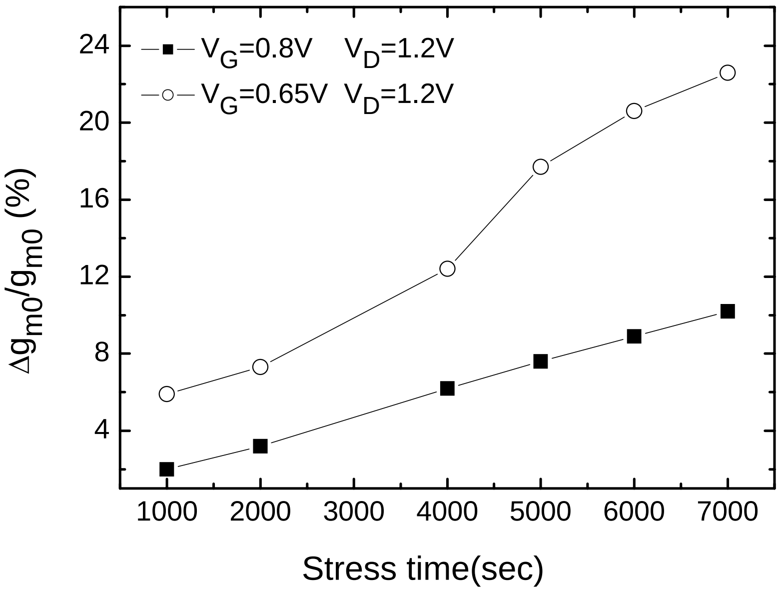


(a)

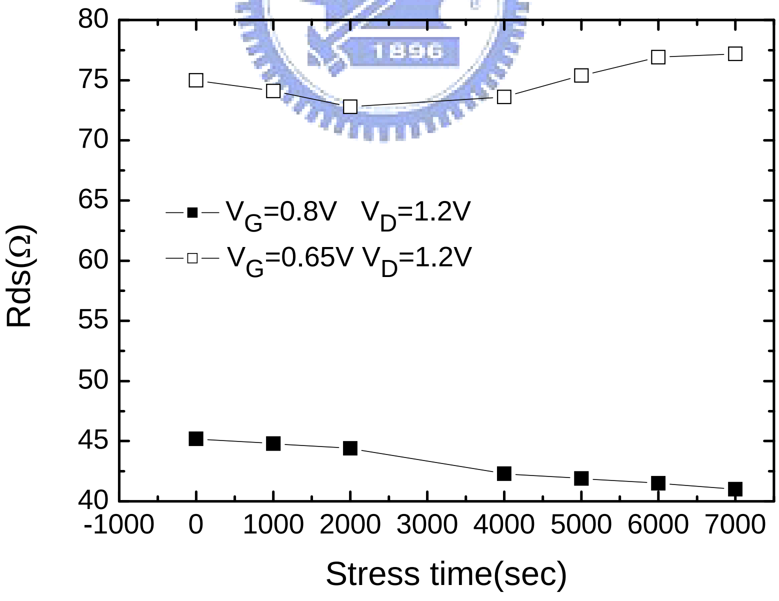


(b)

Fig. 5-7: (a) Extracted C_{gs} with increasing stress time.
(b) Extracted C_{gd} with increasing stress time.



(a)



(b)

Fig. 5-8: (a) Variations of Extracted g_{m0} with increasing HC stress time.
(b) Extracted R_{ds} with increasing HC stress time.

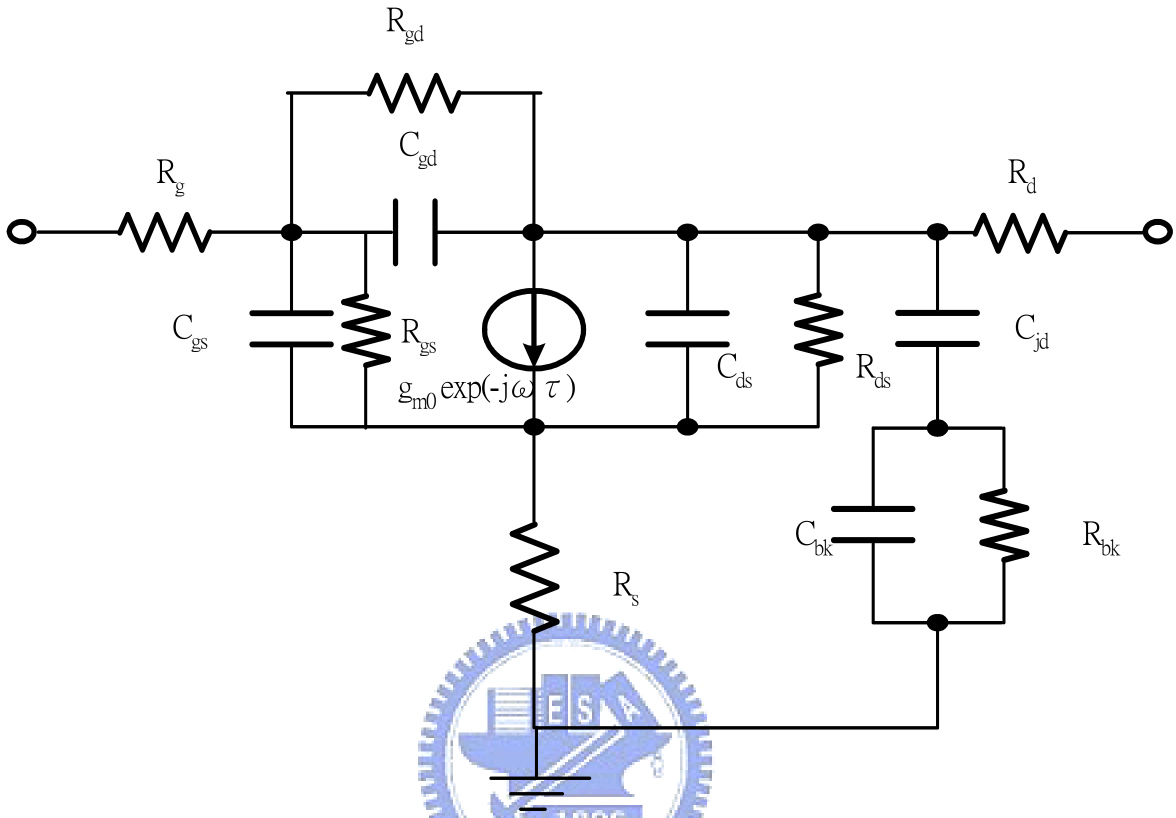


Fig. 5-9: Small-signal model of a MOSFET after HBD.

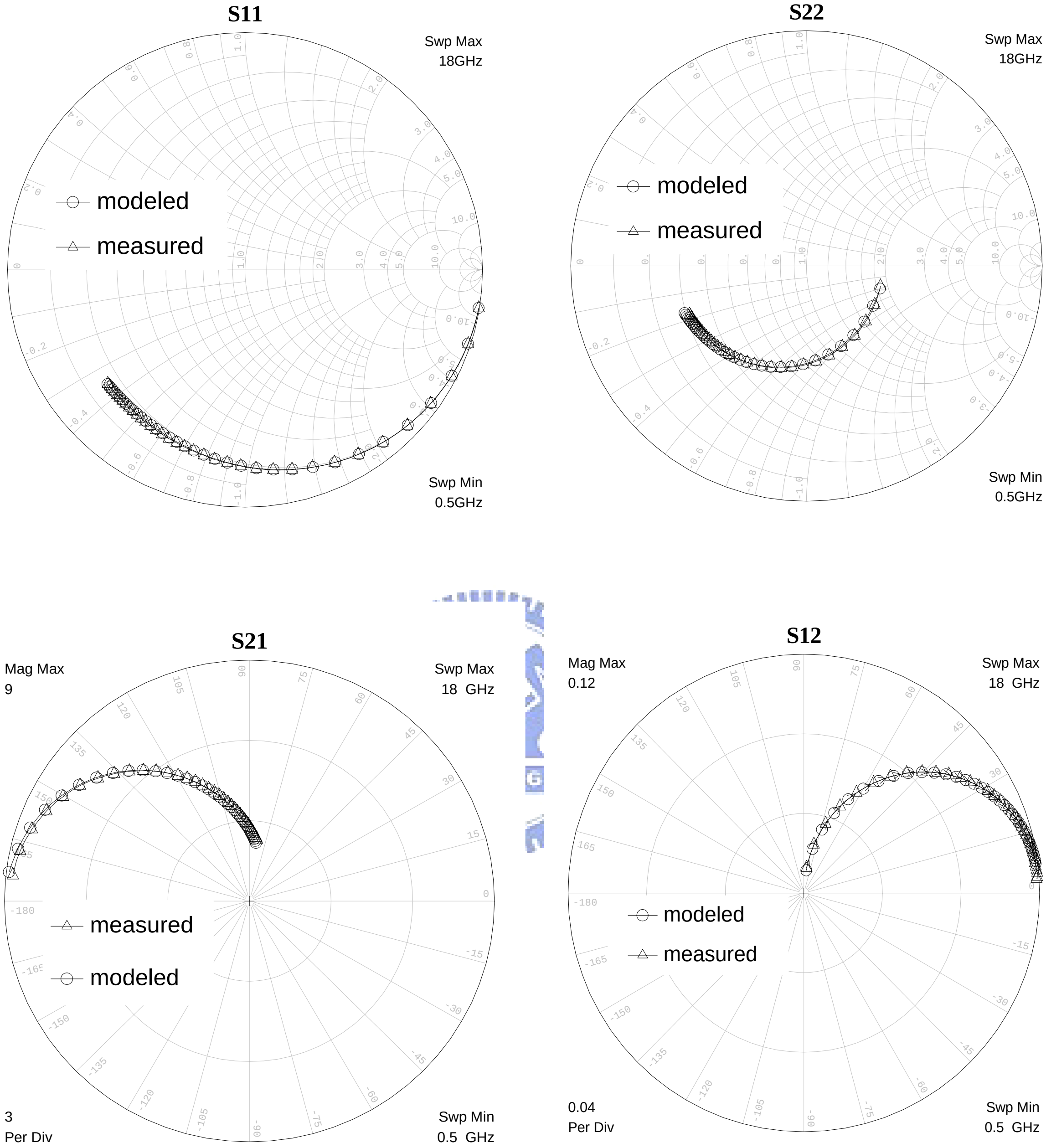


Fig. 5-10: Measured and modeled S parameters after SBD at V_G=0.8V, V_D=1.2V.

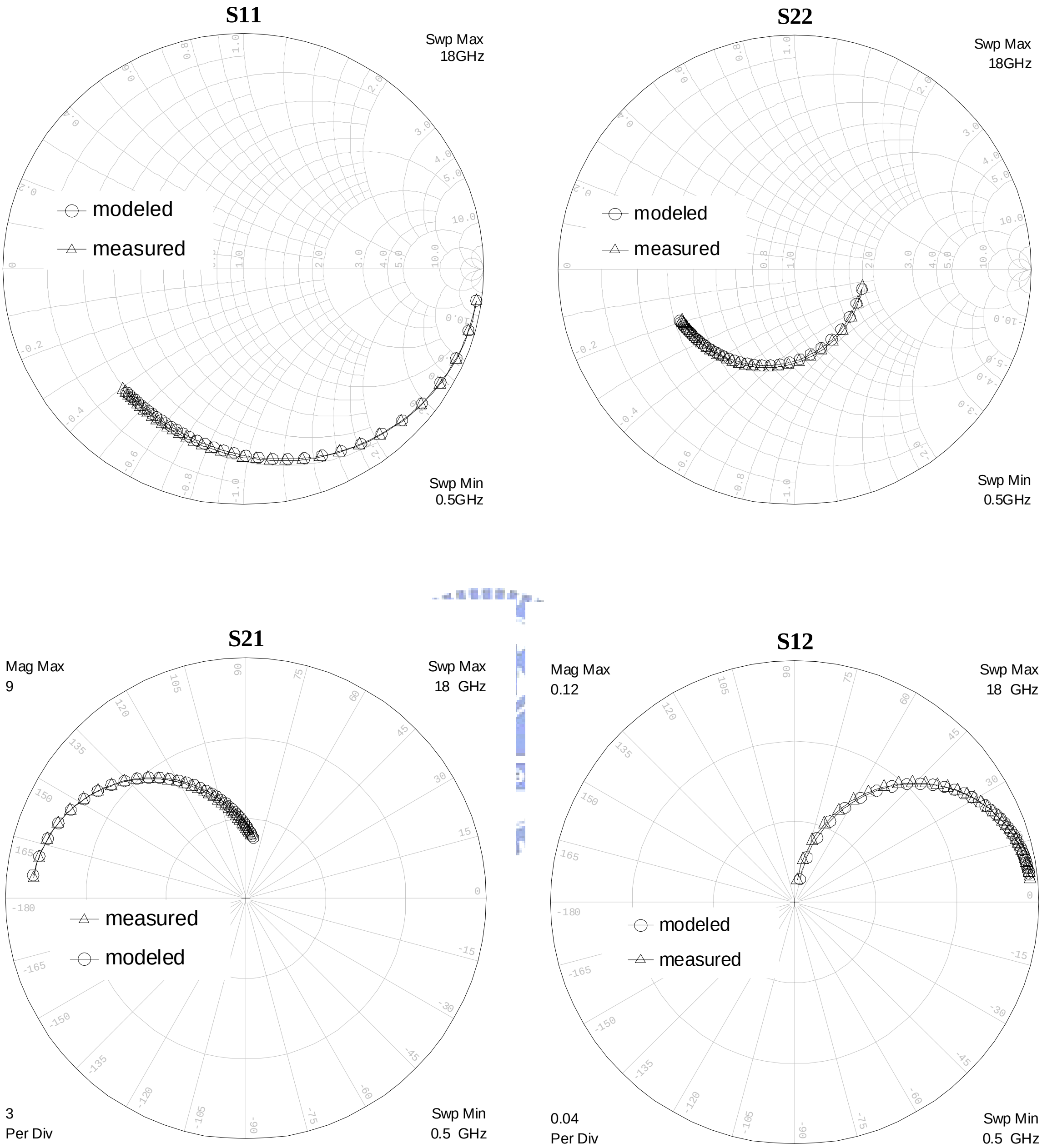


Fig. 5-11: Measured and modeled S parameters after HBD at V_G=0.8V, V_D=1.2V.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

MOSFET are getting more and more important in current commercial market especially for the RF applications. In this thesis, we have examined the effect of HC stress and oxide breakdown on RF MOSFETs. We also have established a conventional small-signal model for the MOSFETs under HC stress and oxide breakdown.

HCS and OBD all reduce the transconductance, output drain current and enlarge threshold voltage of the MOSFET. Consequently, the high frequency and power characteristics will suffer degradation by those effects. In the first instance, we found that the cut-off frequency and maximum oscillation frequency all decreased after stress. Then the RF output power will suffer degradation after HCS and OBD and we find that the RF power and gain are more robust to HC effects by biasing the gate voltage to higher values. On the other hand, the linearity suffers slight degradation after HCS and OBD if biasing the MOSFET at constant drain current. Thirdly, we found that HCS and OBD influence the noise characteristics of MOSFETs more seriously. Therefore the MOSFET reliability must be a critical concern while designing a low noise amplifier. In addition, unlike degradations of other electric parameters, the minimum noise figure suffered more degradation after HBD than that after HCS and it is due to the additional shot noise source in gate oxide after HBD.

Finally, from observing the small-signal model in chapter 5, we found that the transconductance, drain-to-source resistance, gate-to-source capacitance degrade significantly after HC stress and oxide breakdown. We also confirm that the main leakage path locate at the gate and source/channel overlap region.

From above discussions, HC stress and oxide breakdown induced degradations on power and noise performances should be taken into consideration in the design of the RF CMOS integrated circuits.

6.2 Future Work

Because the degradations of noise characteristics are serious, we should use the small-signal model to establish the noise model of MOSFETs under HCS and OBD. On the hand, an accurate large-signal model is necessary for the analog and RF IC designer. We should establish a complete large-signal model considering HCS and OBD effect. It may help us to explain the degradations of DC and power characteristics more clearly.

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