Chapter 1

Introduction

1.1General Background and Motivation

In recent years, organic thin film transistors(OTFTs) have attracted tremendous attention due to their potential advantages of easy processing, simple structure, large coverage area ,and low process temperature, providing compatibility with polymer substrates. It can be applied to low-cost large-area displays such as AMLCD/AMOLED, low end electronics such as smart card, identification tags or MRT tickets. The performance of pentacene base OTFT even can compare with hydrogenated amorphous silicon thin-film transistors.[1],[2].

There are four methods to form organic semiconductor film: (1)solution-processed deposition, (2)electro-polymerization, (3) vacuum evaporation, (4) Langmuir-Blodgett Technique [4]. Among a lot of organic semiconductor materials, we use Poly(3-hexylthiophene) P3HT as the semiconducting layer in our research because Poly(3-hexylthiophene) P3HT has many potential advantages for use the semiconduction layer in field-effect transistors. (1)Poly(3-hexylthiophene) P3HT is a well-known polymer as an organic semiconductor and has shown the field-effect mobility from 10^{-4} cm^2/Vs in 1988 to 0.2 cm^2/Vs in 2003. [3],[4],[5]. (2) Poly (3-hexylthiophene) P3HT has high solvent selectiveness, can dissolve in toluene, xylene, chloroform and so on. (3) Poly (3-hexylthiophene) P3HT is solution processed, therefore can be processed by spin coating.

1.2 Introduction of Poly(3-hexylthiophene) P3HT

The field-effect mobility of P(3-hexylthiophene) P3HT is strongly influenced by the

structure of the polymer chain and the direction of intermolecular π-π stacking. The structure of the polymer chain of P3HT had been shown in Fig. 1-1. The 3-alkyl substituents can be incorporated into a polymer chain with two different regioregularities: head to tail(HT) and head to head(HH)[6],[7]. R represents the alkyl side chain(C6H13 for P3HT), which allows P3HT to be dissolved in solvents like chloroform. This solution processability enables simple film deposition. A regiorandom P3HT consists of both HH and HT 3-hexylthiophene in a random pattern while a regioregular has only one kind o 3-alkylthiophene, either HH or HT. This type of order is known as regioregularity and has been shown to give much higher field-effect mobility values over regiorandom material[8]. In our experiments, regioregular P3HT (HT regioregularity of 98.5%) and high grade solvent, chloroform, were purchased from Aldrich Chemical Company. A dramatic increase in mobility was observed relative to regiorandom poly-3-alkylthiophenes[9] when regioregular P3HT consisting of 98.5% head to tail(HT) linkages, so we did not perform further purification to these chemicals in our experiments. After being deposited on the substrate, P3HT backbones may form tow different morphologies, edge-on or face-on of lamella structure as shown in Fig1-2. the higher mobility is give by edge-on structure since the carriers can move more efficiently through intra-chain transport along the direction of π-π stacking. Two different methods are applied to deposit the P3HT film, one is spin coating and while the other is dip coating. The mobility of dip-coated films is usually higher than that of the spin-coating that's maybe due to the evaporation rate of solvents. Lower evaporation rate results in a slower crystal growth with better ordered polymer structure[10],[11]. In spite of that method provide the higher field effect mobility, the dip-coating method can not be applied for coverage of a large area. Therefore, in all of our experiments, we used spin-coating technique as a key process of organic layer deposition.

1.3 P3HT base OTFT use Bottom-Contact Structure

There are two different designs of contemporary OTFTs. One is the so-called top-source-drain contact (TP) or top-electrode TFT design, where both source and drain contact pads are deposited on top of an active layer through a shadow mask. The other is named as bottom-source-drain contact (BC) or bottom-electrode TFTs, where drain and source contact metal is patterned on the gate dielectric prior to the active layer deposition. In general, the field effect mobility of top-source-drain contact(TP) TFTs are one order larger than bottom-source-drain contact(BC). It attribute to the morphologies of active layer that is more disorder when the active layer is deposited on metal. The advantage of BC is the pattern process can use conventional lithography technique. We choose the bottom-source-drain contact (BC) design in our experiment. The schematic diagram of the OTFT in this experiment is shown in Fig 1-3, and the comb structure for source/drain electrodes is shown in Fig 1-4. An+ type silicon wafer is formed as common gate electrode. Source and Drain metal patterned by lift-off method use conventional lithography technique after formed the insulator. The device is complete after deposit the P3HT for active layer.

1.4 Operation of Organic Thin Film Transistor

Refer to [3], the operation of the P3HT base OTFT is described below. Organic thin film transistors are opposed to the usual inversion mode operation of silicon MOSFETs and primarily operated as a P-type accumulation-mode enhancement type transistor.

Mode (A):When zero bias was applied to three contacts of OTFT, the schematic diagram is shown in Fig 1-5(a). if applied a small drain bias, Vd, in this condition, the source-drain current, Ids, will be small and ohmic.

Mode (B):When a negative bias,Vg, is applied to the gate electrode, the schematic diagram is

shown in Fig 1-5(b), the voltage is dropped over the insulator and over the semiconductor near insulator/semiconductor interface and accumulate more positive charge in the accumulation region. The additional positive chare is supplied by the ohmic source and drain contact and will reduce the resistance of channel. When a small bias is applied on the drain contact, the source-drain current will larger than that of Mode A

Mode(C):When a positive bias is applied the band bending occurs in the semiconductor at the insulator interface. Charge will reject from the interface and depletion region will form, the schematic diagram is shown in Fig 1-5(c). The channel resistance is large so the source-drain current will smaller than that of Mode A. Because of the large band gap, inversion layer cannot be observed in the organic TFTs.

Mode(d):When a negative enough bias than gate is applied to drain electrode in mode(a), the positive charge near the drain will be swiped in to drain electrode and form a depletion region . the schematic diagram is shown in Fig 1-5(d). This condition is similar to saturation mode of silicon MOSFETs. In this mode the source-drain current will not increase with increase drain bias voltage.

1.5 Thesis Organization

In chapter 1, we describe our background and motivation of our study.

In chapter 2, we employ different electrode materials such as Ni, Cr, Pt such as Ni, Cr, Pt to find another contact materials can substitute the Au that is expensive. Next we change the thickness of source/drain adhesion layer to research the influence of the distance between the contact metal and the interface of organic semiconductor and insulator.

In chapter 3, we investigate the electric reliability of P3HT OTFTs during various electrical stress conditions. Research the hot carrier degradation and polarization phenomenon in P3HT OTFTs.

In chapter 4, we fabrication the P3HT-based OTFTs with low temperature process (the max process temperature is 120℃). The insulator is silicon dioxide which is formed by LPD (Liquid Phase Deposition) method and we use an isolation dielectric structure to suppress gate leakage current.

In chapter 5, we will describe the conclusions and future work.

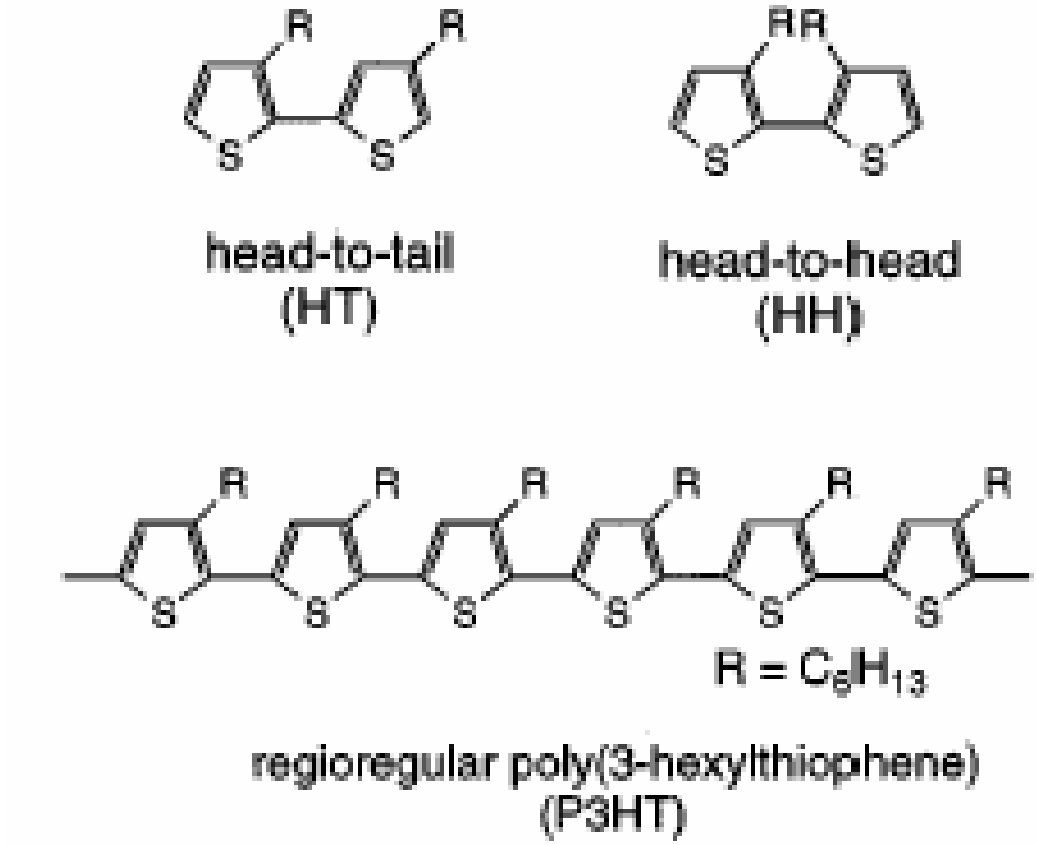
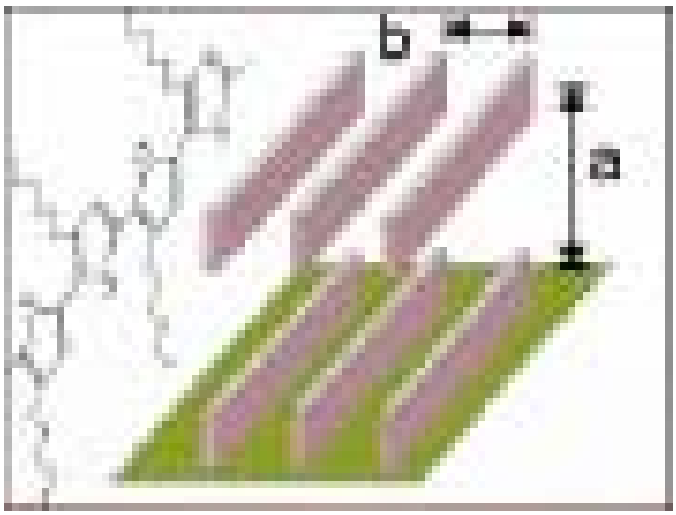
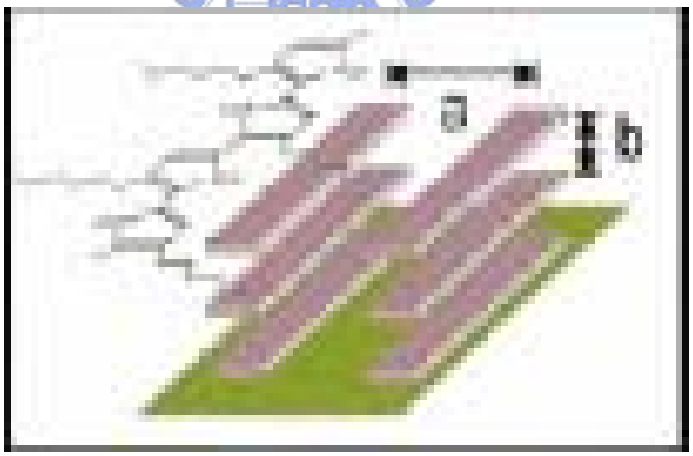


Figure 1-1:The structure of the polymer chain of P3HT



(a)



(b)

Figure1-2: Two different orientations of ordered P3HT(a)Edge-on orientation(b)Face-on orientation

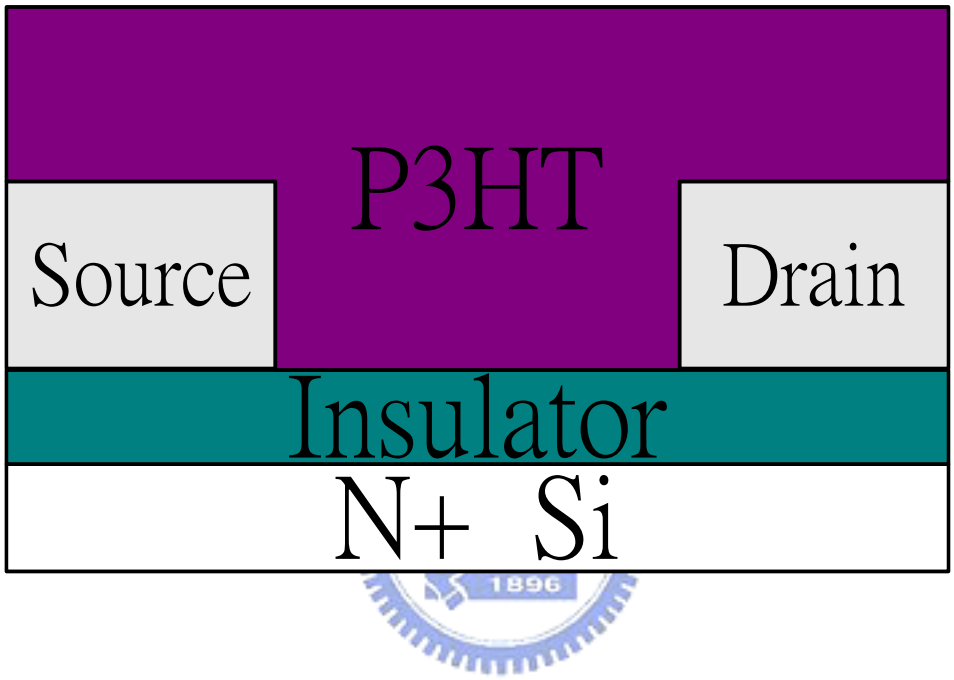


Figure1-3:The schematic diagram of the Bottom-contact OTFT

Figure 1-4:The comb structure for source/drain electrodes

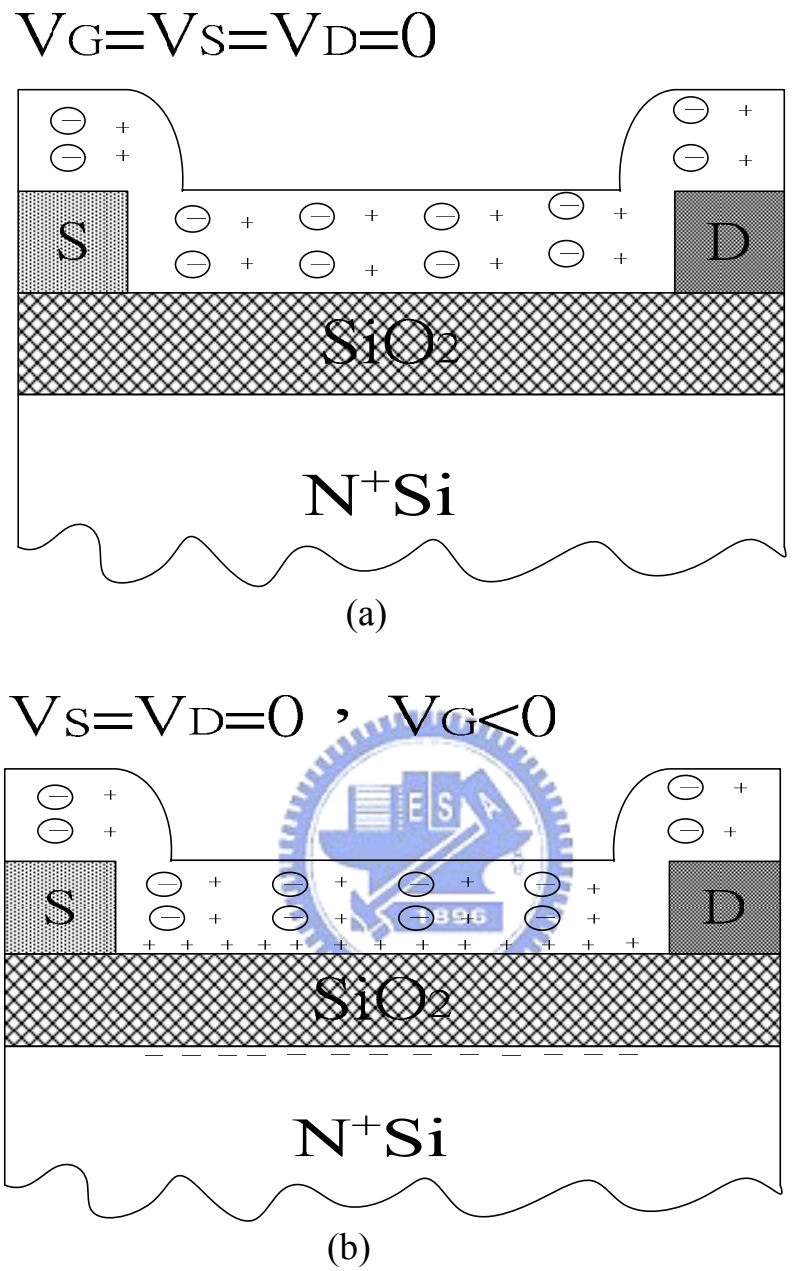
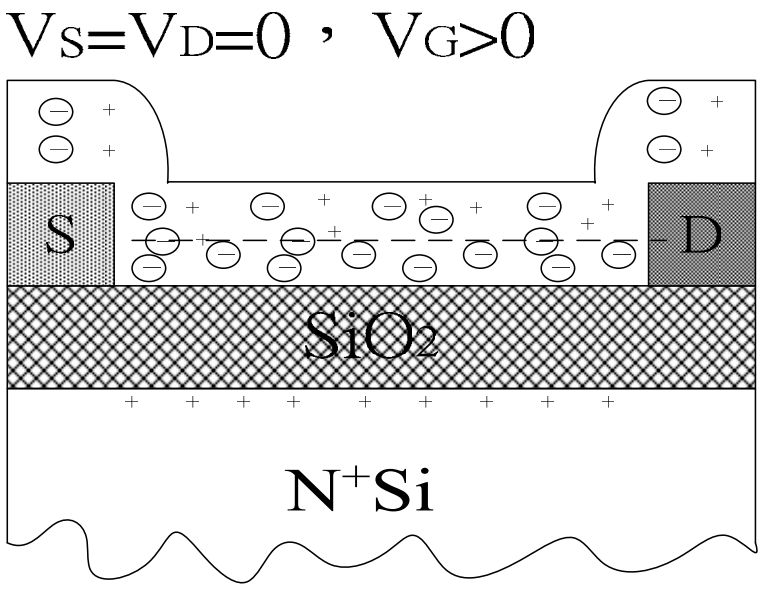
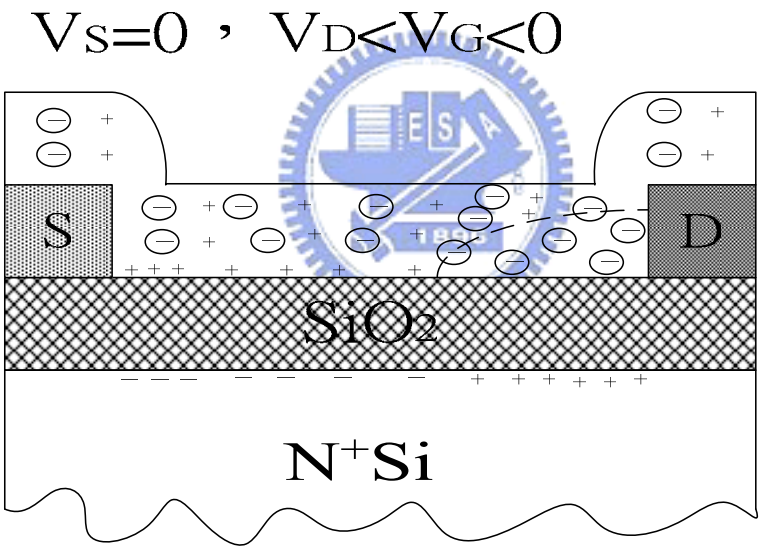


Figure 1-5:Schematic of operation of organic thin film transistor, showing a lightly p-doped semiconductor: + indicates a positive charge in semiconductor ; - indicate a negatively charge counterion(a) no-bais (b) accumulation mode (c) depletion mode (d) channel pinch-off (continute)



(c)



(d)

Figure 1-5:Schematic of operation of organic thin film transistor, showing a lightly p-doped semiconductor: + indicates a positive charge in semiconductor ; - indicate a negatively charge counterion(a) no-bais (b) accumulation mode (c) depletion mode (d) channel pinch-off

Chapter 2

Contact Resistance of P3HT OTFTs

2.1 Introduction

There are many parameters will impact the performance of OTFTs. The contact resistance between the source/drain electrodes and the organic semiconductor is an important one of them[12],[13],[14]. The contact resistance between the source/drain electrodes and the semiconductor becomes increasingly important to device performance as the channel length decreases. The contact resistance dominates the overall device resistance when the channel length is small enough.

Materials of source/drain electrodes and the source/drain structure both affect the contact characteristics between the source/drain electrode and the organic semiconductor. Unlike the FET of single-crystalline silicon, polycrystalline silicon, or hydrogenated amorphous silicon, the P3HT material cannot be optimized easily by semiconductor doping or silicide formation. Such properties of organic semiconductors deteriorate the performance of devices; moreover, the chemical compound always increase the contact resistance between the source/drain electrode and the organic semiconductor[15],[16]. It is a straightforward method to find a suitable electrode material which forms ohmic contact with the organic active layer and thus to improve the performance of OTFTs. Au is a well know material applied in OTFTs as the contact material. It is stable and the work function is match with P3HT, but just too expensive. In this chapter, we try to find the other cheaper material to substitute Au. Therefore we employed different electrode materials, such as Ni,Cr and Pt to check whether it can form good ohmic contact between the source/drain electrodes and the organic semiconductors. Next, we adjust thickness ratio of the

adhesion layer over the contact metal to check its effect to the contact resistance and the ON current.

2.2 Fabrication of Organic Thin Film transistors

2.2.1 Process Flow of P3HT-base OTFTs Fabrication

The P3HT TFTs use a bottom-contact structure fabricated on a silicon substrate as shown in Fig 1-3(a). The P3HT device process flow is as following. At first, an n-type bare silicon wafer was cleaned by the standard RCA cleaning process. After that, phosphorus atoms were diffused into an n-type silicon wafer by $POCl_3$ to form a common gate electrode. After diffusing, we used dilute HF to remove SiO_2 and measured its sheet resistance(3~4Ω/□) .Before the insulating layer of silicon dioxide was deposited, the n+ silicon wafer must be cleaned by the standard RCA cleaning process again. An insulating layer of silicon dioxide is deposited on the silicon substrate by PECVD using TEOS and O_2 source gas at 350℃. Afterwards, source and drain regions were defined through the photo lithography process followed by thermal evaporation steps of 20-nm thick Ti as an adhesion layer and 100-nm contact material. Later, the wafer was then immersed in acetone to lift-off the photo resist and to form the source/drain regions. The samples after S/D patterning were treated with 3 minute IPA cleaning and 5 minute D.I water cleaning. Next, oxide surfaces were treated with hexamethyldisilazane (HMDS) to improve the adhesion between the polymer chain and the oxide surface. P3HT of 0.3 wt.% dissolved in chloroform was deposited by the spin-coating method to form the active layer. P3HT solution was filtered by a 0.2-μm pore-size PTFE filter and then spun onto the wafer surface. The detail spin-coating parameters is: 200RPM for 10s, 500RPM for 25s and 2000RPM for 25s. Finally, the sample was cured at 120℃ for 3 minutes. Process flow is shown in Fig2-1.

2.2.2 Modification of Oxide Surface

Oxide surfaces were treated with hexamethyldisilazane (HMDS) to improve the adhesion between the polymer chain and the oxide surface. Modification of the substrate surface prior to the deposition of regioregular P3HT has also been found to influence the film morphology. For example, treatment of SiO_2 with hexamethyldisilazane (HMDS) replaces the hydroxyl groups at the SiO_2 surface with methyl or alkyl groups. The apolar nature of these groups apparently attracts the hexyl side chains of P3HT, favoring lamellae with an edge-on orientation **[7].** According to [7], the mobility of OTFTs with an edge-on orientation P3HT film is higher than that with a face-on orientation.

2.2.3 The Layout of Bottom-Contact OTFT

There are two kinds of layout: linear type and finger type as shown in Fig2-2. An interdigitated geometry as shown in Fig 2-2(b) for the source/drain contacts is chosen to minimize the device area and the associated gate to source/drain leakage current. The linear type: the channel length (L) is in a range of 10~50 μm and the channel width is in a range of 300~500 μm. The finger type: the channel length (L) is in a range of 10~50 μm and the channel width is in a range of 10000~1000 μm

2.3 Electrical Characteristics of P3HT OTFTs

2.3.1 Measurement

Current-voltage characteristics of OTFT were measured in the air with a semiconductor parameter analyzer HP4156. All measurements were carried out in an electrically shielded box. The drain-source current, I_{DS}, was measured as a function of the drain-source voltage, V_{DS}, to observe FET-like characteristics. And also I_{DS} was measured as a function of the gate voltage, V_G,

at small drain-source voltage, which was constructed to determine the gate bias modulation of the FET conductive channel.

Three parameters were extracted from the experimental I-V curves: (1) the transistor threshold voltage (V_T), (2) the current modulation (the ratio of the current in the accumulation mode over the current in the depletion mode, also referred to as ON-OFF current ratio), and (3) the field effect mobility (μ). The detail extraction method will be discussed in the following section.

2.3.2 Threshold Voltage and OFF Current Definition

Inorganic semiconductors, such as Si or Ge, can be operated in three modes: depletion mode, accumulation mode, and inversion mode. For organic semiconductors such as P3HT OTFTs, they can not be operated in the inversion mode. Therefore, P3HT OTFTs were turned ON in the accumulation mode (V_G<0, see Fig1-4(b)) and were turned OFF in the depletion mode (V_G>0, see Fig1-4(c)).

Because P3HT OTFTs are normally ON devices, we defined that when the current is smaller than a certain value, it was called OFF-current. The corresponding gate voltage (V_G) was defined as threshold voltage (V_{th}). Therefore, we define the normalized off current (I_{OFF}) is 10^{-12} Amp and off current is I_{OFF} *W/L. The magnitude of off current with different channel length and different channel width is listed Table2-1

2.3.3 The Extraction Method of Mobility

P3HT OTFT is PMOS like FET. Therefore, the field effect mobility in the linear regime can be obtained by the calculation described below. At low drain voltage (V_D), source-drain current (I_{DS}) increases linearly with V_D (linear regime) and is approximately determined from the following equation (2-1):

$$I_{DS} = \frac{W}{L}\mu C_i (V_G - V_{th} - V_D/2)V_D \qquad \text{as } V_D << V_G - V_{th} \qquad \text{[Equation 2-1]}$$

where L is the channel length, W is the channel width, Ci is the capacitance per unit area of the insulating layer, V_{th} is the threshold voltage, and μ is the field effect mobility, which can be calculated in the linear regime from the transconductance,

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{WC_i}{L}\mu V_D \qquad \text{[Equation 2-2]}$$

by plotting I_{DS} versus V_G at a constant low V_D, with $-V_D << -(V_G - V_T)$, and equating the value of the slope of this plot to g_m. We can compute the linear regime mobility from equation 2-2

2.4 Experimental Detail

In this experiment, there are four different electrode materials such as contact metals, i.e. Cr, Ni and Pt evaporated by e-gun evaporation with the thickness of 100nm. For all materials, they must have an adhesion layer to prevent then from peeling from the SiO_2 surface. We used Ti as an adhesion layer with the thickness of 20nm.

Secondly, we caped very thin Pt on Ni or Cr S/D electrode to improve the contact characteristics.

Thirdly, We adjusted the thickness of adhesion metals. After photolithography process, we prepared four kinds of thickness of adhesion metals: 2nm, 5nm, 20nm and 100nm.

2.5 Results and Discussion

2.5.1 Extraction of Contact resistance of P3HT OTFT

We applied a simple model to estimate the contact resistance between source/drain electrodes and P3HT [17], [18] . For small drain bias V_D, and at high gate drive, it is assumed that

the OTFTs ON resistance, R_{on}, consists of the channel resistance, R_{ch}, and the contact resistance, R_c.

That is,

$$I_{DS} = \frac{W}{L}\mu C_i (V_G - V_{th} - V_D / 2)V_D \quad \text{as} \quad V_D << V_G - V_{th} \qquad \text{[Equation 2-3]}$$

$$R_{on} = \frac{\partial V_D}{\partial I_{DS}}\Big|_{\substack{V_G \\ V_D \to o}} = R_{ch} + R_c \qquad \text{[Equation 2-4]}$$

and the channel resistance in the linear region is given approximately by

$$R_{ch} = \frac{L}{W \mu C_i (V_G - V_T)} \qquad \text{[Equation 2-5]}$$

where L is the channel length, W is the channel width, Ci is the capacitance per unit area of the insulating layer, V_{th} is the threshold voltage, and μ is the field effect mobility. The contact resistance R_c can be extracted by measuring the ON resistance, R_{on}, from the linear region of OTFT output characteristics and by plotting R_{on} W as a function of L. For each device with L ranging from 10 to 50 μm, the drain current was measured at -1V for a gate voltage ranging from 0V to -30V. The resulting width-normalized ON resistance R_{on} W versus L is calculated and the contact resistance is a set of straight lines intersecting at a triangle area

2.5.2 Contact resistance of P3HT OTFT with difference Electrode Materials

P3HT can form an ohmic contact with metal for its work function larger than 4.5eV because the work function of P3HT is 4.5eV. Work functions of all materials we used are larger than 4.5eV; they include Ni(Φ_f=4.84eV), Pt(Φ_f=5.29eV), Cr(Φ_f=4.5eV). The output characteristics I_S vs. V_D of P3HT OTFTs which were fabricated with those contact materials stated above are

shown in Fig2-3. The resulting width-normalized ON resistance $R_{on}W$ versus L is plotted in Fig 2-4. The contact resistance is a set of straight lines intersecting at a triangle area and the results are shown in Table 2-2.

It must be a Schottky contact between Cr and P3HT, as shown in Fig2-1(a). The work function of Cr is 4.5eV that is equal to P3HT. We considered this result originated from the chemical reactivity of Cr with P3HT or the interfacial layer formed at the Cr surface. The work function of chemical compound between Cr and P3HT is smaller than 4.5eV and form the form a Schottky barrier with P3HT.

From Fig 2-1(b), it was observed that the crowding effect was occurred at the small drain bias near the zero voltage. In Table 2-2, we can find the contact resistance of OTFT with Ni as the source/drain contact material is much larger than that with Pt or Au as the source/drain contact materials. The crowding effect is caused by that the contact resistance between source/drain electrodes and the organic semiconductor is large enough to lead to Space-Charge Limited Current(SCLC) larger than ohmic current[19],[20]. The large contact resistance between Ni and P3HT is attributing to work function mismatch and chemical reactivity of Ni with P3HT or the interfacial layer formed at the Ni surface [21].

The output characteristics I_S vs. V_D of P3HT OTFTs with Pt source/drain contact material as shown in Fig 2-3(c) illustrate that the crowding effect is vanished. Pt is a noble metal; comparing to Ni or Cr, they do not react to oxygen or P3HT and contribute to good ohmic contact and small contact resistance. The performance of OTFT with Pt as the contact materials can compare with that with Au as the contact material.

2.5.3 Contact resistance of P3HT OTFT with capping Pt on Ni and Cr S/D metal

The output characteristics I_S vs. V_D of OTFT with Ni as contact metal showed an acceptable result. But the large contact resistance results in low ON current and crowing effect at the small

drain bias near the zero voltage. We attempted to improve the performance by capping a very thin Pt film on the Ni contact metal. The Pt film provides another current path when the drain bias is small near the zero voltage. The output characteristics I_S vs. V_D of capping Pt film on Ni and Cr contact metal is shown in Fig 2-5. The crowding effect is vanished and it exhibited a good I-V characteristics of P3HT OTFT with Ni as contact metal. Even the characteristics I_S vs. V_D of OTFT with capping Pt film on Cr as contact metal also showed a normal property. The resulting width-normalized ON resistance $R_{on}W$ versus L is plotted in Fig 2-6 and the contact resistance is a set of straight lines intersecting at a triangle area and the results are shown in Table 2-3.

It's effective to reduce the contact resistance of OTFT with Ni as contact metal by capping Pt film. Though the OTFT with capping Pt film on Cr as contact metal showed an acceptable property, the contact resistance is 3 times larger than those using Ni as the contact metal under the Pt film. It seems that the ohmic contact is rely on the thin Pt film only. Fig 2-7 shows the transfer characteristics (I_S vs. V_G) of OTFTs in the linear regime with different S/D contact metals and capping Pt film. According to the foregoing description, one can conclude that the OTFT with Pt as contact has an ideal transfer characteristic; OTFT with Ni as contact metal results in low ON current due to large contact resistance; OTFT with Cr as contact metal does not have any normal transfer characteristics; Capping a thin Pt film on Ni as S/D metal can effectively improve the performance by reducing contact resistance.

2.5.4 The Effect of the Thickness of the Adhesion Layer

We adjusted four kind of thickness of adhesion layer in this experiment including 2nm,5nm,20nm and 100nm. The transfer characteristics (I_S vs. V_G) and output characteristics I_S vs. V_D are shown in Fig2.8 and Fig2.9. The width-normalized ON resistance $R_{on}W$ versus L is plotted in Fig 2-10 and the contact resistance is a set of straight lines intersecting at a triangle

area and the results are shown in Table 2-4.

We cannot find particular different in transfer characteristics (I_S vs. V_G), output characteristics and contact resistance. It appear that thickness of adhesion layer isn't affect the performance of OTFT. We compiled the ON current at all W/L ratio device and plotted a normalize on current figure, Fig 2.11. We can find the ON current is inverse proportional to the thickness of adhesion layer. Thicker adhesion layer results in lower ON current. When applied a negative gate bias on OTFT and let the device operation in accumulate mode such as mode(A) that stated in chapter 1.4, the voltage is dropped over the insulator and over the semiconductor near insulator/semiconductor interface and accumulate more positive charge in the accumulation region. The accumulation region formed a low resistance channel and current will flow through this path, the current flow path is shown in Fig 2.12. The thicker adhesion layer result in the longer current flow route and current flow through a higher resistance region, therefore the series resistance will enlarge. So the ON current will decrease with increase the thickness of adhesion layer.

2.6 Summary

The effect of contact resistance between source/drain electrodes and P3HT has been experimentally investigated. We applied a simple model to estimate the contact resistance between source/drain electrodes and P3HT and found that the contact resistance is typically greater than the contact resistance of inorganic transistors.

Because the interfacial layer formed at Ni and Cr surface lead to large contact resistance, even the work function of both are larger(or equal) then P3HT. The crowding effect was occurred when the OTFTs were fabricated by Ni as contact metal. When OTFTs were fabricated by Cr as contact metal isn't shown normal property. Using Pt as S/D contact materials would result in better I-V characteristics.

Capping the thin Pt film on the Ni or Cr as contact meal can greatly reduce the contact resistance of OTFTs. The contact resistance of OTFTs with Pt film on Cr as contact metal is relatively larger than that with Pt film on Ni as contact metal because Cr layer cannot form ohmic contact with P3HT. The extracted field-effect mobility of OTFTs with Pt as contact electrode is 2.6 $x10^{-3}cm^2/V\text{-}s$, and with Pt film on Ni as contact electrode is $2.38x10^{-3}cm^2/V\text{-}s$. OTFTs with a capped thin Pt film on Ni as contact metal can instead of Au or Pt as contact metal for lower cost and acceptable performance.

Thickness of adhesion layer is not a critical parameter to affect the performance of OTFTs except the ON current distribution.

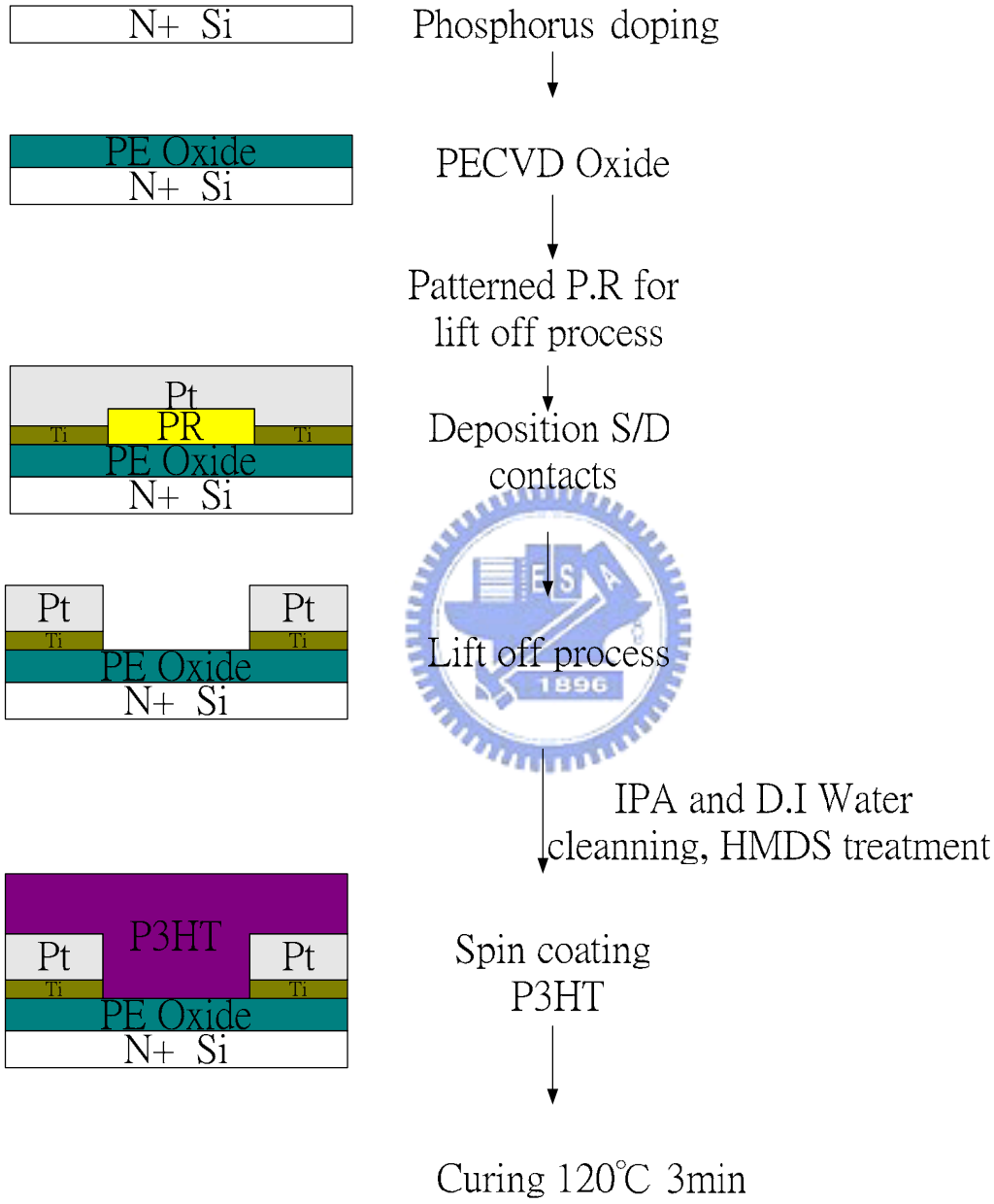
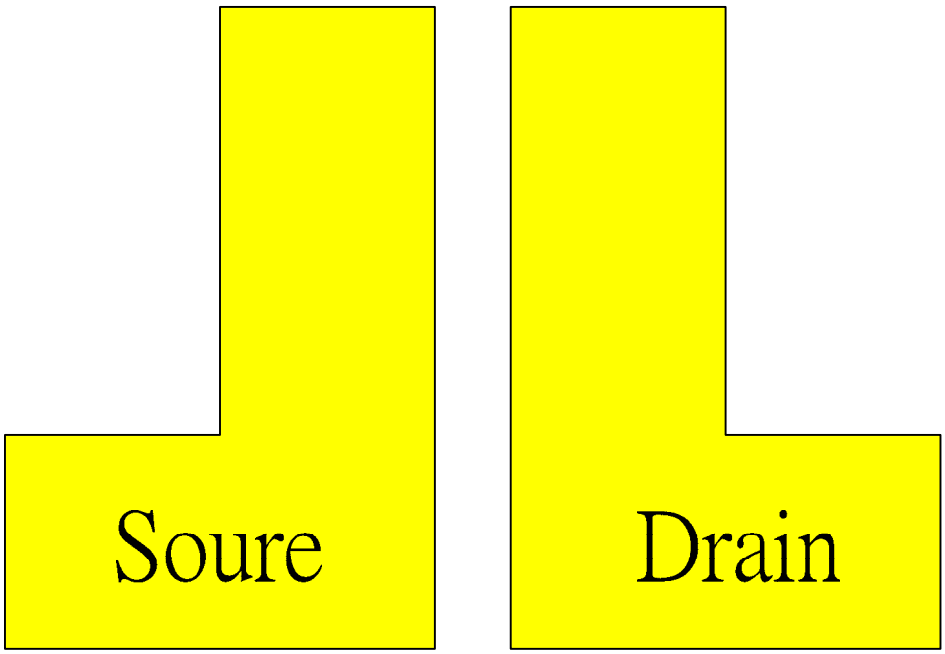


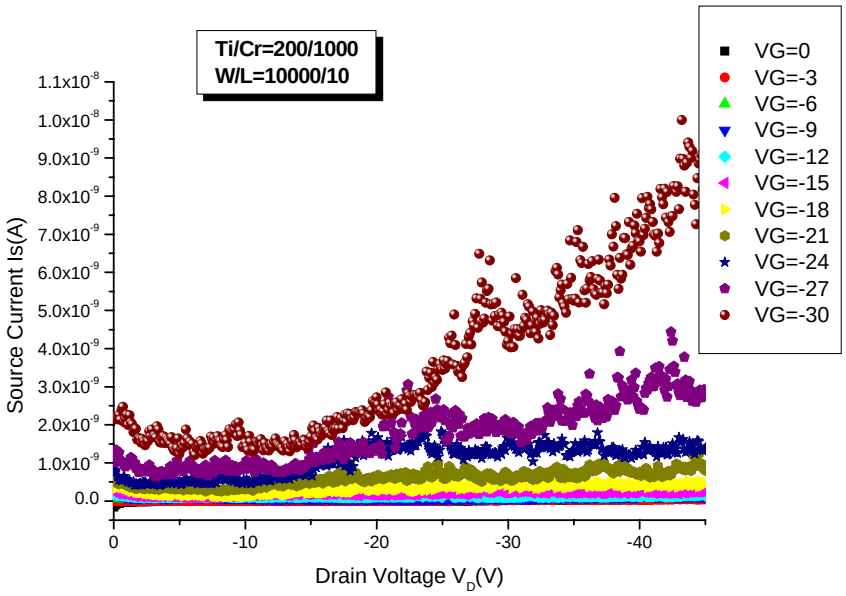
Figure2-1:Process flow of bottom-contact OTFTs



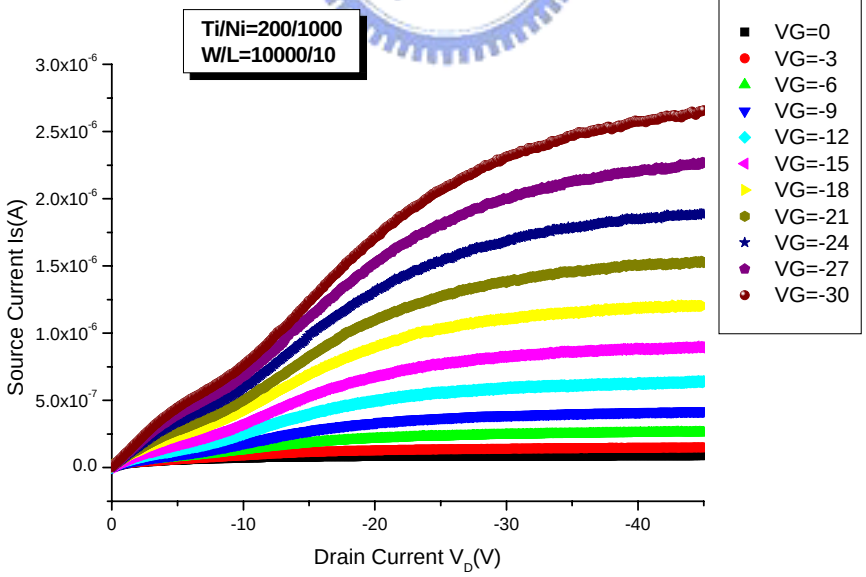
(a)

(b)

Figure2-2: Layouts of bottom-contact OTFTs (a) linear type (b) finger type

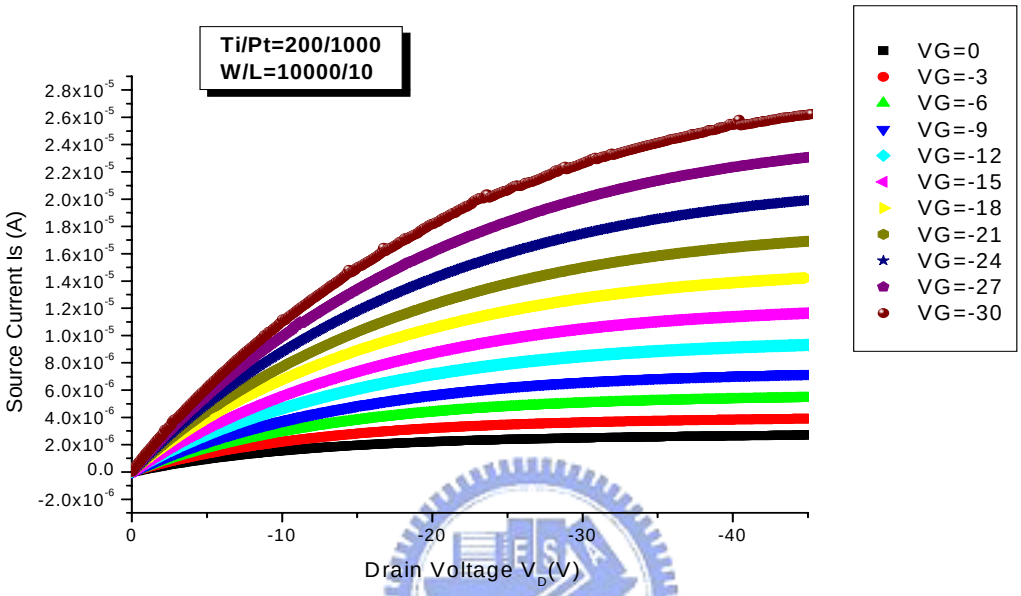


(a)



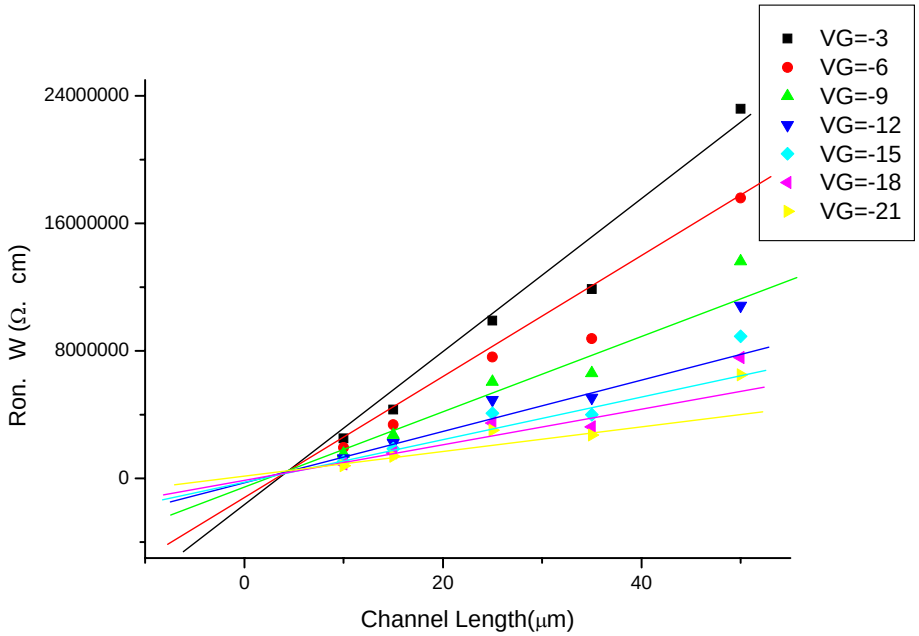
(b)

Figure 2.3: Output characteristics I_S vs. V_D of P3HT OTFTs with (a)Ti/Cr (b)Ti/Ni (c)Ti/Pt Source and Drain contact (continue)

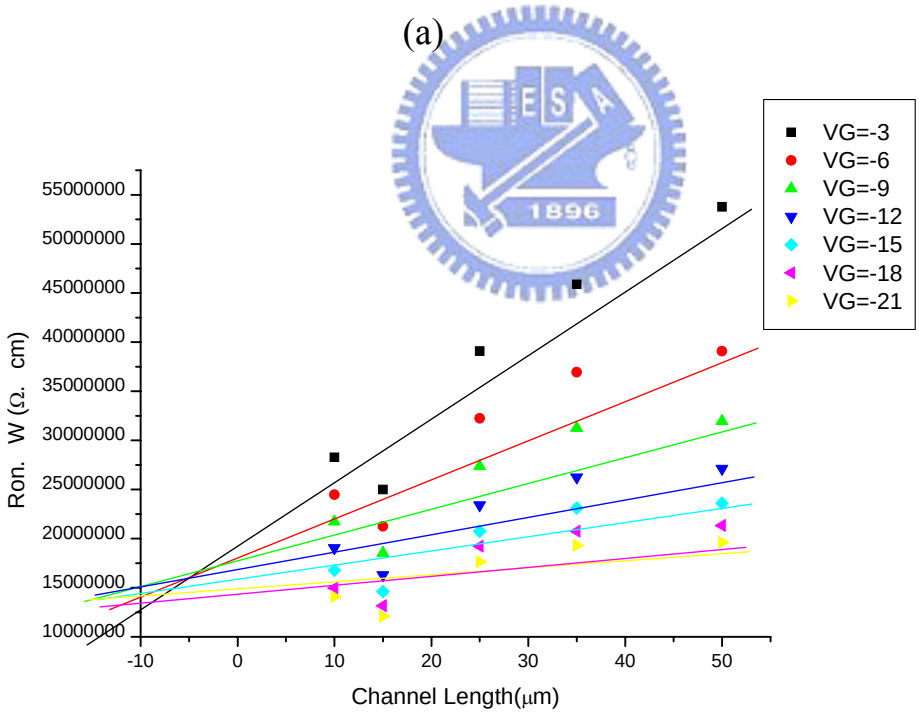


(c)

Figure 2.3: Output characteristics I_S vs. V_D of P3HT OTFTs with (a)Ti/Cr (b)Ti/Ni (c)Ti/Pt Source and Drain contact

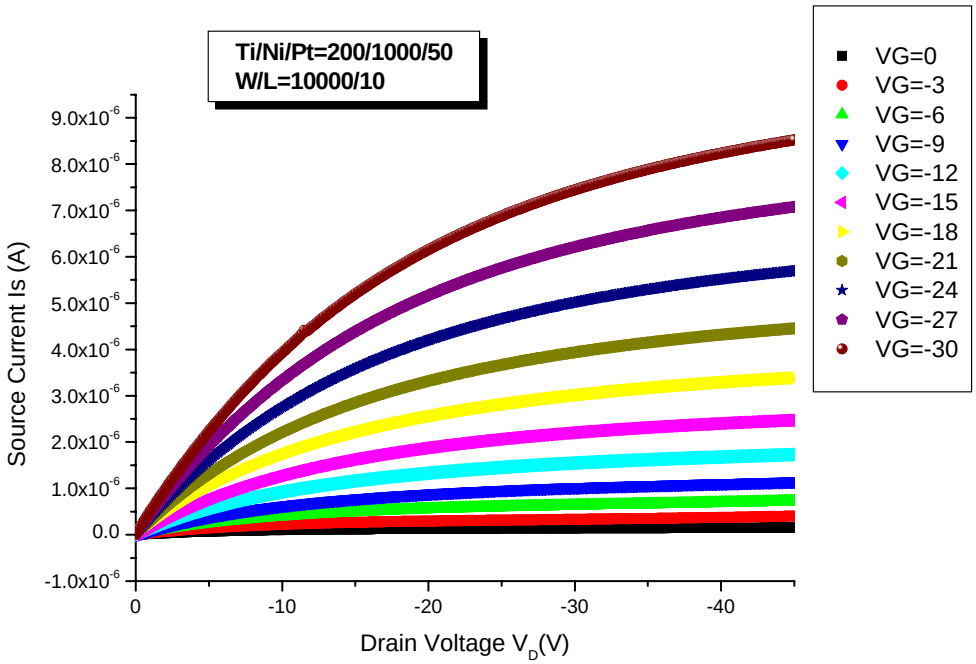


(a)

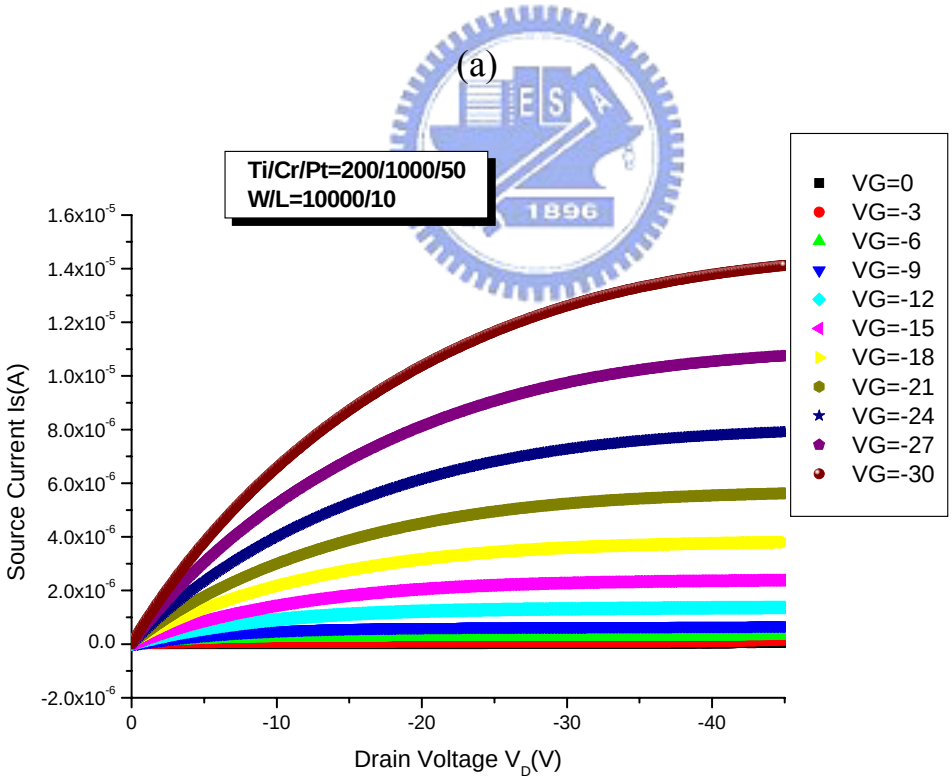


(b)

Figure 2-4: Width-normalized ON resistance as a function of channel length at different gate voltage and with (a)Ti/Pt (b)Ti/Ni Source/Drain contact metal. The solid lines represent the linear least square fit of the date.

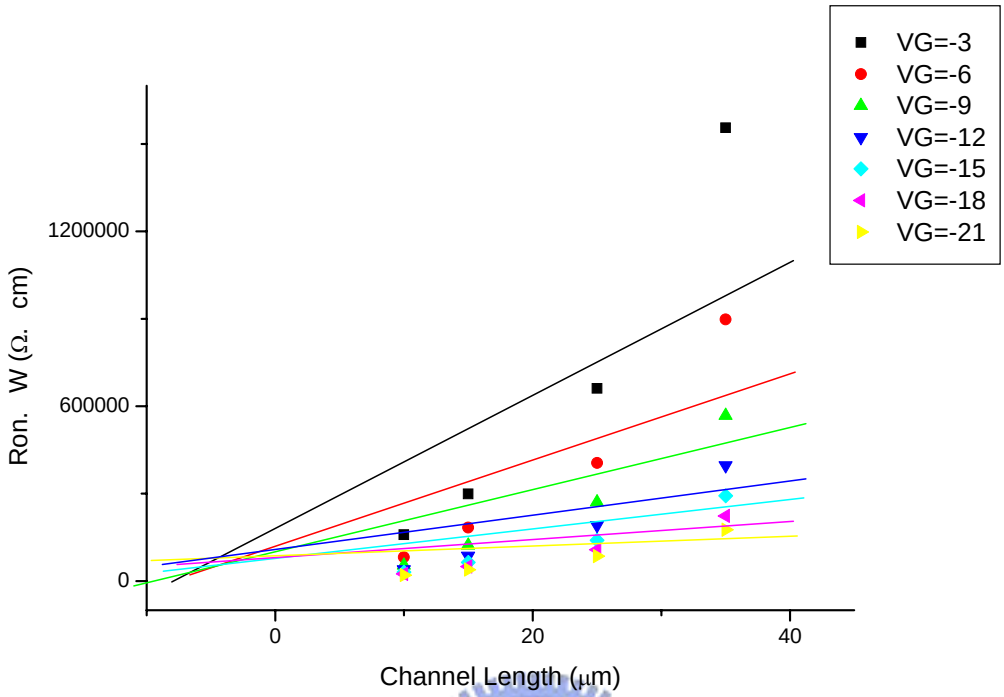


(a)

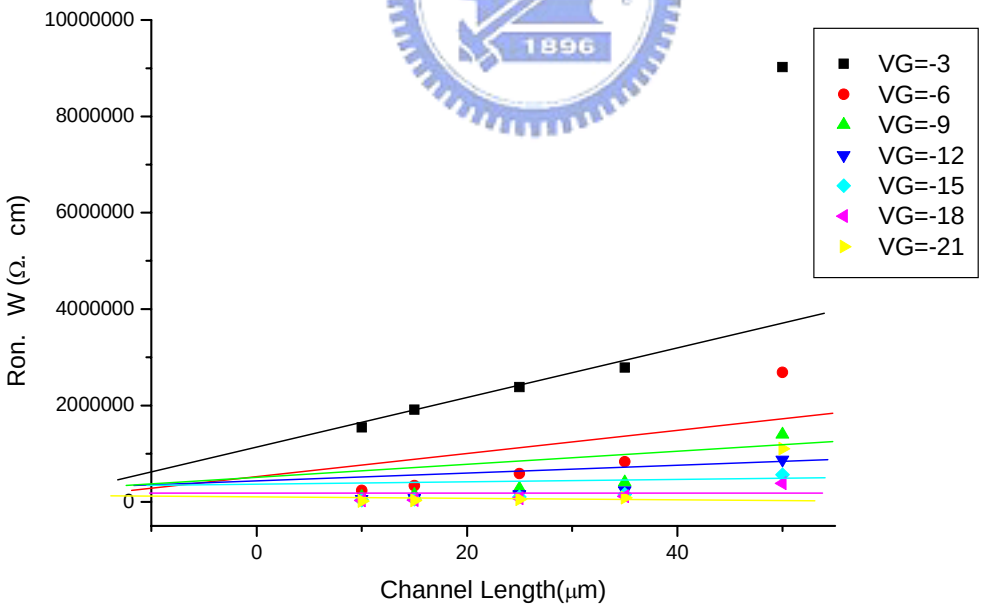


(b)

Figure 2-5 Output characteristics I_S vs. V_D of P3HT OTFTs with capping thin Pt film on (a)Ti/Ni (b)Ti/Cr Source and Drain contact metal.



(a)



(b)

Figure 2-6: Width-normalized ON resistance as a function of channel length at different gate voltage and with capping thin Pt film on (a)Ti/Ni(b)Ti/Cr source/ drain contact metal. The solid lines represent the linear least square fit of the date.

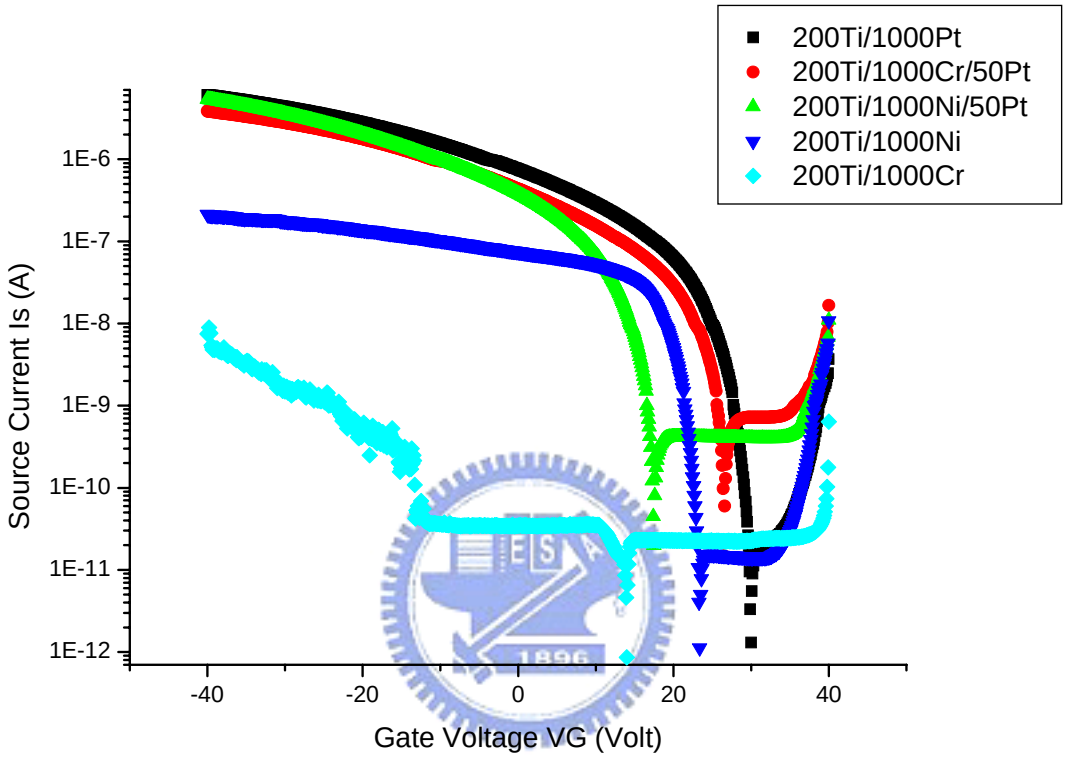


Figure2-7: The transfer characteristics (I_S vs. V_G) of OTFTs in the linear regime with different Source/Drain contact metals and capping Pt film.

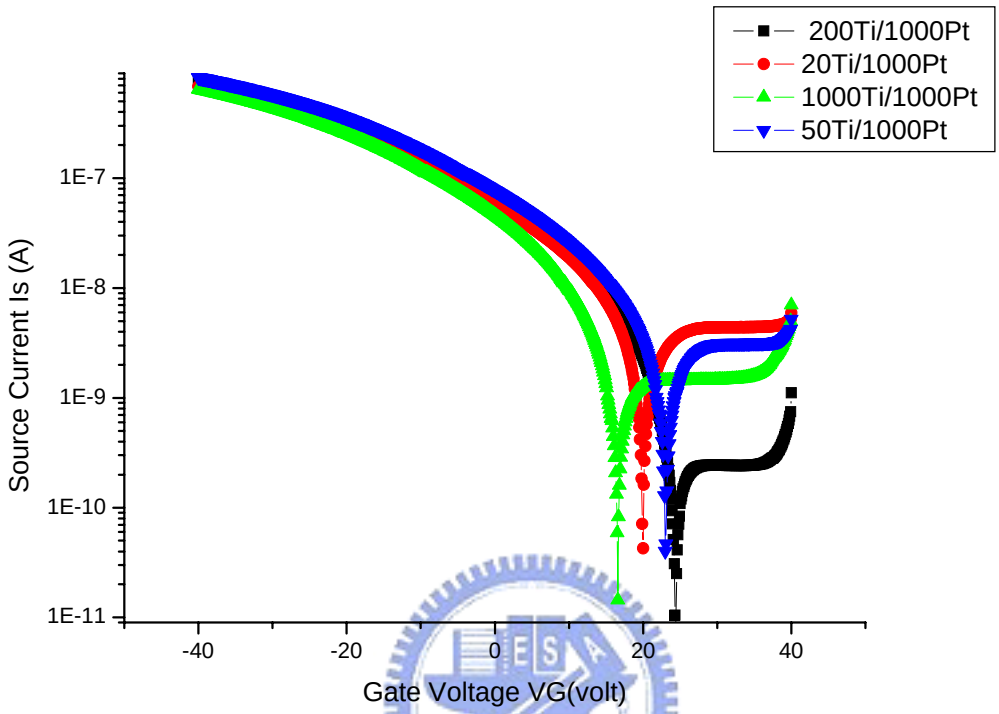
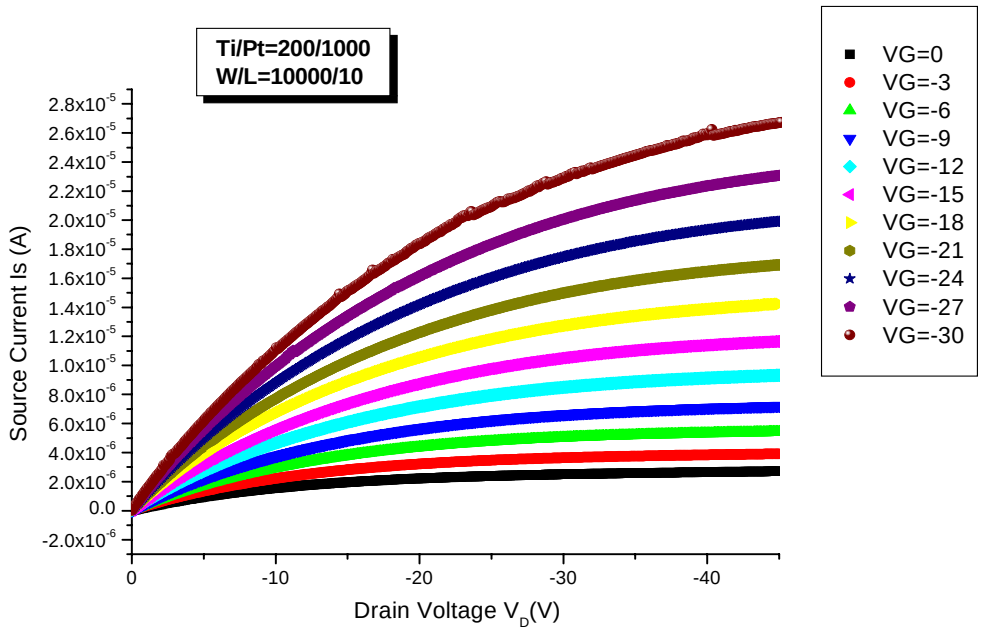
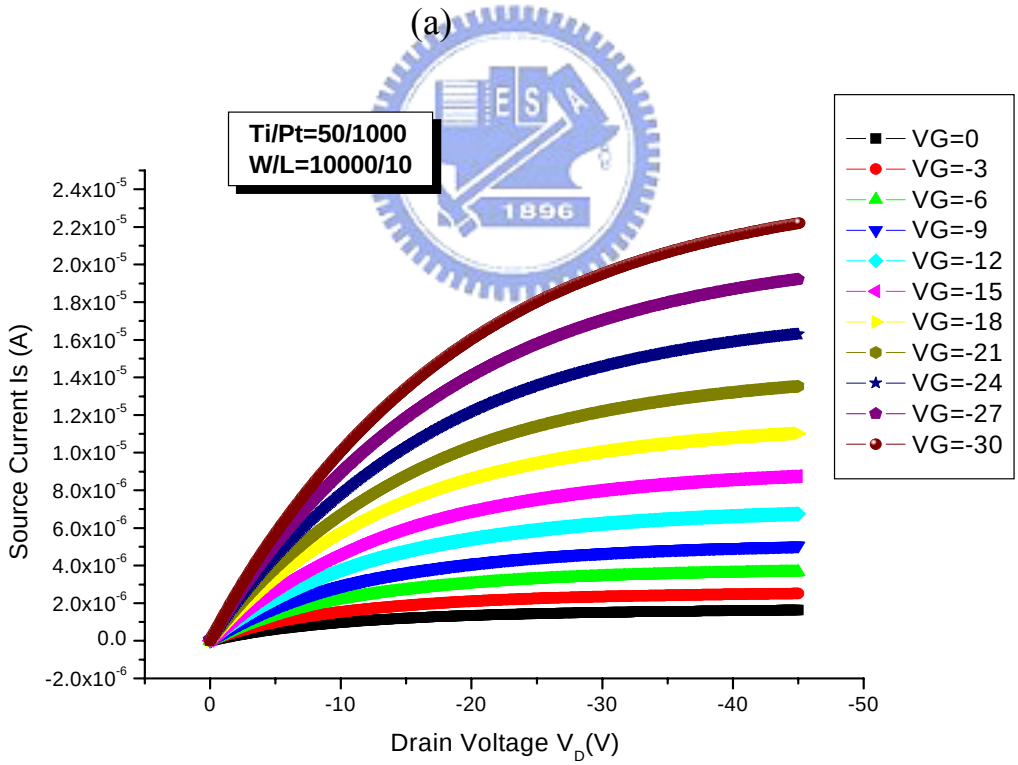


Figure 2-8: The transfer characteristics (I_S vs. V_G) of OTFTs in the linear regime with different thickness of adhesion layer.

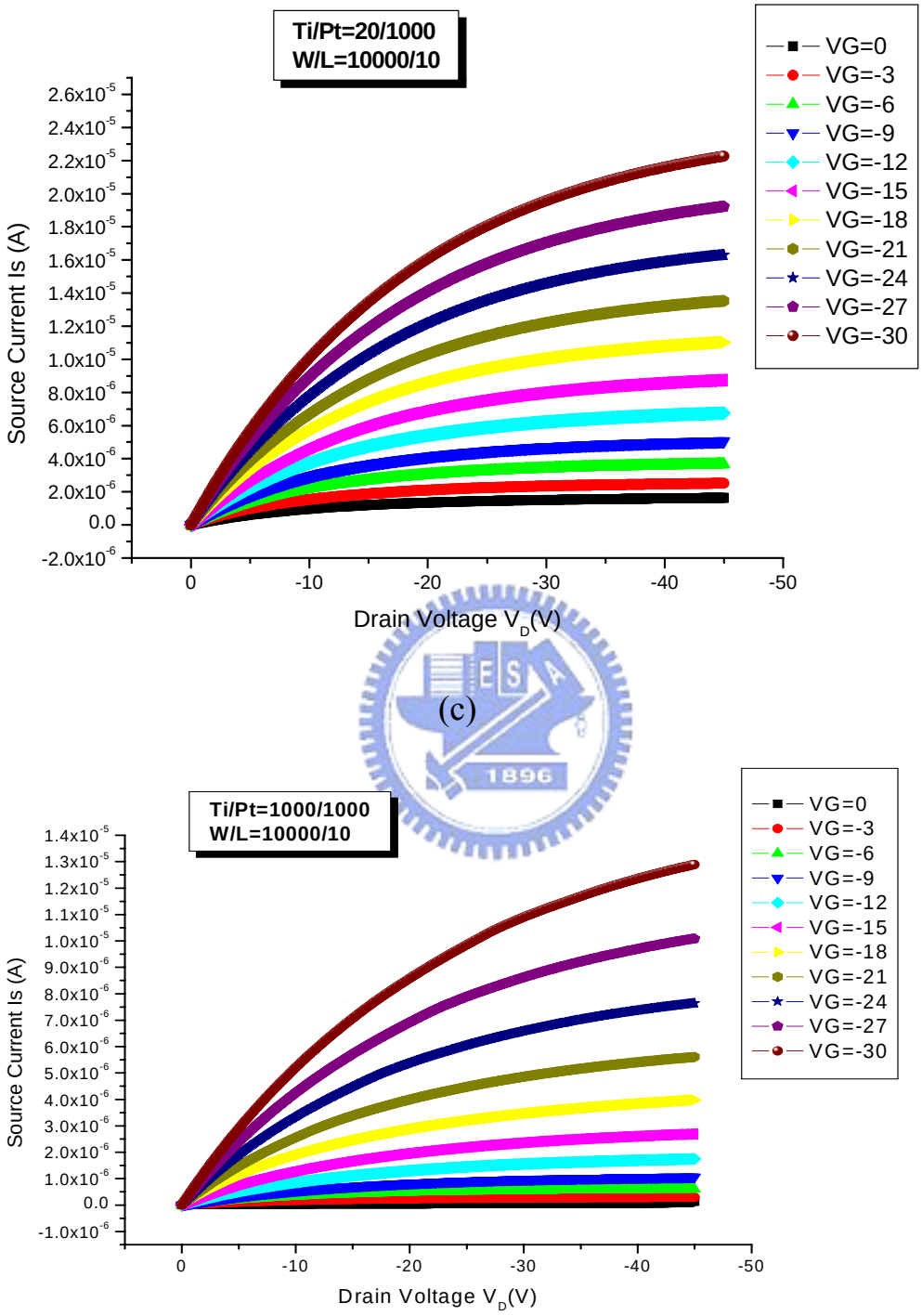


(a)



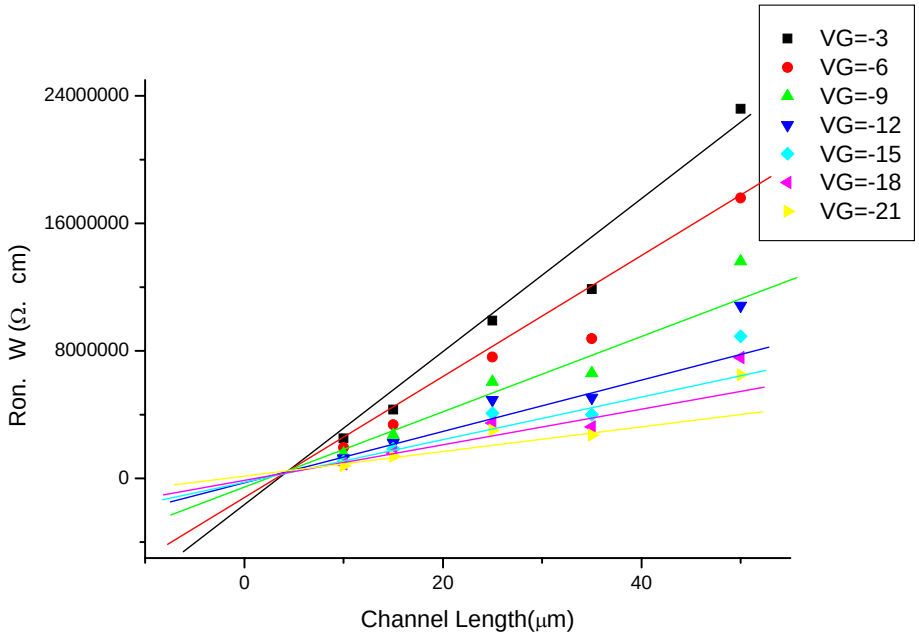
(b)

Figure 2.9: Output characteristics I_S vs. V_D of P3HT OTFTs with (a)Ti/Pt=200/1000 (b)Ti/Pt=50/1000 (c)Ti/Pt=20/1000 (d)Ti/Pt=1000/1000 Source and Drain contact (continue)

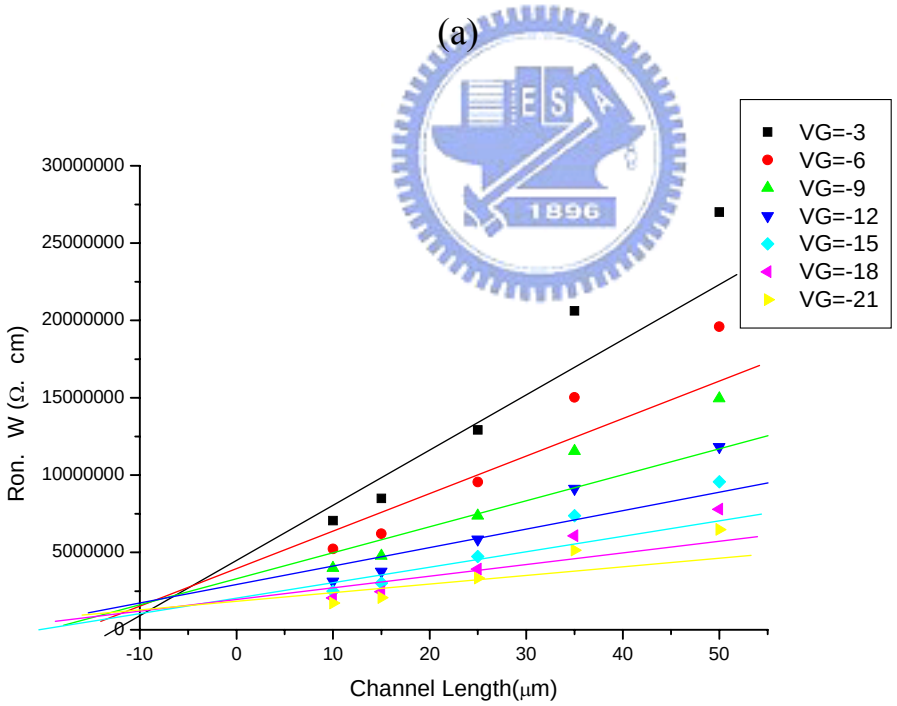


(d)

Figure 2.9: Output characteristics I_S vs. V_D of P3HT OTFTs with (a)Ti/Pt=200/1000 (b)Ti/Pt=50/1000 (c)Ti/Pt=20/1000 (d)Ti/Pt=1000/1000 Source and Drain contact

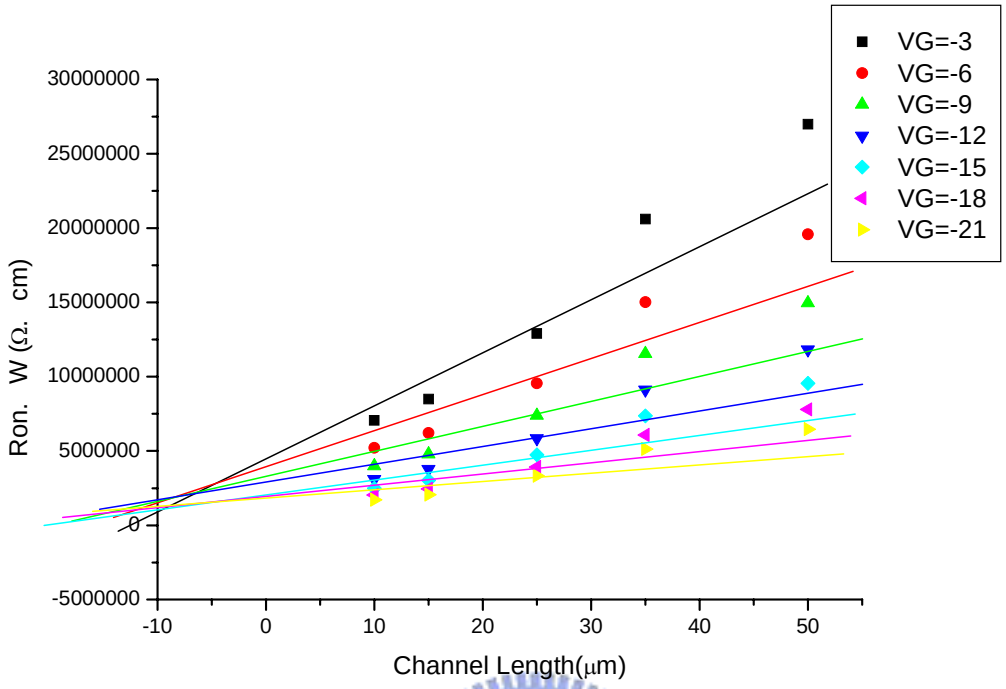


(a)

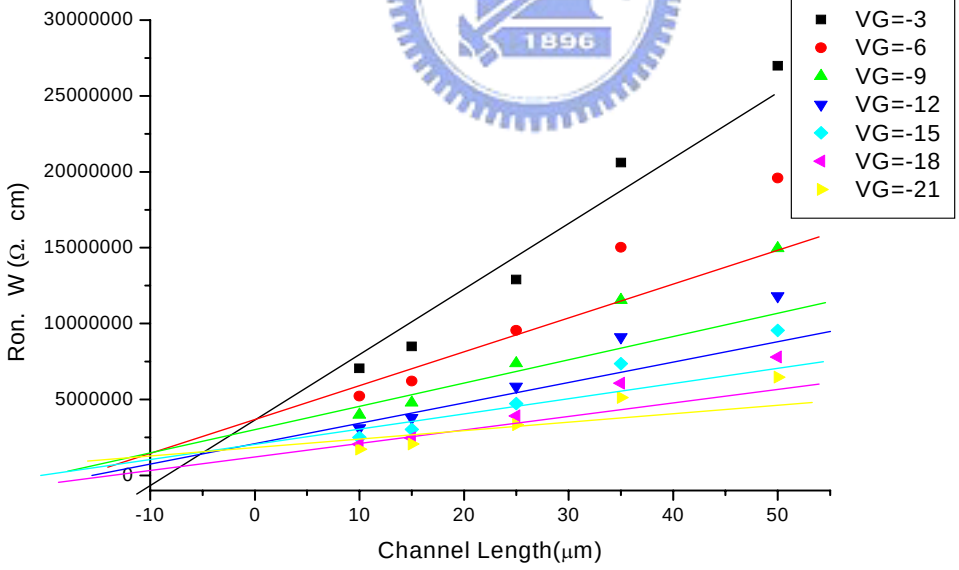


(b)

Figure 2-10: Width-normalized ON resistance as a function of channel length at different gate voltage and with (a)Ti/Pt=200/1000 (b)Ti/Pt=50/1000 (c)Ti/Pt=20/1000(d)Ti/Pt=1000/1000 Source/Drain contact metal. The solid lines represent the linear least square fit of the date. (continue)



(c)



(d)

Figure 2-10: Width-normalized ON resistance as a function of channel length at different gate voltage and with (a)Ti/Pt=200/1000 (b)Ti/Pt=50/1000 (c)Ti/Pt=20/1000(d)Ti/Pt=1000/1000 Source/Drain contact metal. The solid lines represent the linear least square fit of the date.

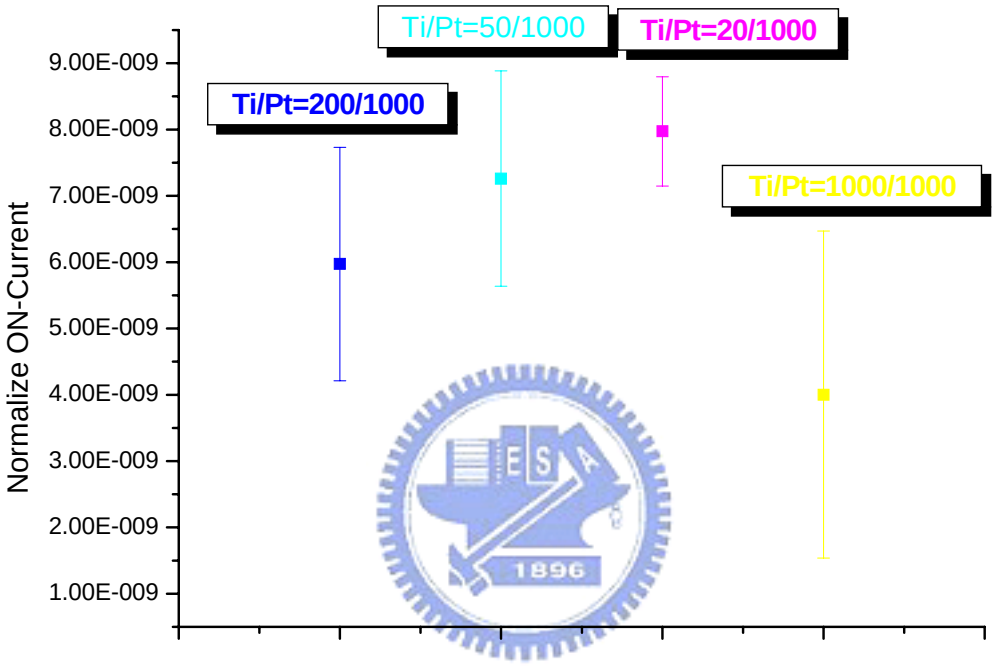


Figure 2-11: Distribution of Normalize ON-Current of different thickness of adhesion layer.

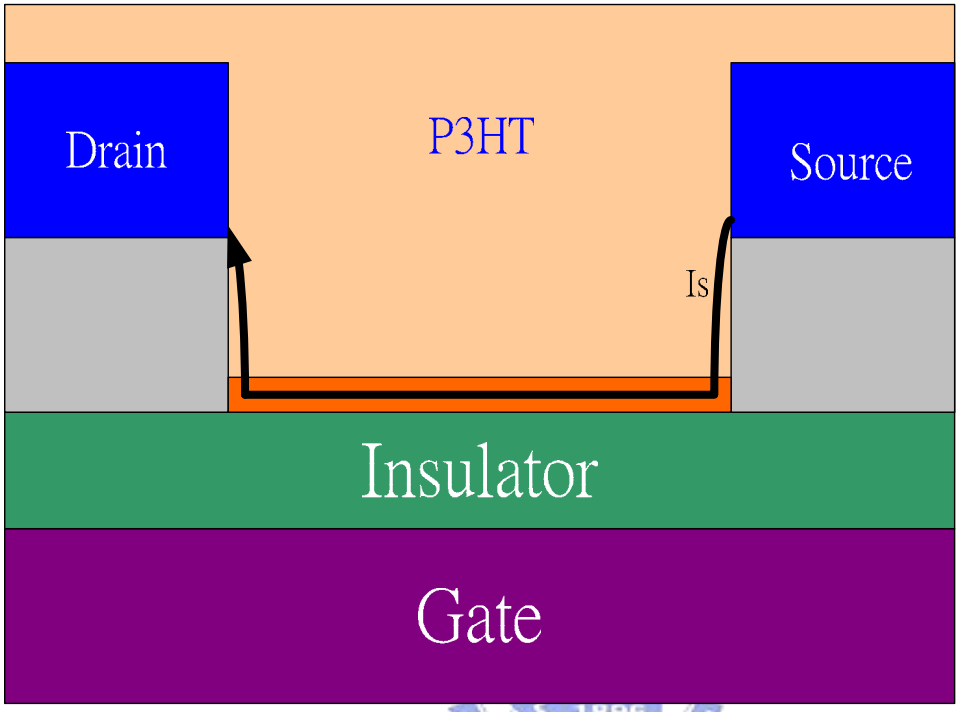


Figure2-12: Current flow of OTFT at accumulation mode.

W/L	I_{NO}(Amp)	Off current(Amp)
W/L=10000/10 μm	1.00E-12	1.00E-09
W/L=5000/10 μm	1.00E-12	5.00E-10
W/L=1000/10 μm	1.00E-12	1.00E-10
W/L=1000/15 μm	1.00E-12	6.60E-11
W/L=1000/25 μm	1.00E-12	4.00E-11
W/L=1000/35 μm	1.00E-12	2.80E-11
W/L=1000/50 μm	1.00E-12	2.00E-11
W/L=500/10 μm	1.00E-12	5.00E-11
W/L=500/15 μm	1.00E-12	3.30E-11
W/L=500/25 μm	1.00E-12	2.00E-11
W/L=500/35 μm	1.00E-12	1.40E-11
W/L=500/50 μm	1.00E-12	1.00E-11
W/L=300/35 μm	1.00E-12	8.50E-12

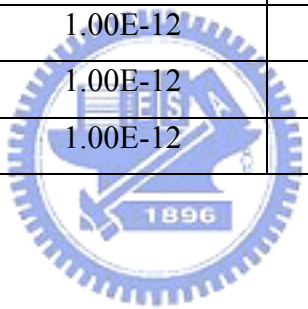


Table2-1: The magnitude of off current with different channel length and different channel width

Source/Drain Metal	Pt	Au	Ni	Cr
Contact Resistance(M Ω)	0.36~0.41	0.3~0.38	13~17.2	X

Table 2-2: The contact resistance between source/drain electrodes and P3HT with different contact materials.

Source/Drain Metal	Pt	Ni	Pt film on Ni	Pt film on Cr
Contact Resistance(M Ω)	0.36~0.41	13~17.2	0.81~1.1	2.1~3.5

Table 2-3: The contact resistance between source/drain electrodes and P3HT with different contact materials and capping thin Pt film.

Thickness of adhesion layer	20Å	50Å	200Å	1000Å
Contact Resistance(M Ω)	0.24~0.47	0.3~0.4	0.36~0.41	0.25~0.8

Table 2-4: The contact resistance between source/drain electrodes and P3HT with different thickness of adhesion layer.

Chapter 3

Electric Stability of P3HT OTFTs

3.1 Introduction

TFT with organic semiconductors as the active layer is widely investigated. P3HT-based OTFTs have improved remarkably through optimization of process parameters and is comparable to amorphous silicon thin film transistors[22],[23]. OTFTs exhibit great potential for special application such as flexible display, RF tags, and smart cards. Comparing to inorganic semiconductor, the stability of OTFTs is poor with time evolution while different environmental ambient such as nitrogen, oxygen or moisture would affect the performance of organic device[15],[24],[25]. Organic materials are more sensible and weaker than inorganic materials. Besides, electric stability of OTFTs during long time operation is another important subject needed of research.

In this experiment, we investigated the characteristics of bottom-contact P3HT OTFTs under various voltage stress conditions. Here, we find that polarization phenomenon during voltage stress, and thus we designed several experiments to further investigate these special properties of P3HT OTFTs.

3.2 Experimental Detail

OTFTs in this experiment are fabricated by conventional process as described in chapter 2. The bottom-contact OTFTs with Ti/Pt as the adhesion layer and source/drain metal are deposited SiO_2 by PECVD as the gate insulator. Thickness of adhesion layer and source/drain metal is 20nm and 100nm respectively. The sample will be stored in vacuum for 2 days to let the oxygen

atoms out-diffuse before measurement. The Electric characteristics are measured by HP 4156 in atmosphere.

3.3 Result and Discussion

3.3.1 Hot Carrier Stress

First, we measured the electric characteristics of OTFTs without any stress in the atmosphere as the control sample. We can differentiate the actual variations cause by stress measurements from those by oxygen auto doping. The transfer characteristic I_S vs. V_G was illustrated in Fig 3-1. We can find the threshold voltage increases with the stress time due to the oxygen auto doping effect. Oxygen diffusing into P3HT as p-type dopants will increase the conductivity of the semiconductor and enlarge the threshold voltage.

Next, we applied a constant gate bias of -10 V and a constant drain bias of 0, -12, -16 and -20 V respectively for 0 - 5000 second while the source electrode was ground. In this stress condition, the electric field near the drain side should accelerate the free holes in the depletion region and cause some damages at interface or the gate insulator. Fig 3-2 shows the transfer characteristics I_S vs. V_G of OTFTs after various voltage stress; the threshold voltage shift ratio are summarized in Fig 3-3. The trend of threshold voltage shift when applied gate of -10 V and ground source and drain electrode can be attributed to polarization effect[15]. The negative gate bias of -10 V will alter the direction of dipoles, as shown in Fig 3-4, and the effect of oxygen auto doping which may increase the threshold voltage would be compensated.

We can find a slight decrease for the threshold voltage in all stress condition when the stress time shorter than 100~200 sec and then a significant positive threshold voltage shift was observed when applied gate electrode of -10 V and drain electrode of -12, -16 and -20 V, respectively as increasing the stress time. The negative gate bias could cause holes to inject into

the gate oxide, forming positive trapped charges. These hole traps did not cause the degradation of oxide in short time as shown in Fig 3-5 that the gate leakage current of OTFTs did not change after short time stress. But these hole traps reduced the threshold voltage and a slight decrease for threshold voltage when stress time shorter than 100~200 sec can be observed. When stress time larger than 200 sec, the strong electric field established between the gate and the drain electrodes twirled the direction of dipoles in the organic active layer as illustrated in Fig 3-6. The single side polarization effect at drain side will counterbalance that decrease threshold voltage because of applied gate electrode of -10 V. Therefore, the trend of threshold voltage of additional applied drain voltage (-12, -16 and -20 V) is similar to that of no stress in atmosphere. Moreover, the oxygen auto-doping during stress measurements further increased the threshold voltage, so that the effect of hole trapping was overwhelmed.

In Fig 3-5, we found the increase rate of gate leakage current that isn't different significantly when applied drain bias of -12 and -20(hot carrier stress condition) after stress 5000 sec respectively. Fig 3-7 shows the normalize field-effect mobility of OTFTs after stress. The field-effect mobility μ of OTFTs after hot-carrier stress isn't change conspicuously. Therefore, we can indicate the interface between P3HT and oxide didn't degrade during hot-carrier stress. These results show the hot-carrier produce hardly in OTFTs of our experiment resulting from the long channel length and low field-effect mobility of OTFTs. The smallest channel length in our device is 10μm, a long channel length comparing to conventional MOSFETs, resulting in weak lateral electric field. The low field-effect mobility (~10^{-3} cm/V-s) implies a short mean free path so that the carriers hardly store energy.

To verify the hypothesis about the polarization effect at drain side, we applied a reverse electric field for samples after hot carrier stress and to see whether the direction of dipoles near

the drain side could be reversed or not. Consequently, while always keeping source electrodes grounded, we applied a constant gate bias of -10 V and drain bias of -20 V for 10 sec, and then changed the drain bias to 0 V for another 10 sec , next, V_D = -20 V for 20 sec, then V_D = 0 V for another 20 sec, and so forth. In this way, the potential difference between the gate and the drain electrode was kept in 10 volts while the direction of the electric field changed alternatively. The result of threshold voltage shift is shown in Fig 3-8. The direction of dipoles in the active layer is varied with the change of the electric field because more dipoles reacted to the applied electric field with increasing the stress time, the threshold voltage versus iterative times oscillated.

In Fig 3-3 we can find the threshold voltage of OTFTs exposing to the atmosphere increase with time because of the oxygen auto doping. The trend of threshold voltage shift when only applied gate of -10 V and ground source and drain electrode is attributed to polarization effect. The negative gate bias of -10 V will alter the direction of dipoles and decrease the threshold voltage to absorb the effect of oxygen auto doping that will increase the threshold voltage. If we further increase the negative gate bias or enlarged the drain voltage to +20 V, the threshold voltage would start to decrease. On the other hand, if we applied a negative drain bias that the threshold voltage will increased gradually with stress time similarity to no stress condition.

In Fig 3-7 we can find the field-effect mobility did not change with stress time except the case of VG = -10 V and VD = 20 V, implying that the OTFTs were quite stable under normal operation conditions. The decrease of field-effect mobility under V_G= -10 V and V_D = +20 V stress condition was presumably attributed to the severe hole injection to the gate insulator and the associated trap state creation near the P3HT and SiO2 interface under large voltage difference of 30 volts between the gate and the drain electrode. Nevertheless, as a p-type transistor, bias conditions such as V_G= -10 V and V_D = +20 V will not occur in the circuit design.

3.3.2 Polarization Phenomenon in P3HT OTFTs

We found the polarization properties of P3HT OTFTs affect the threshold voltage shift enormously in various voltage stress condition. Next we try to investigate the properties further.

A paper reported some self-assembled monolayers have built-in dipole field of 1MV/cm [43]. To produce the same field as applying a voltage across the 100nm thick SiO2 gate insulator, a gate voltage of 10V is necessary. So, we should differentiate this phenomenon is caused by the P3HT itself or the HMDS film. The HMDS treatment is used for improving the adhesion and interface states between oxide and P3HT. We prepared a sample without the HMDS treatment and measured it after alternative voltage stress repeatedly. The result of threshold voltage shift is depicted in Fig 3-9. The trend is similar to Fig 3-8 that device is fabricated with HMDS treatment. We can confirm that the polarization effect is caused by the P3HT film itself through test.

After verifying the origin of dipole-field, we applied a constant gate bias of 25, 50, 75 and 100 V respectively while the drain and source electrode was grounded for 0 to 1000 second. Fig 3-10 shows the normalized threshold voltage shift ratio of OTFTs after stress. We can find the final shift ratio is as large as the bias voltage and it appear to saturate at last. Fig 3-11 is the threshold voltage shift ratio of OTFTs under 50 V gate bias stress for 400 sec repeated for six times. The threshold voltage shift rate is decreased after 800s and saturated later certainly. When the gate bias applied, the electric field established and twirled the direction of dipoles in organic active layer. The dipole built a field that direction opposite to that established by gate bias as shown in Fig 3-12. The dipoles built-in field will reinforce with the stress time and decrease the net electric field in organic active layer, so that threshold voltage shift rate is decreased with stress time. When the dipoles built-in field equal to the electric field established by gate bias, the threshold voltage shift affected by polarization effect will stop and the positive shift afterward is caused by the oxygen auto doping. The larger voltage bias established stronger electric field and

twirled more dipoles in organic active that result in larger threshold voltage shift as shown in Fig 3-10.

We observed the threshold voltage shift rate shorter than 200 sec in Fig 3-10 and found that isn't direct proportioned to gate bias voltage. That indicated the dipoles in P3HT film cannot turn their direction suddenly. It needs a constant time to turn the direction of dipoles even the huge electric field established by 100 V gate bias.

Fig 3-13 is the threshold voltage shift ratio after the dipole filed was built and the gate bias was removed. We can find the built-in field of dipole will release with time in atmosphere and decrease the threshold voltage. The shift rate decrease with time and the shift ratio is located at 0.75 after 1000s. It indicates the polarization will release when additional electric field was removed but the threshold voltage cannot return to initial value (the blue line is the initial threshold voltage in Fig 3-10). It should attribute to some unrecoverable breakage of P3HT film during stress or the direction of dipole be fastened. According to the curve of threshold voltage iterative times oscillated with applied vibration voltage stress shown in Fig 3-8 or Fig 3-9, the direction dipole be fastened is more possible in our inference.

3.4 Summary

The electric reliability of P3HT OTFTs is tested. The field-effect mobility and gate leakage current did not be affected significantly after hot-carrier stress. The threshold voltage shift is attribute to polarization effect of P3HT film.

The polarization phenomenon in P3HT OTFTs is investigated. The dipole built-in field is originated from the P3HT film. Threshold voltage shift ratio saturated after a span and the last value is as large as the gate bias. The threshold voltage shift rate isn't direct proportion to gate bias voltage in the initial stage. The polarization will release when addition electric field remove in P3HT OTFTs but cannot return to initial characteristics.

To conclusion that state above, the P3HT OTFTs isn't affect significantly by electric stress but polarization effect. The device is operation in AC in generally and the dipoles need a span to turn the direction with additional electric field despite strong or weak. The P3HT OTFTs will quite stable under normal operation conditions.

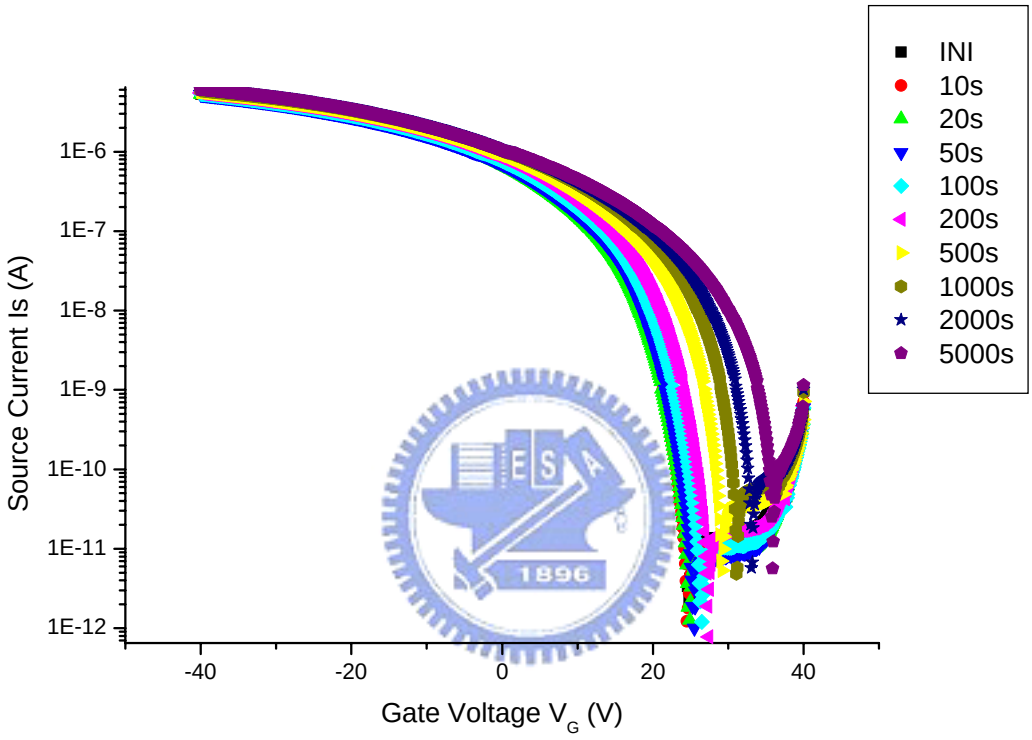
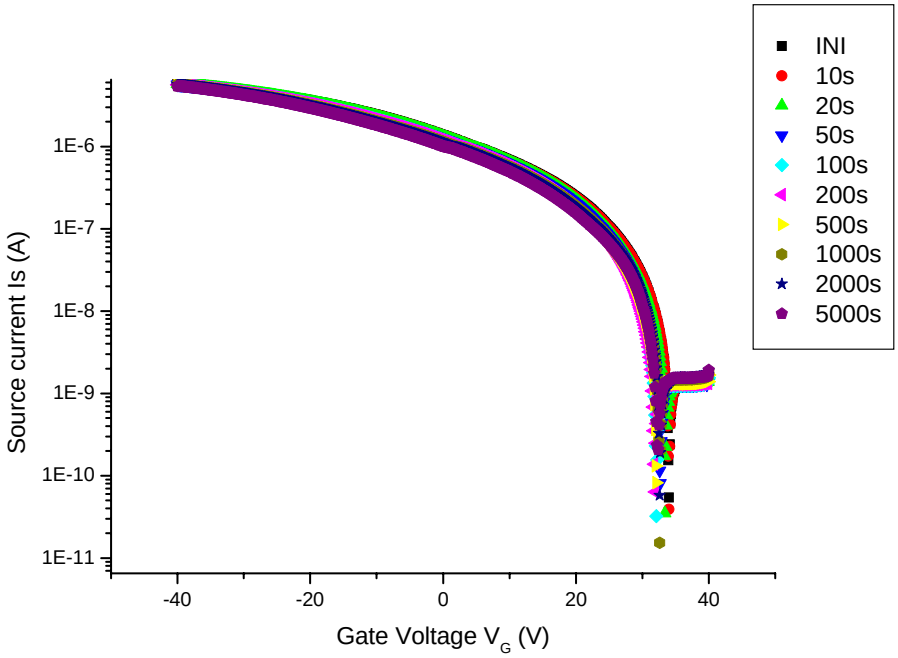
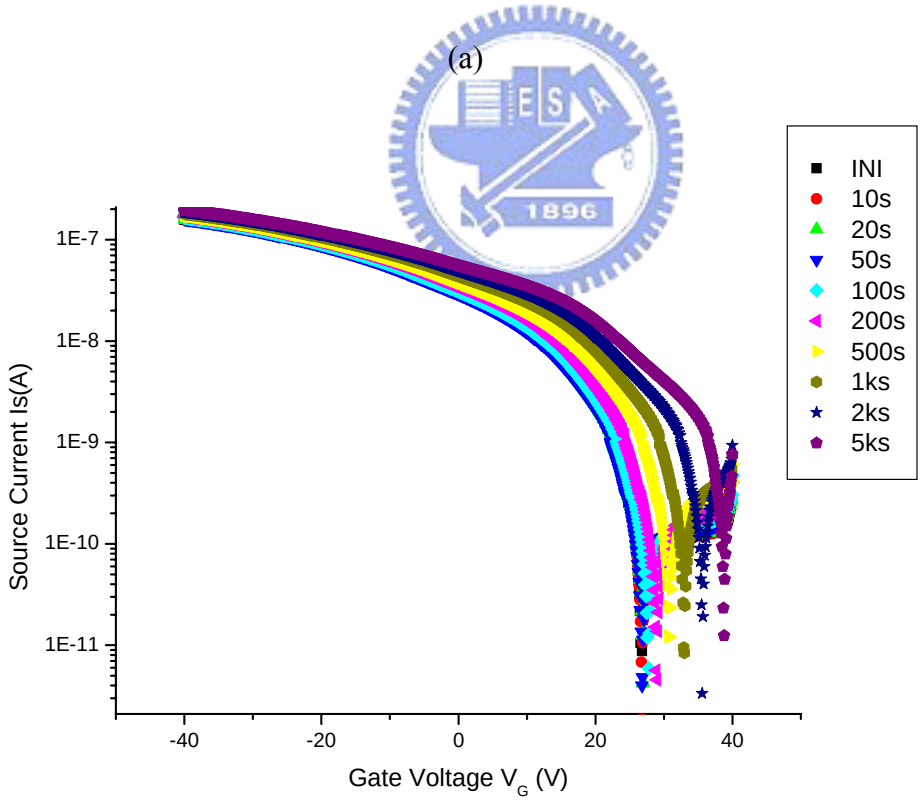


Figure 3-1: The transfer characteristic I_S vs. V_G expose in atmosphere without stress.

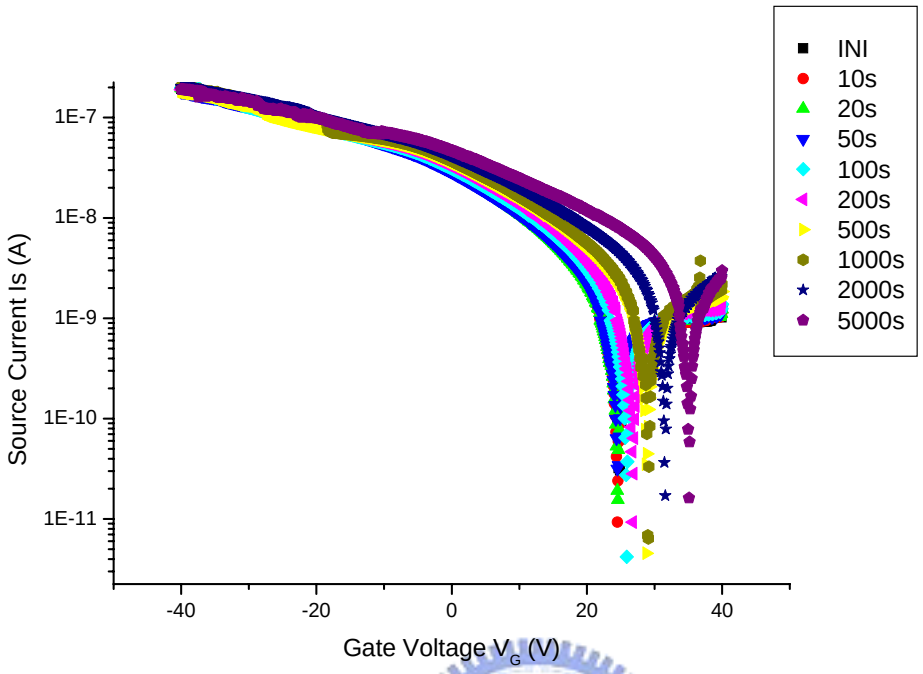


(a)

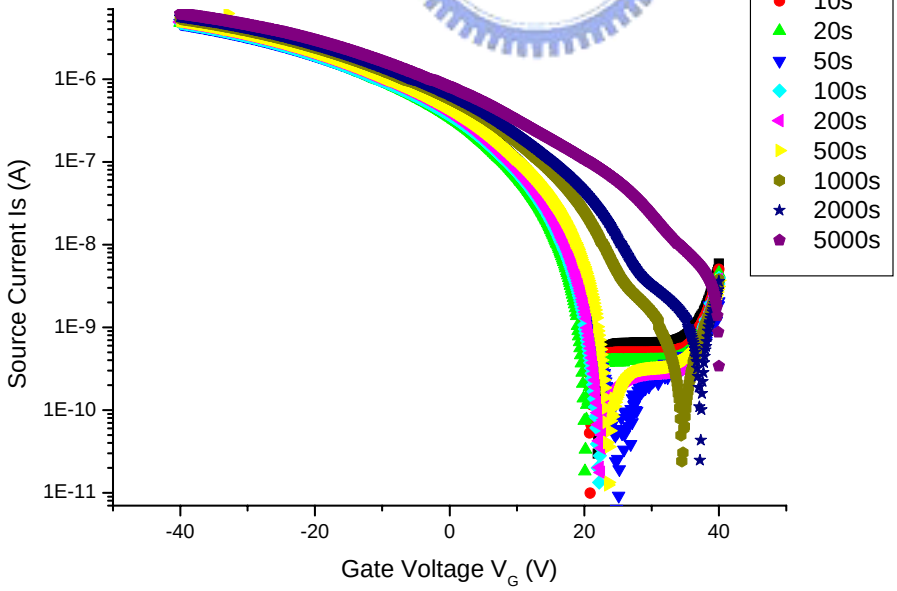


(b)

Figure 3-2: The transfer characteristics I_S vs. V_G of OTFTs with gate bias of -10 V and drain bias of (a)0 V (b) -12 V (c) -16 V (d) -20 V (continuous)



(c)



(d)

Figure 3-2: The transfer characteristics I_S vs. V_G of OTFTs with gate bias of -10 V and drain bias of (a)0 V (b) -12 V (c) -16 V (d) -20 V

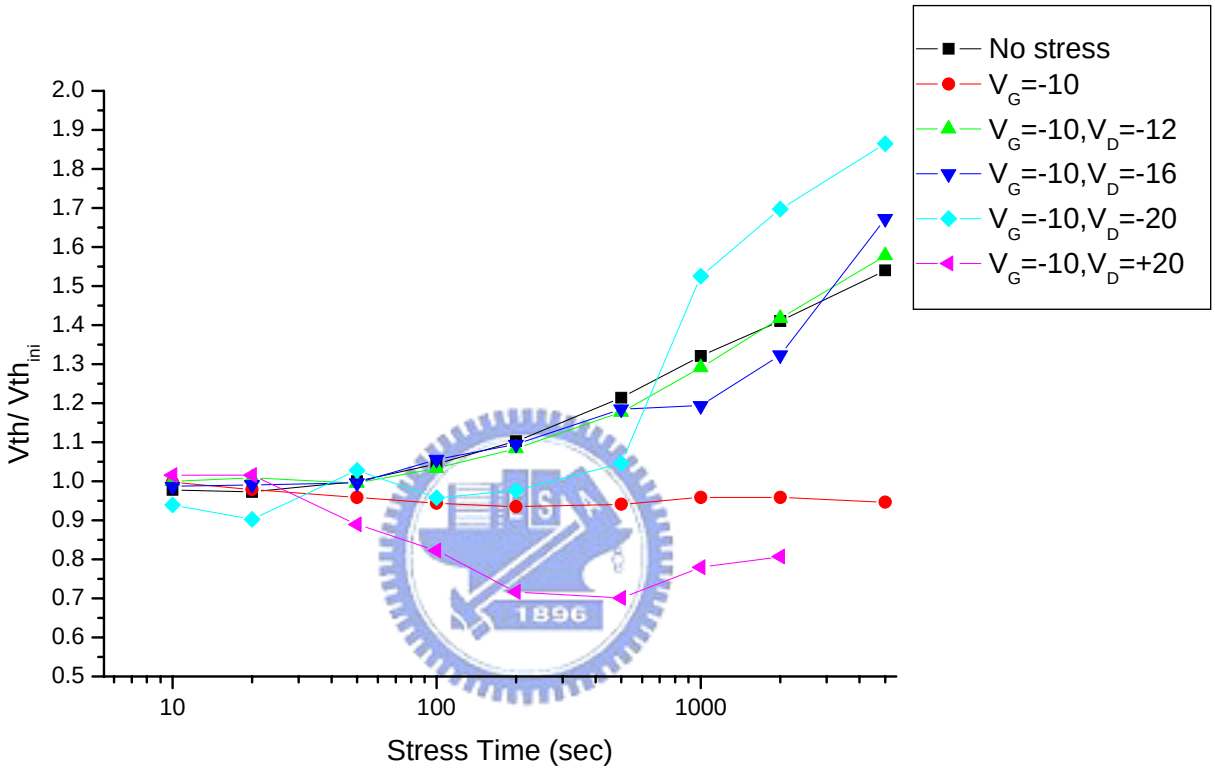


Figure 3-3: Threshold voltage shift ratio after various voltage stress.

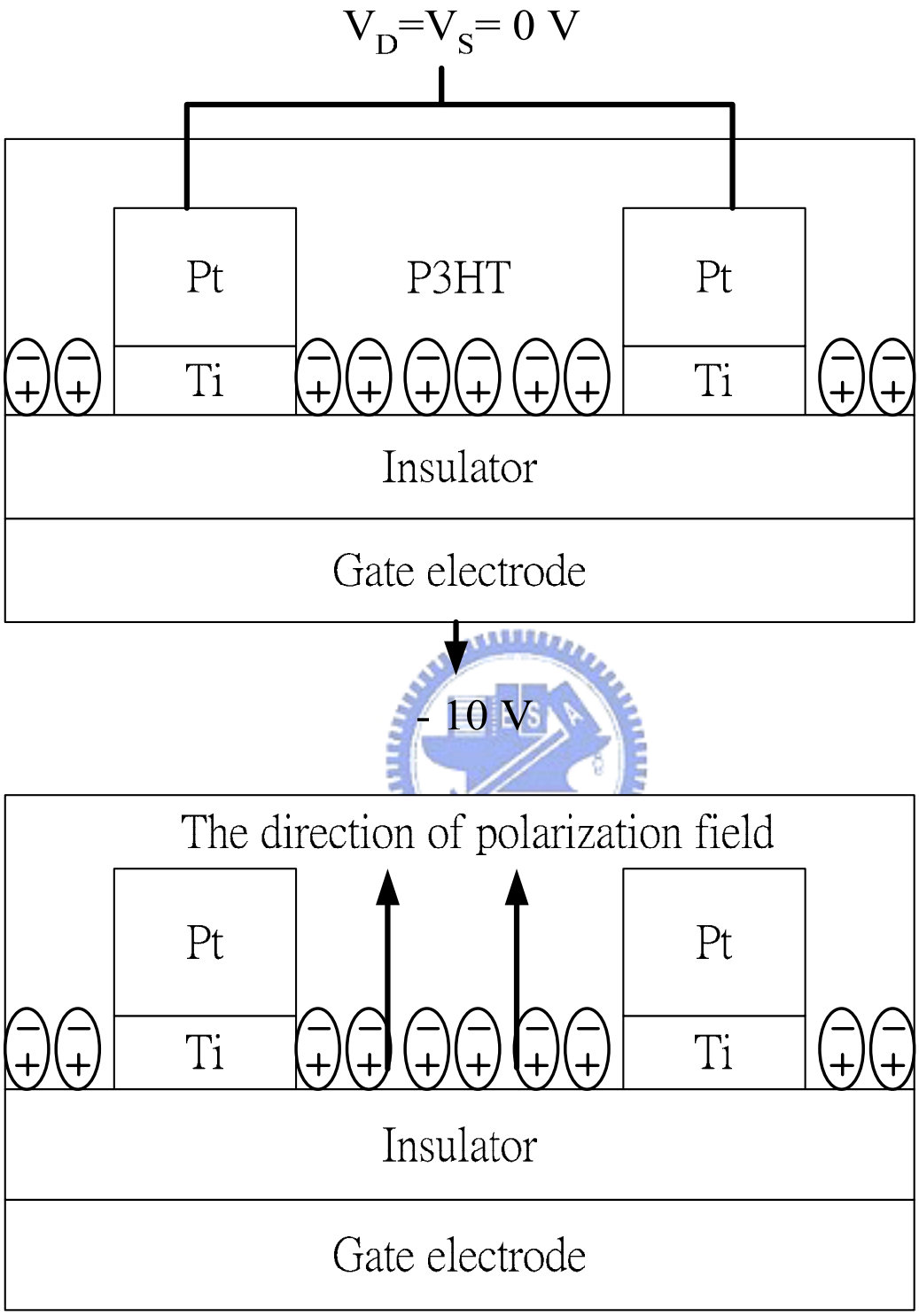
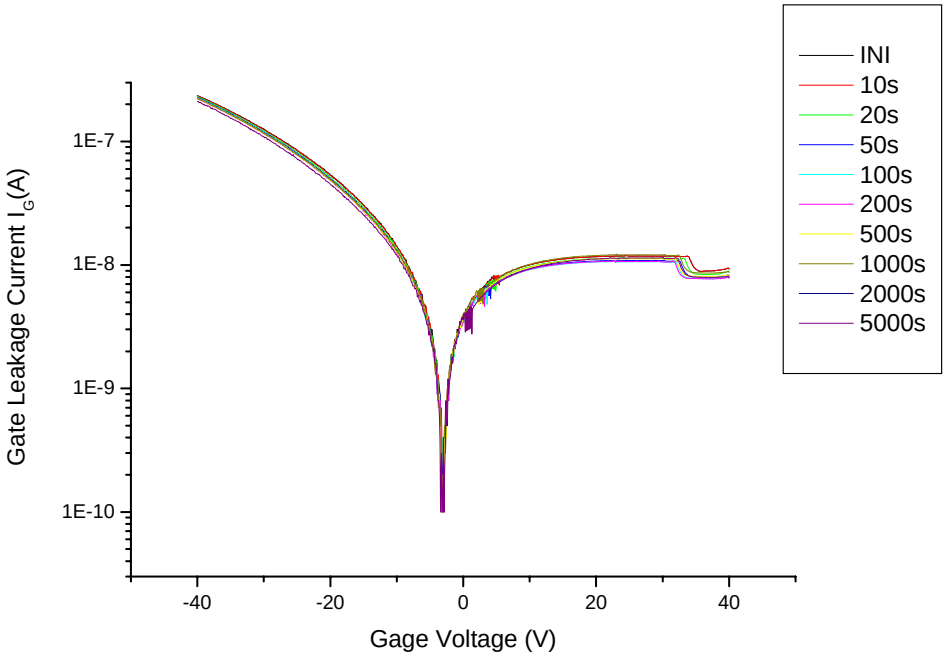
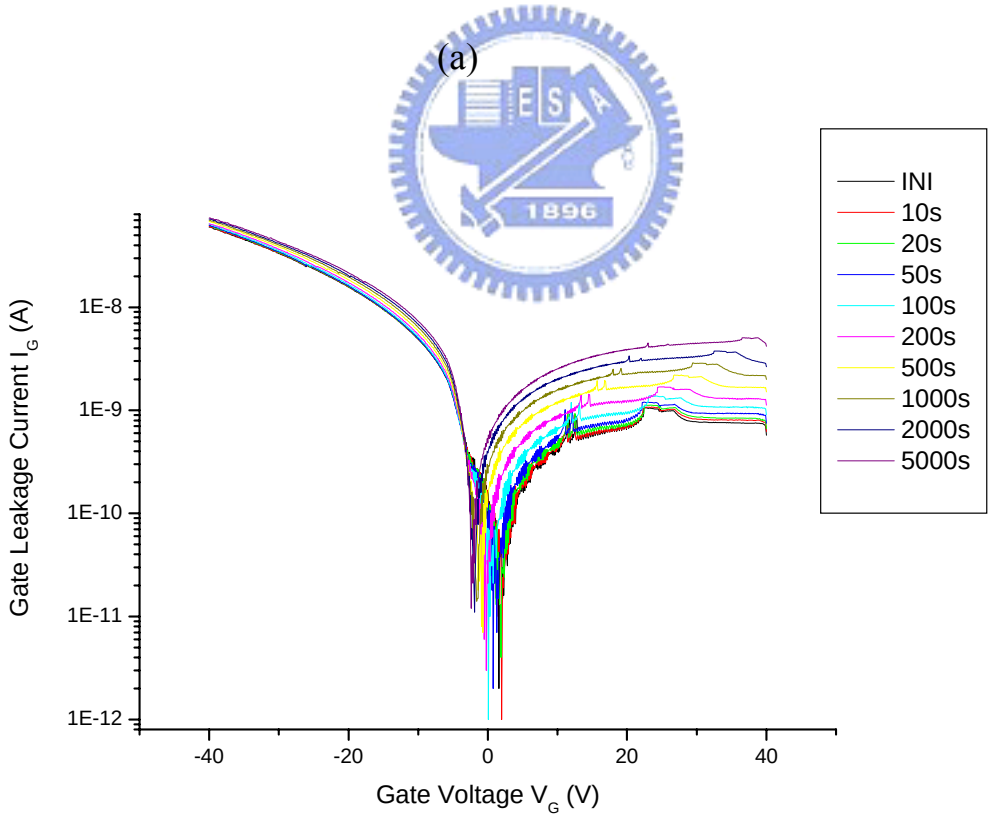


Figure 3-4: The polarization effect in the P3HT polymer with gate bias of -10 V.

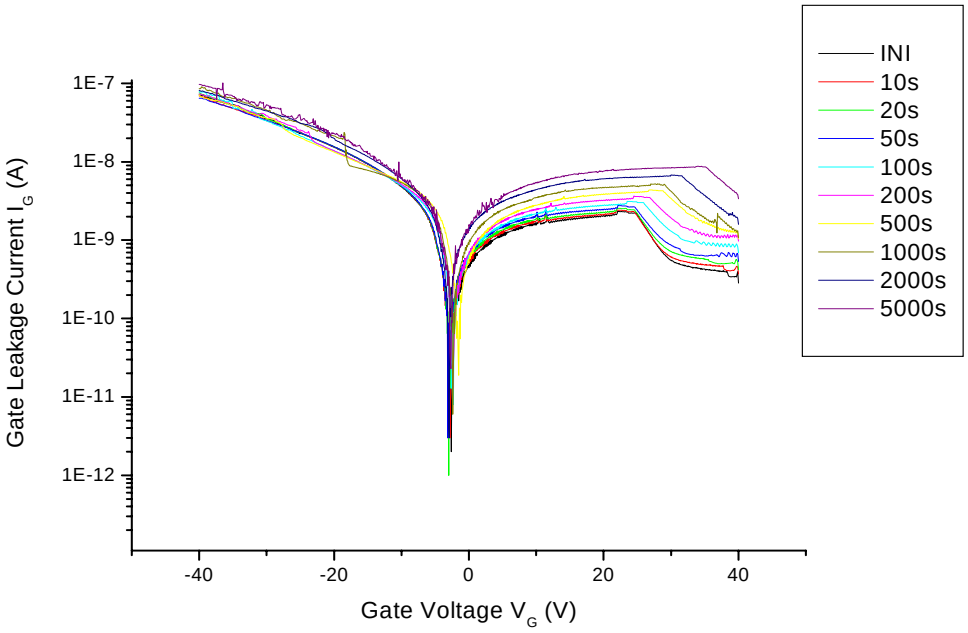


(a)

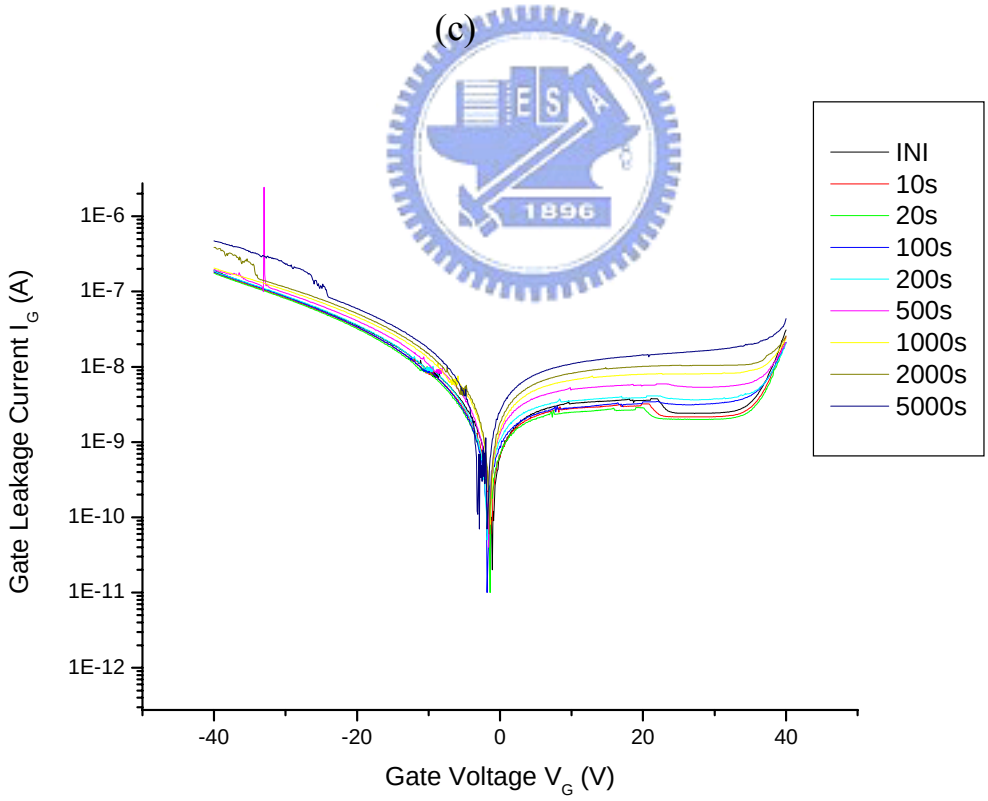


(b)

Figure 3-5: Gate leakage current of OTFTs after stress with gate bias of -10 V and drain bias of (a)0 V (b) -12 V (c) -16 V (d) -20 V (continuous)



(c)



(d)

Figure 3-5: Gate leakage current of OTFTs after stress with gate bias of -10 V and drain bias of (a)0 V (b) -12 V (c) -16 V (d) -20 V

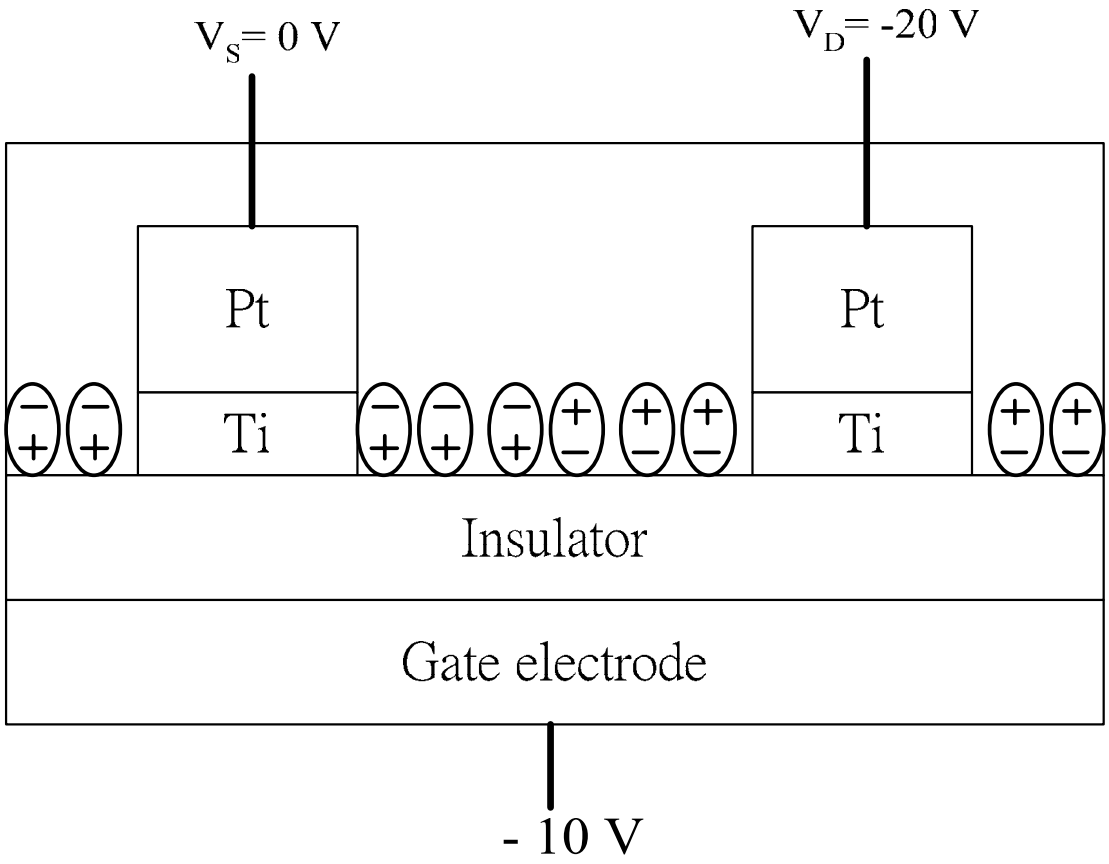


Figure 3-6: Directions of dipoles in the organic active layer when V_G=-10 V, V_D= -20 V and V_S= 0 V.

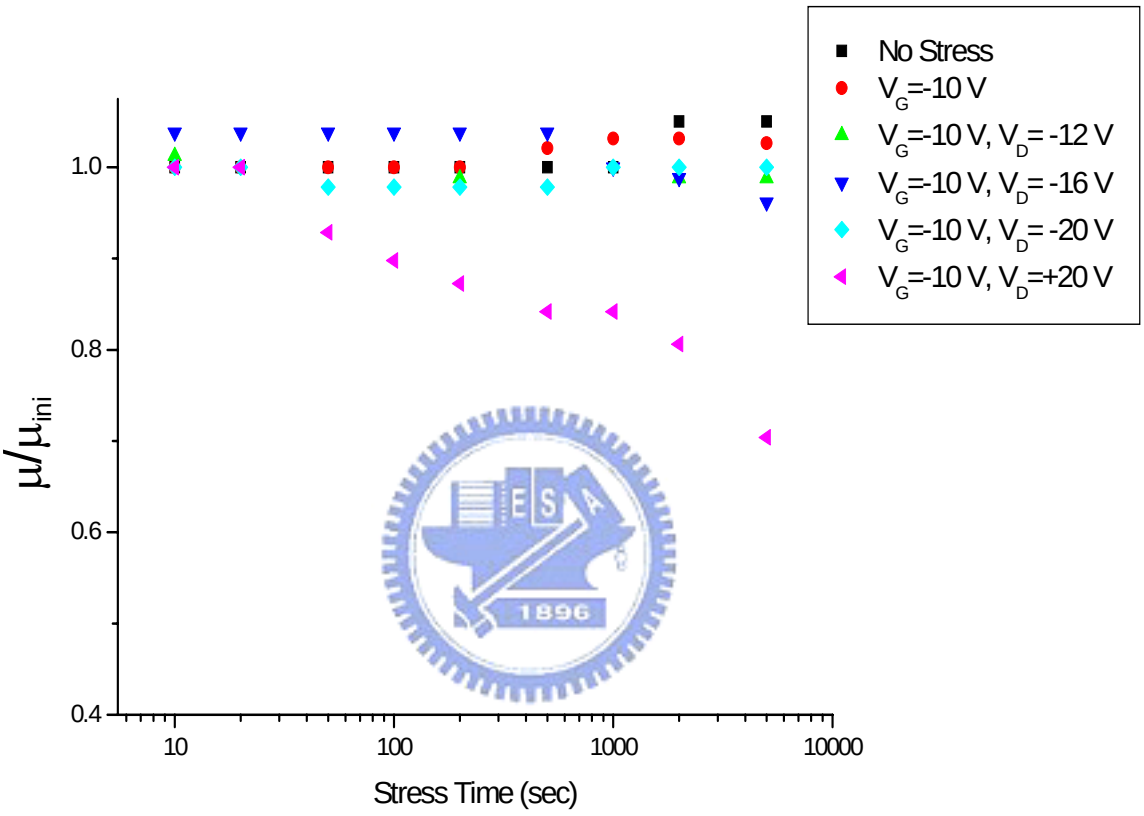


Figure 3-7: Normalize field-effect mobility of OTFTs after stress

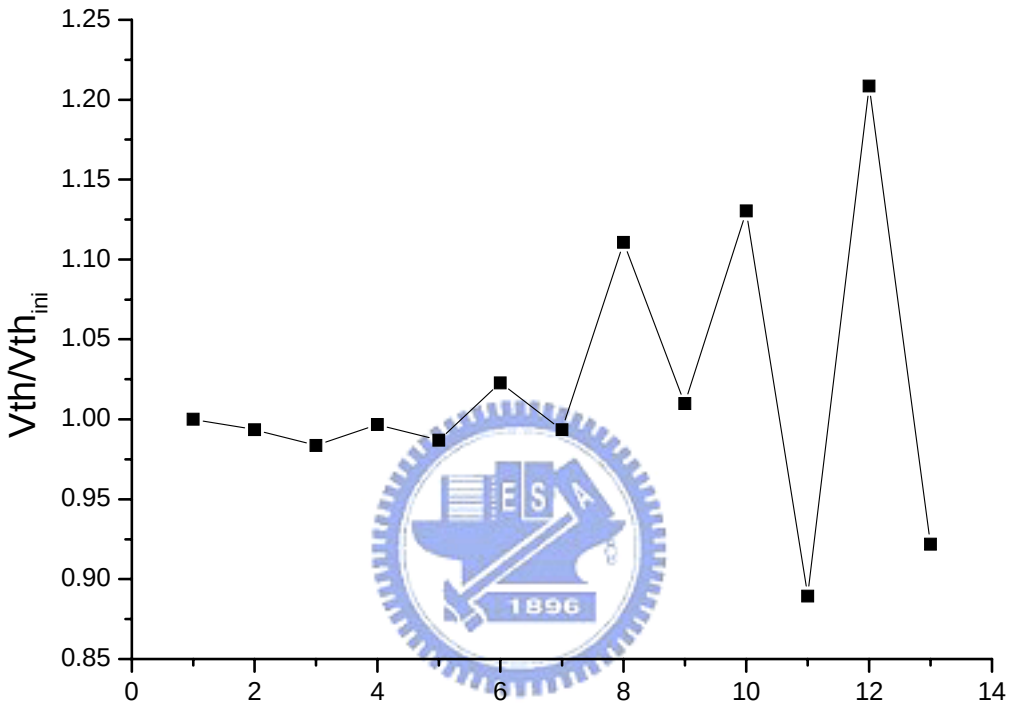


Figure 3-8: Applied gate bias of -10 V and alternative drain bias stress(-20V , 0V) for 10sec, 50sec, 100sec, 500sec, 1000sec and 5000sec. The normalize threshold voltage were measured at the end of each stress time.

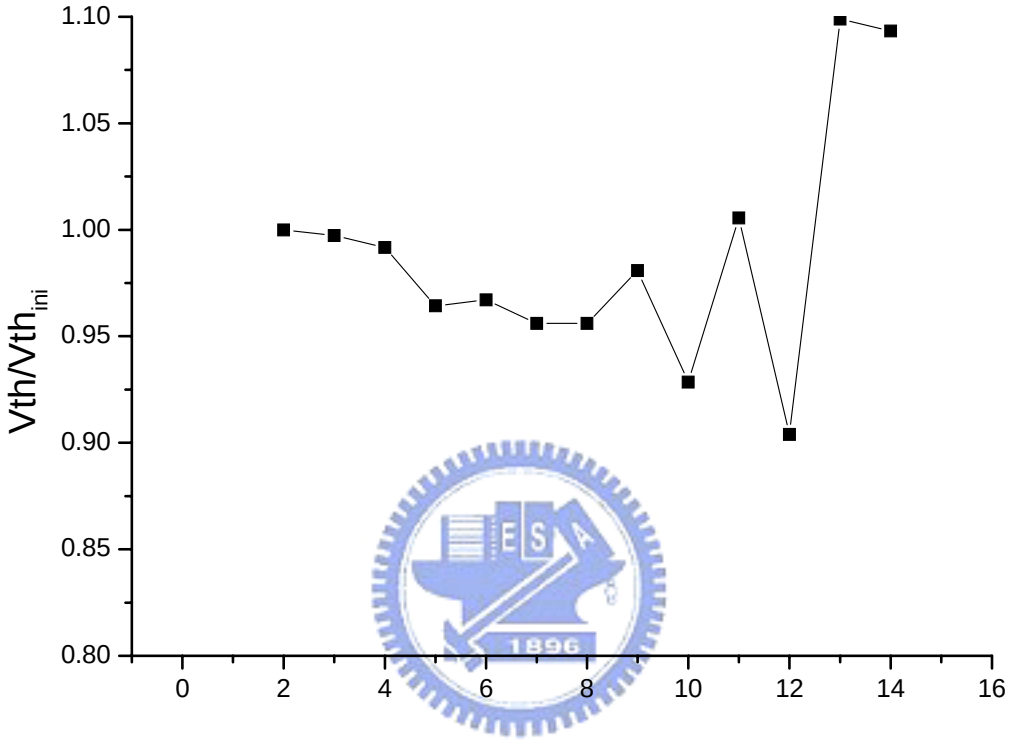


Figure 3-9: Applied gate bias of -10 V and alternative drain bias stress(-20V , 0V) for 10sec, 50sec, 100sec, 500sec, 1000sec and 5000sec. The normalize threshold voltage of OTFTs without HMDS treatment were measured at the end of each stress time.

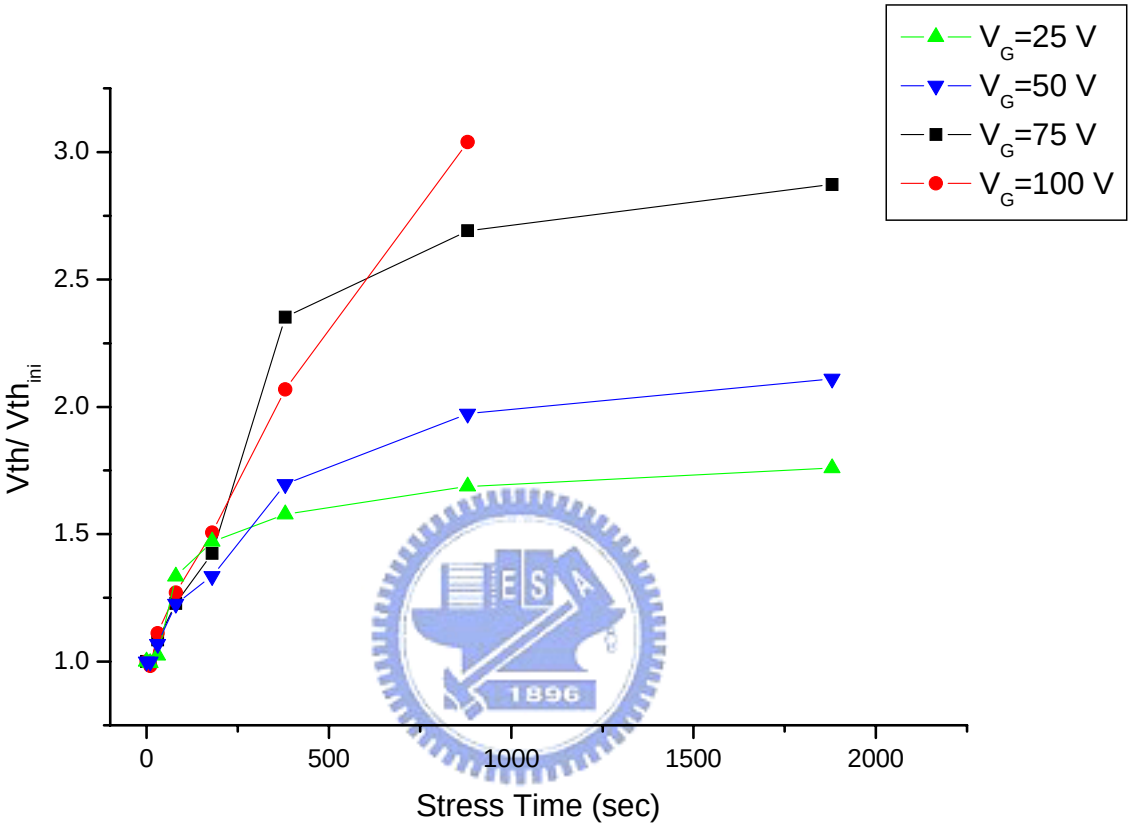


Figure 3-10: Threshold voltage shift ratio after various voltage stress.

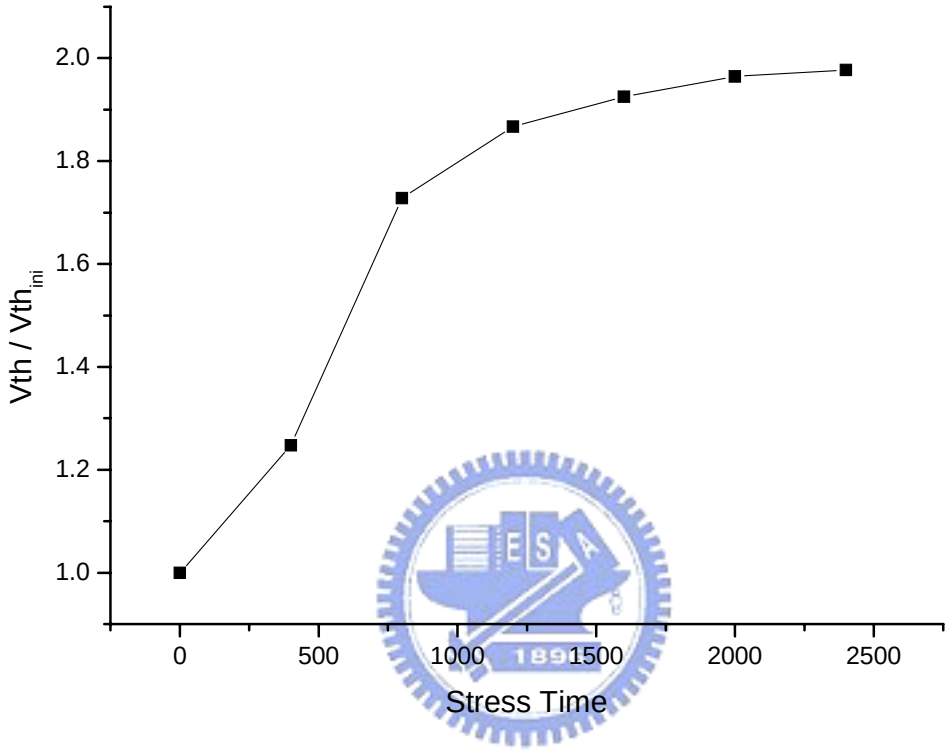


Figure 3-11: Threshold voltage shift ratio of OTFTs after stress under gate bias of 50 V . Etch stress was spaced 400 sec.

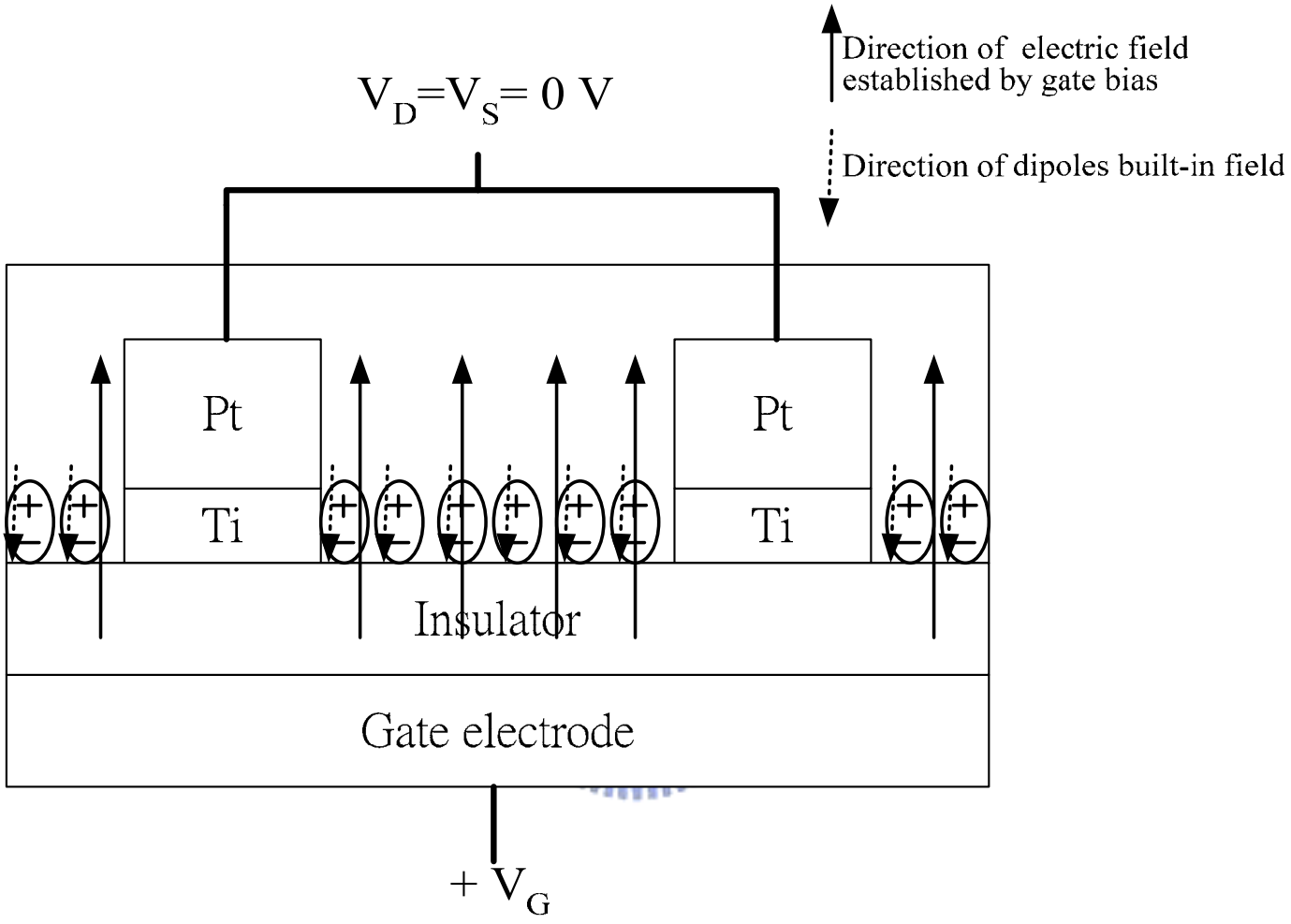


Figure 3-12: The direction of dipole built a field and electric field established by gate bias.

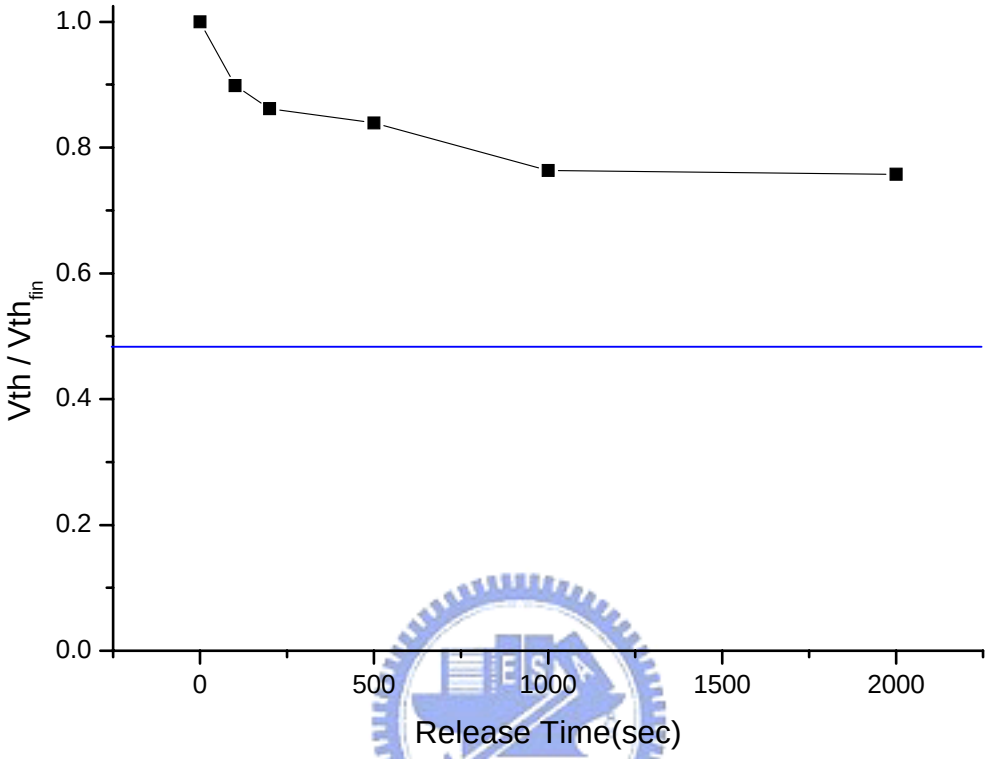


Figure 3-13: Threshold voltage shift ratio after built the dipole filed and remove the gate bias. The blue line is initial threshold voltage.

Chapter 4

Low Temperature Process of P3HT OTFTs with LPD SiO_2 as Insulator

4.1 Introduction

Organic thin-film transistors(OTFTs) allow the fabrication of electronic circuits and active-matrix displays on a variety of substrates, such as silicon, glass, polyimide[26],[27],[28], PEN, PET, and polycarbonate. In the future, the OTFTs will be fabricated on clothes or paper substrate for flexible application. However it requires at least 350℃ to deposit SiO_2 by PECVD, which is not compatible with clothes or paper substrate. Developing an all low temperature process for OTFT circuits is necessary. Although the organic semiconductor layer can be deposited at very low temperature, the gate dielectric of OTFT is hardly deposited with low temperature process with good quality. There are two methods to deposited dielectric with low temperature process for OTFT; one is to deposit SiO_2 by e-gun evaporator[29],[30],[31] and another one is to use organic dielectrics such as polyimide and PVP[32],[33]. The quality of SiO_2 deposited by e-gun evaporator is so bad that the thickness must be thicker than 200nm to avoid the large gate leakage current. Besides the required thickness of organic dielectric is much thicker than SiO_2 while the dielectric constant is relatively low (e.q. dielectric constant of polyimide is 3.0).

Therefore, in this thesis we deposit the SiO_2 by liquid phase deposition (LPD) method, which provides better quality than those deposited by e-gun evaporator or organic dielectrics.

4.2 A brief introduction of LPD method

The LPD technology was first proposed by Nagayama et al. in 1988[34]. In the beginning,

LPD oxide was deposited on glass substrate to prevent the alkali ions from migrating in the glass. In 1993, Homma et al. found that the LPD oxide can be selectively deposited on SiO_2 layer between tungsten wiring[35],[36]. The novel technology was further applied to VLSI device fabrication [37],[38]. From 1993, Yeh's group began to apply LPD oxide as gate insulator in low-temperature processed poly-Si thin-film transistors (LTPS-TFTs) and MOSFETs[39][40].

Conventionally, CVD is the most common method to deposit SiO_2 with low temperature process. Atmospheric pressure CVD(APCVD), which was firstly used in the microelectronics industry, can operates in atmospheric pressure and allows high deposition rate. However, it is susceptible to gas phase reactions, and the films typically exhibit poor step coverage. Since APCVD processes are generally conducted in the mass transport limited regime, the reactant flux to substrates in the reactor must be precisely controlled.

With low pressure CVD(LPCVD) method, silicon oxide can be deposited at 650~750℃ by decomposing tetraethoxysilane(TEOS). TEOS method is useful for depositing insulators on poly-silicon gate, but the high deposition temperature precludes its use over aluminum. The advantages of TEOS deposition are excellent uniformity, conformal step coverage, and good film properties. The disadvantage is the requirement of high temperature process.

Rather than relying solely on thermal energy to initiate and sustain chemical reaction, plasma enhanced CVD(PECVD) uses an rf-induced glow discharge to transfer energy into the reactant gases, allowing the substrate to maintain at lower temperature. Lower substrate temperature is the major advantage of PECVD. However, the properties of PECVD oxides are not stoichiometric because the deposition reactions are so varied and complicated. Moreover, by-products and incidental species are easily incorporated into the resulting films(especially hydrogen and nitrogen). Excessive incorporation of these contaminants may lead to out-gassing

and concomitting bubbling, cracking or peeling during later thermal cycling, and to threshold shifts in CMOS circuits.

From above introduction, though several CVD methods can be used to prepare LTP SiO_2, the processes are complex and the cost of equipment are high. For LPD SiO_2, there are two main advantages in comparison with other CVD methods: First, the substrate temperature during deposition can be greatly reduced, because LPD SiO_2 can be deposited at room temperature. Second, the apparatus used is much simpler and more inexpensive. The characteristics of LTP oxide include (1)room temperature deposition(2) Inexpensive apparatus(3)Large area application(4)Selective deposition(5)dielectric constant 3.9(fluorine incorporated).

The process flow of deposition LPD oxide is shown in Fig.4-1 and described below. First, 35g of silica(SiO_2) powder with the high purity of 99.99% was added into 1 liter of hydrofluosilic acid(H_2SiF_6, 4 mol/l). The solution became saturated with silicic acid[$Si(OH)_4$] after being stirred at 23℃ for 17 hours. Before immersing the substrates, the solution was filtered to remove the undissolved silica. And deionized water(H_2O) was added to the saturated solution as it was stirred. The added H_2O enable the solution to become supersaturated with silicic acid. The quantity of H_2O added was a quarter of saturated solution. The substrate is placed in the solution and we hold the temperature at 22℃ to deposit the oxide layer. Deposition rate is about 25nm/hour.

4.3 Experimental Detail

4.3.1 Normal P3HT-based OTFTs process flow

The P3HT OTFTs with conventional bottom-contact structure in this experiment are fabricated on silicon substrate as discussed in chapter 1 except the deposition method of insulator. After completed the substrate heavy doping for gate electrode, we used the LPD method to

deposit the SiO_2 for insulator. The thickness of SiO_2 is about 1400Å equal to that of previous experiment for compare the experiment result. After conventional lithography process, 20nm Ti for adhesion layer and 100nm Pt for contact metal were deposited by e-gun evaporator. source/srain region were patterned by lift-off process. P3HT film was deposited by spin-coating method and cured at 120℃ for 3min after HMDS treatment. Before measured the electric characteristics, the samples were stored in vacuum 2 days let the oxygen atoms out-diffuse. The electric characteristics of OTFTs were measured by HP4156 and the capacitances of insulator were measured by HP4284.

4.3.2 Process flow of P3HT OTFTs with isolation dielectric under S/D

The quality of LPD oxide insulator without thermally annealing is poorer than that deposit by PECVD [41]. The gate leakage current of OTFTs with LPD oxide insulator are larger than that of previous experiment. In order to suppress the leakage current we stacked a thick isolation dielectric under the source/drain metal. Comparing to the same structure in [42], the isolation dielectrics need only one lithography process because the selectively deposition properties of LPD method. The schematic diagram is showed in Fig 4-2 and the process flow is showed in Fig4-3. After substrate doping, LPD oxide insulator depositing and lithography process, the oxide of 2000Å thickness for isolation dielectric was deposited by LPD method selectively. Then the 20nm Ti for adhesion layer and 100nm Pt for contact metal were deposited by e-gun evaporator. source/drain region was patterned by lift-off process. After HMDS treatment, P3HT film was deposited by spin-coating method and cured at 120℃ for 3 min. Before measured electric characteristics, the sample was stored in vacuum for 2 days let the oxygen atoms out-diffuse. The electric characteristics of OTFTs were measured by HP4156.

4.4 Result and Discussion

4.4.1 Characteristics of LPD oxide insulator

Because of fluorine incorporated, the dielectric constant of LPD oxide is lower than 3.9. The high frequency C-V curve of LPD oxide in this experiment is showed in Fig 4-4. The heavy n-type doping results in that substrate becomes degenerate n-type semiconductor. So the high frequency C-V characteristics of LPD oxide show the M-I-M(metal-insulator-metal)-like properties. The C/Cox is kept at a steady value from -40 V to 40 V and the dielectric constant is about 3.7 after conversion.

Fig 4-5 shows the typical I-V curves of MOS capacitors with LPD oxide as dielectric. The leakage current density is about 20nA/cm^2 at the electric-field of 4MV/cm. Comparing to that of thermal dioxide, the leakage current density of LPD oxide is higher about one order.

4.4.2 Characteristics of OTFTs with LPD oxide insulator

The output characteristics (I_S vs. V_D) are showed in Fig4-6. The output characteristics I_S vs. V_D of OTFTs with LPD oxide insulator show a normal characteristics of field-effect transistor. Fig 4-7 shows the gate leakage current of OTFTs with LPD oxide and thermal oxide. This value is calculated by subtract measured drain current I_D and source current I_S. The profile is dissymmetrical because the P3HT is a normally-on semiconductor. When applied the positive bias, charge will reject form the interface between the insulator and P3HT. Then the depletion region will form and the gate leakage area is only the patterned source/drain region as shown in Fig 4-8(a). When a negative bias is applied to the gate electrode, the voltage is dropped over the insulator and over the semiconductor near insulator/semiconductor interface and accumulates more positive charge in the accumulation region. The accumulation positive chare region will

form the additional gate leakage path and enlarge the gate leakage area as shown in Fig 4-8(b). So the gate leakage current at the negative gate bias is larger than at positive gate bias at the same voltage value. Comparing to OTFTs with thermal oxide insulator, the gate leakage current of OTFTs with LPD oxide is larger about two order at -30V and only 2 times at +30V. The quality of insulator oxide determines the magnitude of gate leakage current at negative gate bias. At positive gate bias, the interface state between P3HT and insulator and the defect in the oxide will affect the gate leakage current greatly because of the large leakage area. The area of gate leakage will dominate the magnitude of gate leakage current in negative gate bias. The importance of oxide quality is relatively slight in this condition, so the gate leakage current of OTFTs with LPD oxide is only 2 times larger than that with thermal oxide at negative bias.

Fig 4-9 shows the transfer characteristics (I_S vs. V_G) of OTFTs with LPD oxide and thermal oxide insulator. We can find the gap of driving current I_S is large at -30V gate bias, but reduce greatly when applied gate electrode of 30V. When applied negative bias at gate electrode and the device be operated in off-state, the slight driving current I_S will be affected enormously by the gate leakage current. The poorer quality of LPD oxide results in the large off-state leakage current and huge power consumption. When the device is operated in on-state, the effect of gate leakage current is relatively smaller because of the large driving current. Although the gate leakage current is great larger when applied positive gate bias, the increase rate of gate leakage current compares to that of driving current is negligible.

The field-effect mobility of OTFTs with LPD is 1.78×10^{-3} and On-Off ratio is 9.4×10^{3} respectively. Comparing to OTFTs with thermal oxide, the value of OTFTs with LPD oxide is slightly increased because of gate leakage current.

4.4.3 Characteristics of OTFTs with LPD oxide insulator and isolation dielectric

The output characteristics (I_S vs. V_D) are showed in Fig4-10. The output characteristics I_S vs. V_D of OTFTs with LPD oxide insulator and isolation dielectric also show a normal characteristics of field-effect transistor. Fig 4-11 shows the gate leakage current of OTFTs with LPD oxide and that with additional isolation dielectric. We can easily find that gate leakage current is reduced about one order because of the additional isolation dielectric. The reducing of gate leakage current when applied negative bias to gate electrode and let the device operate in depletion mode, as shown in Fig 4-8(a), is attributed to the thicker dielectric thickness between source/drain metal and gate electrode. When applied positive bias to gate electrode, the gate leakage path is not only through the thick dielectric layer between source/drain metal and gate electrode but also include accumulation layer area through the thin gate oxide between accumulation layer and gate electrode. The thick isolation layer reduces the leakage current by thicker dielectric thickness states forward. The other role is that modification of electric field distribution between source/drain metal and the semiconductor channel and thereby enhanced charge injection. The additional layer redistributes the electric field to fall on the semiconductor near the area connecting to gate electrode.

Comparing to the output characteristics (I_S vs. V_G) of OTFTs with and without the isolation layer as shows in Fig 4-12, the off-state leakage current is reduce one order by the additional isolation dielectric. The smaller on-state driving current of OTFTs with isolation dielectric maybe result from not only reduces the gate leakage, but also the thicker layer results in lager series resistance stated in chapter 2. The field-effect mobility of OTFTs with isolation dielectric is 1.42×10^{-3} and On-Off ratio is 6.34×10^{3} respectively. Those data include field-effect mobility, off-state leakage current and On-Off current ratio were summarized in Table 4-1. We can find the additional isolation dielectric structure effectively reduces the off-state leakage current but still larger than OTFTs with thermal oxide insulator. The larger series resistance of OTFTs with

additional isolation dielectric structure results in slightly lower field-effect mobility and On-Off current ratio than that with thermal oxide insulator. The lower dielectric constant (k~3.7) is also a parameter affect the performance of OTFTs but not conspicuous in this experiment due to the gate leakage current effect.

4.5 Summry

We developed a new process for OTFTs by use LPD oxide as the gate insulator. The advantage of this process includes low temperature process, large area application, inexpensive apparatus, good insulator quality. The gate leakage properties of OTFTs is investigated and discussed. The performance of OTFTs with LPD oxide insulator is useable and the field-effect mobility is 1.78×10^{-3}, On-Off current ratio is 9.4×10^{3} that is comparable to OTFTs with thermal oxide. The off-state leakage current of OTFTs with LPD oxide insulator is relatively large that needs to improve further.

Next, we deposit a thick isolation dielectric under the source/drain region to reduce the gate leakage current. The LPD method can save one lithography process when fabricate this device because of selectively deposition property. The OTFTs with isolation dielectric can reduce the gate leakage current and off-state current of one order. The field effect mobility of OTFTs with isolation dielectric is 1.52×10^{-3} and the On-Off current ratio is 6.34×10^{3}. Because of lager series resistance, the field-effect mobility and On-Off current ratio is slightly lower than that with thermal oxide.

The process of OTFTs with LPD oxide and isolation dielectric is developed. It applied a solution to fabricate the OTFTs on plastic, clothes and paper substrate.

Stacked isolation dielectric under source/drain region can reduce the gate leakage current but lower the field-effect mobility and On-Off current ratio. It can optimize by adjust the

thickness of gate insulator and isolation dielectric. The structure of stacked isolation dielectric under source/drain region of OTFTs is similar to the LDD structure of conventional MOSFETs that can reduce leakage but increase series resistance. This structure maybe can raise the reliability of OTFTs need further work to investigate.

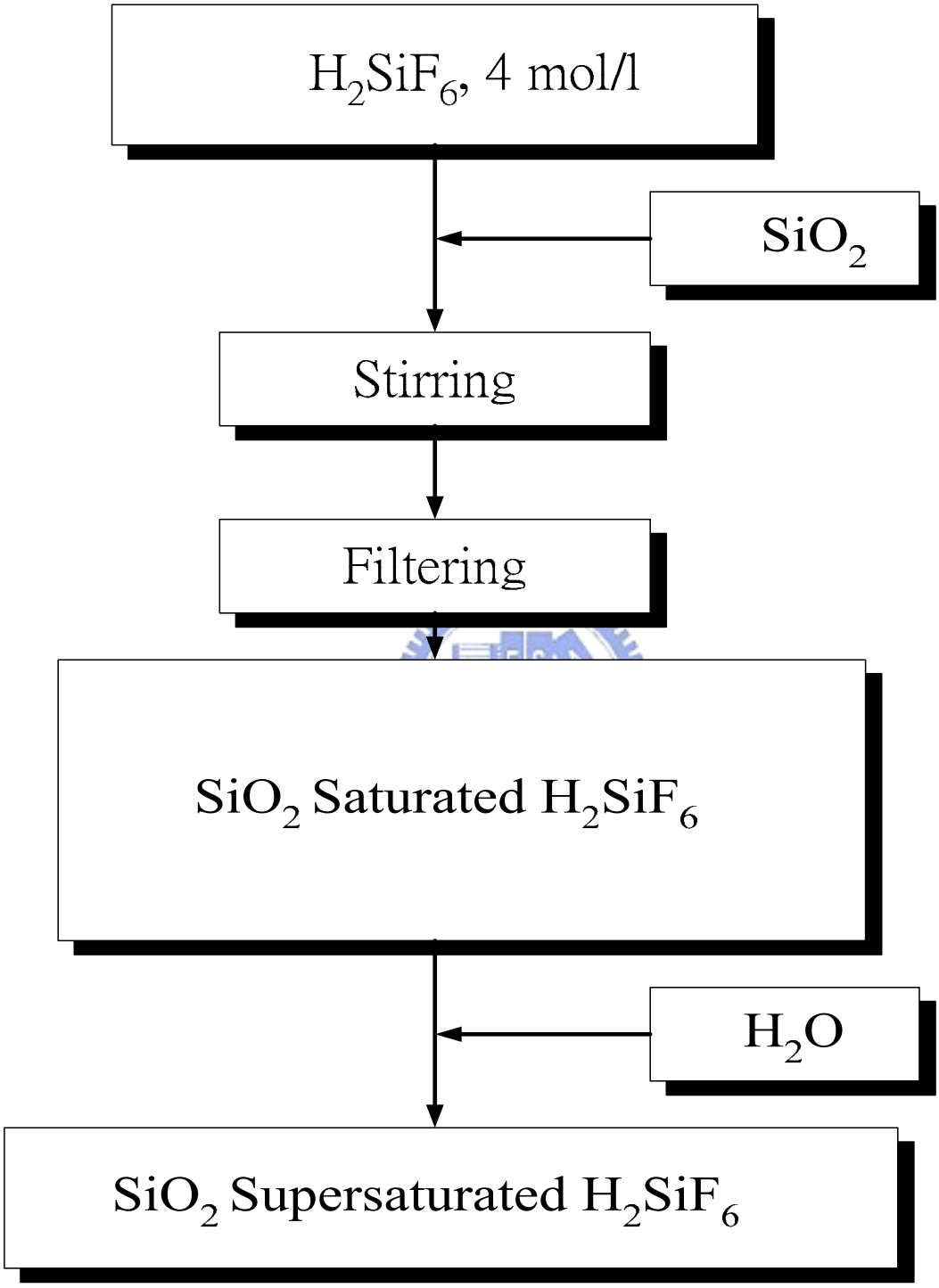


Figure 4-1: The process flow of deposition LPD oxide

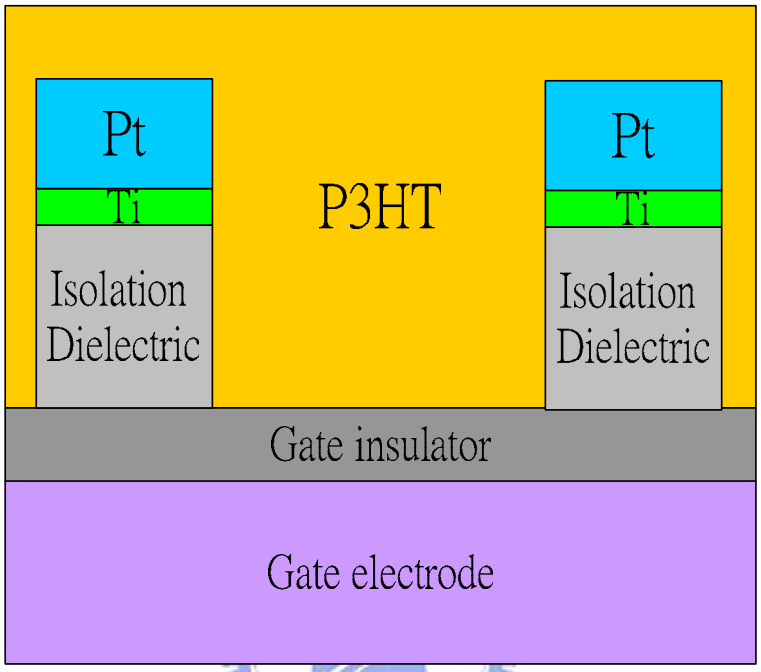


Figure 4-2: The schematic diagram of OTFT with isolation dielectric under Source/Drain region.

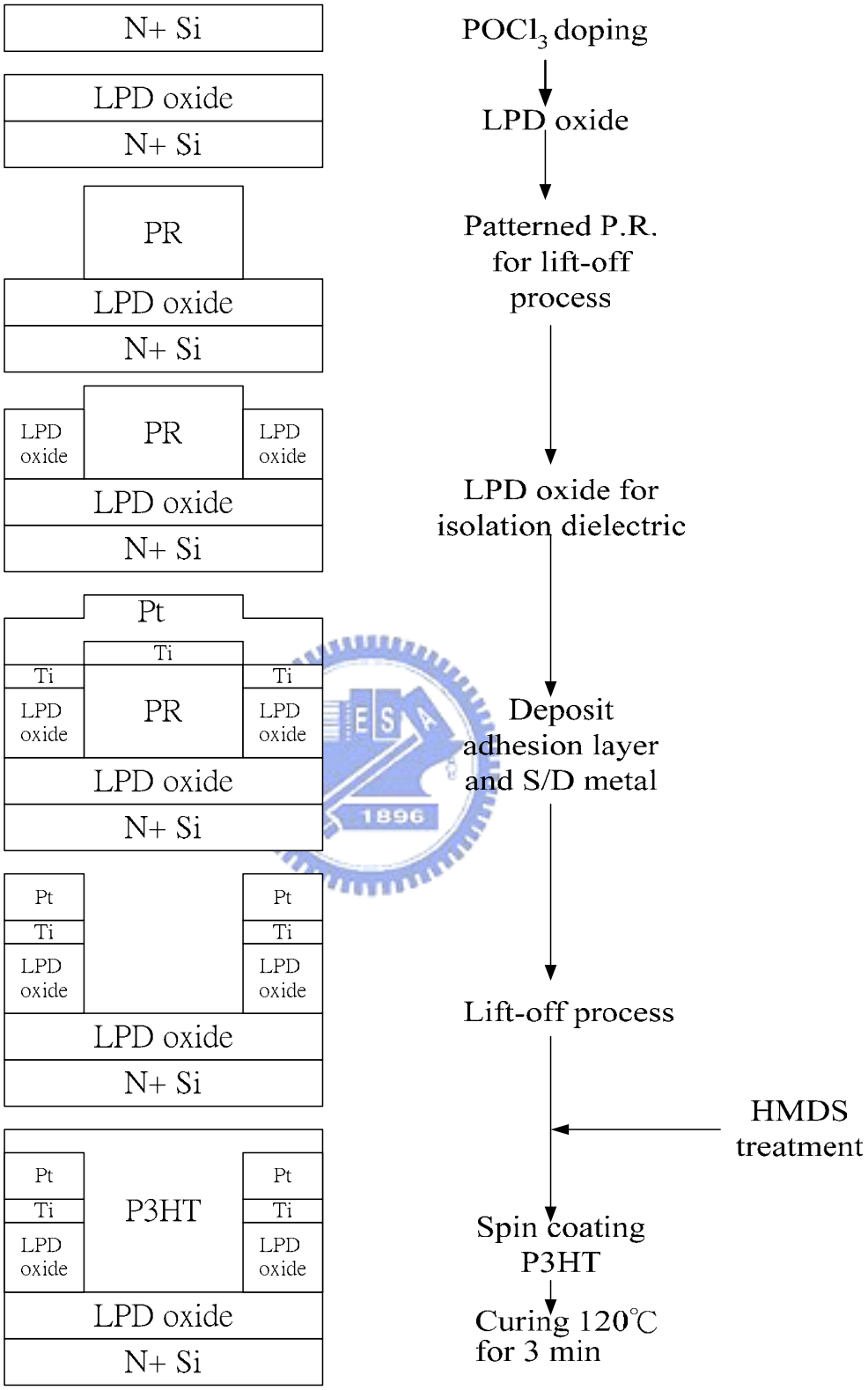


Figure 4-3: Process flow of OTFT with isolation dielectric under source/drain region.

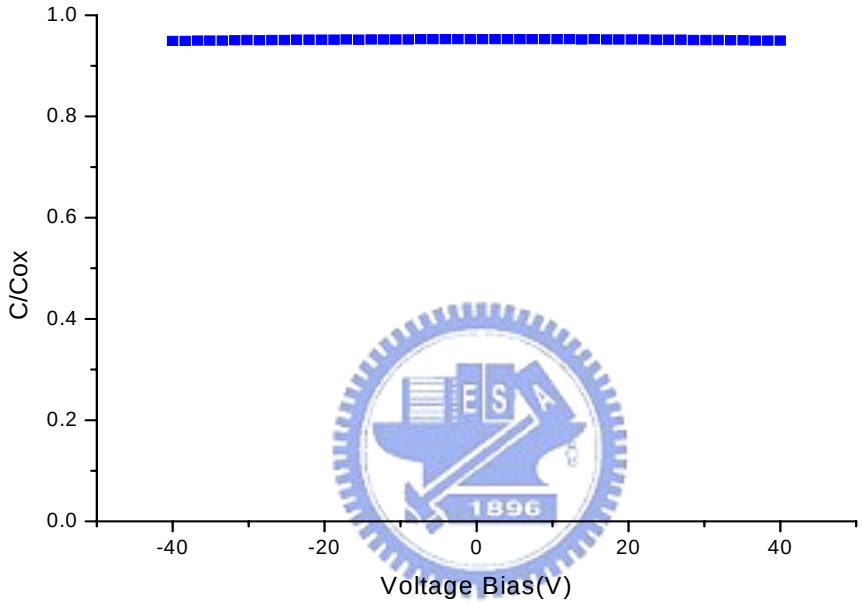


Figure 4-4: The high frequency C-V curve of LPD oxide

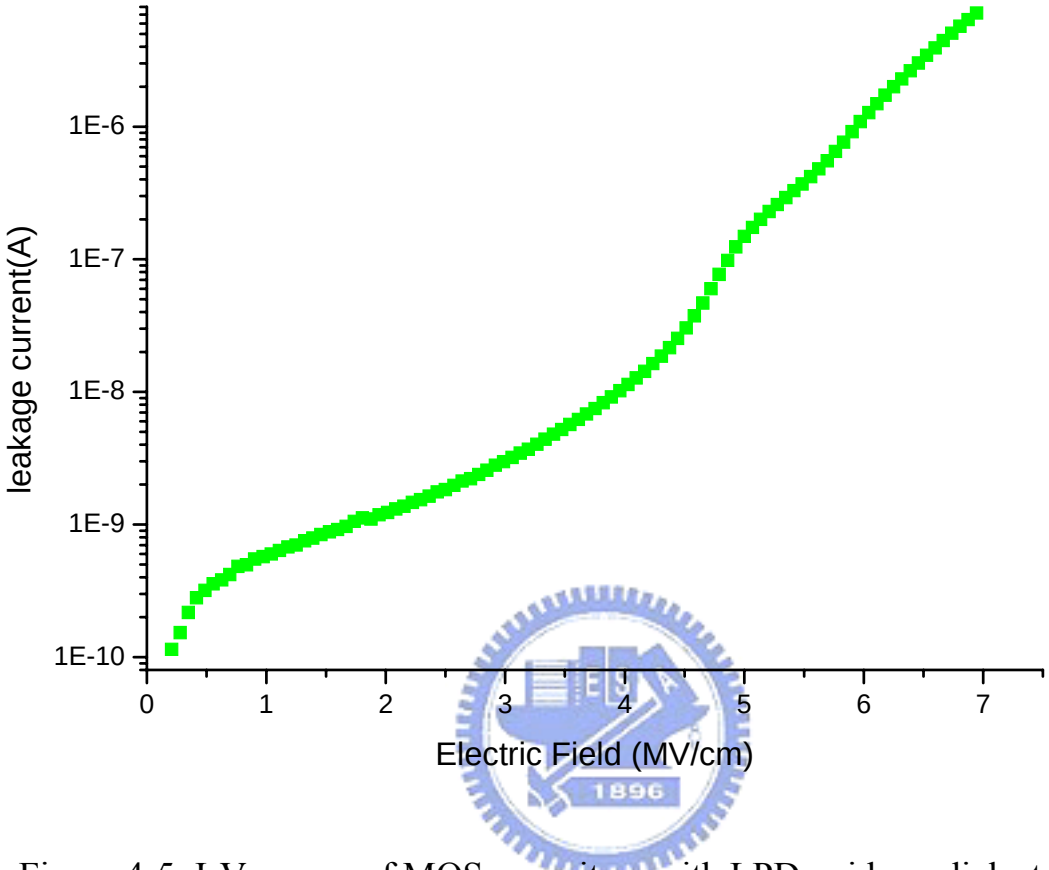


Figure 4-5: I-V curves of MOS capacitors with LPD oxide as dielectric

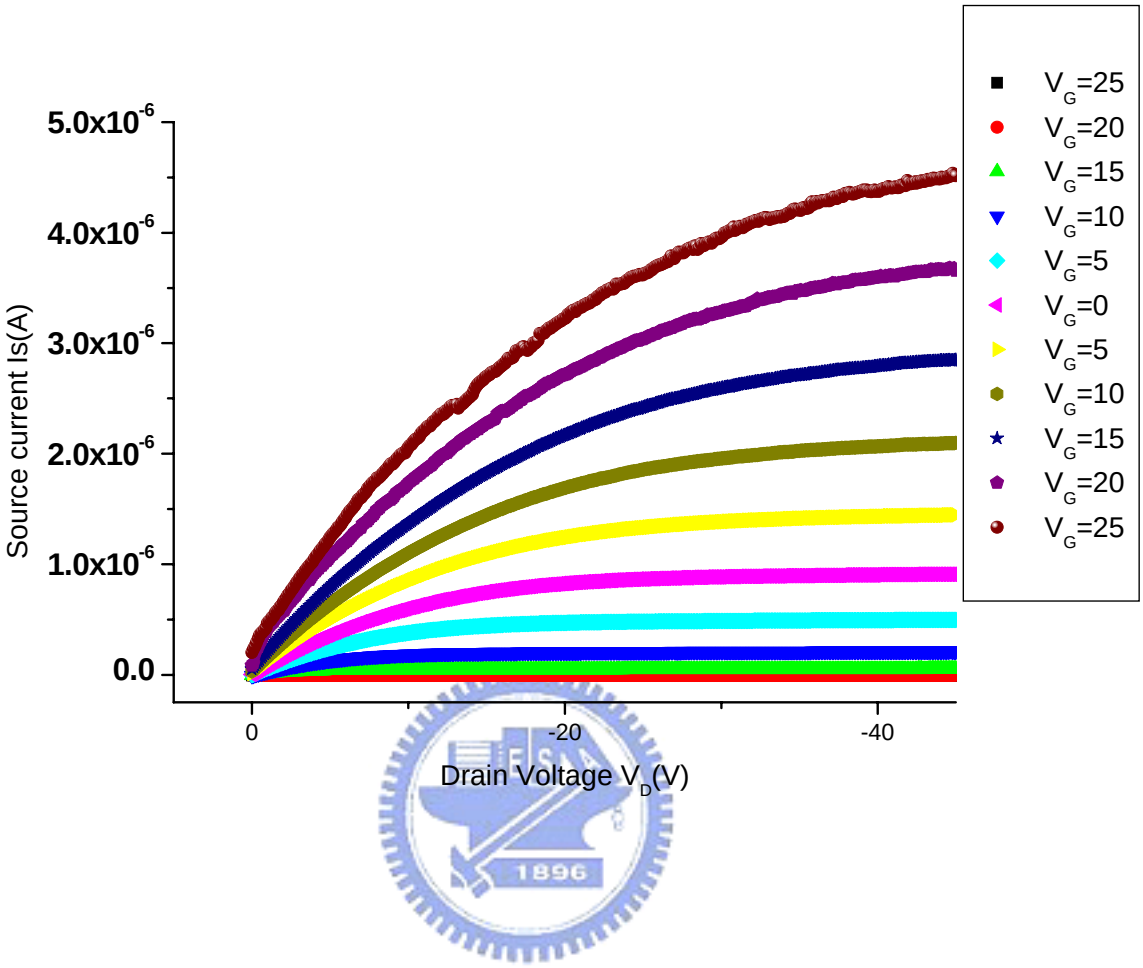


Figure 4-6: Output characteristics I_S vs. V_D of P3HT OTFTs with LPD oxide insulator.

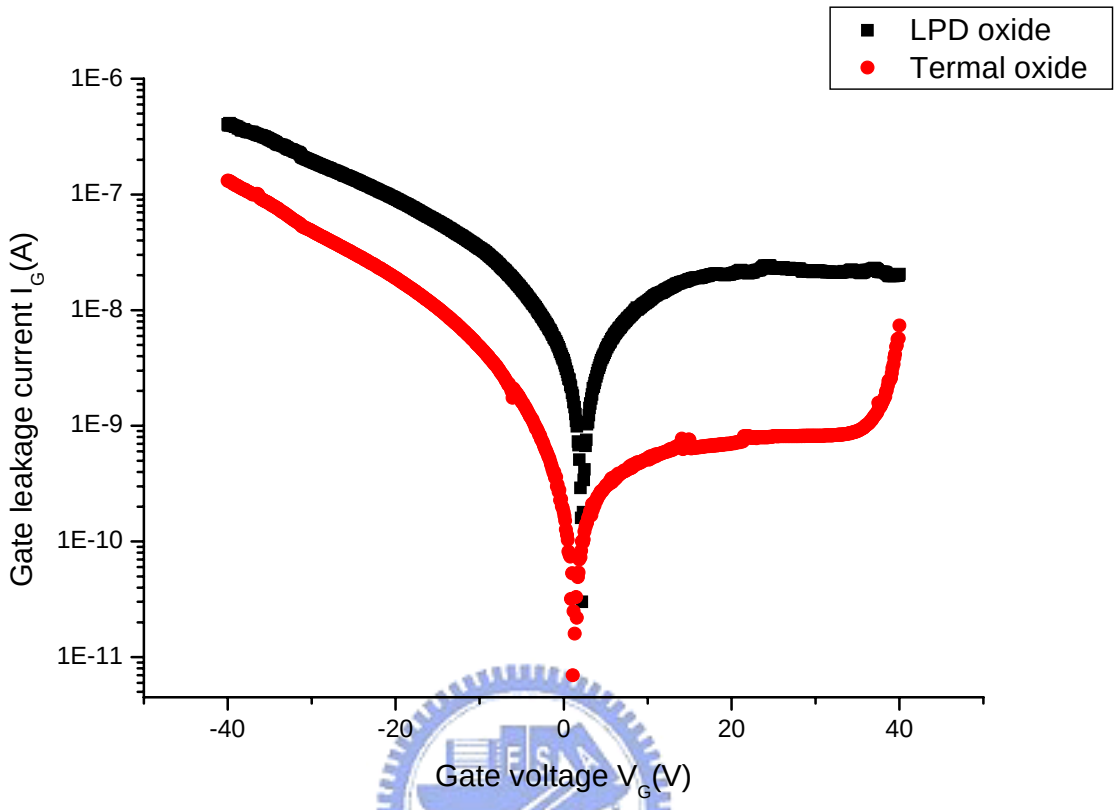


Figure 4-7: Gate leakage current of P3HT OTFTs with LPD oxide and thermal oxide insulator.

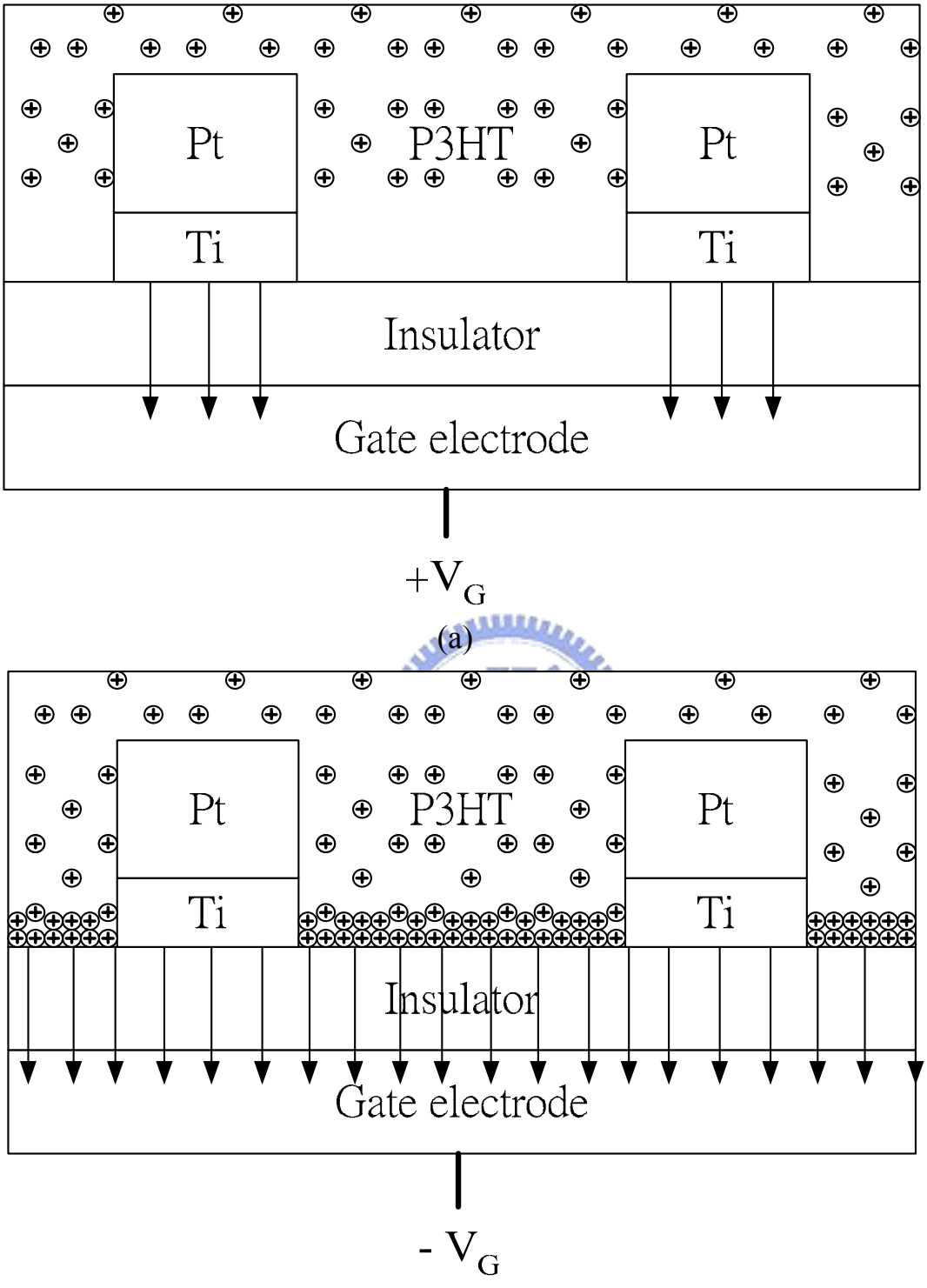


Figure4-8: Gate leakage path of OTFTs at (a)positive gate bias (b) negative gate bias.

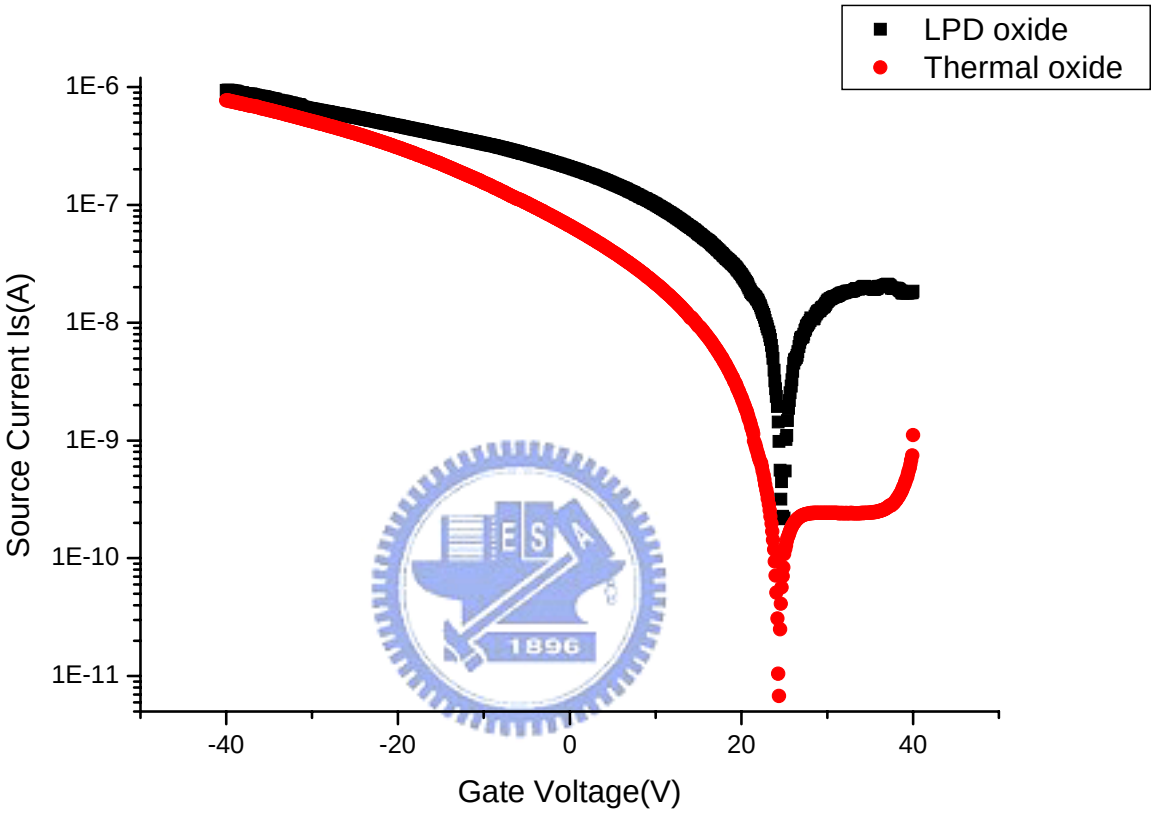


Figure 4-9: The transfer characteristics I_S vs. V_G of OTFTs with LPD oxide and thermal oxide insulator

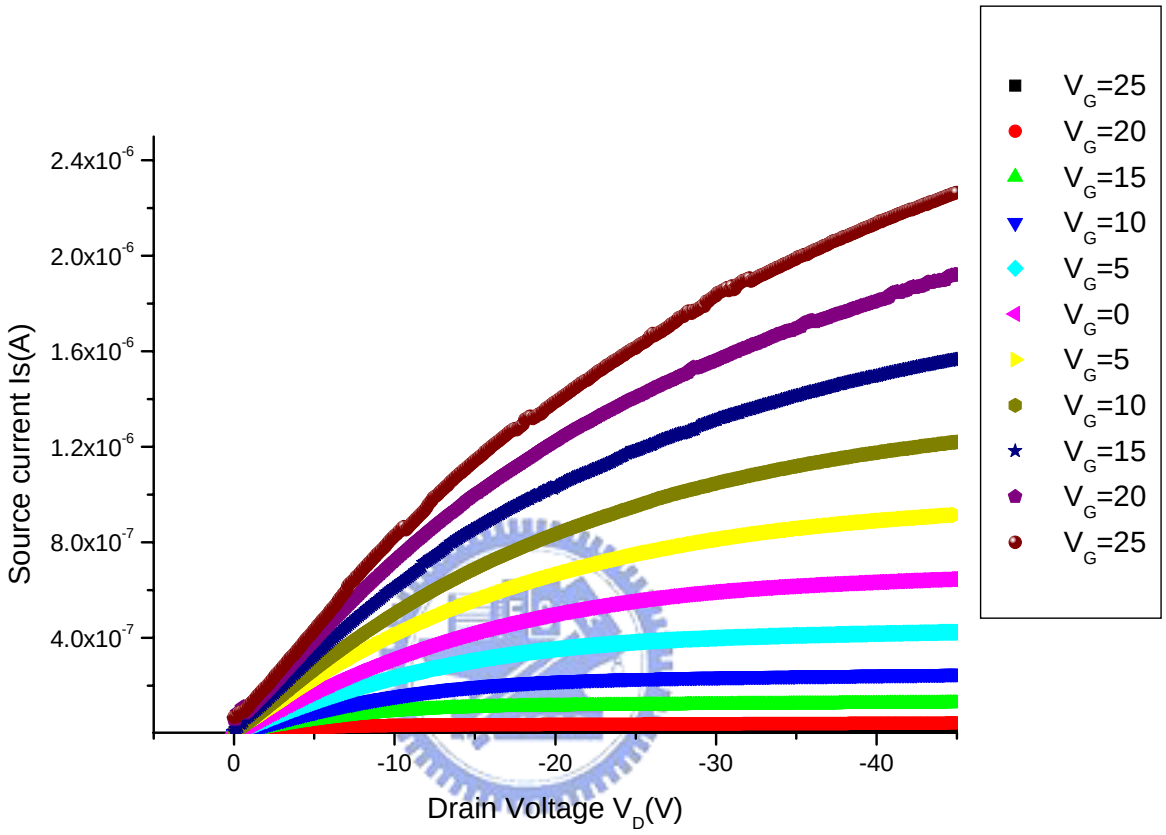


Figure 4-10: Output characteristics I_S vs. V_D of P3HT OTFTs with LPD oxide insulator and isolation dielectric.

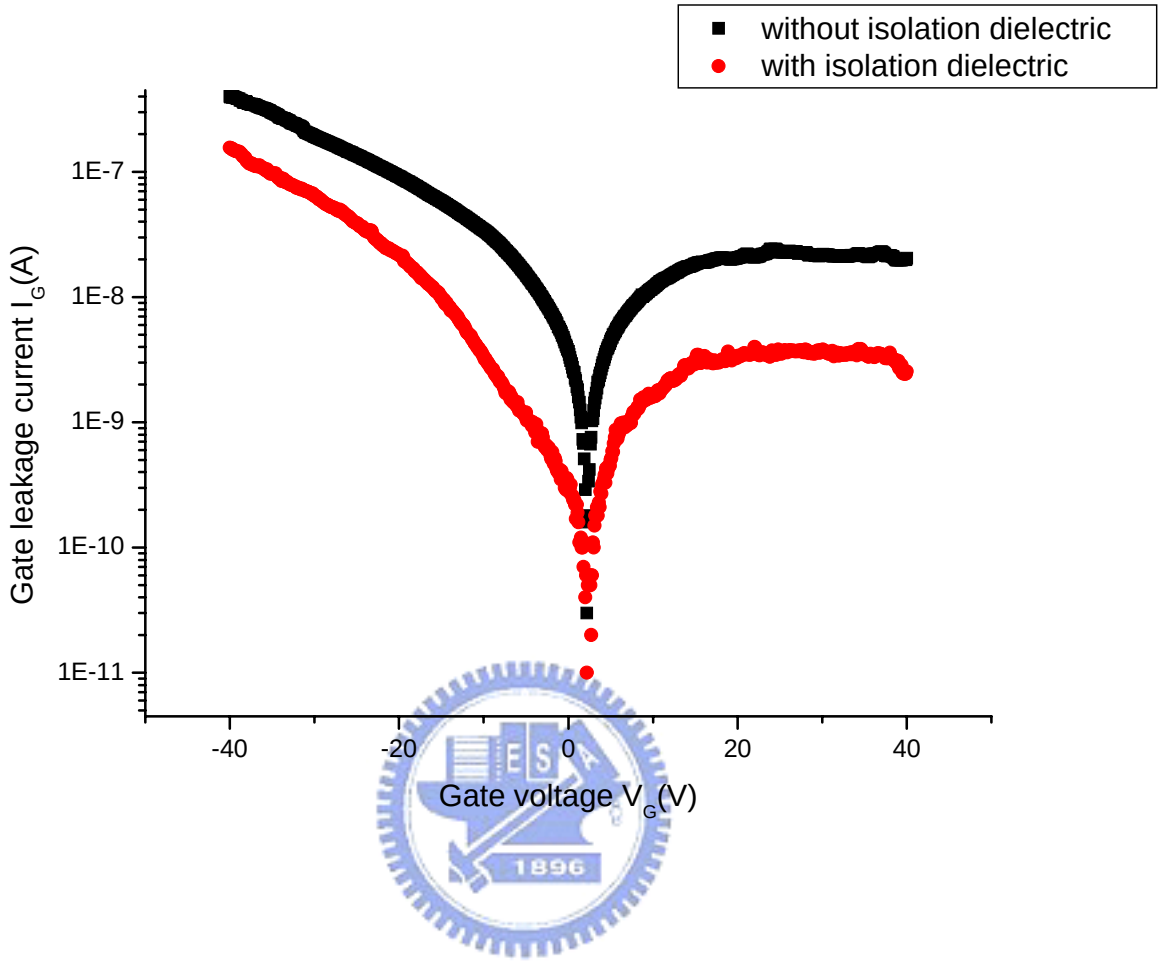


Figure 4-11: Gate leakage current of P3HT OTFTs with and without isolation dielectric.

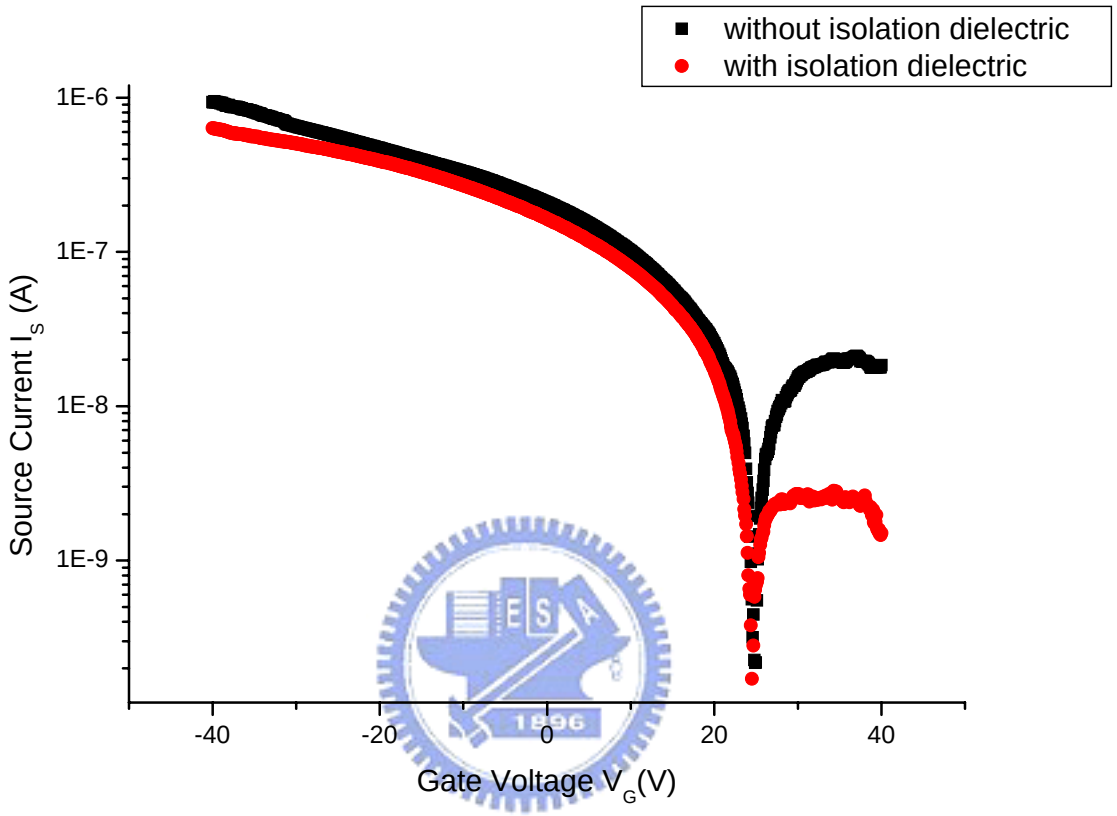


Figure 4-12: The transfer characteristics I_S vs. V_G of OTFTs with and without isolation dielectric.

	Thermal oxide	LPD oxide	LPD oxide with isolation dielectric
Field-effect Mobility μ(cm/V-s)	$1.60x10^{-3}$	$1.78x10^{-3}$	$1.52x10^{-3}$
Off state leakage	$8.4x10^{-10}$	$2x10^{-8}$	$2.55x10^{-9}$
On-Off ratio	$7.73x10^{3}$	$9.4x10^{3}$	$6.34x10^{3}$

Table 4-1:Field-effect Mobility, Off state leakage and On-Off ratio of OTFTs with thermal oxide, LPD oxide and LPD oxide with isolation dielectric.

Chapter 5

Conclusion and Future work

5.1 Conclusions

The feasibility study of Spin-Coating technique, physical and the electrical characteristics of P3HT OTFT are investigated. Here, we conclude our study into three parts: (1) Contact Resistance of P3HT OTFTs (2) Electric Stability of P3HT OTFTs (3) Low Temperature Process of P3HT OTFTs with LPD SiO_2 as Insulator.

5.1.1 Contact Resistance of P3HT OTFTs

The effect of contact resistance between source/drain electrodes and P3HT has been experimentally investigated. We applied a simple model to estimate the contact resistance between source/drain electrodes and P3HT and found that the contact resistance is typically greater than the contact resistance of inorganic transistors.

Because the interfacial layer formed at Ni and Cr surface lead to large contact resistance, even the work function of both are larger(or equal) then P3HT. The crowding effect was occurred when the OTFTs were fabricated by Ni as contact metal. When OTFTs were fabricated by Cr as contact metal isn't shown normal property. Using Pt as S/D contact materials would result in better I-V characteristics.

Capping the thin Pt film on the Ni or Cr as contact meal can greatly reduce the contact resistance of OTFTs. The contact resistance of OTFTs with Pt film on Cr as contact metal is relatively larger than that with Pt film on Ni as contact metal because Cr layer cannot form ohmic contact with P3HT. The extracted field-effect mobility of OTFTs with Pt as contact electrode is

2.6 x$10^{-3}$$cm^2$/V-s, and with Pt film on Ni as contact electrode is 2.38x$10^{-3}$$cm^2$/V-s. OTFTs with a capped thin Pt film on Ni as contact metal can instead of Au or Pt as contact metal for lower cost and acceptable performance.

Thickness of adhesion layer is not a critical parameter to affect the performance of OTFTs except the ON current distribution.

5.1.2 Electric Stability of P3HT OTFTs

The electric reliability of P3HT OTFTs is tested. The field-effect mobility and gate leakage current did not be affected significantly after hot-carrier stress. The threshold voltage shift is attribute to polarization effect of P3HT film.

The polarization phenomenon in P3HT OTFTs is investigated. The dipole built-in field is originated from the P3HT film. Threshold voltage shift ratio saturated after a span and the last value is as large as the gate bias. The threshold voltage shift rate isn't direct proportion to gate bias voltage in the initial stage. The polarization will release when addition electric field remove in P3HT OTFTs but cannot return to initial characteristics.

To conclusion that state above, the P3HT OTFTs isn't affect significantly by electric stress but polarization effect. The device is operation in AC in generally and the dipoles need a span to turn the direction with additional electric field despite strong or weak. The P3HT OTFTs will quite stable under normal operation conditions.

5.1.3 Low Temperature Process of P3HT OTFTs with LPD SiO_2 as Insulator

We developed a new process for OTFTs by use LPD oxide as the gate insulator. The advantage of this process includes low temperature process, large area application, inexpensive apparatus, good insulator quality. The gate leakage properties of OTFTs is investigated and

discussed. The performance of OTFTs with LPD oxide insulator is useable and the field-effect mobility is $1.78x10^{-3}$, On-Off current ratio is $9.4x10^{3}$ that is comparable to OTFTs with thermal oxide. The off-state leakage current of OTFTs with LPD oxide insulator is relatively large that needs to improve further.

Next, we deposit a thick isolation dielectric under the source/drain region to reduce the gate leakage current. The LPD method can save one lithography process when fabricate this device because of selectively deposition property. The OTFTs with isolation dielectric can reduce the gate leakage current and off-state current of one order. The field effect mobility of OTFTs with isolation dielectric is $1.52x10^{-3}$ and the On-Off current ratio is $6.34x10^{3}$. Because of lager series resistance, the field-effect mobility and On-Off current ratio is slightly lower than that with thermal oxide.

The process of OTFTs with LPD oxide and isolation dielectric is developed. It applied a solution to fabricate the OTFTs on plastic, clothes and paper substrate.

Stacked isolation dielectric under source/drain region can reduce the gate leakage current but lower the field-effect mobility and On-Off current ratio. It can optimize by adjust the thickness of gate insulator and isolation dielectric. The structure of stacked isolation dielectric under source/drain region of OTFTs is similar to the LDD structure of conventional MOSFETs that can reduce leakage but increase series resistance. This structure maybe can raise the reliability of OTFTs need further work to investigate.

5.2 Future work

5.2.1 A new method to deposit P3HT thin film

There are three methods to deposit P3HT thin films: (1) spin-coating (2) dip-coating (3) drop-casting. In our experiment, we made use of spin-coating method to deposit P3HT thin films

and attain an optimized deposition parameter for producing P3HT thin films. However, among the three methods to deposit P3HT thin films, the best method is drop-casting. Therefore, in the future we will make use of drop-casting to deposit P3HT thin films, and study the deposition parameters of drop-casting.

5.2.2 Thermal stability of P3HT OTFTs

In addition to studies of device lifetime and the stability of P3HT in different ambient, thermal stability is another topics .This is an important topic for various reasons. First, poly (3-hexylthiophenes) devices will be likely exposed to elevated temperatures during the fabrication process, due to the annealing requirements of other layers. Second, thermal cycling studies provide crucial insights into device lifetime and stability. [44]

5.2.3 An in-situ pacivation layer for protecting the P3HT film

From our experimental results, P3HT OTFTs are sensitive to ambient conditions. Protection from the environment by encapsulation is critical to the stability of P3HT OTFTs. Therefore, using a suitable material as pacivation to protect P3HT film from environmental effect is another important topic.

5.2.4 New gate insulator materials for P3HT OTFTs

From the performance point of view, the most important parameters are charge carrier mobility, ON-OFF current ratio and the operational voltage range. However, the operating voltages of P3HT OTFT required to produce such performance were impractically high, around 50~60V. Although decreasing the thickness of SiO_2 could reduce the operating voltages of P3HT OTFT, the gate leakage current would increase with decreasing the thickness of SiO_2 and affect the

performance of P3HT OTFT. Therefore, the use of high dielectric gate insulator materials is possible for reducing operating voltages of P3HT and gate leakage current. [45], [46], [47]

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