國立交通大學

電子工程學系　　電子研究所碩士班

碩士論文

新穎製程及新穎結構的複晶矽薄膜電晶體之可靠度研究

Reliability Study of Novel Process and Novel Structure Polysilicon Thin-Film Transistors

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新穎結構及新穎製程的複晶矽薄膜電晶體之可靠度研究分析

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摘要

本論文主要分爲兩大部分

一、新穎抗衰退複晶矽薄膜電晶體元件之製作

二、新穎高性能複晶矽薄膜電晶體元件結構之改良

在第一部份，我們提出了將氟離子藉由沈積間隙壁的過程中一同參雜其中，即沈積氟矽玻璃來當間隙壁(Spacer)的輕量參雜結構(Light Doped Drain)薄膜複晶矽結構，來探討此元件與一般 LDD 結構的可靠度分析。發現此新結構具除了有較少的扭曲效應(Kink effect)外，在外加裂化時有較好的抗臨界電壓、驅動電流以及傳導電導的劣化能力，主要是因爲複晶矽介面與含氟的間隙壁之間而外產生較強的矽氟鍵鍵結，不但修補掉複晶矽表面的懸浮鍵，而減少缺陷數目外，還因爲矽氟鍵的鍵能較一般矽氫鍵鍵能強兩倍，更能抵抗電流離子化的撞擊而更穩定。

另一部份，我們提出了多重奈米通道結構的薄膜電晶體，發現其本身的電性效能，在電流開關比(on/off ratio)、汲極引致通道能障底落(Drain Induce Barrier Lowing)、和次臨界電導斜率(subthreshold slope)方面，較單條通道但卻具有近乎等效通道寬度的電晶體而言要好。

此外，在外加直流與交流的劣化條件下，其也在臨界電壓、驅動電流以及傳導電導方面有著優越的表現。其原因可能是由於多重通道結構具有優越的三面閘極(tri-gate)控制能力，而能減低横向電場所導致降低通道間的位障能而使得汲極電流上升而造成更嚴重的劣化；也可能因爲由於多條通道會使得電流分流，而減低自我加熱效應(Self-Heating Effect)，此外也可能因爲本身結構所鈍化曝出的表面積較多及移動率低，而降低表面缺陷和電子加速能量而使得抗劣化效果好。

Reliability Study of Novel Process and Novel Structure in Poly-Silicon Thin-Film Transistors

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Abstract

This thesis can be divided into two major parts:

(1) Reliability study of novel fluorinated spacers process Poly-Si TFTs

(2) Reliability study of novel multiple nanowire channels structure Poly-Si TFTs

In the first part, high reliability polycrystalline silicon thin-film transistors (poly-Si TFTs) with lightly-doped drain (LDD) structure were obtained by using a self-aligned fluorinated silica glass (FSG) spacer technique. The output characteristics of FSG spacer show the superior immunity to kink effect. It is also found that the degradations in Vth shifting, drain current and trans-conductance of FSG spacer after DC stress are improved.

This is attributed to the passivation of fluorine ions reduces the trap states in the LDD region. Additionally, the stronger Si-F bonds also reduce the bonds broken by impact ionization.

In the second part, the experiment results reveal that the novel multiple nanowire structure poly-Si TFTs has a lower DIBL, a lower SS and a higher on/off ratio than the single-channel TFT. In static and dynamic stress reliability experiments, the multiple nanowire poly-Si TFTs reduces the degradation of Vth, SS, Ion, and On/OFF ratio, compared to single-channel TFT. These high reliability results of multiple nanowire poly-Si TFTs can be explained by its robust tri-gate control and its superior channel NH_3 passivation for reducing the poly-Si grain boundary defects.

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終於，兩年的碩士班研究生活，以此論文之告成，即將告一段落。在這兩年裡首先要感謝張俊彥老師與張鼎張老師的細心指導實驗研究與論文上給予充分詳實的指導與鼓勵，此外也讓我學到很多寶貴的知識和學問，也學到處理事情的態度和方法，使我有想法與啟發。感謝我的家人，尤其是我的父親與母親，能在我求學的階段提供給我莫大的幫助與鼓勵，讓我能無後顧之憂地順利完成學業。

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Chapter 1

Introduction

1-1. Overview of polysilicon thin-film transistors technology

The interest in polycrystalline silicon thin-film transistors (poly-Si TFTs) has drastically increased in recent years because of their widely applications on active matrix liquid crystal displays (AMLCDs)[1], and organic light-emitting displays (OLEDs)[2]. Except displays application, poly-Si TFTs also have been applied into some memory devices such as dynamic random access memories (DRAMs)[3], static random access memories (SRAMs)[4], electrical programming read only memories (EPROM)[5], electrical erasable programming read only memories (EEPROMs)[6], linear image sensor[7], thermal printer heads[8], photo-detector amplifier[9], scanner[10], neutral networks[10]. Recently, some superior performances of poly-Si TFTs also have been reported by scaling down device dimension or utilizing novel crystallization technologies to enhance poly-Si film quality [11.12]. This provides the chance for applying poly-Si TFTs into three-dimension (3-D) integrated circuit fabrication. Of course, the application in AMLCDs is the primary trend, which leads to rapid development of poly-Si TFT technology.

Currently, the main application of poly-Si TFT processed at low temperature (below 600^0C) is the AMLCDs and AMOLED. The electron mobility of a poly-Si TFTs ranged from few tens to several hundred cm^2/Vs which are several orders of magnitude higher than in amorphous-Si (a-Si) TFT. That is enough to be used as peripheral-driving circuits including n- and p- channel devices. The fabrication of peripheral circuit can be integrated into the structure, i.e., peripheral circuits and switch pixel elements can be on the same glass substrate, and therefore, it reduces the size of the total panel[13]. In addition, for the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high density, high resolution AMLCDs, and the aperture ratio in TFT array can be significantly improved by using poly-Si TFTs as pixel switching elements[14]. This is because the device channel width can be scaled down while achieving the same pixel driving requirements as in a-Si TFT AMLCDs.

However, reliability of ploy-Si TFT is one of the main constraints toward this direction. In comparison with single-crystalline silicon, granular structure of poly-Si is rich in grain boundary defects arising from lattice discontinuities between different oriented grains as well as intra-grain defects. Moreover, a low process temperature, i.e. less than 600 ^{0}C, also produces numerous defects at the poly-Si\SiO_2 interface and poly-silicon boundaries. Under the operation of high drain voltage and a relatively high gate voltage (hot-carrier condition), the defects acting as trapping centers lead to hot-carrier injection that generates trap states to trap carriers. Carriers trapped by these low energy traps can no longer contribute to conduction, which results in the formation of local depletion region and potential barriers in these grain boundaries. Thus, those trap states are strongly influenced the performance of poly-TFTs and causes severe device degradation. Large leakage current inducing the charge holding issue of AMLCDs is resulted from carrier generation from the poly-Si grain boundary defects. Also, the typical characteristics such as threshold voltage (Vth), subthreshold swing (SS), ON current (Ion), field effect mobility (μ_{eff}) and transconductance (Gm) of TFTs are inferior to those of devices fabricated on single crystal silicon film. The (Gm)max degradation and Vth variation during stress application which results in improper operation and circuit failure is of great importance for circuit designers in order to integrate TFTs in flat-panel displays or VLSI circuits.

There are several approaches toward these obstructions. The main propose is modifying or eliminating these grain boundary traps associated with dangling bonds. One is the enlargement of poly-Si grains, which reduces the total length of the poly-Si grain boundaries in the channel area. However, this approach enhances the variation of TFT performance. Another approach is the passivation of the grain boundary traps. Generally, hydrogenation has been utilized for the passivation, but the hydrogenated TFT has poor immunity against the negative bias temperature stress.

In this thesis, we apply novel process and novel structure to improve the poly-Si reliability. In the novel process of poly-Si TFT, a self-aligned fluorinated silica glass (FSG) spacers with Si-F bonds formation near the interface of source and drain is used due to its stronger dissociation energy of Si-F bonds. In the novel structure TFT, the multiple nano-wire channels with surrounding gate electrode is used due to the superior gate controllability. Two kinds of TFTs are introduced to achieve high reliability under static and/or dynamic stress.

1-2. Motivation

Although poly-Si TFTs have many superior advantages, the presence of a large number of grain boundaries in poly-Si TFTs contributes a large density of defects which cause the localized states in the energy gap and degrade performance. So the reliability issue is one of the most constraints toward the applications.

There are many investigations about the improvement of the poly-Si TFTs reliability. It is reported about the reliability improvement in poly-Si TFTs by fluorine implantation. But it needs an extra implantation, which may cause the implantation damage in the active layer and shifts the threshold voltage. It is known that one of the degradation is caused by the energetic electrons generated by impact ionization near the drain. So we introduce the fluorinated spacer technique to generate the higher dissociation Si-F bonds adjust to the interface of the drain which is the largest lateral electric field region for light doped drain structure. This method needs not additional process step and also can achieve the improvement of reliability.

In the structure aspect, according to CMOS technology, several high performance surrounding gate structures in silicon on insulator (SOI) MOSEFT, such that double-gate, gate-all-around, tri-gate[16], and FinFET[17], have been reported that they have superior gate control over channel than conventional single-gate MOSFET to reduce the non-ideal effects. Thus we employed multiple channels and LDD structure to investigate the reliability on the surrounding gate controllability. For devices with smaller dimension, the number of grain boundaries decreases since there are fewer grains within the channel region. Because the drain voltage drops mainly on the depletion regions located at grain boundaries, fewer grain boundaries represent larger voltage drop on each depletion region under the same drain voltage. Therefore, a large electric field will exist in small dimension TFTs to induce impact ionization effect. If the electric field exceeds 10^5 V/cm, the impact ionization effect will occur and the drain current will increase dramatically. To overcome this inherent disadvantage of small dimension of TFT, we apply the lightly-doped drain (LDD) structure to reduce the lateral electrical field in channel.

1-3. Thesis Outline

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Chapter 2

Poly-Si TFT conduction mechanism and reliability after static and dynamic stress

2-1. TFT transportation mechanism

As mentioned in section 1-1 and 1-2, the device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. Even though the inversion channel region is also induced by the gate voltage as in MOSFETs, the existence of grain structure in channel layer bring large differences in carrier transport phenomenon. Many researches studying the electrical properties and the carrier transport in poly-Si TFTs have been reported. A simple grain boundary-trapping model has been described by many authors in details. In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size L_g and the grain boundary trap density N_t. The charge trapped at grain boundaries is compensated by oppositely charged depletion regions surrounding the grain boundaries. From Poisson's equation, the charge in the depletion regions causes curvature in the energy bands, leading to potential barriers that impede the movement of any remaining free carriers from one grain to another. When the dopant/carrier density n is small, the poly-Si grains will be fully depleted. The width of the grain boundary depletion region x_d extends to be $L_g/2$ on each side of the boundary, and the barrier height V_B can be expressed as

$$V_B = \frac{qn}{2\varepsilon_s} x_d{}^2 = \frac{qnL_g{}^2}{8\varepsilon_s} \tag{1-1}$$

As the dopant/carrier concentration is increased, more carriers are trapped at the grain boundary. The curvature of the energy band and the height of potential barrier increase, making carrier transport form one grain to another more difficult. When the dopant/carrier density increases to exceed a critical value $N^* = N_t / L_g$, the poly-Si grains turn to be partially depleted and excess free carriers start to spear inside the grain region. The depletion width and the barrier height can be expressed as

$$x_d = \frac{N_t}{2n} \tag{1-2}$$

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t{}^2}{8\varepsilon_s n} \tag{1-3}$$

The depletion width and the barrier hight turn to decrease with increasing dopant/carrier density, leading to improved conductivity in carrier transport.

The carrier transport in fully depleted poly-Si film can be described by the thermionic emission over the barrier. Its' current density can be written as [23]

$$J = qnv_c \exp[-\frac{q}{kT}(V_B - V)] \tag{1-4}$$

where n is the free-carrier density, v_c is the collection velocity ($v_c = \sqrt{kT/2\pi m^*}$), V_B is the barrier height without applied bias, and V_g is the applied bias across the grain boundary region. For small applied biases, the applied voltage divided approximately uniformly between the two sides of a grain boundary. Therefore, the barrier in the forward-bias direction decreases by an amount of $V_g/2$. In the reserve-bias direction, the barrier increases by the same amount. The current density in these two directions then can be expressed as

$$J_F = qnv_c \exp[-\frac{q}{kT}(V_B - \frac{1}{2}V_g] \tag{1-5}$$

$$J_R = qnv_c \exp[-\frac{q}{kT}(V_B + \frac{1}{2}V_g)] \tag{1-6}$$

the net current density is then given by

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\sinh(\frac{qV_g}{2kT}) \tag{1-7}$$

at low applied voltages, the voltage drop across a grain boundary is small compared to the thermal voltage kT/q, Eq. (1.7) then can be simplified as

$$J = 2qnv_c \exp(-\frac{qV_B}{kT})\frac{qV_g}{2kT} = \frac{q^2nv_cV_g}{kT}[\exp(-\frac{qV_B}{kT})] \tag{1-8}$$

the average conductivity $\sigma = J / E = JL_g / V_g$ and the effective mobility $\mu_{eff} = \sigma / qn$ then can be obtained

$$\sigma = \frac{q^2nv_cL_g}{kT}\exp(-\frac{qV_B}{kT}) \tag{1-9}$$

$$\mu_{eff} = \frac{qv_cL_g}{kT}\exp(-\frac{qV_B}{kT}) \equiv \mu_0 \exp(-\frac{qV_B}{kT}) \tag{1-10}$$

where μ_0 represents the carrier mobility inside grain regions. It is found that the conduction in poly-Si is an activated process with activation energy of approximately qV_B, which depends on the dopant/carrier concentration and the grain boundary trap density.

Applying gradual channel approximation to poly-Si TFTs, which assumes that the variation of the electric field in the y-direction (along the channel) is much less than the corresponding variation in the y-direction (perpendicular to the channel), as shown Fig. 2-2. The carrier density *n* per unit area (cm^{-2}) induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_{TH} - V_{(y)})}{qt_{ch}} \tag{1.11}$$

$$I_D = \iint J.dx.dz = \iint nq\mu_{eff} \cdot \frac{dv_y}{dy}.dx.dz \tag{1.12}$$

$$= \int_0^W \mu_{eff} dz \int_0^{t_{ch}} nqdx. \frac{dV_y}{dy} = W\mu_{eff}.C_{ox}(V_g - V_{th} - V_y)\frac{dV_y}{dy}$$

where t_{ch} is the thickness of the inversion layer. Therefore, the drain current I_D of poly-Si TFT then can be given by

$$\int_0^L I_D dy = W\mu_{ff} C_{ox}\left[\left(V_g - V_{th}\right)V_D - \frac{1}{2}V_D{}^2\right]$$

$$I_D = \frac{W}{L}\mu_{ff} C_{ox}\left[\left(V_g - V_{th}\right)V_D - \frac{1}{2}V_D{}^2\right] \tag{1-13}$$

Obviously, this I-V characteristic is very similar to that in MOSFETs, except that the mobility is modified.

2-2. Methods of device parameter extraction

In order to clarify the possible mechanisms, the device electrical parameters are important. The methods of typical parameters extraction such as threshold voltage

(Vth), subthreshold slope (SS), drain current ON/OFF ratio**,** field-effect mobility (μ_{FE}) are defined as followed：

2-2-1. Determination of the threshold voltage

Many ways are used to determinate the Vth which is the most important parameter of semiconductor devices. In poly-Si TFTs, the method to determinate the threshold voltage is *constant drain current method.* The gate voltage at a specific drain current I_N value is taken as the threshold voltage. This technique is adopted in most studies of TFTs. Typically, the threshold current $I_N = I_D / (W_{eff} / L_{eff})$ is specified 100 nA for Vd in saturation region in this thesis.

2-2-2. Determination of the subthreshold slope

Subthreshold slope *SS* (V/dec.) is a typical parameter to describe the gate control toward channel. The SS should be independent of drain voltage and gate voltage. However, in reality, SS might increase with drain voltage due to short-channel effects such as charge sharing, avalanche multiplication, and punchthrough-like effect. The SS is also related to gate voltage due to undesirable factors such as serial resistance and interface state. In this experiment, the SS is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude (from 10^{-8}A to 10^{-9}A).

2-2-3. Determination of On/Off Current Ratio

Drain On/Off current ratio is another important factor of TFTs. High On/Off ratio represents not only large turn-on current but also small off current (leakage current). It affects gray levels (the bright to dark state number) of TFT AMLCD directly.

There are many methods to specify the on and off current. The practical one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage is in saturation region.

2-2-4. Determination of the field-effect mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain voltage (Vd = 0.1V). The transfer I-V characteristics of poly-Si TFT can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{TH})V_D - \frac{1}{2}V_D{}^2] \tag{3-1}$$

where

C_{ox} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{TH} is the threshold voltage.

If V_D is much smaller than V_G-V_{TH} (i.e. $V_D << V_G - V_{TH}$) and $V_G > V_{TH}$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \tag{3-2}$$

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \qquad (3\text{-}3)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox}WV_D}g_m \qquad (3\text{-}4)$$

2-3. Stress mechanism

2-3-1 Static Hot-Carrier Stress

It is reported that the ON-state stressing is the limiting instability condition in poly-TFTs[2-1] which is in contrast to hydrogenated amorphous silicon (a-Si:H) TFT's, where the degrading rate depends only on the gate bias and is independent of drain bias[2-2]. During the operation of poly-TFTs with grain boundary defects and intra-grain defects in Poly-Si film and a large number of interface states at the SiO_2/poly-Si interface, most of the applied voltage drops across the grain boundaries since they have much larger resistances than the grains. The lateral electric field in the grain boundaries will be much higher than in the grains, and at large drain voltages, impact ionization may occur. Then the generated hot-carriers will be injecting into the gate oxide and/or breaking the Si-H bonds and strained Si-O bonds[2-3]. Moreover, the poly-TFTs' non-ideal effect, Kink effect, which is due to the holes injected and stored in a floating body to cause the reduction of the threshold voltage and a parasitic bipolar element is resulting in positive-feedback effect to enhance the generation of the hot-carriers shown in fig.2-3[2-4]. This kink effect associated with float-body is especially dramatic for n-channel devices, because of the higher impact-ionization rate of electrons.

Unlike to the fundamental MOSFETs theory, the poly-Si TFT electrical parameters such as threshold voltage (Vth), maximum transconductance (Gm,max), On current (Ion), and subthreshold slope (SS) could depend on grain, grain boundaries, and/or interface properties. The deep traps existing in grain boundaries have been demonstrated to affect mainly threshold voltage and much less Gm,max. On the other hand, tail states from grain regions in the interface and/or from grain boundaries mainly contribute to the decrease of (Gm)max [2-5][2-6]. The subthreshold slope depends mainly on intra-grain traps distributed uniformly inside the poly-Si film and also on the deep interface states [2-7]. Therefore, it is obvious that depending on the nature of state generation after stress, electrical parameters can provide useful information in order to clarify poly-Si TFTs degradation under hot carrier stress conditions. These points are summarized on the Table I.

Self-heating effect is also another mechanism especially occurred in the wide-channel poly-Si TFTs that is because the temperature of poly-Si TFTs can reaches over 350^0C during the operation in the high stress power(stress power = Vds × Id) condition to dissolute the weak Si-H bonds [2-8].

2-3-2 Dynamic Hot-carrier Stress

Dynamic stress is closer to real operation condition than the static stress. It is reported that the reliability evaluation method proposed under the static stress conditions may not be suitable for the reliability evaluation under the dynamic stress [2-9]. The dynamic stress degrades the poly-Si TFT more seriously than the static stress. The impact ionization generation hot electrons and hot holes near drain at ON state. However, as the device is changed from ON state to OFF state, the drain avalanche hot carrier (DAHC) will occur to cause serious degradation and generate more hot electrons and hot holes near drain [2-10].At the switching period, a transient current (I = C dV/dt) can be observed to damage the device [2-11]. According the pervious reports, the dynamic stress degradation mainly depend on the stress frequency (f), stress temperature, and falling time (Tf)[2-12].

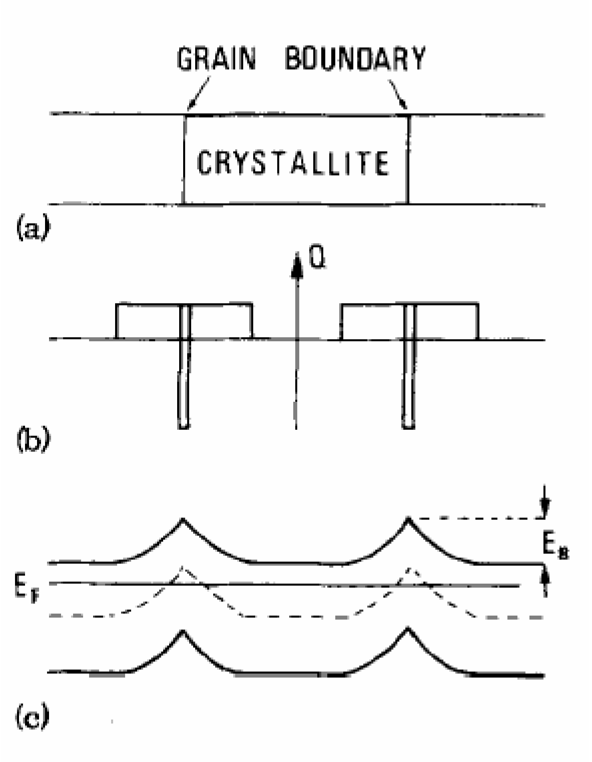

Fig. 2-1. Sketch of the band diagram of the polycrystalline silicon films

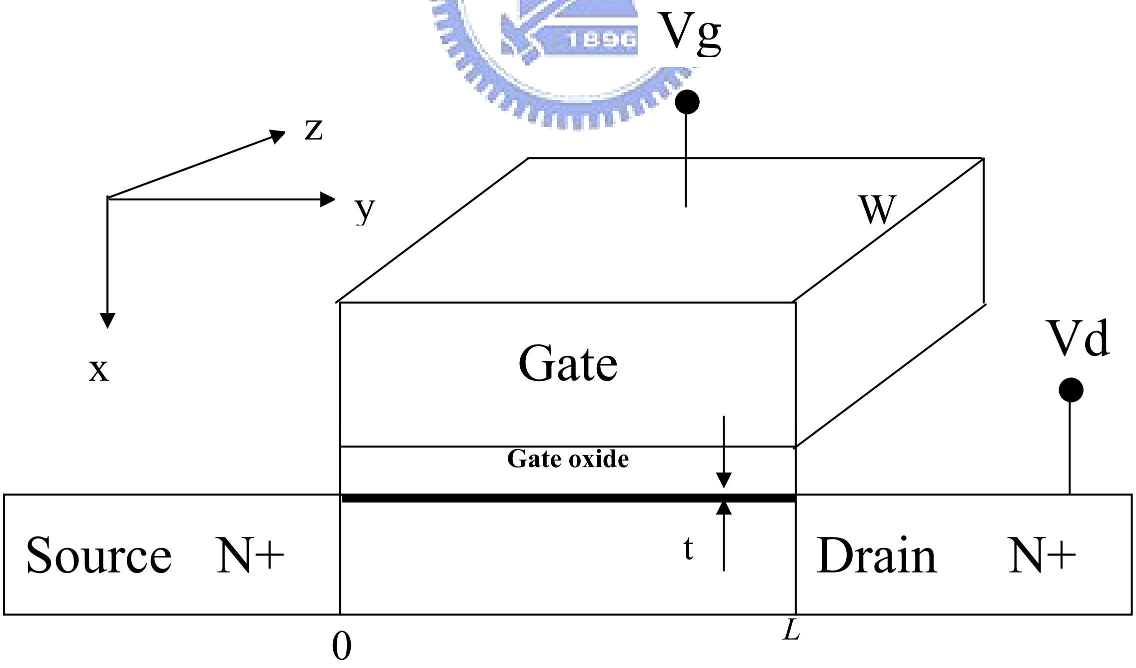

Fig. 2-2. A schematic MOSFET cross section, showing the axes of coordinates and the bias voltages at the four terminals for the drain-current model.

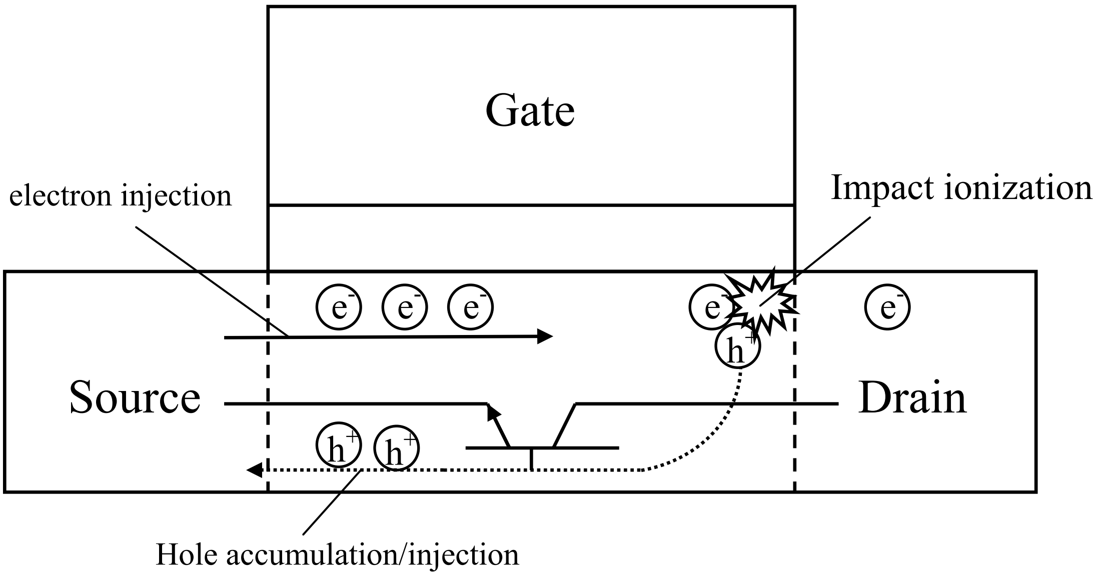

Fig. 2-3. Kink effect is due to the holes injected and stored in a floating body to cause the reduction of the threshold voltage and a parasitic bipolar element is resulting in positive-feedback effect to enhance the generation of the hot-carriers

Table 1 Variation of experimental electronic parameters and corresponding possible degradation mechanics.

Electrical parameters after stressing	**Mainly depending on**
$\Delta G_{m,max}$	➢ Interface state generation ➢ State generation in the grain boundaries (tail state)
ΔVth	➢ Charge injected into the gate oxide ➢ Interface state generation (deep states) ➢ State generation in the grain boundaries(deep states)
ΔS (subthreshold swing)	➢ Intra-grain defect density generation (bulk state) ➢ Interface state generation (deep states)

Chapter 3

Device structure and Fabrication

In this thesis, the novel process TFT with self-aligned fluorinated silica glass (FSG) spacers mentioned and their fabrications are described in part I. The new structure TFT with multiple nanowire channels mentioned and their fabrications are described in part II.

Part I. Poly-Si TFT with Self-aligned Fluorinated Silica Glass (FSG) Spacers

3-1. Fluorinated Silica Glass (FSG) Spacers Device Structure

We fabricate the conventional top-gate Light Doped Drain (LDD) polysilicon TFT structure incorporated with fluorinated silica glass (FSG) spacer and conventional TEOS silicon dioxide spacer. The schematic cross section view of devices is shown in Fig. 3-1. The devices used here have a gate width W=10 um and length L=3 um. In these devices, high reliability on FSG spacers of TFT can be observed.

3-2. FSG Spacers Device Fabrication Process

Step1. Substrate.

6-inch p-type single crystal silicon wafers with (100) orientation were used as the starting materials. After an RCA initial cleaning procedure. Si wafers were coated with 550-nm-thick thermally grown SiO_2 in steam oxygen ambient at 980°C.

Step2. Active region formation.

Uundoped 50nm-thick amorphous-Si layer were deposited by low-pressure chemical vapor deposition (LPCVD) on buried oxide by pyrolysis of silane (SiH_4) at 550°C. The amorphous-Si films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24 hrs in N_2. The active islands (mask1), including source, drain and channel with different dimension, were patterned and transferred by reactive ion etching (RIE) (transformer couple plasma) using the mixture of Cl_2 and HBr.

Step3. Gate oxide formation.

After defining the active region, the wafers were boiled in H_2SO_4 + H_2O_2 to ensure cleanliness of the wafers before deposition. A buffered HF dip was performed to remove the native oxide on the silicon surface. Soon, the gate insulator was deposited in a horizontal furnace using TEOS and O_2 gases at 700°C. The thickness of the TEOS oxide thin film is 50nm.

Step4. Gate electrode formation.

After deposition of gate oxide, 200nm-thick undoped poly-Si films were deposited immediately on the gate oxide by LPCVD at 620°C. The poly-Si layers were patterned and transferred by RIE (transformer couple plasma) to define the gate electrode and to be the mask for self-aligned implantation.

Step5. Self-aligned LDD N^- implantation and annealing .

After gate electrode formation, phosphorus ions at a dose of 5×10^{13} cm^{-2} and an energy of 17keV were implanted to form the light doped source/drain regions. Then all wafers were subjected to a rapid thermal anneal (RTA) at 820°C for

20seconds for dopants activation.

Step6. fluorine doped TEOS oxide spacer formation.

After n- implantation and dilute HF dip to remove the native oxide, the wafer was loaded into a plasma enhanced chemical vapor deposition (PECVD) system using the mixture gases of CF_4 and TEOS at 300 °C to grow a 300nm-thick fluorine doped TEOS oxide (FSG) on the exposed gate and source/drain regions. For comparison, wafer with conventional TFTs were also processed on the same run by deliberately depositing only the TEOS oxide without fluorine dopants. Then the FSG layers and the conventional TEOS oxide were anisotropically etched by RIE (metal ether) to form the sidewall spacer abutting the poly-Si gate without additional mask.

Step7. Self-aligned Source/drain N+ implantation and annealing .

Phosphorus ions at a dose of 5×10^{15} cm^{-2} and an energy of 17keV were implanted to form the n^+ gate, source/drain regions and were activated by rapid thermal anneal (RTA) at 820°C for 20seconds also.

Step8. Metallization .

The 500nm-thick TEOS oxide were deposited as passivation layer and patterned into the source/drain/gate contact holes. The 500nm-thick aluminum (Al) layer was deposited by physical vapor deposition (PVD) and patterned for source, drain and gate metal pads. Finally, the finished devices were sintered at 400°C for 30 minutes in an N_2 ambient.

Part II. Novel Multiple Nanowire Channels Poly-Si Thin-Film Transistors

3-3. Multiple Nanowire Channels Device Structure

The TFTs, with a gate length of 0.5 um, consisting of ten strips of multiple 67 nm wire channels (M10) TFT, and a single-channel structure (S1) with W = 1 um TFT, were fabricated. Figure 2a presents the structure of the M10 TFT. Figure 2b presents the cross-section of the M10 TFT perpendicular to the AA’ direction. This M10 TFT has a conventional top-gate LDD MOSFET structure. Figure 2c presents cross-section of the M10 TFT perpendicular to the BB’ direction, in which the channels were surrounded by the gate electrode as tri-gate structure. Figure 3 presents device electrical characteristics simulation results using the DESSIS software package from ISE. The double-gate TFT simulation results serve to tri-gate TFT due to the similar dimension. Figure 3a shows the encroachment of electrical field from drain side of S1 TFT. However, in Fig. 3b, M10 TFT can confine the electrical field due to its superior tri-gate control. Therefore, it is expected that the M10 TFT tri-gate structure can suppress effectively short channel effects. Figure 4a and 4b present the scanning electron microscope (SEM) photograph of the poly-Si active region of the M10 TFT, and the 67-nm-wide multiple nano-wire channels in the M10 TFT, respectively. Figure 4c presents a plane view of transmission electron micrograph (TEM) photograph of the active region of the proposed TFTs. The average grain size in the polysilicon channel formed by solid phase crystallization is approximately 30 nm.

3- 4. Multiple Channels Device Fabrication Process

Step1. Substrate.

6-inch p-type single-crystal silicon wafers with (100) orientation were used as the starting substrate. After a standard cleaning procedure, silicon wafers were coated with 400-nm-thick thermally grown SiO_2 in steam oxygen ambient at 1000°C

Step2. Poly-Si thin film formation .

Undoped 50-nm-thick amorphous-Si layers were deposited by low pressure chemical vapor deposition (LPCVD) at 550°C. The amorphous-Si films were recrystallized by solid phase crystallization (SPC) method at 600°C for 24hrs in N_2 ambient. After Ebeam direct writing and transformer couple plasma (TCP) etching, the device active region source, drain and multiple channels were formed.

Step3. Gate oxide formation.

After defining the active region, the wafers were cleaned in H_2SO_4/H_2O_2 and NH_4OH/H_2O_2 solution to remove residue of polymer before gate oxide deposition. A buffered HF dip was performed to remove the native oxide on the silicon surface. Then, a 26-nm-thick layer of tetra-ethyl-ortho-silicate (TEOS) gate oxide was deposited by LPCVD at 700^0C. The thickness of gate oxide was determined by N&K optical analyzer.

Step4. Gate electrode formation.

After deposition of gate insulators, 150-nm-thick poly-silicon films were formed immediately on the gate insulators by LPCVD at 620°C. The second poly-Si layers were patterned by EBeam lithography and transformer couple plasma (TCP) etching to define the gate electrode and to be the mask for self-aligned implantation.

Step5. LDD and source/drain formation.

After the gate definition, the implantation for lightly-doping source and drain was performed by phosphorous ions at a dosage of 5×10^{13} cm^{-2}. A 200nm-thick TEOS was then deposited by LPCVD, and anisotropically etched by reactive ion etching (RIE) to form a sidewall spacer abutting the poly-Si gate. Next, the self-aligned source and drain regions were formed by phosphorous ions implantation at a dosage of 5×10^{15} cm^{-2}. After the source and drain formation, doping activation was performed by rapid thermal anneal (RTA).

Step6. Passivation layer and contact hole formation.

After doping activation, a 300-nm-thick TEOS oxide layer was deposited by LPCVD as the passivation layer. The 5×5 um^2 contact holes were patterned by reactive ion etching (RIE) subsequently.

Step7. Metallization.

The 300-nm-thick aluminum layers were deposited by physical vapor deposition (PVD) and then patterned to form the gate, source and drain contact metal pads.

Finally, the devices were sintered at 400°C in hydrogen ambient for 30 min.

Step8. Passivation.

It is well known that grain boundary passivation is very effective in improving the performance of poly-Si TFTs. Therefore, to reduce trap density and improve interface quality, wafers were immured in an NH_3 plasma generated by plasma enhanced CVD (PECVD) for 1 hr.

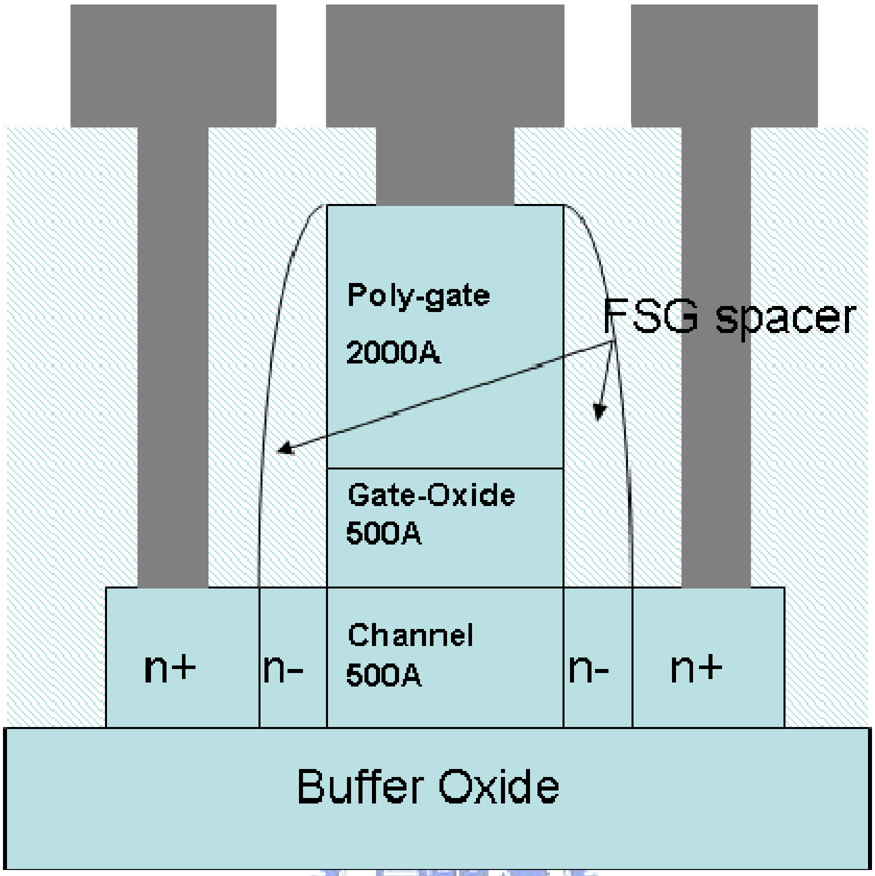

Fig. 3-1. The cross section view of the Fluorinated Silica Glass (FSG) Spacers Device Structure

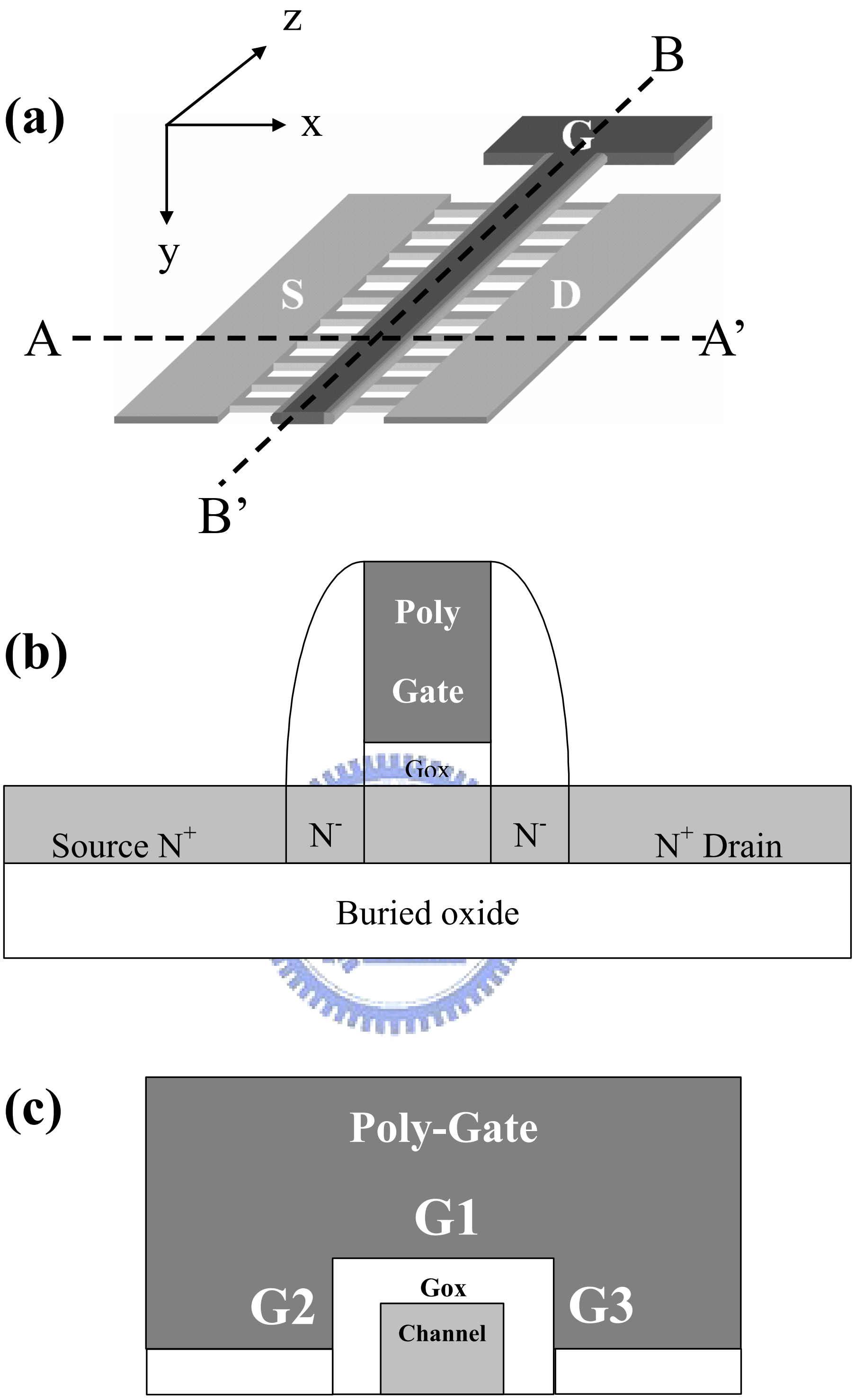

Fig. 3-2. (a) Schematic diagram of M10 poly-Si TFT. (b) Cross-section view of Fig. 1a AA' direction, as a conventional top-gate LDD MOSFET structure. (c) One of channel cross-section view of Fig. 1a BB' direction, as a tri-gate structure. Active layer, gate oxide, and poly-gate thickness are 50 nm, 26 nm and 150 nm, respectively.

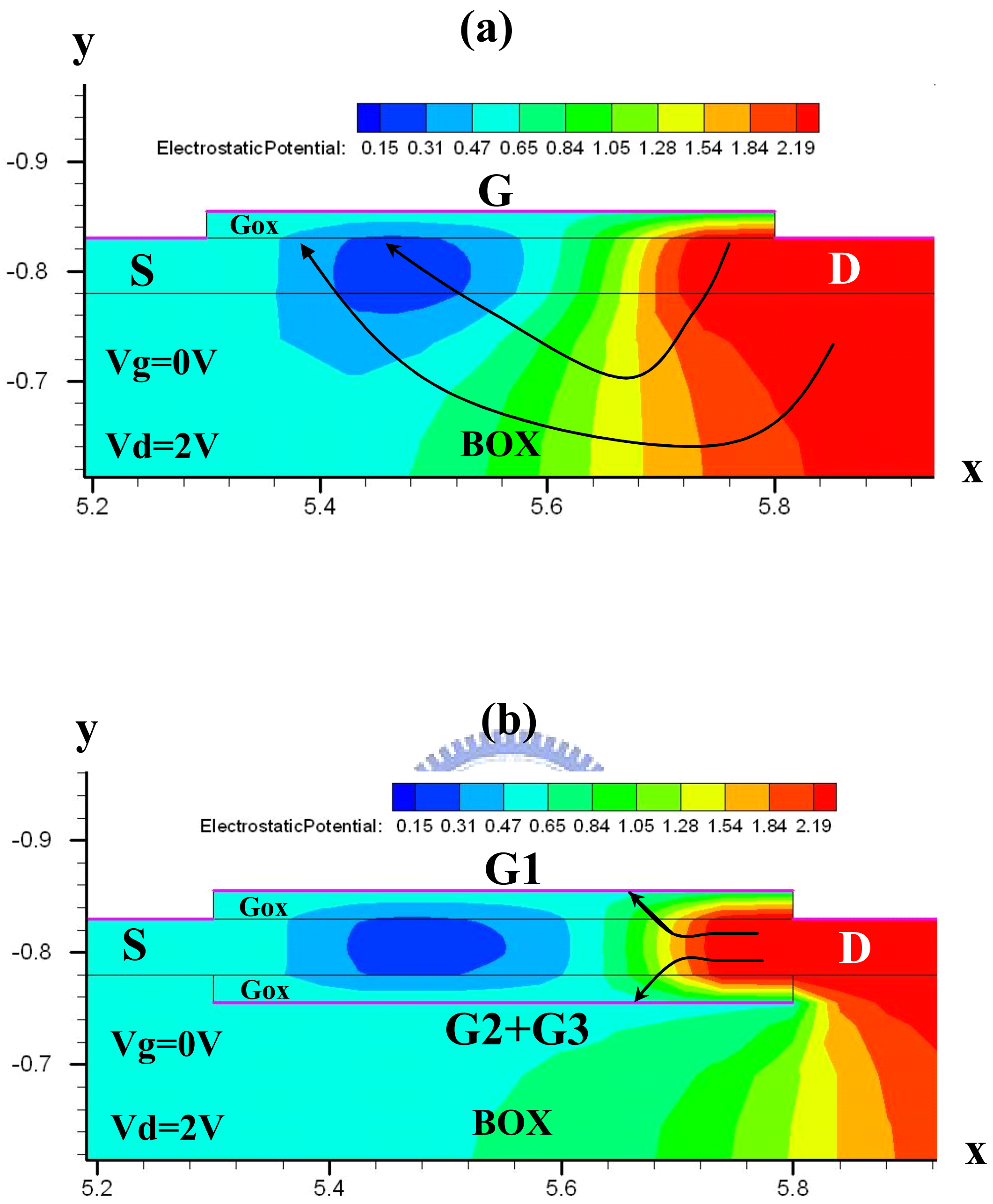

Fig. 3-3. Simulation results of potential contour plots and electrical field lines of (a) single-top-gate TFT (b) tri-gate TFT with L = 0.5 um, gate oxide = 26 nm, channel thickness = 50 nm at Vg = 0 V, Vd = 2 V.

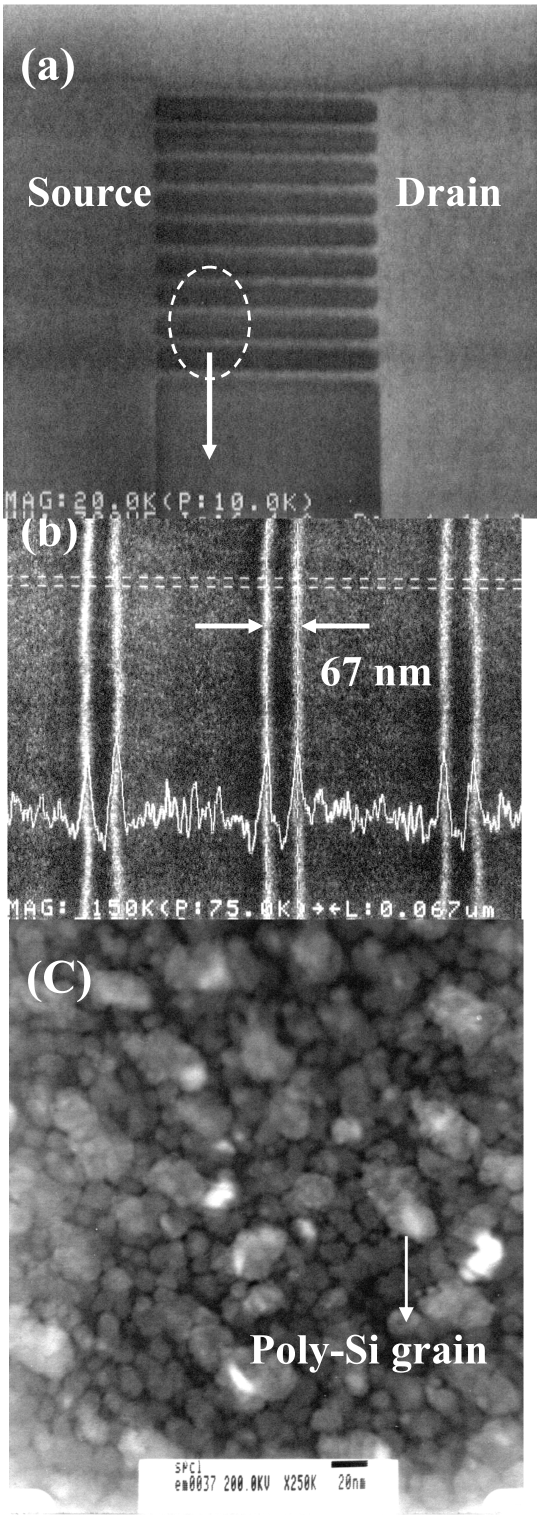

Fig. 3-4. (a) Scanning electron microscopy (SEM) photography of active pattern with the source, the drain and multiple nano-wire channels of M10 TFT. (b) Magnified area of multiple nano-wire channels. The each nano-wire width is 67 nm. (c) Transmission electron microscopy (TEM) photography of poly-Si grains by solid phase crystallization. The average poly-Si grain size is about 30 nm.

Chapter 4

Experiment results and discussion

In this chapter, the Poly-Si TFT with Self-aligned Fluorinated Silica Glass (FSG) Spacers is discussed in part I and the novel multiple nanowire Channels Poly-Si Thin-Film Transistors part is discussed in II.

Part I. Poly-Si TFT with Self-aligned Fluorinated Silica Glass (FSG) Spacers

4-1. Performance of Fluorinated and TEOS Spacers Poly-Si TFTs

Figure 1 shows the Fourier transform infrared (FTIR) spectra of undoped SiO_2 and FSG films between 400 cm^{-1} and 2000 cm^{-1}. The FTIR spectra were measured from an unpatterned wafer with undoped SiO_2 and FSG layer respectively. The main peak of function group Si-F is around 930 cm^{-1}. The signal of Si-F bonds is clearly observed in the FSG film.

Figures 4.2 (a) and 4.2 (b) show the comparison of transfers and output curves for poly-Si TFTs with TEOS and SiOF spacer. It is found the Id-Vg characteristics for Vd= 0.1 V of W/L=10um/5um in both types of poly-Si TFTs were nearly the same. This indicates the introduction of FSG spacer in poly-Si TFT device does not degrade electrical performance.

In Id-Vd characteristics for Vg-Vth = 0,1,2,3,4 V, it is found that the kink effect occurs in both poly-Si TFTs. However, the drain current in the saturation region of TEOS spacer TFT is increasing more seriously than SiOF spacer TFT, especially at high gate voltages. The kink effect in poly-Si TFTs is attributed to channel avalanche multiplication occurred in the high fields near drain side, associated with the floating body effect. The suppression of kink effect for the poly-Si TFT with FSG spacers is more significant than the TEOS spacer poly-Si TFT. The fluorine ions in the sideward spacer near drain side strongly passivate the Si dangling bonds to avoid the occurrence of hot carriers.

4-2. Reliability after DC stress of Fluorinated and TEOS Spacers Poly-Si TFTs

In this work, the static stress is used to degrade the poly-Si TFT. The stressing bias of the gate potential Vgs and the drain potential Vds are fixed at 15V, and 30V, respectively. Figures 4.3(a) and 4.3(b) show the different degradation behaviors of drain current and trans-conductance between TEOS and FSG spacer under static stress, respectively. For TEOS spacer, the curve of the trans-conductance decreases monotonically and shows a parallel shift in the positive direction with the increase of the stress time. For FSG spacer, Gm,max is initially increased and then it starts to decrease after 1000 seconds stressing, while remains unchanged for Vgs > 17V.

Figure 4.4 shows the degradation of the maximum trans-conductance defined as

ΔGm,max/Gm,max$_0$, where ΔGm,max= Gm,max- Gm,max$_0$, Gm,max$_0$ is the initial transconductance and Gm,max is the transconductance after stress. Figure 4.5 shows the degradation of drain current at Vds=5V. The more serious degradation of TEOS spacer TFT in both Gm and Ion is found. This is due to the reducing of potential barrier in the channel by passivating the dangling bonds and traps in grain boundaries by fluorine ions.

Figure 4.6 shows the threshold voltage variations (ΔVth) after stressing. In contrast with the large Vth shift for the TEOS spacer TFT, Vth shift for the SiOF spacer TFT was smaller. Vth is strongly dependent on the deep trap states which originate from the dangling bonds in the grain boundaries of the sideward channel [4-1]. The degradation of TEOS spacer TFT is due to deep states generated in the grain boundaries and at the gate oxide/channel interface with stress duration by breaking the weak and/or strained Si-H, Si-O bonds and even the strong Si-Si bonds[]. However, for SiOF spacer TFT, the superior reliability is due to the passivation of dangling bonds by fluorine ions near drain side. Since the dissociation energy of Si-F bonds is about twice of the Si-H bonds, Si-F is hardly broken by the stressing and thus generation of positive fixed charges in the gate oxide is suppressed[]. Moreover, the suppression of kink effect for the poly-Si TFT with FSG spacers also reduces the degree of degradation under the same stress condition.

Figure 4.7 shows the comparison of the sub-threshold slope variation ΔSS characteristics of TEOS spacer TFT and SiOF spacer TFT for Vd= 0.1 V where ΔSS=SS - S_0, S_0 is the initial sub-threshold slope and S is the sub-threshold slope for each stress time. Initially, the ΔSS of SiOF spacer TFT is smaller than in the TEOS spacer TFT, but ΔSS is then rapidly degraded to approach the curve of TEOS spacer TFT after 6000 second. The sub-threshold swing varies with stress is also associated with the interface deep state generation, so less degradation in SiOF spacer TFT is due to the SiOF spacer TFT with better interface property at spacer regions near drain can reduce the variation of SS. But when the Si-F bonds formed only under sidewall spacers were broken in long term stress, SiOF spacer TFT loses the advantage of stronger passivation.

Part II. Novel Multiple Nanowire Channels Poly-Si TFTs

4-3. Performance of Novel Multiple Nanowire Channels Poly-Si TFTs

Figure 4.8 plots a typical normalized transfer curve and the field effect mobility of TFT devices with a single-channel and multiple nanowire channels, respectively. The transfer characteristics imply that the ON-state current of multiple nanowire channel TFTs is approximately similar to that of single-channel TFTs. This fact suggests that the single-channel and multiple nanowire channel TFTs can yield almost the same carrier mobility, indicating that the carrier mobility is not degraded in multiple nano-wire channel TFTs. Additionally, the leakage current of multiple nano-wire channels TFTs is reduced significantly as gate voltage (V_g) becomes more negative at V_d = 2 V, compared to the single-channel TFTs. The multiple nano-wire channels TFTs therefore has a higher current ON/OFF ratio ($>10^8$) than single-channel TFTs. Also, multiple nano-wire channel TFTs has a smaller subthreshold slope (SS), and is free of drain induced barrier lowering (DIBL), because they exhibit better gate control ability. The electrical characteristics of multiple nano-wire channel TFTs are also better because the width of each nano-wire channel is close to the size of a polysilicon grain, approximately 30 nm, as presented in Fig. 1c. Therefore, multiple nano-wire channels has fewer effective grain boundary defects than single-channel

TFTs. Moreover, the effect of NH_3-plasma passivation more efficiently affects multiple nano-wire channel TFTs than it does in single-channel TFTs, because the former has split nano-wire structures that are mostly exposed to NH_3 plasma. Figure 3 depicts the output characteristics of single-channel TFTs with channel length (L) of 0.5 μm and width (W) of 1 um, as well as those of multiple nano-wire channel TFTs with channel length (L) of 0.5 μm and width (W) of 67nm×10 = 0.67 μm. The applied gate voltage was maintained at a constant value of V_g - V_{th} = 0.5, 1.0 and 1.5 V, to avoid that threshold voltages were different. The suppressed kink-effect was observed for multiple nano-wire channel TFTs, because they had fewer polysilicon grain boundary defects and exhibited more efficient NH_3 plasma passivation.

Table II lists the electrical parameters of the TFTs, including threshold voltage (V_{th}), subthreshold slope (*SS*), ON/OFF ratio and DIBL. V_{th} is defined as the gate voltage required to achieve a normalized drain current of $I_d = (W/L) \times 10^{-7}$ A at V_d = 2 V. DIBL is defined as $\Delta V_g / \Delta V_d$ at $I_d = 10^{-10}$ A. The effective trap state density (Nt) were extracted from the slope of $ln\ (I_d / V_g)$ versus $(1 / V_g)$ characteristics[9] for devices with multiple and single-channel TFTs , to elucidate the effect of grain boundary defects on the performance of such TFT devices.

In Fig. 4.10, multiple nano-wire channel TFTs exhibited a lower slope, indicating a lower effective trap state density (Nt ~ 1.81×10^{11}) than single-channel TFTs (Nt ~

2.12×10^{11}). This result is also consistent with the aforementioned comparison of the performance of multiple nano-wire channels with that of single-channel TFTs.

4-4. Reliability after DC and AC stress of Novel Multiple Nanowire Channels Poly-Si TFTs

The static hot carrier stress condition is determined at kink-effect occurrence, Vd = 6 V and Vg = 3V, and the source potential is common. The dynamic pulse train stress is defined at constant Vd = 6 V and dynamic Vg = 3V (high), 0V (low) with the duty cycle of 50%, and the source potential is common. The waveform of the pulse train is shown in Fig.4.11. In this section, we discuss the deceive reliability after a series of stress frequency (f), rising time (tr), falling time (tf) and substrate temperature conditions.

Fig. 4-12 (a) depicts typical M10 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second. Fig.4.12 (b) depicts typical S1 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second.

Figure 4-13 depicts trans-conductance degradation of S1 and M10 TFT as a function of the stress time with different frequencies (DC, f = 1K Hz, and f = 1M Hz). The S1 and M10 TFT show the similar Gm degradation. These results reveal that the S1 and M10 have similar tail state generation.

Figure 4-14 and 4-15 depict the threshold voltage and subthreshold swing variation of S1 and M10 TFT as a function of the stress time with different frequencies, respectively. For M10 TFT the Vth and SS variation is much lower than the S1 TFT. The results indicate that the M10 TFT has less deep states. Firstly, the M10 TFT has more effective NH_3 plasma passivation than that of S1 TFT due to the ten split nanowire channels of M10 TFT has wide NH_3 plasma passivation area. Secondly, M10 TFT has robust tri-gate control, thus the additional two side-gate surface scattering (Fig. 3b) reduce the hot carrier effect. Therefore, the deep states generation of M10 TFT by the hot carrier impaction is lower than which of S1 TFT. Notably, for S1 TFT, the Vth and SS variation increase with the frequency increasing from 1 K Hz to 1 MHz. These results reveal that the device reliability is strongly dependent on the transient current Id (displace current).

$$I_d = C_{ox} \cdot \frac{dV_g}{dt} \approx C_{ox} \cdot f \cdot \overline{V_g}$$

where f is frequency, $\overline{V_g}$ is average gate voltage.

Thus, the transient current induced hot carrier is dependent on the frequency.

Figure 4-16 and 4-17 depict the ON current (I_{ON}) variation and ON/OFF ratio of S1 and M10 TFT as a function of the stress time with different frequencies, respectively. The M10 TFT shows lower I_{ON} variation than S1 TFT. These results reveal that the S1 TFT has high Vth variation and increase with the frequency increasing. Thus, the I_{ON} of S1 TFT is much lowering than that of M10 TFT. For the ON/OFF ratio, although the S1 and M10 TFT have the similar degradation behavior, the ON/OFF ratio of M10 still remains exceed 10^8, under different frequencies.

Figure 4-18 depicts Gm degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz. For S1 TFT (dash-line) with the same falling time of 100 ns, the S1 TFT has the similar Gm degradation. However, for the same rising time of 100 ns, as the falling time increasing from 100 ns to 1 us, the Gm degradation is reduced from 40% to 20% at the stress time at 1000 second. These results reveal that the device reliability is strongly dependent on the transient current. According to the Uraoka et al. report [4-2], only the transient current induced by the falling period would cause more damage near the drain. Figure indicates clearly that the amount of the hot carriers generated depends on the pulse falling time. Therefore, using the dynamic stress with longer falling time will be helpful for the reliability improvement in the poly-Si TFTs. On the other hand, for M10 TFT, however the Gm degradation dependent on falling time is not significant. These results indicate that M10 TFT has highly effective NH_3 plasma passivation and robust tri-gate control to screen the transient current hot carrier effect, which induced by the falling period.

Figure 4-20 and 4-21 depicts Vth variation and ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz. For the same reason, the Vth variation and ON current (Ion) degradation of S1 TFT (dash-line) is highly dependent on the falling time rather than rising time. As the falling time increasing from 100 ns to 1 us, the Vth variation and ON current (Ion) degradation are reduced. Again, M10 TFT has highly effective NH_3 plasma passivation and robust tri-gate control to screen the transient current hot carrier effect, which induced by the falling period.

Figure 4-22 depicts Gm degradation of S1 and M10 TFT as a function of the stress time with different subtract temperature with 25^0C, and 75^0C under the same frequency of 1 KHz, and the same Tr = Tf =100 ns. For both S1 and M10 TFT, the Gm degradation is reduced with the temperature increasing from 25^0C to 75^0C. These results reveal that hot carrier effect is reduced with the temperature increasing. As the temperature increasing, the mean free path (λ) [4-3] is decreasing.

$$\lambda = \lambda_0 \cdot \tanh(\frac{E_P}{2kT})$$

Thus, that hot carrier energy is reduced as the mean free path (λ) is decreasing.

Figure 4-23 and 4-24 depicts Vth variation and ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with 25^0C, and 75^0C under the same frequency of 1 KHz, and the same Tr = Tf =100 ns. For both S1 and M10 TFT, the Vth variation and ON current (Ion) degradation is reduced with the temperature increasing from 25^0C to 75^0C. For the same reason, hot carrier effect is reduced with the temperature increasing as the mean free path (λ) decreasing.

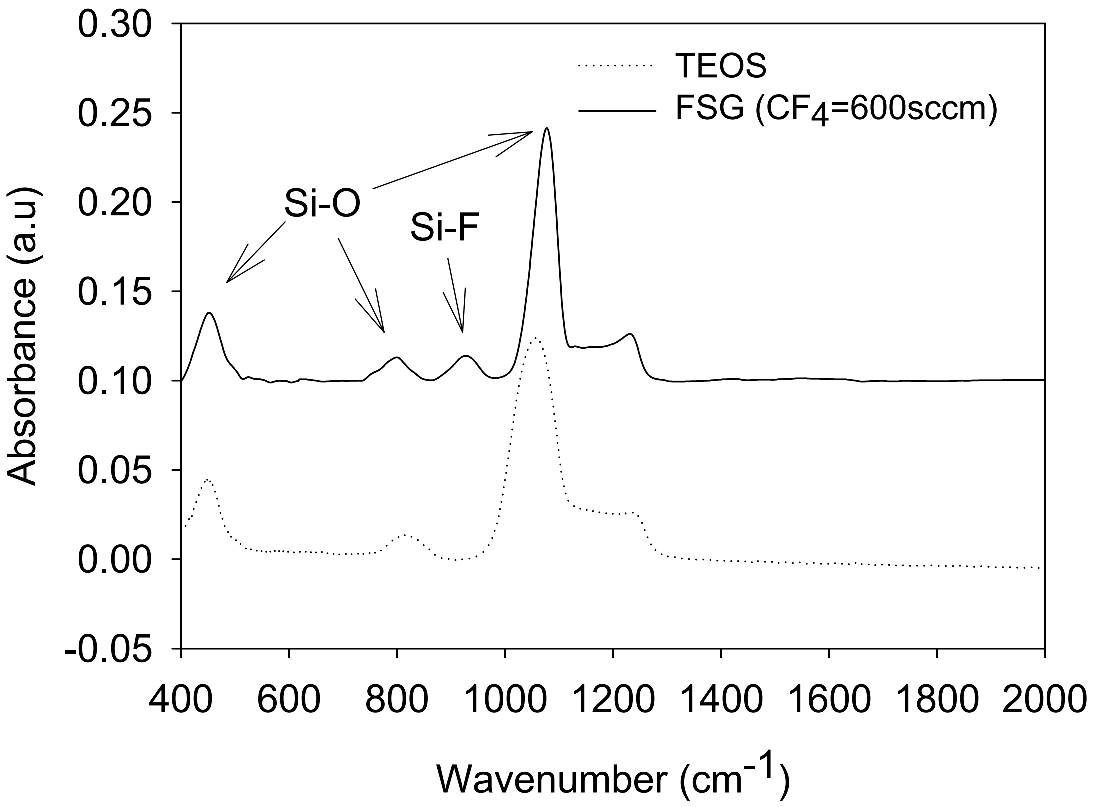

Figure4.1 FTIR Spectra of FSG film and TEOS film between 2000cm-1 and 400 cm-1

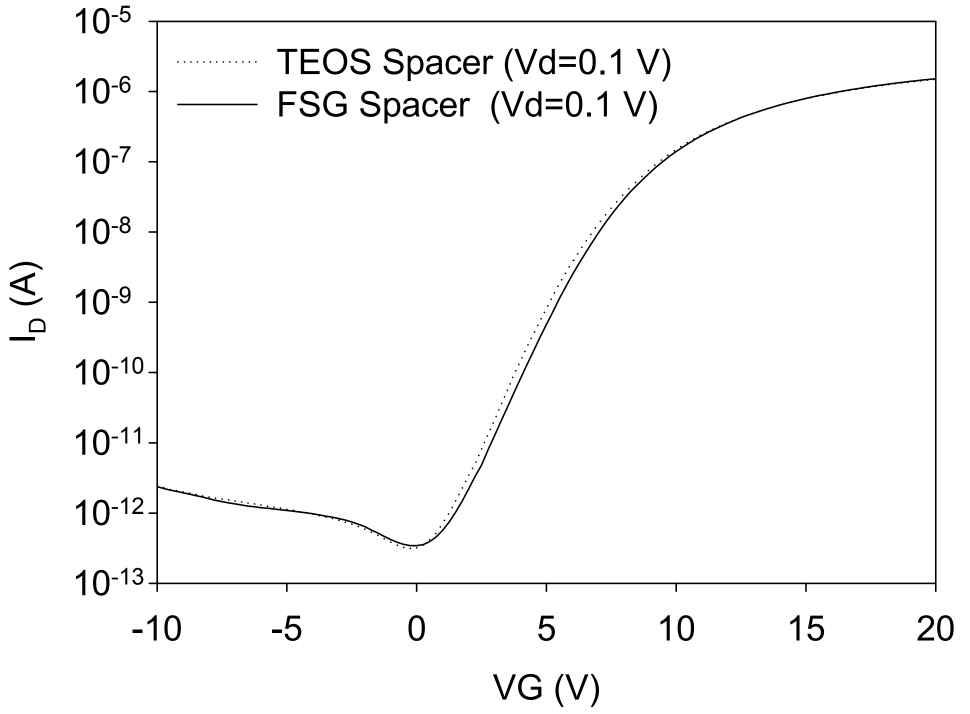

Figure4.2 (a) Comparsion of Id-Vg characteristics of FSG spacer TFT and TEOS spacer TFT for Vd=0.1 V (W/L=10um/5um)

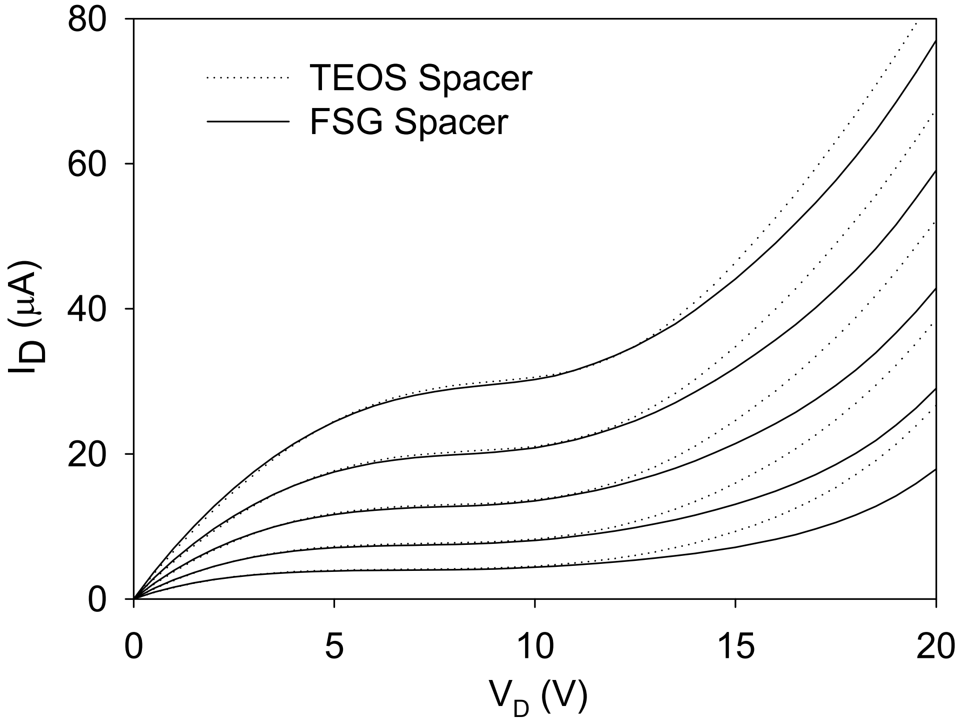

Figure 4.2 (b) Comparsion of output characteristics for FSG spacer and TEOS spacer TFT, W/L=10um/5um, VG-Vth= 0,1,2,3,4 V

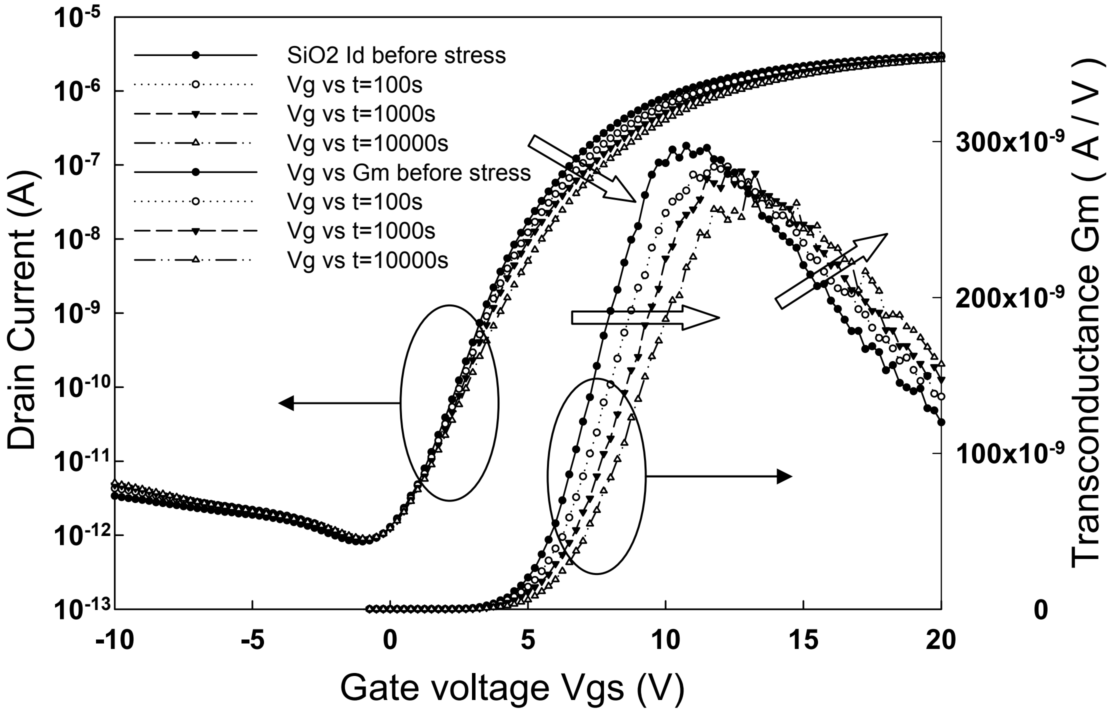

Fig4.3 (a) The degradation of drain current and trans-conductance by static stress in TEOS spacer structure

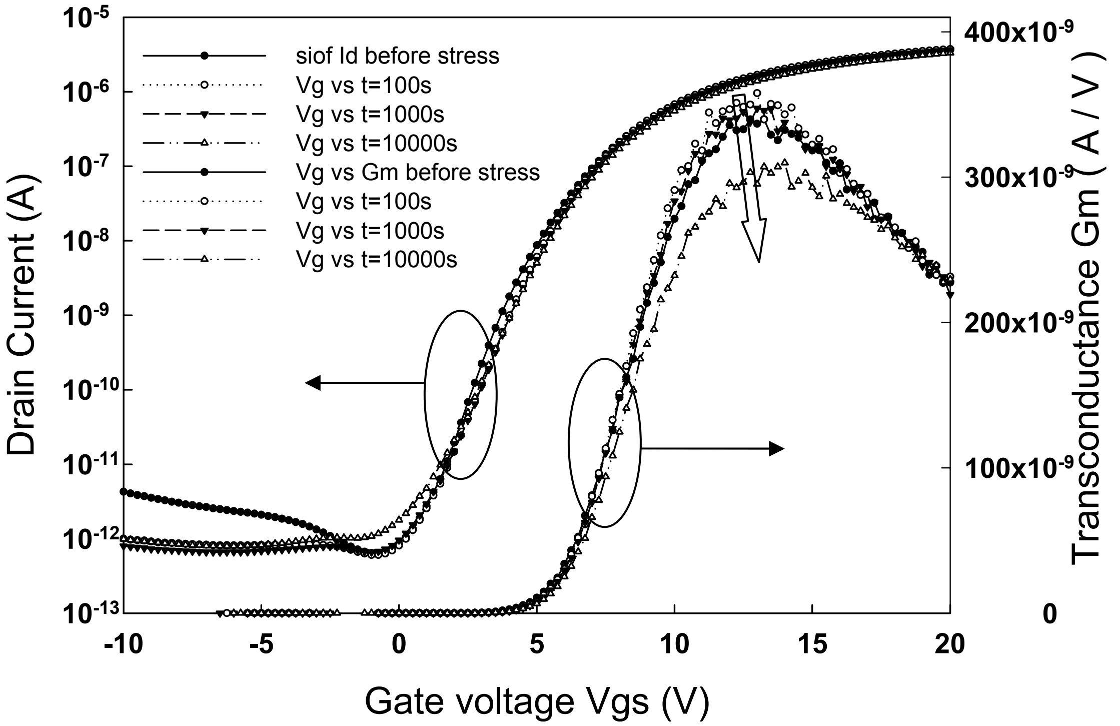

Figure 4.3 (b) The degradation of drain current and trans-conductance by static stress in SiOF spacer structure.

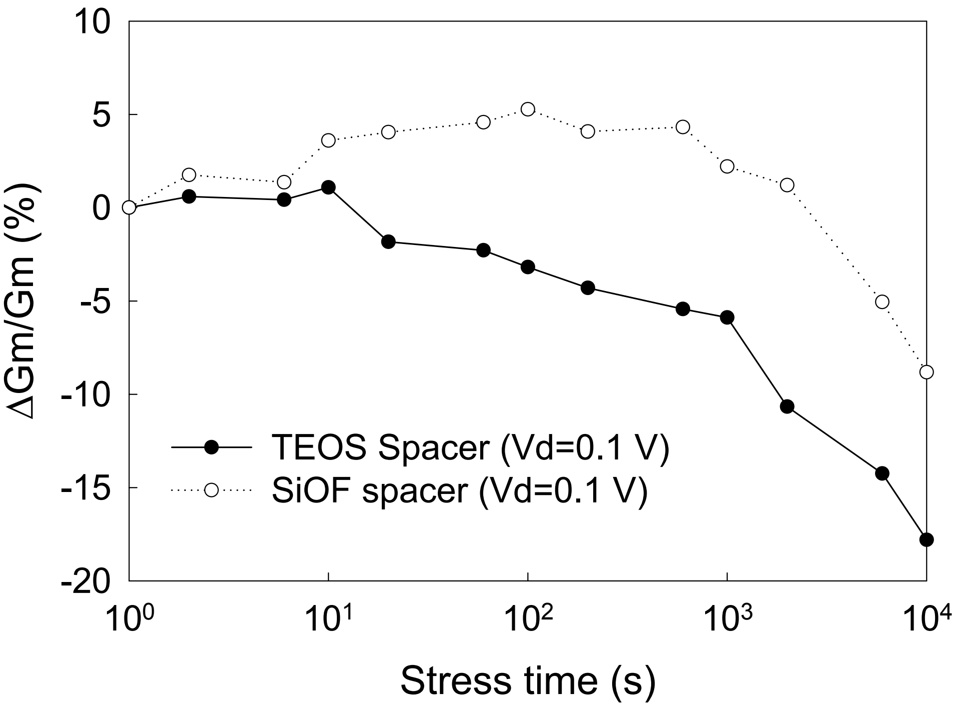

Figure 4.4 Comparsion of ΔGm/Gm characteristics of SiOF spacer TFT and TEOS spacer TFT for Vd=0.1V (W/L=10um/3um)

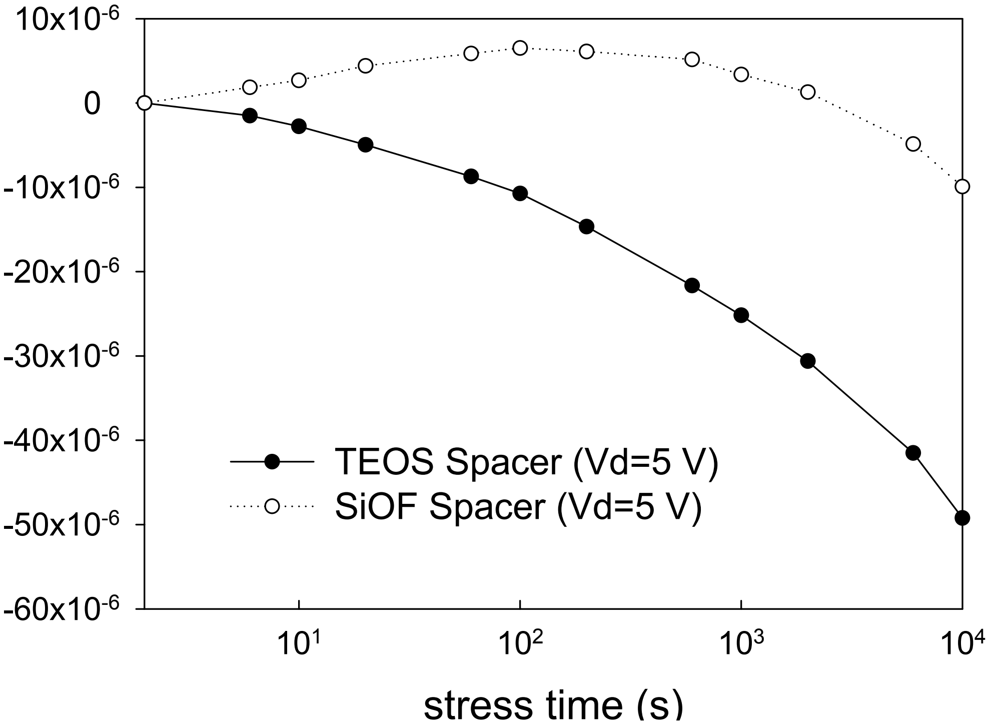

Figure 4.5 Comparsion of ΔIon characteristics of SiOF spacer TFT and TEOS spacer TFT for Vd=5V (W/L=10um/3um)

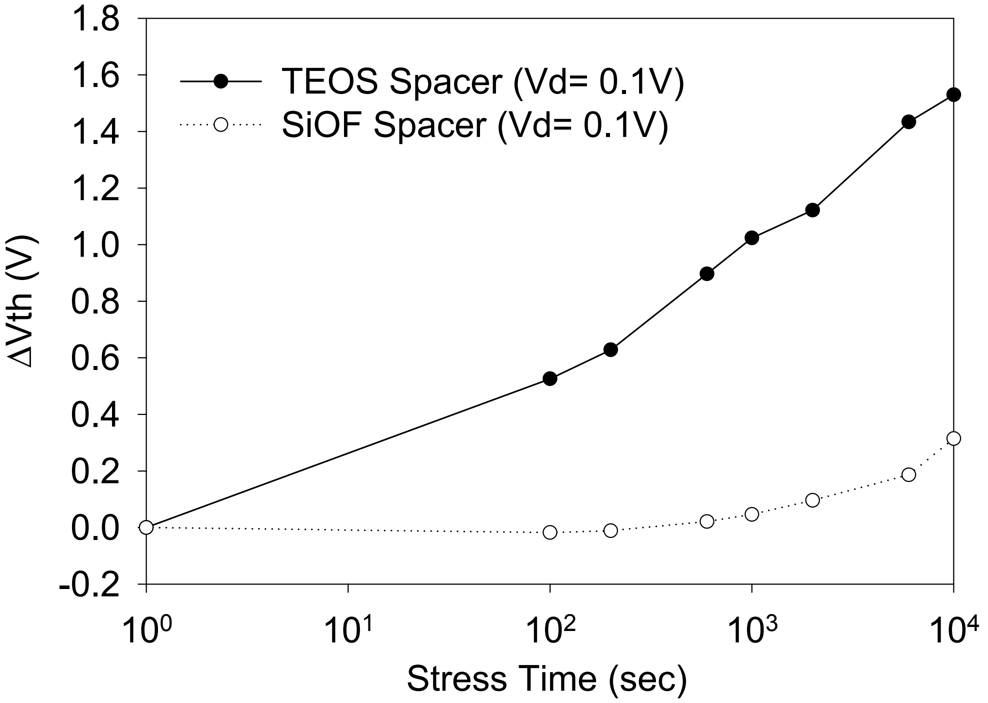

Figure 4.6 Comparsion of ΔVth characteristics of FSG spacer TFT and TEOS spacer TFT for Vd=0.1V (W/L=10um/3um)

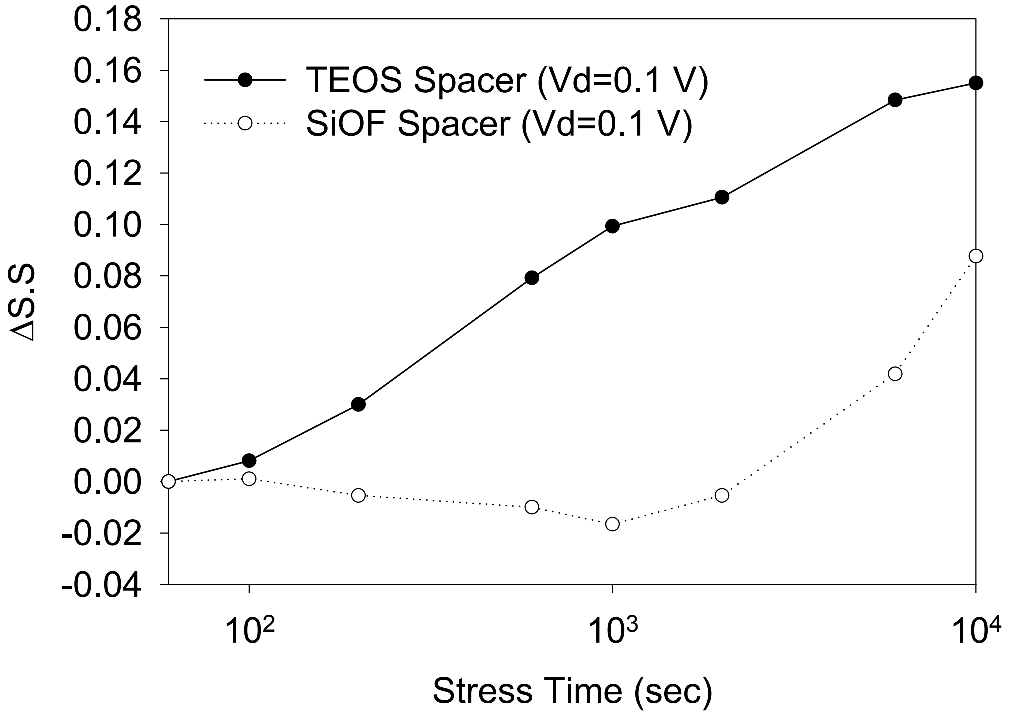

Figure 4.7 Comparison of ΔSS characteristics of SiOF spacer TFT and TEOS spacer TFT for Vd=0.1V (W/L=10um/3um)

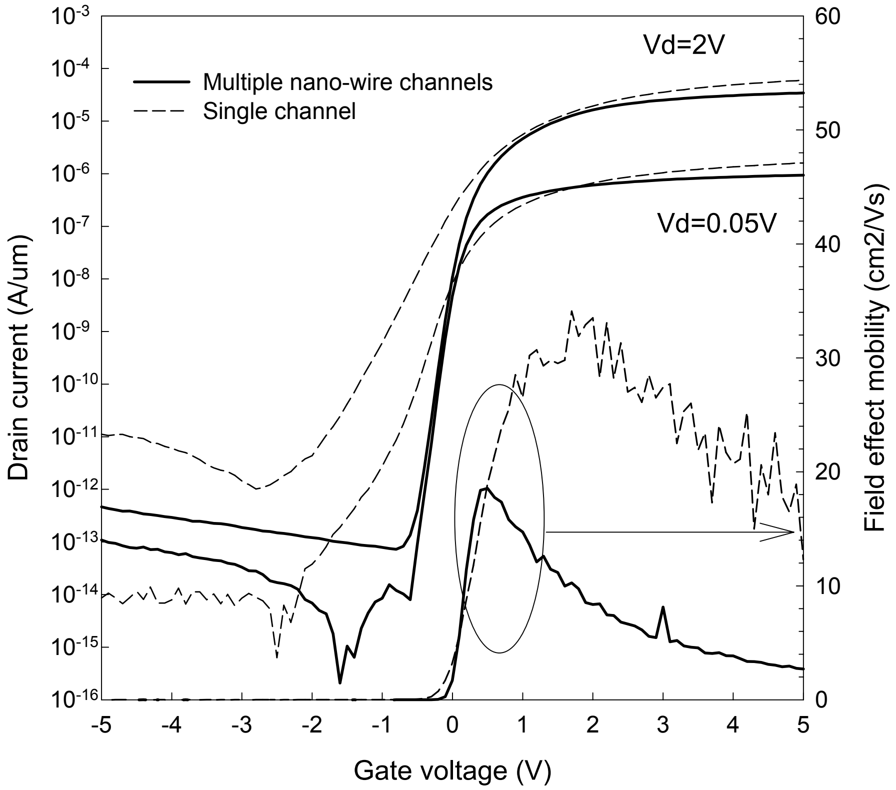

FIG. 4.8. Comparison of I_d-V_g transfer characteristics of multiple nano-wire channels (W/L = 67nm×10/0.5um) and single-channel (W/L = 1um/0.5um) polysilicon TFTs.

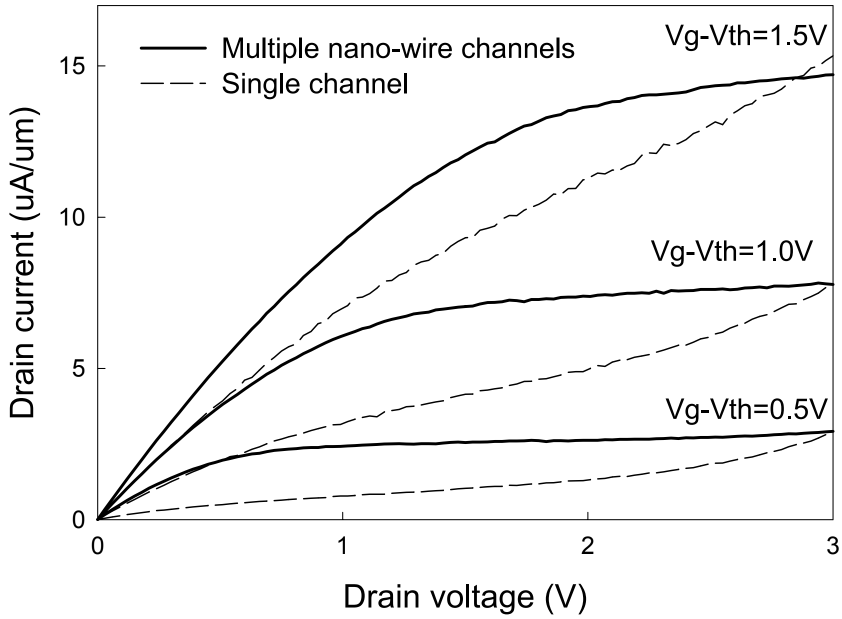

FIG. 4.9. Comparison of I_d-V_d output characteristics of multiple nano-wire channels (W/L = 67nm×10/0.5um) and single-channel (W/L = 1um/0.5um) polysilicon TFTs.

Table II Device parameters of single-channel TFTs with L/W = 0.5um/1um, and multiple nano-wire channels TFTs with L/W = 0.5um/67nm×10. All parameters were extracted at V_d = 2V, except for the field-effect mobilities which were extracted at V_d = 0.05V.

	Mobility (cm^2/VS)	V_{th} (V)	SS (mV/dec.)	Ion / Ioff	DIBL (V/V)
Single Channel	34.01	-0.11	360	5.90×10^7	0.40
Multiple channel	32.50	0.23	110	4.73×10^8	0

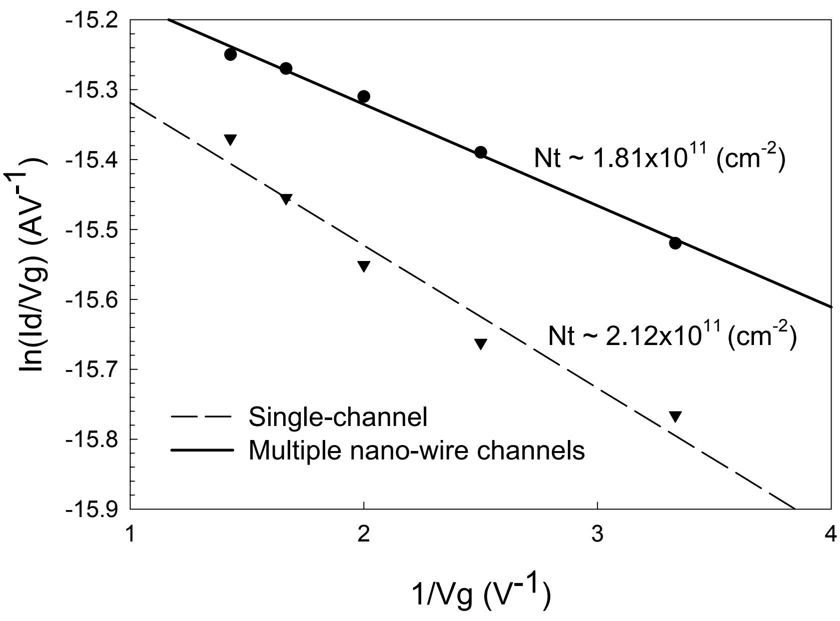

FIG. 4.10 Effective trap state density of multiple nano-wire channels (W/L = 67nm×10/0.5um) and single-channel (W/L = 1um/0.5um) polysilicon TFTs.

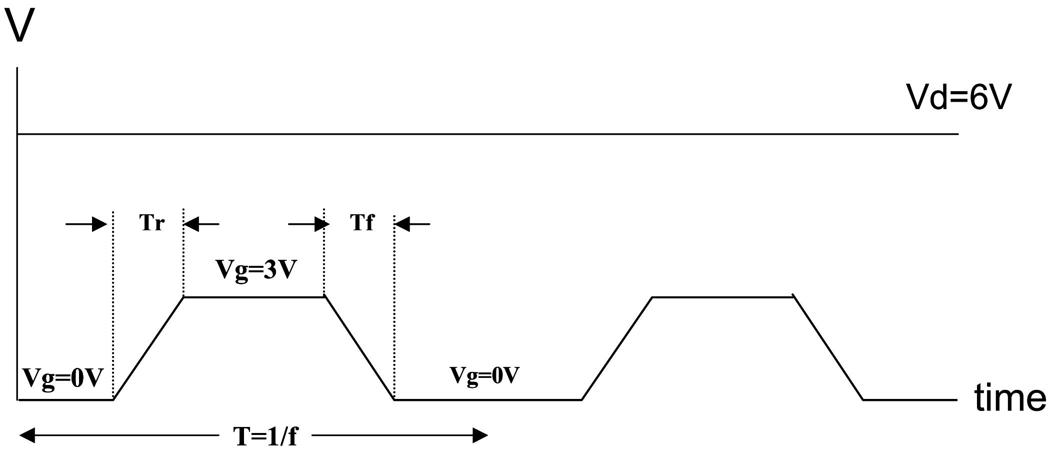

FIG. 4-11. The AC stress waveform of the pulse train.

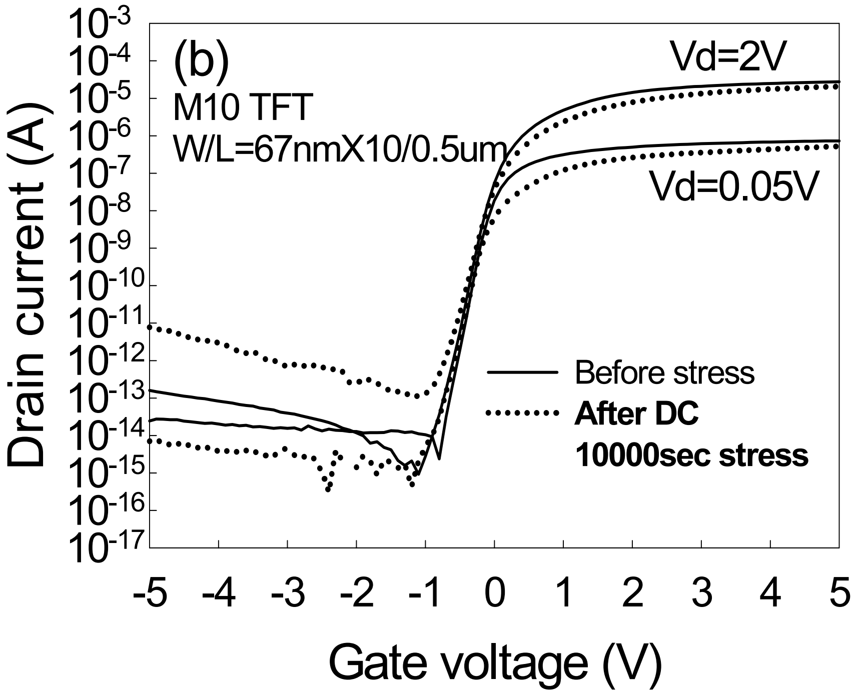

FIG. 4.12(a) Typical M10 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second.

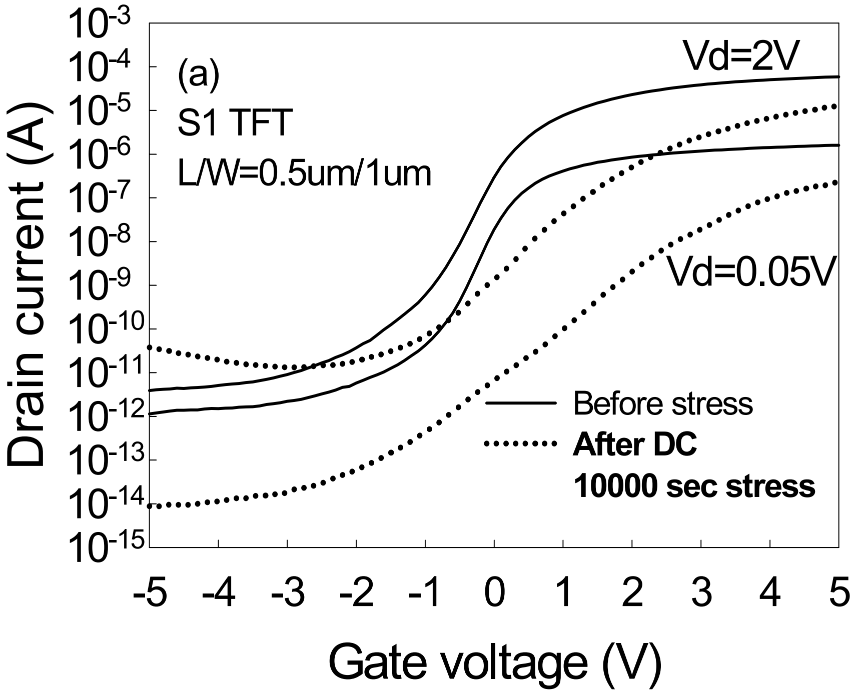

FIG. 4.12(b) Typical S1 poly-Si TFT I_d-V_g curves before and after DC hot carrier stress at 10000 second.

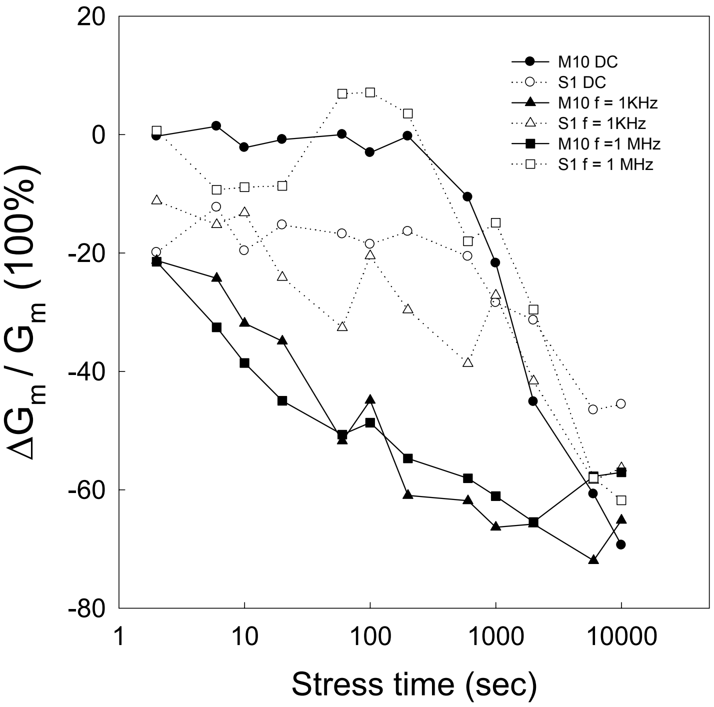

FIG. 4.13 Transconductance degradation of S1 and M10 TFT as a function of the stress time with different frequencies (DC, f = 1K Hz, and f = 1M Hz).

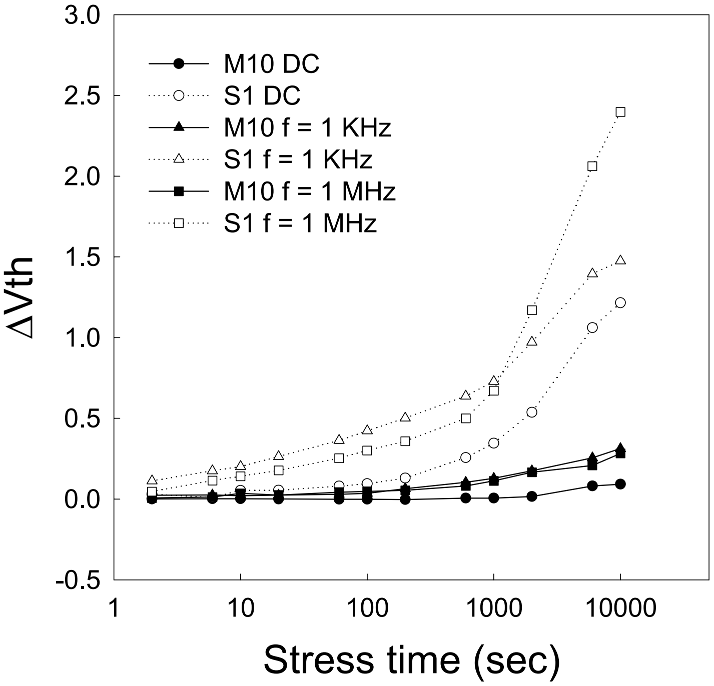

FIG. 4.14. Teshold voltage of S1 and M10 TFT as a function of the stress time with different frequencies.

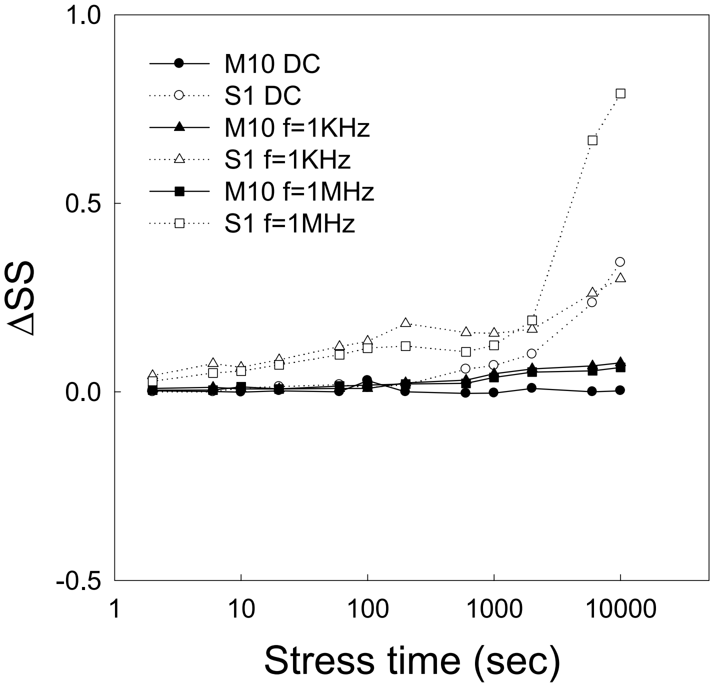

FIG. 4.15. Subthreshold swing variation of S1 and M10 TFT as a function of the stress time with different frequencies.

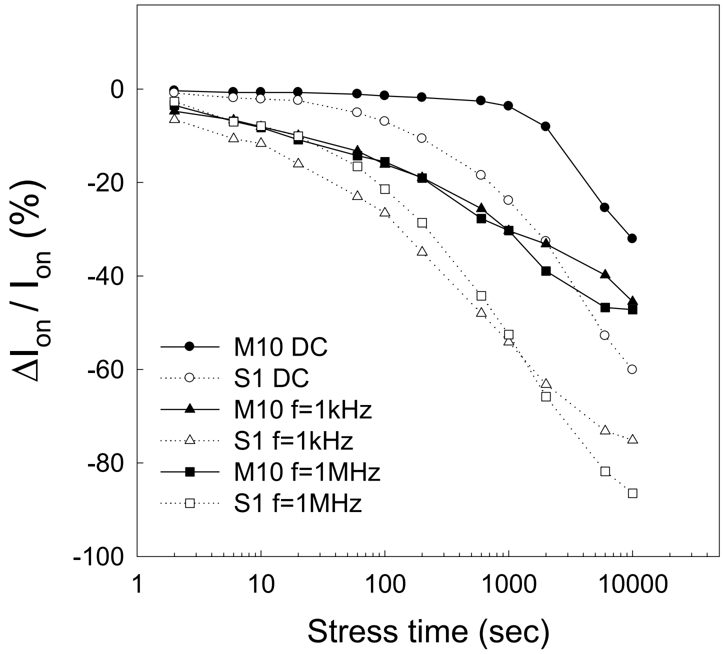

FIG. 4.16. ON current (I_{ON}) variation of S1 and M10 TFT as a function of the stress time with different frequencies.

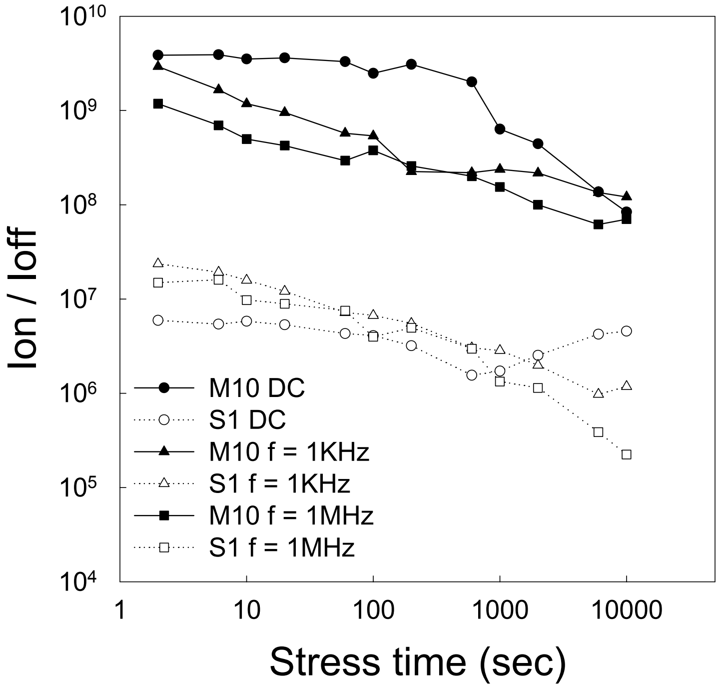

FIG. 4-17. ON/OFF ratio of S1 and M10 TFT as a function of the stress time with different frequencies.

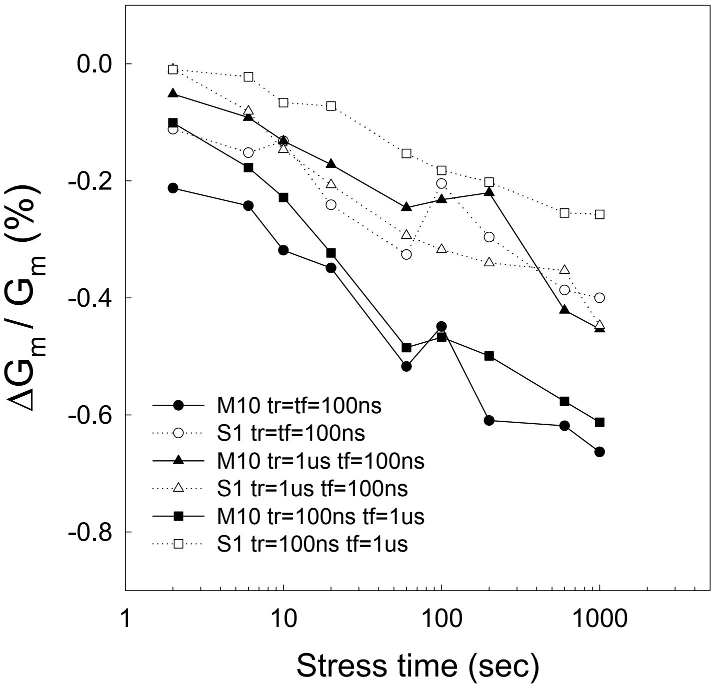

FIG. 4-18. Gm degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

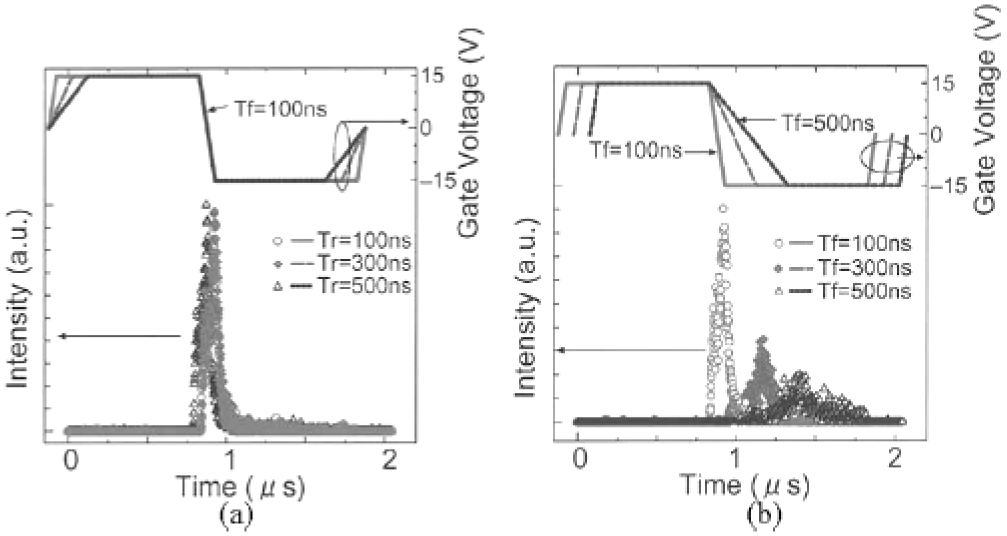

Fig. 4-19. Dependence of emission intensity on (a) pulse rise time and (b) pulse fall time. Emission intensity is independent of the pulse rise time. However, we have found that it strongly depends on the fall time.

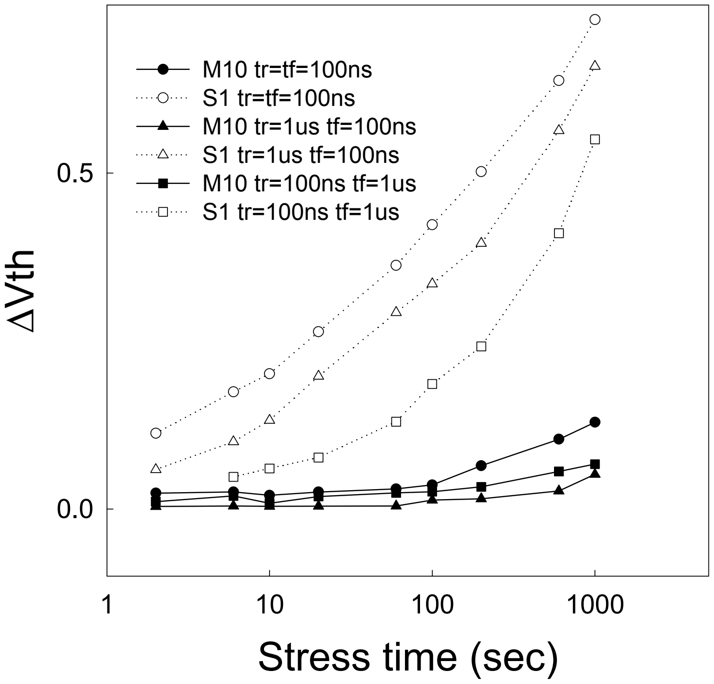

FIG. 4-20. Vth variation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency of 1 KHz.

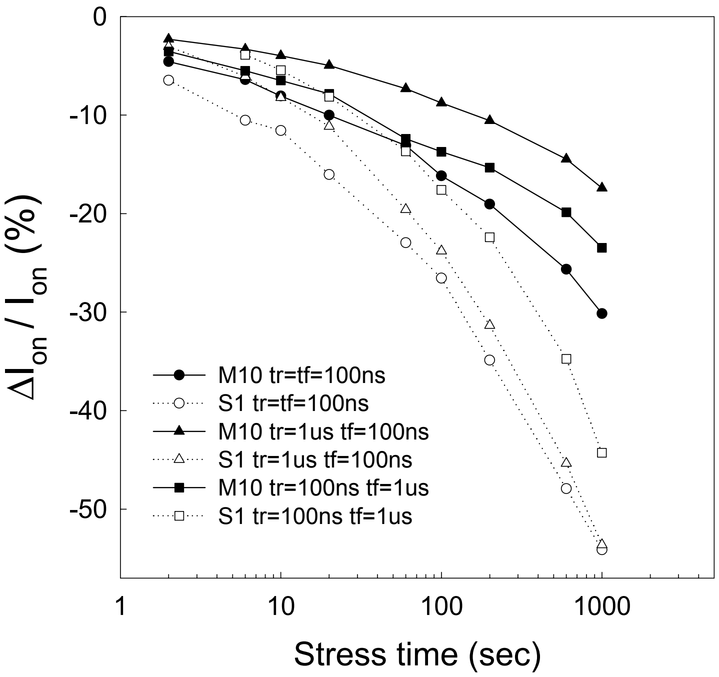

FIG. 4-21. ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with different rising time (Tr) and falling time (Tf) under the frequency.

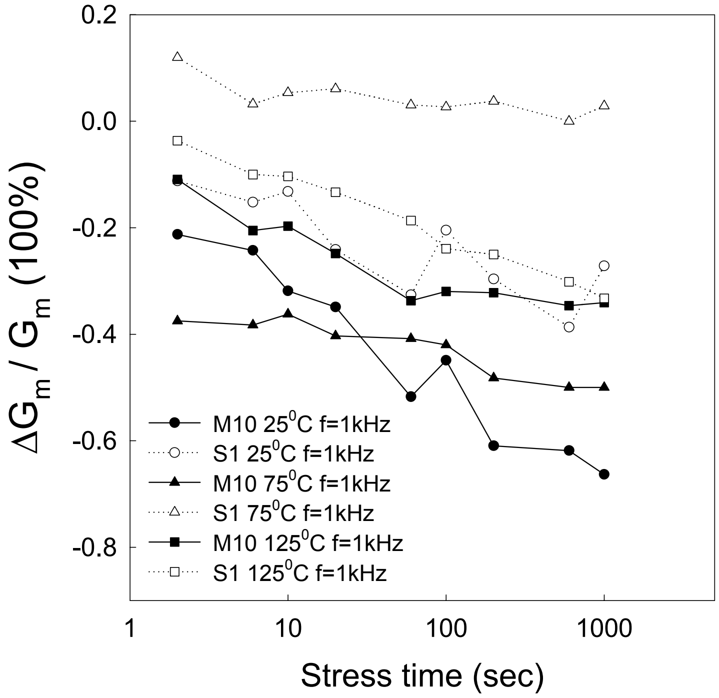

FIG. 4-22. Gm degradation of S1 and M10 TFT as a function of the stress time with different subtract temperature with 25^{0}C, and 75^{0}C under the same frequency of 1 KHz.

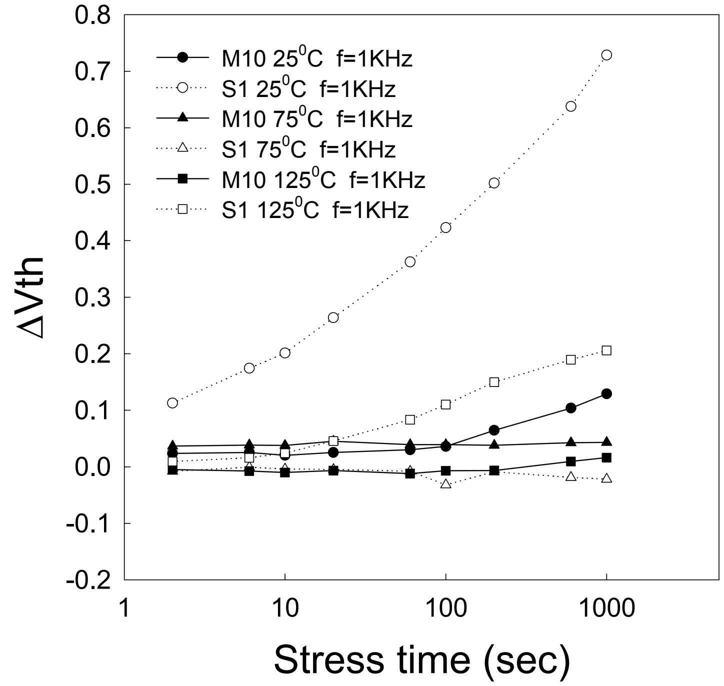

FIG. 4-23. Vth variation of S1 and M10 TFT as a function of the stress time with 25^0C, and 75^0C under the same frequency of 1 KHz.

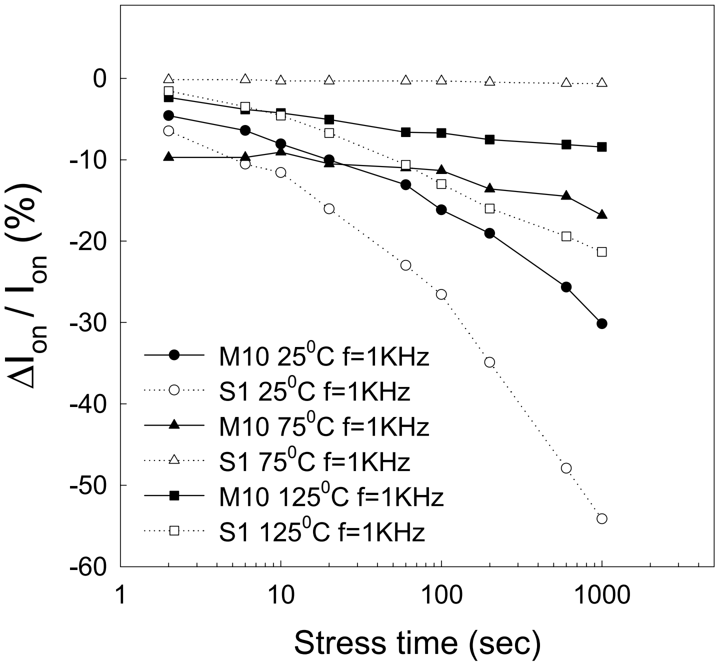

FIG. 4-24. ON current (Ion) degradation of S1 and M10 TFT as a function of the stress time with 25^0C, and 75^0C under the same frequency of 1 KHz.

Chapter 5

Conclusion

For the first part, we have proposed and successfully demonstrated the novel poly-Si TFT device with FSG film as the spacers to enhance the electrical characteristics due to fluorine passivation effect. The poly-Si TFT with FSG spacers exhibits superior endurance against hot carrier effect, leading to improved electrical reliability and suppressed kink effect than the TFT with TEOS SiO_2 spacer. In addition, the manufacture processes are compatible with the conventional TFT process. This indicates our proposed poly-Si TFT with FSG spacers is a promising technology for application in the TFT-LCDs.

In the second part, the performance and AC & DC reliability of multiple nanowire poly-Si TFTs are investigated. The experiment results reveal that the multiple nanowire poly-Si TFTs has higher performance than single-channel TFT, including a high ON/OFF current ratio, a low subthreshold slope, an absence of DIBL and favorable output characteristics. In static and dynamic hot-carrier stress experiments, the multiple nanowire poly-Si TFTs reduces the degradation of Vth, SS, Ion, On/OFF ratio and DIBL, for all kind of frequency, rising time, falling time and temperature, compared to single-channel TFT. These high reliability results of multiple nanowire poly-Si TFTs can be explained by its robust tri-gate control and its superior channel NH_3 passivation on the poly-Si grain boundary. The fabrication of this novel multiple nano-wire channel structure TFTs is easy and involves no additional processes. Such TFTs are thus highly promising for use in future high-performance poly-Si TFT applications.

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Reliability Study of Novel Process and Novel Structure Polysilicon Thin-Film Transistors