國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

超薄二氧化鉿閘極絕緣層之特性研究

Characteristics of Ultra-Thin HfO_2 Gate Insulator

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A Thesis

Submitted to Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

In Partial Fulfillment of the Requirements

for the Degree of

Master of Science

In

Electronics Engineering

June 2005

Hsinchu, Taiwan, Republic of China

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摘　要

當場效電晶體的閘極介電層厚度微縮至 1.5 奈米厚時，將產生一些諸如電子穿遂效應等嚴重的問題，因此極需以高介電係數材料取代二氧化矽作為閘極絕緣層，其中二氧化鉿就是目前被認為最有可能取代二氧化矽的材料。本實驗以鋁-二氧化鉿-矽之 MIS 電容結構為分析元件，首先利用直流濺鍍法沉積鉿金屬於 P 型和 N 型矽基板上，所沉積的金屬鉿厚度為 20 Å，接著以低溫通氧氣的爐管，分別在 200℃、300℃、400℃和 500℃下以 15 分鐘或 30 分鐘氧化金屬鉿，得到氧化鉿薄膜，其中部份試片在氧化後立刻以 850℃的快速熱退火處理 30 秒。在不同氧化條件下的薄膜電性，經由 C-V 和 I-V 量測得知，並討論量子效應的漏電流機制，另外也藉由磁滯效應、崩潰分佈、定電流加壓測試和在高溫下量測來討論各種氧化條件下元件的可靠度。在相同的等效厚度下，二氧化鉿薄膜在 1 伏特下的漏電流比二氧化矽薄膜少了兩個數量級以上。在相同的氧化條件下，P 型二氧化鉿電容比 N 型二氧化鉿電容有較好的電特性及可靠度，氧化溫度越高會產生越厚的介面層，使得薄膜等效厚度增加，可靠度也變差，但可改善磁滯效應。此外，以快速熱退火處理二氧化鉿薄膜無法改善薄膜特性。

Characteristics of Ultra-Thin HfO_2 Gate Insulator

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ABSTRACT

When the MOSFET gate insulator is scaled below 1.5 nm, some serious problems such as direct electric tunneling will occur. Therefore, high dielectric constant material is very desirable to replace SiO_2. Hafnium oxide is a most promising material for future MOSFET gate oxide applications. In this study, we used Al-HfO_2-Si MIS capacitor as our analysis device. First, we used DC sputter system to deposit 20 Å hafnium metal on p-type and n-type silicon substrate. Then we proceeded with furnace under 200℃, 300℃, 400℃ and 500℃ oxidation temperature and 15 or 30 minutes oxidation time to prepare HfO_2 thin film. After oxidation process, we had an additional RTA treatment at 850℃ for 30 seconds. The electrical characteristics of the film under different oxidation condition were discussed by C-V and I-V curves. Moreover, the conduction mechanism with quantum effect was also analyzed. The reliability of the film under different oxidation condition was discussed by hysteresis effect, breakdown distribution, constant current stress and high temperature measurement. With the same equivalent oxide thickness (EOT), the magnitude of leakage current of HfO_2 film is less than that of SiO_2 film over 2 orders at 1 V. Under the same oxidation condition, p-type HfO_2 capacitor has better electrical characteristics and reliability than n-type HfO_2 capacitor. Under higher oxidation temperature, it would result in thicker interfacial layer, larger EOT, worse reliability but better hysteresis. In addition, RTA treatment couldn't improve the quality of HfO_2 film.

誌 謝

首先，我要感謝我的指導教授張國明老師，在這兩年中所給我指導與教誨，使我在學術研究及待人處事上獲得長足的進步。

接著，我要感謝實驗室王敬業學長，在實驗過程中不斷的給予建議與指導，並且提供我寶貴的經驗，以及其他實驗室的伙伴們，從旁陪伴以及協助，使得本論文可以順利的完成。

另外，感謝國立交通大學半導體中心、國家奈米元件實驗室（NDL）提供我良好的研究環境和設備，同時也要感謝技術人員熱心的協助，因此使我的研究可以順利進行。而對於諸位口試委員的蒞臨指導與建議，在此也深表感謝之意。

最後，要感謝我的父母與親友，有了他們的支持與鼓勵，才能讓我在無後顧之憂的情況下讓我順利完成學業與論文。

Contents

Chapter 5 Reliability of Al/HfO_2/Si MIS Capacitors

Chapter 6 Conclusion and Future Work

Table Captions

Chapter 1

Chapter 3

Chapter 4

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 1

Introduction

1.1 Background and Motivations

1.1.1 Scaling of Oxide Thickness

For more than 30 years, SiO_2 films have been the preferred material for gate dielectric in metal-oxide semiconductor (MOS)-based structures. However, in order to increase the output of the products and reduce the cost, the scaling down of the device dimension is an inevitable tendency. In addition, the demand for the device performance and circuit stability is more and more strict, that means, high speed operation and low leakage current are necessary. To reach high speed, we can reduce channel length or lower operating voltage. If we lower operating voltage, we must raise the capacitance of gate oxide to maintain enough channel charges. Consequently, we need to reduce the oxide thickness to increase oxide capacitance. According to the SIA (Semiconductor Industry Association) roadmap, CMOS with gate length below 70 nm will need an oxide thickness of less than 1.5 nm, which corresponds to two or three layers of silicon dioxide atoms. But reducing the thickness of silicon dioxide to these dimensions results in an exponential increase of direct tunneling current [1]. The resulting gate leakage current will increase the power dissipation and will deteriorate the device performance and circuit stability for VLSI circuits.

Figure 1-1 shows the several kinds of conduction mechanisms of the leakage current passing through the oxide layer, which contain hot carrier injection, Fowler-Nordheim tunneling and direct tunneling. When the oxide thickness is less than 2 nm, the dominant leakage mechanism is direct tunneling. This results that the leakage current increase rapidly with the decrease of the oxide thickness. From fig. 1-2, when the equivalent oxide thickness (EOT) is 2 nm, the leakage current density of SiO_2 is 10^{-2} A/cm^2, which is lower than logic limit but higher than wireless limit. We could use SiON to replace SiO_2 and reduce the leakage current density about one order to make it lower than wireless limit. However, when the EOT is less than 2 nm, SiON also couldn't be used for wireless application. In addition, the leakage of SiO_2 even is larger than logic limit when the EOT is down to 1.5 nm, and SiON also couldn't be used for logic application when the EOT is less than 1.3 nm. Thus, we have no choice but use high-k materials instead of SiO_2 to be the gate insulator. High-k dielectrics could effectively reduce the leakage current density about 4 orders.

1.1.2 Roadmap of Gate Dielectric

Fig. 1-3 shows the low operating power (LOP) scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling. In 2005, the EOT is 1.4 nm and the leakage current density of the oxynitride is below the leakage limit line. However, after 2006, the EOT is below 1.3 nm and the oxynitride is incapable of meeting the limit on the gate leakage current density. Fig. 1-4 shows the high-performance logic scaling-up of gate leakage current density limit and simulated gate leakage due to direct tunneling. In 2006, the EOT is only 1 nm but the leakage current density of the oxynitride is still below the limit line because the application of high-performance logic could endure larger gate leakage current. However, after 2007, the oxynitride couldn't be used for high-performance logic anymore. Table 1-1 is the roadmap of 2004 ITRS (International Technology Roadmap for Semiconductor) for the high-performance logic technology. After 2006, the requirement of EOT even reduces to less than 1 nm. It would be a big challenge because the leakage current is too large to be acceptable for SiO_2 under such a thin thickness (Fig. 1-2). Replacing SiO_2 by SiON could effectively reduce leakage current. However, fig. 1-4 shows that oxynitride is also incapable of meeting the limit on gate leakage current density. Therefore, we need to aggressively seek a feasible high-k material to replace SiO_2.

1.2 High-k Material

1.2.1 Advantages of High-k Material

As SiO_2 film is less than 2 nm, the leakage current becomes unacceptable. The direct way to reduce the leakage current is to make the oxide thickness thicker, which can repress the direct tunneling. According to the formula : $C / A = \varepsilon_r\varepsilon_0 / t_{ox}$, if we want the capacitance is still large enough, we need to choose some higher ε_r than that of SiO_2 ($\varepsilon_r = 3.9$). The material with higher dielectric constant than 3.9 is called high-k material. Under the same EOT, we could expect that the leakage current of the high-k material is lower than that of the conventional SiO_2 film due to the thicker physical thickness. In the last few years, high-k material has attracted a great deal of attention because of their potential for replacing SiO_2 as gate dielectric in MOSFETs.

1.2.2 Challenges of High-k Material

Although high-k material is expected to replace SiO_2 ideally, there are many problems to use high-k material practically. The issues for choosing a high-k material

may include： (1) low dielectric constant interfacial layer between substrate and high-k material (2) degradation of carrier mobility (3) shift of threshold voltage (4) thermal stability (5) boron penetration prevention (6) poly interface and poly gate electrode (7) compatibility with traditional CMOS process [1]-[4]. The high-k problems waiting to be solved is shown in fig. 1-5, which contains important regions consisting of the silicon interface and silicon interfacial layer, high-k film, and the interface between poly and high-k region (poly interfacial layer). The integration of the stack into a robust transistor flow is very crucial. The required high-k transistor integration is different than a baseline pure oxide or nitrogen-bearing gate dielectric. Unless special details are followed for the integration of the high-k material with the interfaces and subsequent transistor flow, the desired electrical properties will not be achieved. The specifications below are many electrical properties that will need to be achieved [5]：

- High Performance EOT $\leqq$ 1 nm with leakage current density (J_g) $\leqq$ 1.0 A/cm^2
- Low Standby Power $\leqq$1.6 nm with $J_g \leqq$ 2.2E-3 A/ cm^2
- Density of interface traps (D_{it}) $\leqq$ 5E10 / cm^2 • eV
- High frequency (100 kHz) capacitance-voltage (C-V) hysteresis $\leqq$ 10 mV
- Thickness uniformity (3ρ) $\leqq$ 4 %
- Thermal stability (physical and electrical) at 1000°C, 10 sec
- Surface mobility $\geqq$ 95 % of SiO_2 (current 2 nm baseline)
- High-k compatible post-gate etch clean strategy
- Reliability comparable to SiO_2 (current 2 nm baseline)
- DRAM requirements for J_g (10^{-8} A/cm^2) and thermal stability (1000°C, 60 sec)

Table 1-2 shows the reliability challenges of high-k gate dielectrics, metal gate and copper/low-k interconnects. The main reliability issues include：(1) dielectric breakdown characteristics (hard and soft breakdown) (2) influence of charge trapping and NBTI on threshold voltage stability (3) stability and number of fixed charges. All the issues mentioned above still need more effort to overcome.

1.3 Why choose HfO_2

There are many kinds of high-k materials, including Al_2O_3, Y_2O_3, Ta_2O_5, TiO_2, ZrO_2 and HfO_2 etc. Table 1-3 lists basic characteristics of several high-k dielectrics. Unfortunately, many high-k materials such as Ta_20_5, TiO_2, $SrTiO_3$, and $BaSrTi0_3$ are thermally unstable when directly contacted with silicon [6] and need an additional barrier layer which may add process complexity and impose thickness scaling limit.

Also, materials with too low or too high dielectric constant may not be adequate choice for alternative gate dielectric application. Ultra high-k materials such as STO or BST may cause fringing field induced barrier lowering effect [7]. Materials with relatively low dielectric constant such as $A1_2O_3$ and Y_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4 [8].

Among the medium-k materials compatible with silicon, oxides of Zr and Hf are attracting much attention recently. Especially, Hf forms the most stable oxide with the highest heat of formation (ΔH_f = 27l Kcal/mol) among the elements in IVA group of the periodic table (i.e. Ti, Zr, Hf). Unlike other silicides, the silicide of Hf can be easily oxidized [9]. HfO_2 possesses a dielectric constant of up to 25 [10], a large bandgap of 5.7 eV with sufficient band offset of larger than 1.5 eV [11], and well thermal stability in contact with silicon [12]. HfO_2 is very resistive to impurity diffusion and intermixing at the interface because of it's high density (9.68 g/cm^3) [13]. In addition, HfO_2 is the first high-k material showing compatibility with polysilicon gate process [14]. These properties make HfO_2 one of the most promising candidates for alternative gate dielectric application. Although inadequate mobility of HfO_2 MOSFETs is among the biggest concerns, various techniques have been explored to enhance the mobility. Introduction of strained silicon substrate [15], for example, drastically improved the mobility by changing the band structure of the substrate rather than changing the dielectric itself. However, the characteristics and mechanism of HfO_2 are not totally understood.

1.4 Thesis Organization

Following chapters in the thesis are primarily organized as follow：

In chapter 2, we make a comparison of various preparation methods of HfO_2.

In chapter 3, we make a description of experimental details. DC magnetron sputtering system is used to deposit hafnium on silicon surface.

In chapter 4, we discuss the characteristics of ultra-thin HfO_2 insulator by Metal-Insulator-Semiconductor (MIS) capacitors.

In chapter 5, we discuss the reliability of ultra-thin HfO_2 insulator by Metal-Insulator-Semiconductor (MIS) capacitors.

In chapter 6, we make the conclusions for this thesis and provide some suggestions for future work.

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Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length high-performance (HP) (nm) [1]	45	37	32	28	25	22	20
EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	1.3	1.2	1.1	1.0	0.9	0.8	0.8
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.4	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.1	2.0	1.8	1.7	1.3	1.2	1.2
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	2.2E+02	4.5E+02	5.2E+02	6.0E+02	9.3E+02	1.1E+03	1.2E+03
Nominal power supply voltage (V_{dd}) (V) [6]	1.2	1.2	1.1	1.1	1.1	1.0	1.0
Saturation threshold voltage (V) [7]	0.21	0.20	0.20	0.21	0.18	0.17	0.16
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (μA/μm) [8]	0.03	0.05	0.05	0.05	0.07	0.07	0.07
Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (mA/mm) [9]	♦ 980	1110	1090	1170	1510	1530	1590
Required "mobility/transconductance improvement" factor [10]	1.0	1.3	1.3	1.4	2.0	2.0	2.0
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	0.8	0.7
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	♦ 180	180	180	171	162	153	144
Ideal NMOS device gate capacitance (F/μm) [14]	7.40E-16	6.39E-16	6.14E-16	5.69E-16	6.64E-16	6.33E-16	5.76E-16
Parasitic fringe/overlap capacitance (F/μm) [15]	2.40E-16	2.40E-16	2.40E-16	2.30E-16	2.20E-16	2.00E-16	1.90E-16
High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	♦ 1.20	0.95	0.86	0.75	0.64	0.54	0.48
Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	♦ 1.00	1.26	1.39	1.60	1.86	2.20	2.49
Nominal logic gate delay (NAND Gate) (ps) [18]	♦ 30.24	23.94	21.72	18.92	16.23	13.72	12.13
NMOSFET power-delay product (J/μm) [19]	1.41E-15	1.27E-15	1.03E-15	9.66E-16	1.07E-15	8.33E-16	7.66E-16
NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	3.96E-07	6.60E-07	6.05E-07	6.05E-07	8.47E-07	7.70E-07	7.70E-07

Table 1-1 High-performance Logic Technology Requirements Roadmap.
(ITRS：2004 update)

Reliability Difficult Challenges	
Difficult Challenges	Summary of Issues
High-k Gate Dielectrics	1. Dielectric breakdown characteristics (hard and soft breakdown) 2. Influence of charge trapping and NBTI on threshold voltage stability 3. Stability and number of fixed charges
Metal Gate	1. Impact of metal-ion drift and/or diffusion on gate dielectric reliability 2. Work function control and stability 3. Metal susceptibility to oxidation 4. Thermo-mechanical issues due to large thermal expansion mismatch 5. Impact of implantation
Copper / Low-k Interconnects	1. Stress migration of Cu vias and lines 2. Cu via and line electromigration performance 3. Thermal-mechanical stability of the interfaces between metals, barriers and interlevel dielectrics and resulting line-to-line leakage 4. Time Dependent Dielectric Breakdown (TDDB) of the Cu/low-k system 5. Reliability impact of lower thermal conductivity of low- k dielectric 6. Reliability issues due to the porous nature of the low- k dielectrics and moisture 7. Reliability impact of the lower mechanical strength in the Cu/low- k system, including the impact of packaging

Table 1-2 Reliability difficult challenges. (ITRS：2004 update)

Material	Dielectric constant (k)	Energy band gap E_g (eV)	ΔE_c (eV) to Si	ΔH_F (eV/O atom)
SiO_2	3.9	8.9	3.2	-4.68
Si_3N_4	7	5.1	2	—
Al_2O_3	9	8.7	2.3	-5.76
Y_2O_3	15	5.6	2.3	-4.93
CeO_2	26	5.5		-5.02
Ta_2O_5	26	4.5	1-1.5	-2.09
La_2O_3	30	4	2.3	-6.62
TiO_2	80	3.5	1.2	-4.86
HfO_2	25	5.7	1.5	-5.77
ZrO_2	25	7.8	1.4	-5.66
$HfSi_xO_y$	15-25	～6	1.5	-5.24
$ZrSi_xO_y$	12-25	6.5	1.5	-5.21

Table 1-3 Characteristics of various high-k materials.

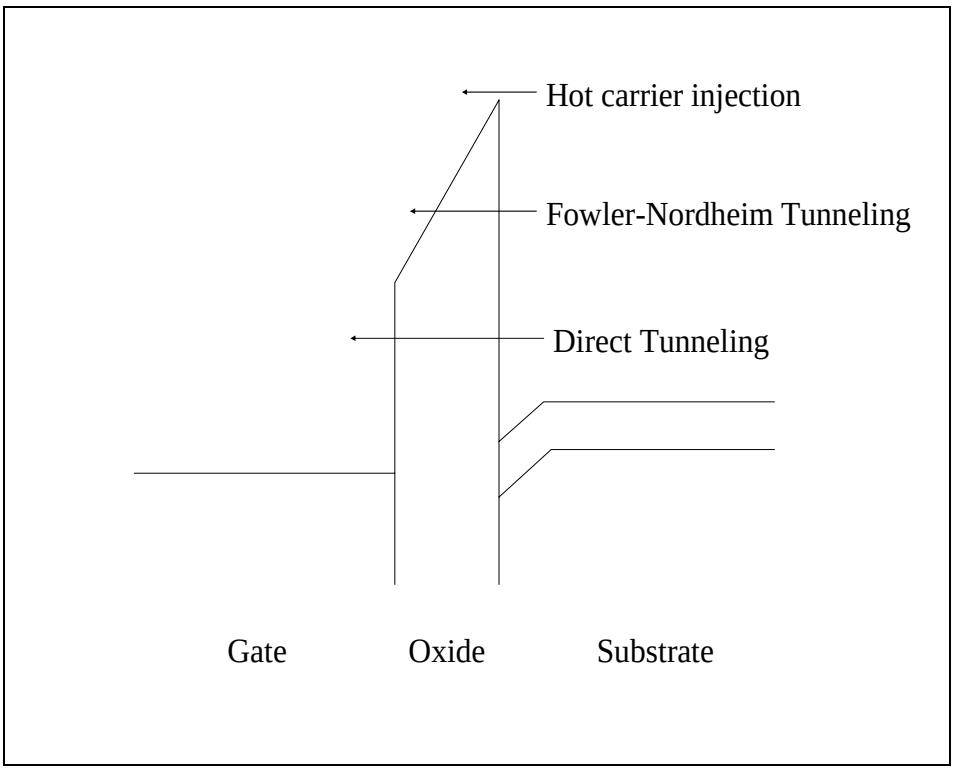

Fig. 1-1 Conduction mechanism in oxide for the MOS structure.

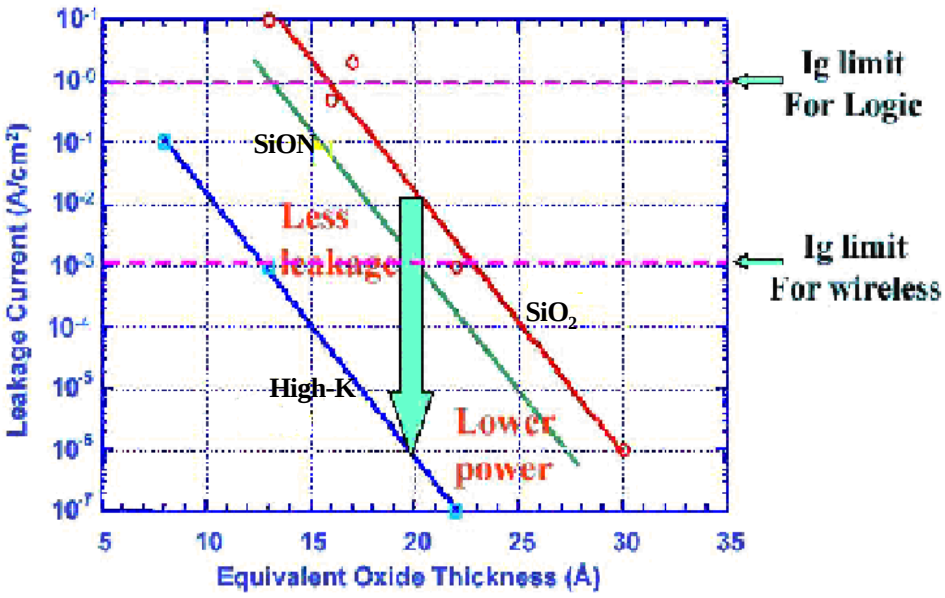

Fig. 1-2 Gate leakage reduction by high-k dielectric.
(B-Y Nguyen, 6th TRC October 27-28, 2003 *Motorola*)

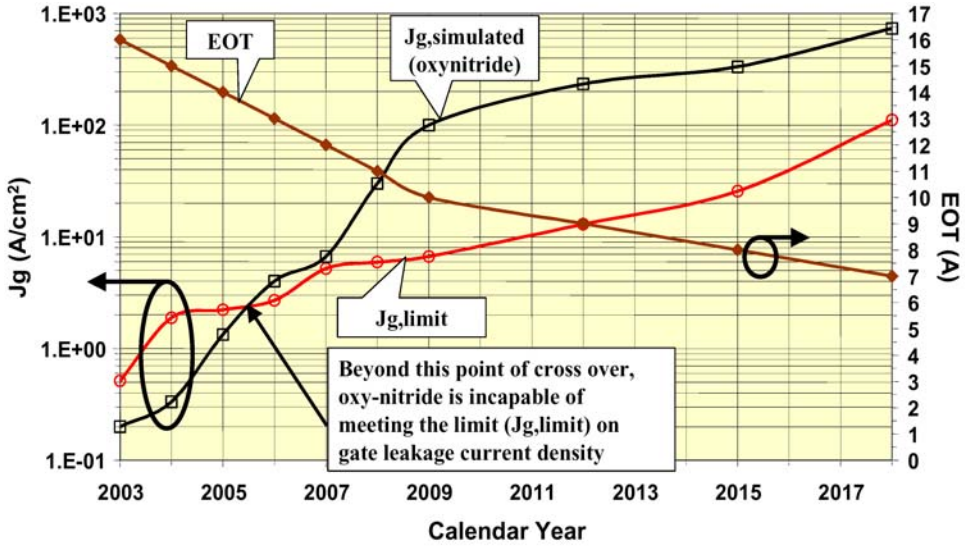

Fig. 1-3 LOP logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling. (ITRS：2004 update)

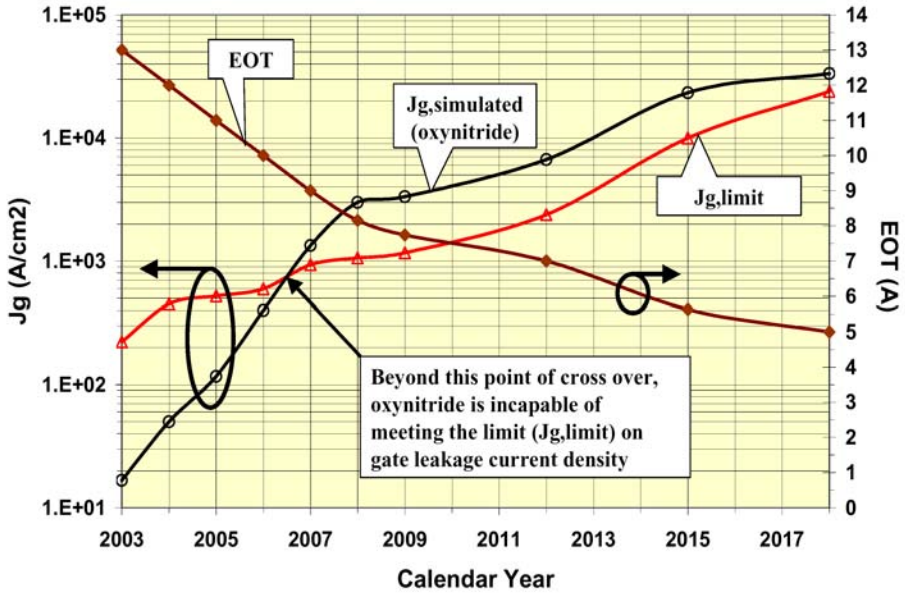

Fig. 1-4 High-performance logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling. (ITRS：2004 update)

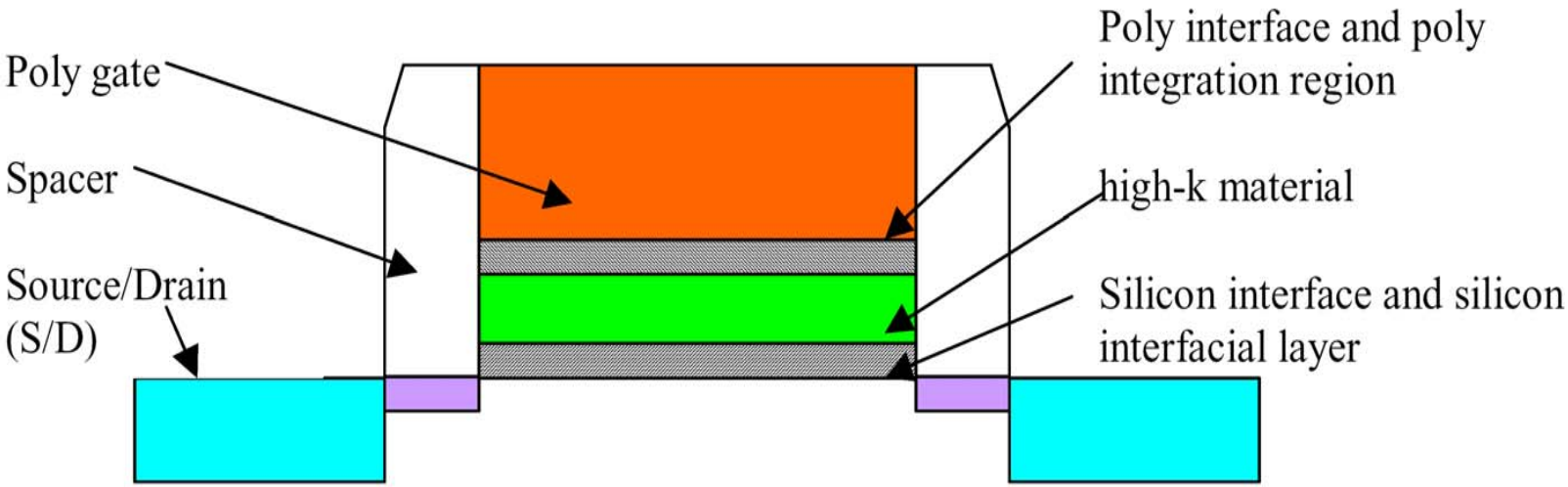

Fig. 1-5 Important high-k regions to be optimized for 1 nm high-k transistors.
(International SEMATECH Confidential and Supplier Sensitive, 2002)

Chapter 2

Preparation methods of HfO_2

There are various methods to prepare high-k thin films, such as chemical vapor deposition (i.e. ALCVD, MOCVD, PECVD etc.) [1]-[3] and physical vapor deposition (i.e. Sputtering, PLD etc.) [4][5]. Among which, the usual methods for preparing HfO_2 films are ALCVD, MOCVD and Sputtering. We compare these three methods below.

2.1 ALCVD

The major difference between conventional chemical vapor deposition (CVD) and ALCVD (atomic layer CVD) arises from how precursors are introduced to the substrate and how the substrate surface is applied to control growth. In ALCVD, precursors are introduced alternatively to the substrate surface with an inert gas purge between each. The precursors are not allowed to be in contact with each other in the gas phase. This results in a surface-controlled, layer-by-layer process for the deposition of thin films with atomic layer accuracy. Each atomic layer formed in the sequential process is a result of saturated surface controlled reactions. It provides well controlled growth of very thin films and excellent step coverage. Fig. 2-1 shows how ALCVD Al_2O_3 and HfO_2 were deposited by ligand exchange reaction. Trimethyl aluminum $Al(CH_3)_3$ (TMA) and H_2O were used for Al_2O_3 deposition and hafnium tetrachloride $HfCl_4$ and H_2O were used for HfO_2 deposition. Much more detail on the surface chemistry is presented elsewhere [6].

ALCVD Hf-based high-k materials have demonstrated the feasibility of EOT scaling down to 1 nm by using $HfAl_xO_y$ on nitrided surfaces [7]. HfO_2 with Al_2O_3 in it, such as $HfAl_xO_y$ or $HfO_2/Al_2O_3/HfO_2$, shows much better scaling capability than just HfO_2. Fig. 2-2 shows the scaling limits of different Hf-based high-k materials for ALCVD. HfO_2 could be utilized but was unable to scale below ~1.7 nm. $HfSi_xO_y$ deposition has shown great promise and has been scaled to 1.6 nm with leakage current four orders of magnitude lower than SiO_2. The physical defects observed in the thin HfO_2 limit the physical thickness scaling. However, the charge trapping is worsened by the presence of Al_2O_3. It has been found that the interfacial layers and high-k bulk materials both are very important for suppressing traps in high-k

dielectric. Some initial physical analysis data suggests the O_3 chemical oxide may be a very promising approach for EOT scaling of ALCVD high-k stacks because chemical oxide has been demonstrated as a good starting surface for ALCVD growth. The rapid thermal SiO_2 or SiON grown at the reduced partial pressure of reaction gases also is considered a possible solution for further reducing interfacial layer thickness. In the future, the project will focus on solving the charge trapping and mobility degradation of HfO_2 with Al_2O_3 in it. Besides the electrical characterizations of ALCVD high-k materials, the issues related to manufacturing (such as uniformity, repeatability, and cost of ownership (COO)), need to be addressed before ALCVD high-k can be used in the IC industry. The uniformity and repeatability of HfO_2 is quite reasonable (std. dev. 3–4%) [7]. But the COO is another big problem. Currently, ALCVD is a very slow process. The deposition time for a 3 nm HfO_2 film is over 4 min without counting time for stabilization, pumping down and up, and wafer transfer. This can result in a total of 10–15 min for 2–4 nm HfO_2 deposition. The very slow throughput might be the major showstopper to using ALCVD tools for mass production.

2.2 MOCVD

MOCVD (metal-organic CVD) is a widely used technology for depositing a variety of thin films, including metal oxide and metal silicate films, for high-k gate dielectric applications. The basic steps in MOCVD deposition method are as follows:

1. MO precursor in company with N_2 process gas and O_2 process gas are injected into the reactor.
2. The sources are mixed inside the reactor and transferred to the deposition process chamber.
3. At the deposition process chamber, high temperature results in the decomposition of sources and other gas-phase reactions, forming the film precursors that are useful for film growth and byproducts.
4. The film precursors transport to the growth surface.
5. The film precursors absorb on the growth surface.
6. The film precursors diffuse to the growth site.
7. At the surface, film atoms incorporate into the growing film through surface reaction.
8. The byproducts of the surface reactions desorb from the surface.
9. The byproducts transport to the main gas flow region away from the deposition area toward the reaction. Then the wafer exits.

From fig. 2-3, it is apparent that 1 nm EOT can be achieved with MOCVD metal oxide films when a metal electrode is used. However, most of the devices with MOCVD HfO_2 and $HfSi_xO_y$ when a poly-Si gate is used have EOT greater than 2 nm. Unlike metal electrode, using poly-Si electrode requires the high-k gate stack to go through a 1000°C/10 sec S/D activation anneal step. This step not only results in chemical and structural changes in the high-k film, but also affects interfaces between the high-k film/substrate and the high-k/poly-Si electrode. All devices fabricated with MOCVD ZrO_2 and ZrSiO films using poly-Si gate electrode were too leaky to give any meaningful C-V results. In general, using poly-Si gate electrode results in around 0.7 to 1 nm higher EOT for gate stacks fabricated with HfO_2 and $HfSi_xO_y$ gate dielectric films. This additional interfacial oxide thickness is too large to be acceptable. In view of this, the MOCVD is not a good tool for high-k material deposition with poly-Si gate. However, the MOCVD has very good throughput and can process a 25-wafer lot in ~2 hours (roughly 4X better than ALCVD). Thus, from a throughput perspective, the MOCVD has a distinct advantage over the ALCVD [7].

2.3 DC Magnetron Sputtering

The usual HfO_2 film with DC magnetron sputtering method is reactively sputtered from an Hf target in an Ar + O_2 ambient onto Si substrate. The advantages of the DC magnetron sputtering are simple and cheap. In addition, the HfO_2 film prepared by CVD system easily contains organic impurities and/or oxygen vacancies inside. This will cause leakage current through Frenkel-Pool effect or trap assisted tunneling [8]. Less contaminants are produced by the process of the sputtering because there is no other unnecessary chemicals. However, the uniformity of the DC sputtering is worse than that of the ALCVD and the MOCVD in 12 inch diameter Si wafer. Further, sputtering in an O_2 ambient easily produces SiO_2 interfacial layer. Therefore, we decide to sputter Hf in an Ar ambient only. After pure Hafnium has been deposited on Si substrate, we put the wafer into furnace system with O_2 ambient at some low temperature for oxidation. At some low temperature (＜500℃), Si will not react with O_2 to form the SiO_2. Then, the HfO_2 film is prepared without SiO_2 interfacial layer.

2.4 References

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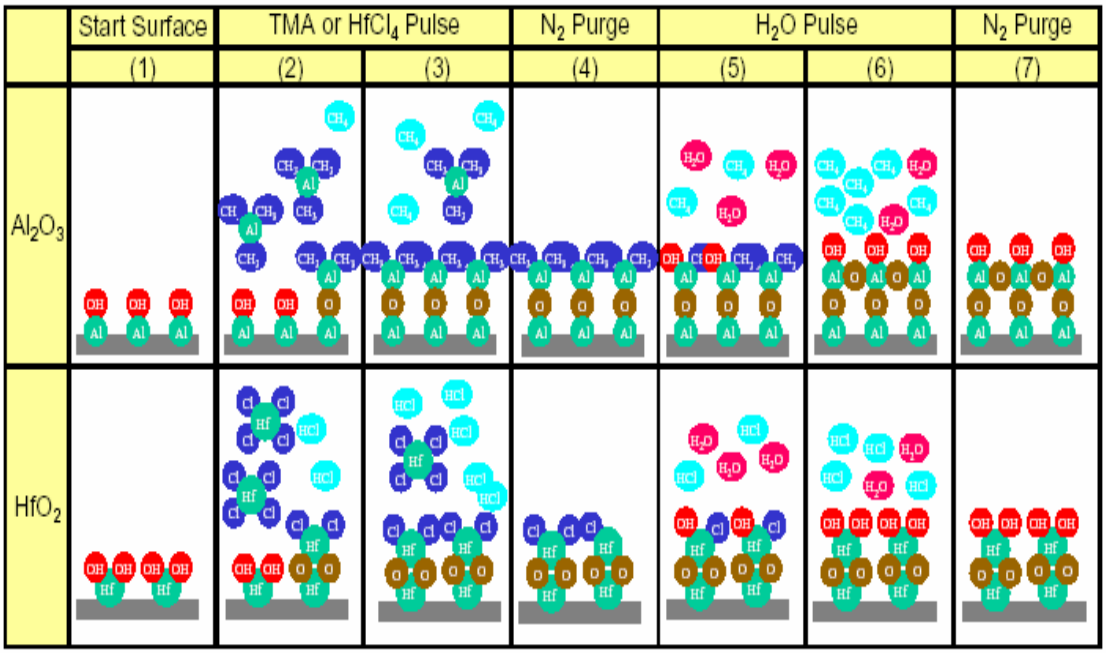


Fig. 2-1 ALCVD growth mechanism of AL_2O_3 and HfO_2.
(International SEMATECH Confidential and Supplier Sensitive, 2002)

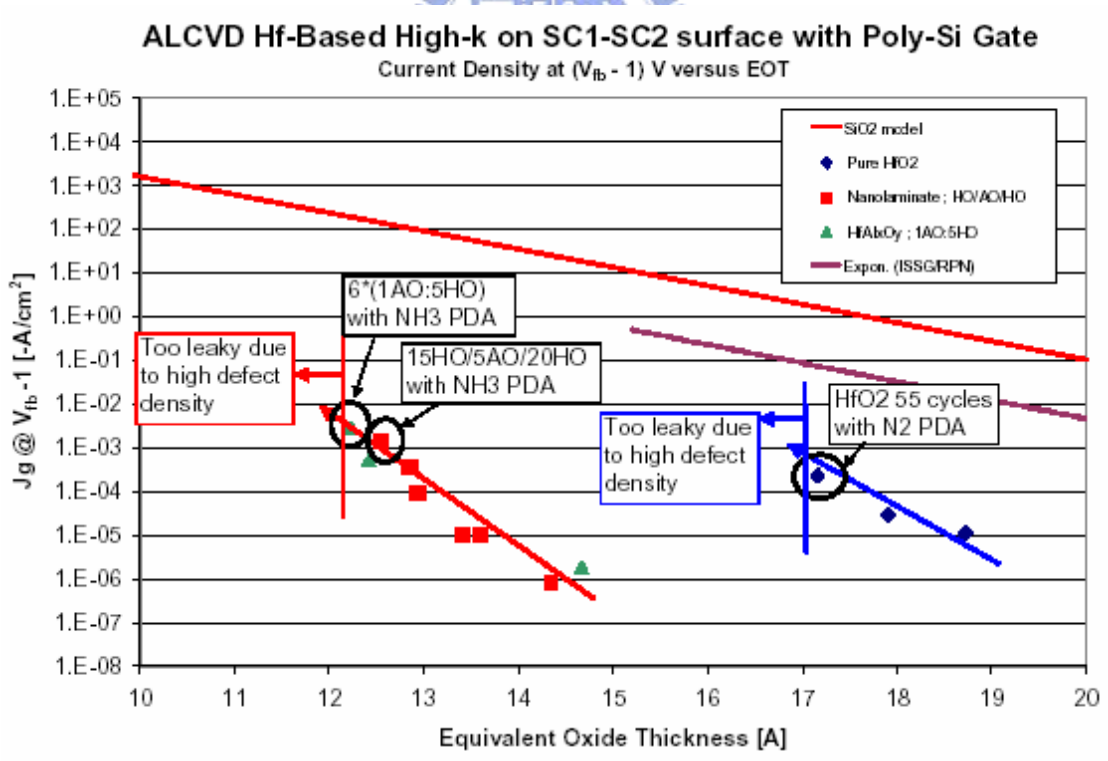


Fig. 2-2 Scaling limits of different ALCVD Hf-Based high-k Materials.
(International SEMATECH Confidential and Supplier Sensitive, 2002)

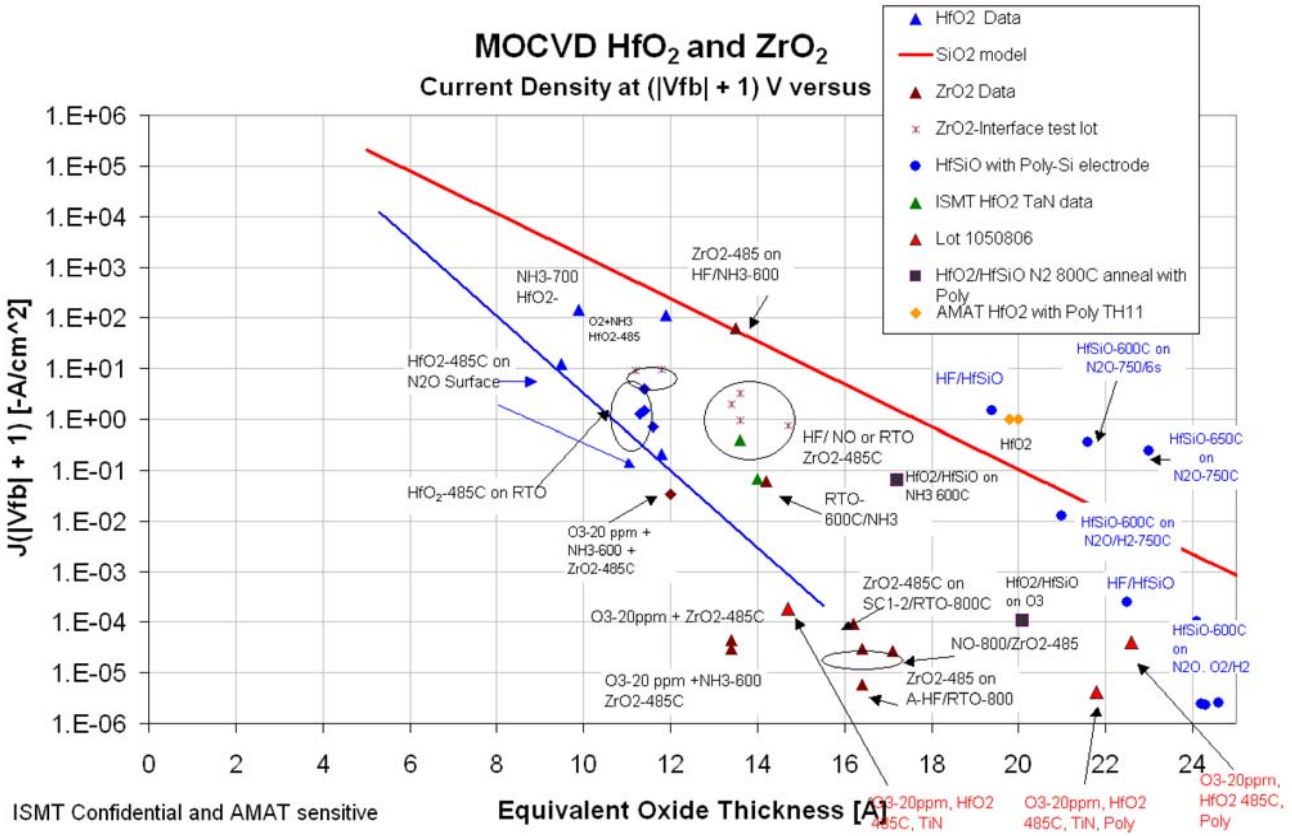


Fig. 2-3 Scaling limits of MOCVD HfO_2 and ZrO_2.

(International SEMATECH Confidential and Supplier Sensitive, 2002)

Chapter 3

Experiments of Al/HfO_2/Si MIS Capacitor

3.1 MIS Capacitors Fabrication Process

In this thesis, isolated Al gated capacitors were fabricated to study ultra thin HfO_2 gate dielectrics. Figure 3-1 shows the fabrication flow of this experiment. The starting wafer was four inch (100) orientated n-type wafer with phosphorus doped or p-type wafer with boron doped. It was one side polished and its resistivity was 5~10 ohm-cm. After standard initial RCA cleaning, wafers were put into furnace and grew a 5000Å thermal oxide layer at 1050℃. The oxide thickness was measured by a well-calibrated ellipsometer at a wavelength of 632.8 nm with the refractive index set at 1.462.

Mask #1 defined the active regions and initial clean was performed again. Then, continued with DC magnetron sputtering hafnium on the wafers and oxidized them in furnace system. The thickness of as-deposit hafnium thin films was 20 Å which was read by the sensor inside the sputtering system. During sputtering, chamber pressure was maintained around 7.6×10^{-3} torr and the flow rate of Ar was 24 standard cubic centimeters per minute (sccm). The oxidation conditions were 200℃, 300℃, 400℃ and 500℃ respectively for 15 or 30 minutes, as shown in Table 3-1, with oxygen flow rate 5000 sccm. After oxidation process, pure aluminum was thermally evaporated on the top side of wafers.

Mask #2 defined the top electrode. Then, we used wet etching to etch undefined Al and HfO_2 films. After patterning, backside native oxide was stripped with diluted HF solution, and Al was deposited as bottom electrode. Finally, samples were sintered in pure N_2 at 400℃ in furnace for 30min to recover the process induced damages. The detailed fabrication process flow was listed as follows.

1. Initial RCA cleaning.

2. Thermally grow 5000Å wet oxide at 1050℃.

3. Mask #1：define active region and then RCA clean again.

4. DC magnetron sputtering hafnium 20 Å.

5. Thermal oxidize hafnium in furnace in an O_2 ambient at 200℃, 300℃, 400℃ and 500℃ respectively for 15 or 30 minutes.

5-1. RTA treatment at 850℃ for 30 seconds.

6. Thermally evaporate 5000 Å aluminum as top electrode.

7. Mask #2：define top electrode and then wet etch undefined Al and HfO_2 films.

8. Strip backside native oxide and coat 5000 Å aluminum as bottom electrode.

9. Al sintering in pure N_2 at 400℃ in furnace for 30min.

After the Al/HfO_2/Si MIS capacitors were prepared, we used semiconductor parameter analyzer (HP4156A) and C-V measurement (HP4284) to analysis electric characteristics (i.e. I-V, C-V, EOT, leakage current density etc.). Then we tested their reliability, including stress induced leakage current (SILC), constant current stress (CCS), constant voltage stress (CVS), Hysteresis effect.

3.2 Sputtering system

Four inch high purity hafnium target was used to deposit thin film by DC magnetron sputtering system. The sputtering conditions were as follows. In the DC sputtering process chamber, the wafers were mounted on a face-down holder which can rotate during deposition to increase film uniformity. The system was pumped down to 2×10^{-6} torr first. This process made the chamber clean enough and thus decreased the impurity of the deposited hafnium film. Then the deposition pressure was controlled at 7.6×10^{-3} torr. Before started to deposit hafnium, the surface of the hafnium target was treated by low power pre-sputtering cleaning for ten minutes. The inert gas source was argon (Ar) and its flow rate was 24 sccm. It has heavy atomic weight and could be served as a heavy iron to knock down the hafnium atoms on the target surface. Therefore, the hafnium atoms could be sputtered onto the wafers. The thickness of the deposited hafnium was read by the sensor inside the sputtering system. Then, the oxidation process of hafnium was performed by furnace system. The DC magnetron sputtering power was set at 120 W and the corresponding deposition rate was 0.3 Å/s. The thickness of hafnium films was 20 Å.

3.3 Furnace system

After hafnium had been deposited on silicon, we need an oxidation process to make it become hafnium dioxide. These Si wafers deposited with hafnium films were immediately loaded into furnace tube just as the sputtering process was finished. To start with, the tube temperature was set at 200℃, 300℃, 400℃ and 500℃ respectively as different process conditions and sufficient N_2 gas was purging continuously. After the tube temperature was stable in five minutes letter, N_2 gas was closed and O_2 gas was introduced. The oxygen gas flow rate was set at 5000 (sccm). We provided sufficient oxygen gas and proper time to oxidize these films.

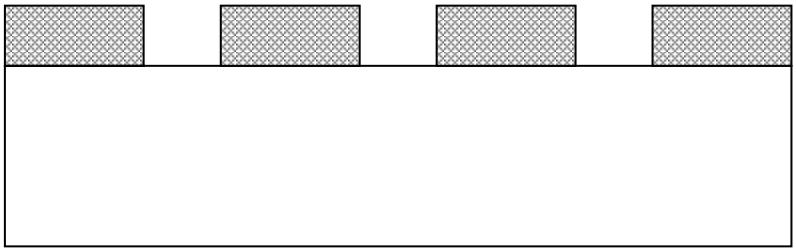
3.4 Rapid Thermal Annealing system

METAL RTA-AG 610 was a single-wafer lamp-heated and computer-controlled rapid thermal processing (RTP) system. Water and compressed dry air (CDA) cooling system were used to cool down the quartz chamber. High intensity visible radiation heating and cold-heating chamber walls allow fast wafer heating and cooling rate. The 12 tungsten-halogen lamps were distinguished into five groups, and the relative percentage of lamp intensity can be adjusted individually for each group to achieve uniform temperature distribution. Temperature was obtained from pyrometer and precise controlled by computer. Two gas lines were used in the system which can be switched between Ar and N_2.

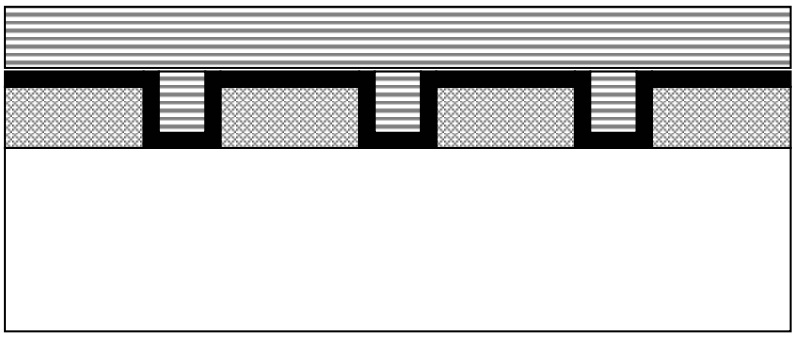
Before RTA process started, one minute N_2 gas purge was performed to minimize the water vapor introduced during wafer loading and also swept unwanted particles induced during process. A fast heating rate of 60℃/s was chosen in this work. When anneal was complete, chamber temperature was quickly cooled down from 850℃ to 500℃ by N_2 purge 30 seconds. Then, the chamber was slowly cooled down to 280℃ without N_2 purge to avoid creaking of films. After five minutes later, wafers can be taken out from the chamber. By two-steps-cooling method, films' creaks can be avoided

Wafer Number	Wafer Type	Oxidation Temperature (℃)	Oxidation Time (minute)
1	p-type	200	15
2		300	15
3	n-type	200	15
4		300	15
5	p-type	400	15
6			30
7		500	15
8			30
9	n-type	400	15
10			30
11		500	15
12			30

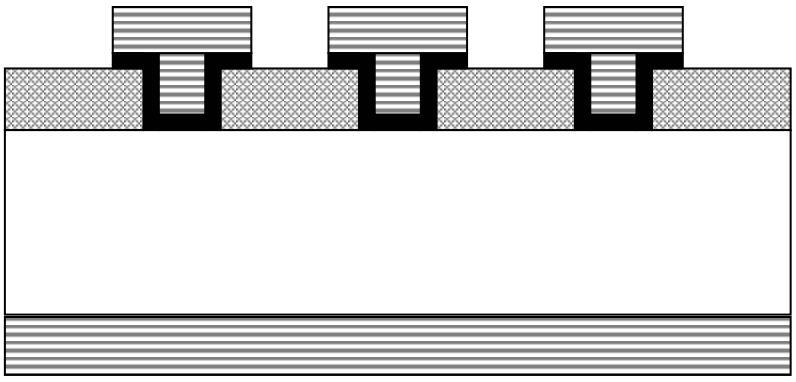
Table 3-1 The oxidation temperature and time of HfO_2 films.



1. Initial RCA clean.
2. Thermally grow 5000 Å wet oxide.
3. Mask #1：define active region and RCA clean.



4. Sputtering 20 Å hafnium.
5. Thermal oxidize hafnium films in furnace.
   (200℃, 300℃, 400℃ and 500℃ / 15 or 30 minutes)
   5-1. RTA treatment at 850℃ for 30 seconds.
6. Thermal coating 5000 Å aluminum on top.



7. Mask #2：pattern top electrode and etch Al and HfO_2.
8. Strip native oxide on backside and coat bottom Al electrode.
9. Al sintering (N_2_400℃_30min).

Figure 3-1 Fabrication flow chart of ultra thin HfO_2 MIS capacitor.

Chapter 4

Electrical Characteristics of Al/HfO_2/Si MIS Capacitors

4.1 Capacitance-Voltage Characteristics

In our experiments, we used HP2484A LCR meter to measure the 1MHz high frequency C-V characteristics of our MIS capacitors. We swept the gate bias from inversion region to accumulation region. There were three different die areas (i.e. 6.25×10^{-6}, 2.5×10^{-5} and 1×10^{-4} cm^2) for discussing area depend effects. In addition, the oxidation temperature was ranging from 200℃ to 500℃ with 15 or 30 minutes.

Table 4-1 shows the measurement results of HfO_2 capacitors under different process conditions with 6.25×10^{-6} cm^2 die area. Unfortunately, while the oxidation temperature is lower than 400℃, we only get the effective C-V characteristics of n-type HfO_2 capacitors under 300℃ 15minutes oxidation condition. The failure in quasi-static C-V measurement is due to the leakage current higher than the displacement current for most gate bias. Under such a low oxidation temperature, hafnium atoms may react with oxygen atoms to form HfO_2 but with very weak chemical bonding. We find that this weakly bonding type of HfO_2 layer couldn't bear much gate bias but it has an effective accumulation capacitance. It seems that n-type HfO_2 capacitors could have stronger chemical bonding than p-type HfO_2 capacitors under low oxidation temperature. Table 4-2 and 4-3 show the measurement results of HfO_2 capacitors with 2.5×10^{-5} cm^2 and 1×10^{-4} cm^2 die area respectively.

Fig. 4-1 shows the 1MHz high frequency C-V characteristics of p-type HfO_2 capacitors with different die area under 400℃-15 minutes oxidation condition. We could see that the capacitors with smaller die area have larger accumulation capacitance, but the size of die area doesn't influence the flat band voltage (V_{FB}). Besides, the slopes of these three C-V curves are almost the same. Fig. 4-2 shows the 1MHz high frequency C-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. Under 400℃-15 minutes oxidation condition, the capacitor has the largest accumulation capacitance and the smallest $|V_{FB}|$. The higher oxidation temperature and the longer oxidation time make the more negative flat band voltage shift. There exists several types of charges, including

interface trapped charge (Q_{it}), fixed oxide charge (Q_f), oxide trapped charge (Q_{ot}) and mobile ion (Q_m), in the dielectric layer and at the substrate interface. To simplify, we call all these charges as interface effective positive charge Q_i (C/cm^2). So, the flat band voltage can be expressed as follows：

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \gamma\frac{Q_m}{C_{ox}} - \gamma\frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}(\Phi_S)}{C_{ox}} \approx \Phi_{MS} - \frac{Q_i}{C_i}$$

The influence of Q_i is to introduce an equivalent negative charge within semiconductor. Because the work function difference and interface effective positive charge will both make the band near semiconductor surface bending downward, a negative voltage must be applied on metal to reach flat-band condition [1]. Thus, the more negative V_{FB} means more positive charges were produced at the interface during oxidation process. Fig. 4-3 shows C-V characteristics of three different gate dielectrics, including SiO_2, $(SiO_2)_{0.5}(Si_3N_4)_{0.5}$ and Si_3N_4 [2]. ΔV_{FB} for nitride and oxynitride devices with respect to oxide device are 0.15 and 0.04 V. Interfacial fixed charge is $7.5\times10^{11}/cm^2$ for nitride and $2\times10^{11}/cm^2$ for oxynitride. The fixed charge of the nitride film shows greater than oxynitride gate stack. This is due to increased bond-strain in the bulk and at internal dielectric interface. Increased bond-strain results in more “border traps”. Comparing fig. 4-2 to fig. 4-3, ΔV_{FB} for HfO_2 under 400℃-15 minutes oxidation condition with respect to SiO_2 device is about 0.2 V. This is because of more stress in the HfO_2 device, which generates more intrinsic defects, including bulk traps in film, border traps and interfacial traps. In addition, oxidation temperature affects ΔV_{FB} seriously. The higher oxidation temperature would cause more stress in the device and generate more intrinsic defects. It may be caused by our improper cool down process. These defects directly influence the quality of the insulator layer and the substrate interface (i.e. gate leakage, carrier mobility, reliability etc.). In addition, 400℃ oxidation temperature makes the slope of C-V curve apparently stepper than 500℃ oxidation temperature. It seems oxidation time doesn’t affect the slope of C-V curve. Consequently, for p-type HfO_2 capacitor, under 400℃-15 minutes oxidation condition could obtain the best C-V characteristics.

4.2 Equivalent Oxide Thickness (EOT)

From C-V characteristics, like fig. 4-1 and fig.4-2, equivalent oxide thickness (EOT) could be obtained by the following formula：

$$t_{ox} = \varepsilon_r \cdot \varepsilon_0 \cdot A / C$$

Where ε_r is the dielectric constant of SiO_2 ($\varepsilon_r = 3.9$), ε_0 is the permittivity in vacuum

(ε_0 = 8.85×10^{-14} F/cm). A is the area of the capacitors (A = 6.25×10^{-6}, 2.5×10^{-5} and 1×10^{-4} cm^2) and C is the accumulation capacitance measured at $|V_G - V_t| = 1$ V at 1 MHz. According to this formula, we could calculate all the electrical EOT of our capacitors, which listed in Table 4-1, 4-2 and 4-3. We see that n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 300℃-15 minutes oxidation condition have the smallest EOT of 9.2 Å. For p-type HfO_2 capacitors, with 6.25×10^{-6} cm^2 die area under 400℃-15 minutes oxidation condition have the smallest EOT of 17.3 Å. In addition, under the same oxidation condition, we find that p-type capacitors have smaller EOT than n-type capacitors. It might be attributed to that the diffusion rate of hafnium and oxygen atoms in n-type substrate is larger than in p-type substrate.

Fig. 4-4 shows EOT of p-type HfO_2 capacitors with different die areas. Under every different oxidation conditions, the devices with smaller die area have the smaller EOT. It is a very strange phenomenon. Devices with different die area on the same wafer under the same oxidation condition should have the same EOT. It is probably due to that the smaller die area attracts the larger ratio of edge charges around the device and thus has larger capacitance measured by HP4284, as shown in fig 4-1. If we eliminate the edge charge effect, the devices with different die area on the same wafer have the same EOT in fact. Fig. 4-5 shows EOT of p-type and n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. Higher oxidation temperature causes larger EOT of the device. Besides, longer oxidation time also slightly increase EOT of the device. The increase of EOT might result from the increase of interfacial layer which grown in the oxidation process. As shown in fig 4-6, during oxidation process, hafnium and oxygen atoms would diffuse to substrate and form an HfSiO interfacial layer. We will discuss the possible reasons of such EOT tendency by analyzing current-voltage characteristics.

4.3 Current-Voltage Characteristics

4.3.1 Leakage Current

Fig. 4-7 shows the J-V characteristics of p-type HfO_2 capacitors with different die areas (6.25×10^{-6}, 2.5×10^{-5} and 1×10^{-4} cm^2) under 400℃-15 minutes oxidation condition from 0 V to -1 V. We observed that the gate leakage current density becomes only a little larger while die area decreases. From table 4-1, 4-2 and 4-3, EOT of these three devices are 17.3 Å, 21.0 Å and 22.3 Å respectively. Fig. 4-8 shows J-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions (400℃-15 minutes, 400℃-30 minutes, 500℃-15

minutes and 500℃-30 minutes) from 0 V to -1 V. The EOT of these four devices are 17.3 Å, 17.4 Å, 23.8 Å and 23.9 Å respectively. Apparently, the device under higher oxidation temperature and longer oxidation time has lower gate leakage current. In fig. 4-7, 5 Å increase of EOT (from 17.3 Å to 22.3 Å) only reduces a little gate leakage at V_G = -1 V. But in fig. 4-8, 6.5 Å increase of EOT (from 17.3 to 23.8 Å) reduces gate leakage even more than 2 orders at V_G = -1 V. Thus, from fig. 4-7, three similar magnitudes of gate leakage reveal that the thickness of devices with three different die area on the same wafer might be the same. As shown in fig. 4-8, the main reason of such a large repression of gate leakage between 400℃-15 minutes and 500℃-15 minutes oxidation conditions is the increase of thickness. Higher oxidation temperature could also make HfO_2 film have stronger chemical bonding to effectively resist gate leakage. Besides, the devices under 500℃-15 minutes (EOT = 23.8) and 500℃-30 minutes (EOT = 23.9) oxidation condition have almost the same thickness but have about an order difference of gate leakage at V_G = -1 V. Thus, the longer oxidation time mainly increases the intensity of chemical bonding.

Fig. 4-9 shows measured and simulated J-V characteristics of NMOSFET with SiO_2 gate insulator. Gate leakage current density of 20 Å SiO_2 gate insulator at V_G = 1 V is about 3×10^{-2} A/cm^2. From fig.4-9, however, gate leakage current density of the HfO_2 capacitor with EOT = 17.3 Å at V_G = -1 V is only about 3×10^{-4} A/cm^2. Even thinner EOT of HfO_2 capacitor but has less gate leakage than SiO_2 device about 2 orders. Consequently, replacing SiO_2 with HfO_2 for gate insulator could effectively reduce gate leakage.

Then, we make plots of gate leakage versus EOT for further discussing. As shown in fig. 4-10, we could obviously find that, whether for n-type or for p-type HfO_2 capacitors, gate leakage at $|V_g|$ = 1 V of different die areas are almost the same, even if their EOT are not the same. With the increase of EOT, however, the gate leakage doesn't decrease. Consequently, we think the EOT of devices with different die areas on the same wafer should be the same in fact. From fig. 4-11, we observe that, whether for n-type or for p-type HfO_2 capacitors, while the oxidation temperature rises, the EOT becomes larger and the leakage becomes less. Higher oxidation temperature makes the HfSiO interfacial layer become thicker, as shown in fig. 4-6. The thicker interfacial layer causes the larger EOT of HfO_2 gate insulator. Higher oxidation temperature also makes the chemical bonding stronger. Thicker physical thickness and stronger chemical bonding both contribute to the decrease of gate leakage current. Longer oxidation time slightly increases EOT and decreases gate leakage current. In addition, another interesting phenomenon is that under the same

oxidation condition, n-type HfO_2 capacitor has larger EOT but larger gate leakage current than p-type HfO_2 capacitor. The larger EOT might result from the larger diffusion rate of hafnium in company with oxygen atoms in n-type substrate than in p-type substrate. Generally, the device with larger EOT has less leakage current. Thus, we think the HfO_2 layer grown on p-type substrate has better quality of resisting gate leakage than on n-type substrate.

Fig.4-12 shows J-V characteristics of n-type and p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area from -1 V to +1 V. For p-type, the leakage current under positive gate bias is much lower than negative case by 3 orders. For n-type, the leakage current under negative gate bias is lower than positive case by 1 order. The reverse leakage is thought to be dominated by surface leakage [3]. The surface generation current has been reported to be linearly correlated to the interface state density [4]. These interface states are caused by the dangling bonds at the Si/SiO_2 interface [5][6]. This component is often masked by surface leakage, especially at low temperatures [7][8]. This is illustrated in fig. 4-13.

Fig. 4-14 shows J-V characteristics of n-type HfO_2 capacitors with different die areas under 400℃-30 minutes oxidation condition from 0 V to +10 V. In this figure, we could see the devices with 6.25×10^{-6}, 2.5×10^{-5} and 1×10^{-4} cm^2 die area, generate breakdown at V_G = 3.85 V, 3.50 V and 3.10 V respectively. The device with smallest die area has the biggest breakdown voltage (V_{BD}), which means the best quality of resisting leakage current. We think more ratio of leakage current could pass through the gate insulator from edge side between HfO_2 layer and isolation oxide in the device with smaller die area. The leakage current which doesn't pass through HfO_2 layer doesn't destroy the structure of HfO_2 layer. Thus, the device with less ratio of leakage current passing through the HfO_2 layer could have larger breakdown voltage. Fig.4-15 shows J-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions (400℃-15 minutes, 400℃-30 minutes, 500℃-15 minutes and 500℃-30 minutes), correspond separating EOTs with 17.3 Å, 17.4 Å, 23.8 Å and 23.9 Å, from 0 V to -10 V. Breakdown voltages of these four devices are -6.05 V, -6.30 V, -7.15 V and -7.50 V. We could find that the device with thinner thickness and weaker chemical bonding generates breakdown more easily. In addition, like SiO_2, thicker HfO_2 shows more abrupt breakdown characteristics compared to thinner HfO_2.

Fig. 4-16 displays gate current as a function of the gate voltage for four oxide degradation stages in a 2000 μm^2 SiO_2 NMOSFET. After SBD, a large increase of the

substrate current is observed in the whole voltage range [9]. Fig. 4-17 shows four oxide degradation stages of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 400℃ 15 minutes oxidation condition. Like SiO_2 NMOSFET, HfO_2 capacitor has four degradation stages. This hints HfO_2 might have similar breakdown mechanism with SiO_2.

4.3.2 Band-gap Diagram and Conduction Mechanism

Selecting a gate dielectric with a higher permittivity than that of SiO_2 is an essential choice. The required permittivity must also be balanced against barrier height to limit tunneling. For electrons traveling from the silicon substrate to the gate, this barrier is the conduction band offset, ΔE_C. A gate dielectric must have a sufficient ΔE_C value to poly-Si, and to other gate materials, in order to obtain low off-state currents (leakage). If the experimental ΔE_C is < 1.0 eV, it will likely preclude the oxide's use in gate dielectric applications because thermal emission or tunneling would lead to unacceptably high leakage currents [10]. Among the several materials that have been investigated as gate dielectrics, as shown in Table 1-3, the dielectric constant generally exhibits an inverse relationship to the energy band gap.

Fig. 4-18 shows the energy band diagram of the SiO_2 MIS capacitor with Al gate. The energy band gap of SiO_2 is 8.9 eV. Fig. 4-19 shows the energy band diagram of the HfO_2 MIS capacitor with Al gate. The energy band gap of HfO_2 is 5.7 eV [10]. The electron affinity 2.82 eV for HfO_2 is obtained from the measurement of Fowler-Nordheim tunneling current of metal/ HfO_2/Si MIS capacitors [11]. Taking the work function of Al as $\Phi_{Al} = 4.1$ eV, the barrier height of Al/ HfO_2 is $\Phi_{Al/\ HfO_2} = 1.28$ eV and the barrier height of HfO_2/Si is $\Phi_{Si/\ HfO_2} = 1.13$ eV.

There are many possible conduction mechanisms in insulators [12]. For SiO_2, the dominate conduction mechanism was believed to be Fowler-Nordheim tunneling in the medium field (6~10MV/cm), low temperature region (T＜200℃) [13]. As the thickness scales down, it would show the direct tunneling characteristics [14]. The weak temperature dependence of this tunneling process is well-known. The schematic illumination of conduction mechanism is shown in fig. 4-20, including Schottky emission, F-N tunneling, and Frenkel-Poole emission.

The leakage current governed by the Schottky emission is as following:

$$J_{SK} = A^* T^2 \exp\{ -q[\varphi_B - (qE / 4\pi\varepsilon_o\varepsilon_d)^{1/2}] / kT \}$$

where A* is a constant, φ_B is the potential height on the surface, E is the electric field, ε_0 is the permittivity in vacuum, ε_d is the dynamic dielectric constant, T is the temperature, and k is the Boltzmann constant. Fig. 4-21 shows the Schottky plot of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. The gray filled circles on each curve indicate where the individual slope of the curves becoming constant, which means the generation of Schottky emission happened. For the substrate electron injection case, the experimental results fit the Schottky emission theory well. While electric field is between 1 MV/cm to 16 MV/cm, the fitting slopes are almost constant. N-type HfO_2 capacitors under 300℃-15 minutes oxidation condition begins to generate Schottky emission at V_G = 0.09 V. Even for n-type capacitors under 500℃-30 minutes oxidation condition, which have largest EOT, Schottky emission occurs at very low bias V_G = 0.82 V.

Fowler-Nordheim (FN) tunneling is the flow of electrons through a triangular potential barrier illustrated in fig. 4-20. Tunneling is a quantum mechanical process similar to throwing a ball against a wall often results that the ball goes through the wall without damaging the wall or the ball. It also loses no energy during the tunnel event. The probability of this event happening, however, is extremely low, but an electron incident on a barrier typically several nm thick has a high probability of transmission. The FN current (I_{FN}) is given by the expression [15]:

$$I_{FN} = A_G A \varepsilon_{ox}^2 \exp\left(\frac{-B}{\varepsilon_{ox}}\right)$$

where the A_G is the gate area, ε_{ox} is the oxide electric field, and A and B are usually considered to be constants. A and B are given as the following:

$$A = \frac{q^3\left(m/m_{ox}\right)}{8\pi h\Phi_B} = 1.54\times10^{-6}\frac{\left(m/m_{ox}\right)}{\Phi_B}\left[\frac{A}{V^2}\right]$$

$$B = \frac{8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qh} = 6.83\times10^7\sqrt{\left(m_{ox}/m\right)\Phi_B^3}\left[\frac{V}{cm}\right]$$

where m_{ox} is the effective electron mass in the oxide, m is the free electron mass, and Φ_B is the barrier height at the silicon-oxide interface given in units of eV in the expression for B. Φ_B is actually an effective barrier height that take into account barrier height lowering and quantization of electrons at the semiconductor surface. Rearranging I_{FN} formula gives by:

$$\ln\left(\frac{I_{FN}}{A_G \varepsilon_{ox}^2}\right) = \ln\left(\frac{J_{FN}}{\varepsilon_{ox}^2}\right) = \ln(A) - \frac{B}{\varepsilon_{ox}}$$

A plot of $\ln(J_{FN}/\varepsilon_{ox}^2)$ versus $1/\varepsilon_{ox}$ should be a straight line if the conduction through the oxide is pure Fowler-Nordheim conduction [15]. The slop of linear F-N plot gives A and the intercept yields B. Fig. 4-22 shows F-N plot of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. The gray filled circles on each curve indicate the slopes of the each curves becoming constant, which means the generation of F-N tunneling happened. N-type HfO_2 capacitors under 300℃-15 minutes oxidation condition begins to generate F-N tunneling at V_G = 1.42 V. We could find that device with thinner EOT generates F-N tunneling at smaller gate bias. It is consistent with our prediction.

The leakage current governed by Frenkel-Poole emission is as following:

$$J_{FP} = B \cdot E \cdot \exp\{ -q[\varphi_t - (qE / \pi\varepsilon_o\varepsilon_d)^{1/2}] / kT \}$$

where B is a constant, φ_t is the barrier height of trap level. The Frenkel-Poole emission is due to the field-enhanced thermal excitation of trapped electrons into the conduction band. Fig. 4-23 shows Frenkel-Poole plot of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation condition. The gray filled circles on each curve indicate the slopes of the curves becoming constant, which means the generation of Frenkel-Poole emission happened. N-type HfO_2 capacitors under 300℃-15 minutes oxidation condition begins to generate Schottky emission at V_G = 0.21 V. While electric field is between 4 MV/cm to 16 MV/cm, the fitting slopes are almost constant, indicating Frenkel-Poole emission is one conduction mechanism of leakage current. Even for n-type capacitors under 500℃-30 minutes oxidation condition, which have largest EOT, Schottky emission occurs at very low bias V_G = 0.92 V. From above, we could find that Schottky emission occurs at very low gate bias and F-N tunneling occurs at higher gate bias than both Schottky emission and Frenkel-Poole emission. In addition, n-type HfO_2 capacitors under 300℃-15 minutes oxidation condition always generate Schottky emission, F-N tunneling or Frenkel-Poole emission happened earliest because of smallest EOT.

4.4 RTA Treatment

In our experiments, after oxidation process, we could have an additional RTA treatment at 850℃ for 30 seconds to HfO_2 film. Fig. 4-24 shows 1MHz high

frequency C-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die areas under 400℃-15 minutes oxidation condition without / with RTA. The device with RTA treatment has smaller accumulation capacitance and smaller slope of C-V curve than without RTA treatment. Fig. 4-25 shows J-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die areas under 400℃-15 minutes oxidation condition without / with RTA. The device with RTA treatment has larger leakage current than without RTA treatment. From above results, we know that RTA treatment couldn't improve the quality of HfO_2 film in J-V and C-V characteristics. This is due to HfO_2 is unit-combined structure and thus couldn't be enhanced the value of dielectric constant by RTA treatment. In the other hand, high-k material, like Ta_2O_5, which isn't unit-combined structure could be enhanced the value of dielectric constant by RTA treatment [16]. In addition, when the temperature rises to 800℃～900℃, HfO_2 would change the lattice structure from amorphous type to polycrystalline type and thus increase gate leakage current. Consequently, we don't suggest using RTA treatment to HfO_2 film.

4.5 References

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Wafer Type	Oxidation Temperature & Time	200℃ 15min	300℃ 15min	400℃ 15min	400℃ 30min	500℃ 15min	500℃ 30min
P	**EOT**	N/A	N/A	17.3	17.4	23.8	23.9
	Jg (A/cm^2) @ -1 V			2.3×10^{-4}	1.9×10^{-4}	8.8×10^{-7}	8.6×10^{-8}
N	**EOT**	N/A	9.2	21.8	21.9	24.3	25.5
	Jg (A/cm^2) @ 1 V		7.8×10^{-2}	8.0×10^{-4}	8.0×10^{-4}	1.1×10^{-6}	7.8×10^{-7}

Table 4-1 Measurement results of HfO_2 capacitors with 6.25×10^{-6} cm^2 die area.

Wafer Type	Oxidation Temperature & Time	200℃ 15min	300℃ 15min	400℃ 15min	400℃ 30min	500℃ 15min	500℃ 30min
P	**EOT**	N/A	N/A	21.0	21.4	29.1	29.9
	Jg (A/cm^2) @ -1 V			2.1×10^{-4}	1.7×10^{-4}	1.9×10^{-6}	2.2×10^{-7}
N	**EOT**	N/A	11.3	27.4	28.6	31.3	33.4
	Jg (A/cm^2) @ 1 V		5.9×10^{-2}	1.0×10^{-3}	8.0×10^{-4}	3.0×10^{-6}	8.4×10^{-7}

Table 4-2 Measurement results of HfO_2 capacitors with 2.5×10^{-5} cm^2 die area.

Wafer Type	Oxidation Temperature & Time	200℃ 15min	300℃ 15min	400℃ 15min	400℃ 30min	500℃ 15min	500℃ 30min
P	**EOT**	N/A	N/A	22.3	23.2	30.3	32.0
	Jg (A/cm^2) @ -1 V			2.0×10^{-4}	1.6×10^{-4}	3.5×10^{-6}	4.4×10^{-7}
N	**EOT**	N/A	13.2	28.9	29.8	33.7	36.4
	Jg (A/cm^2) @ 1 V		4.8×10^{-2}	1.3×10^{-3}	1.1×10^{-3}	1.0×10^{-5}	2.3×10^{-6}

Table 4-3 Measurement results of HfO_2 capacitors with 1×10^{-4} cm^2 die area.

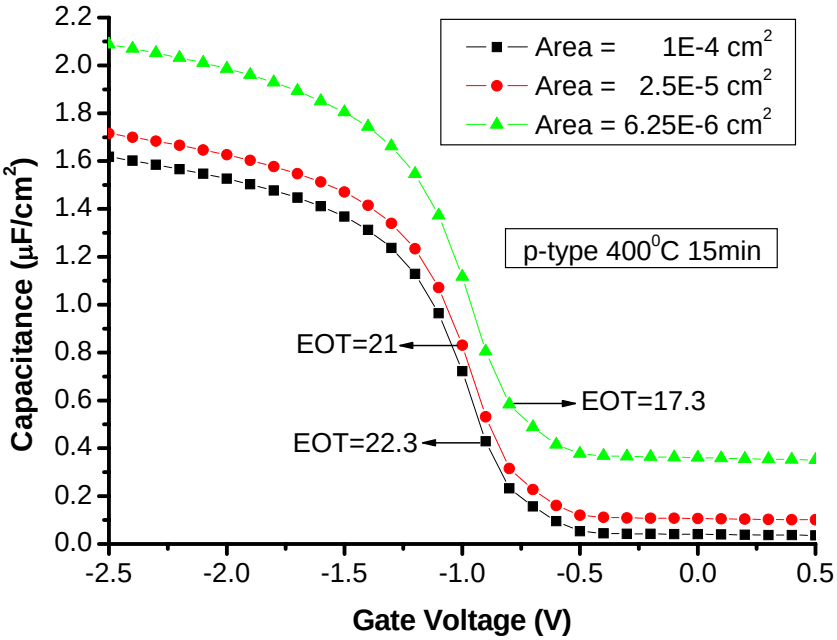


Fig. 4-1 1MHz high frequency C-V characteristics of p-type HfO_2 capacitors with different die areas under 400℃ 15 minutes oxidation condition.

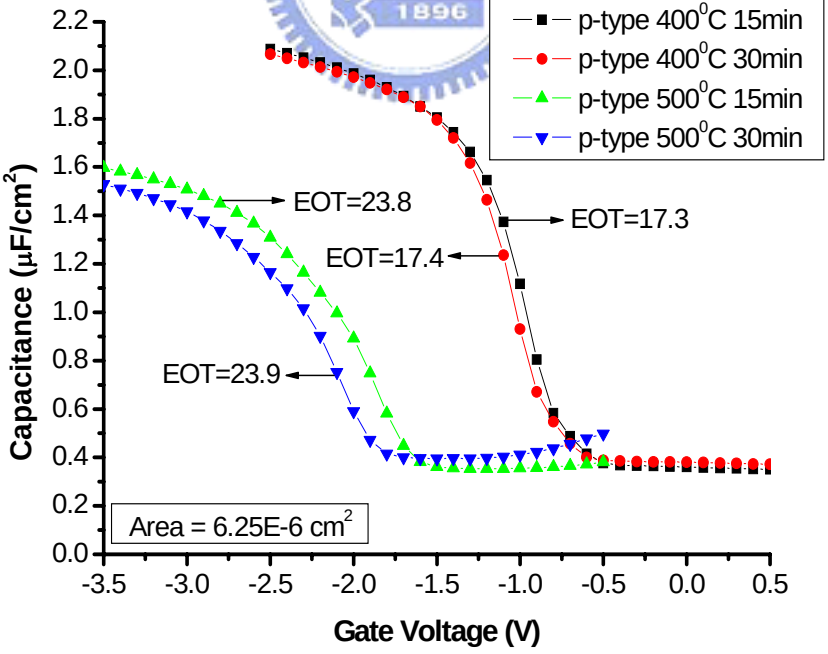


Fig. 4-2 1MHz high frequency C-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions.

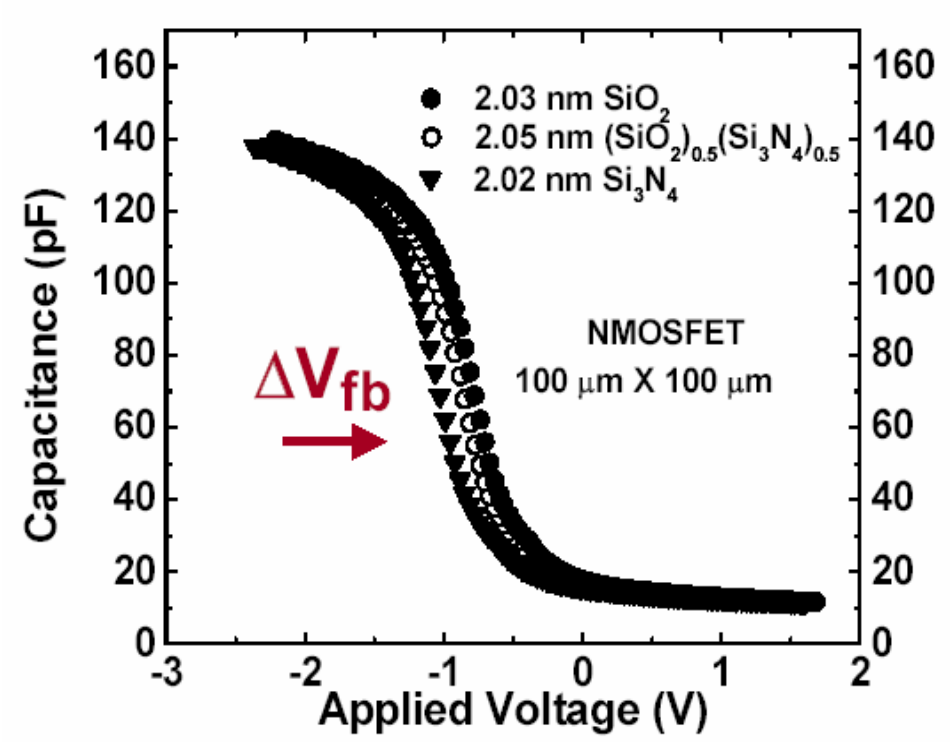


Fig. 4-3 C-V characteristics of SiO_2, $(SiO_2)_{0.5}(Si_3N_4)_{0.5}$ and Si_3N_4 NMOSFET. (Gerry Lucovsky, NC State University, 2003)

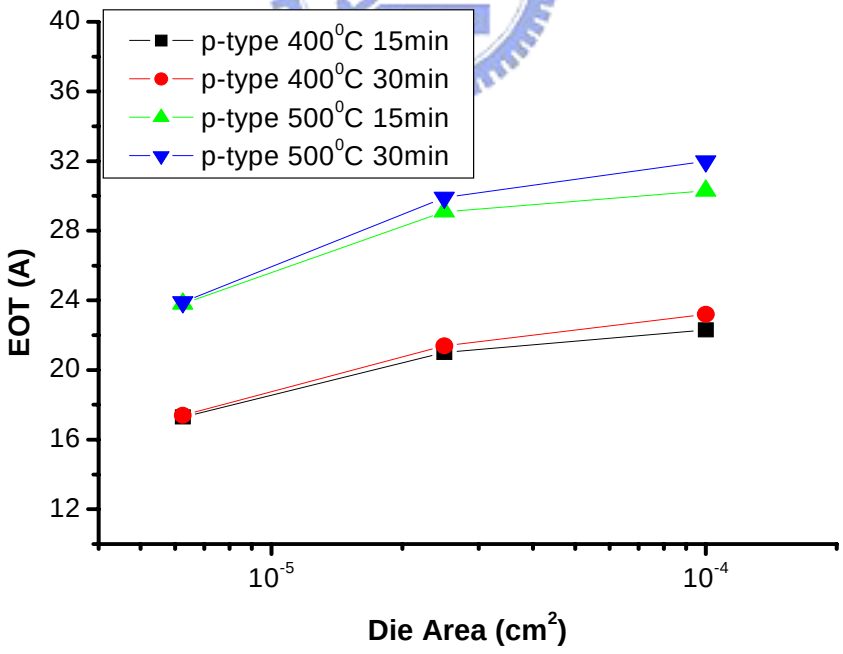


Fig. 4-4 EOT of p-type HfO_2 capacitors with different die areas.

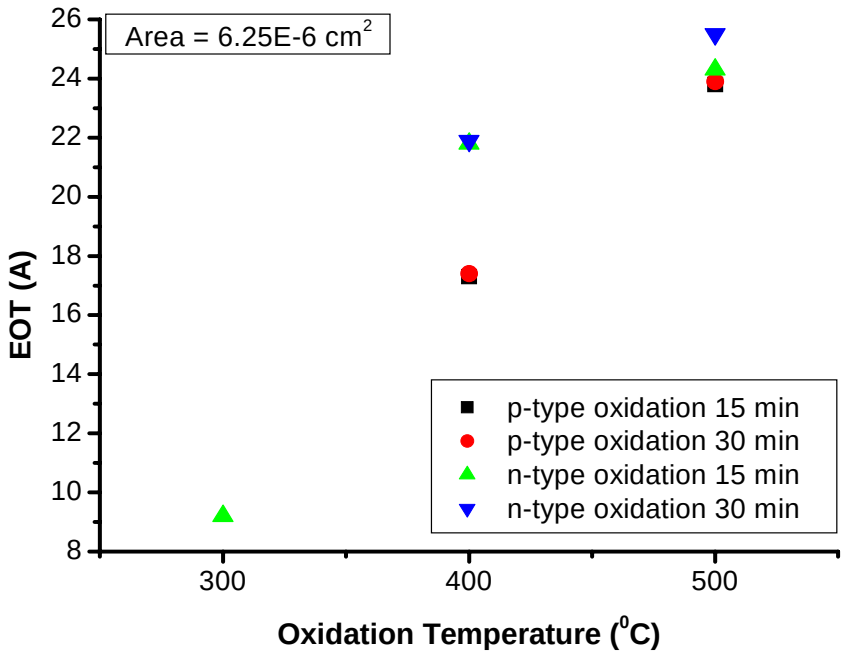


Fig. 4-5 EOT of p-type and n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions.

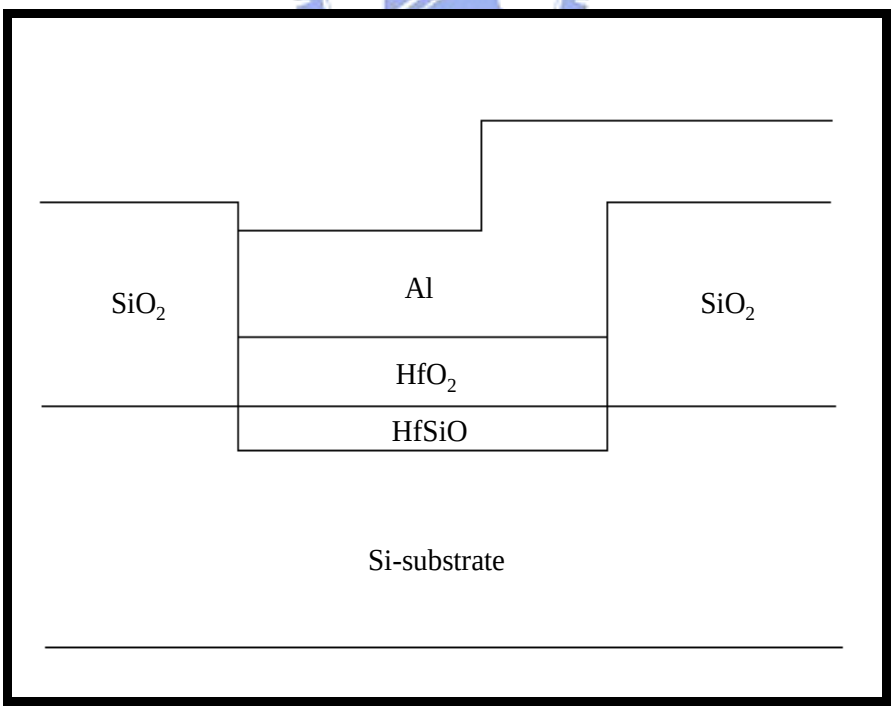


Fig. 4-6 Illustration of HfO2 capacitor.

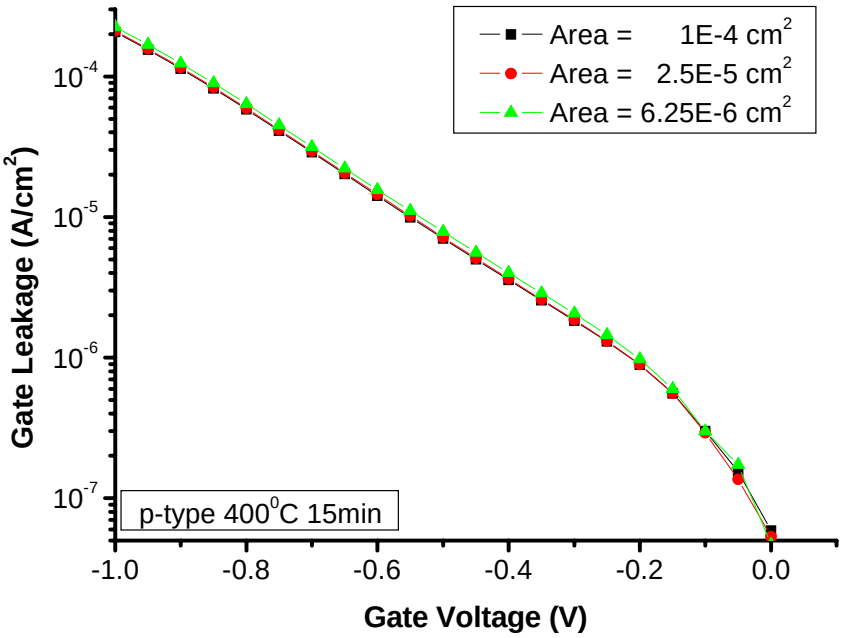


Fig. 4-7 J-V characteristics of p-type HfO_2 capacitors with different die areas under 400℃ 15 minutes oxidation condition from 0 V to -1 V.

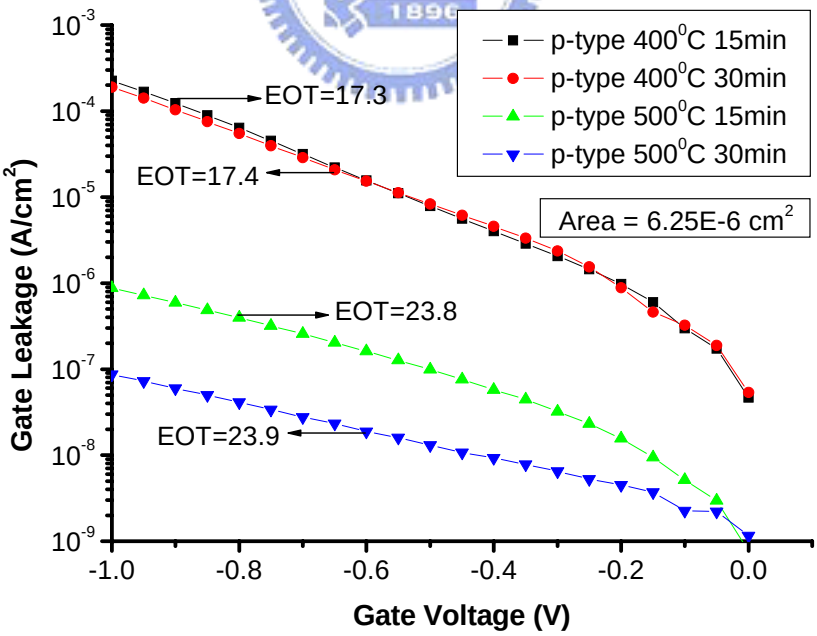


Fig. 4-8 J-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions from 0 V to -1 V.

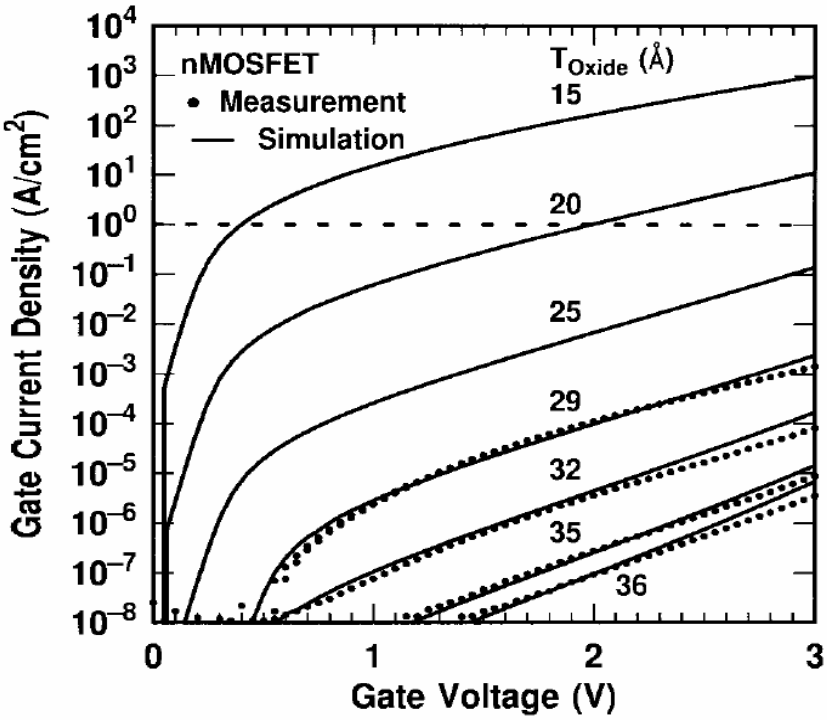


Fig. 4-9 Measured and simulated J-V characteristics of NMOSFET with SiO_2 gate insulator. The dotted line indicates the 1 A/cm^2 limit for leakage current. (S. H. Lo, et. al (IBM), IEEE EDL 1997)

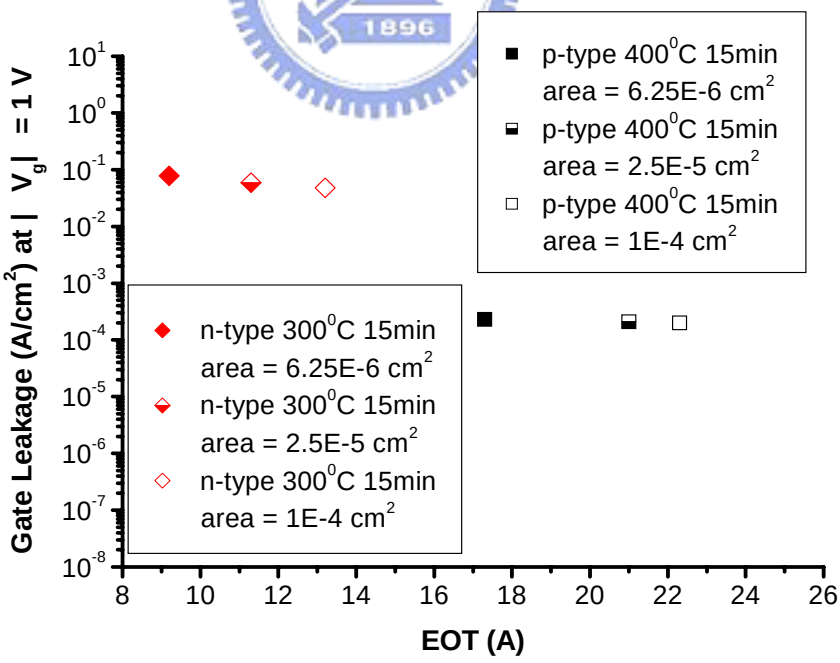


Fig. 4-10 Gate leakage at ｜Vg｜= 1 V of n-type and p-type HfO_2 capacitors with different die area.

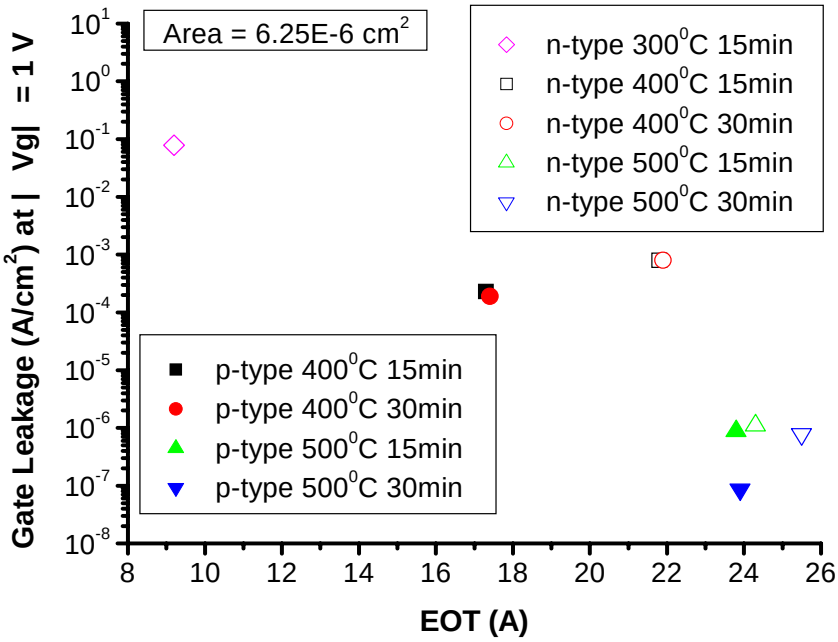


Fig. 4-11 Gate leakage at ｜Vg｜= 1 V of n-type and p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation condition.

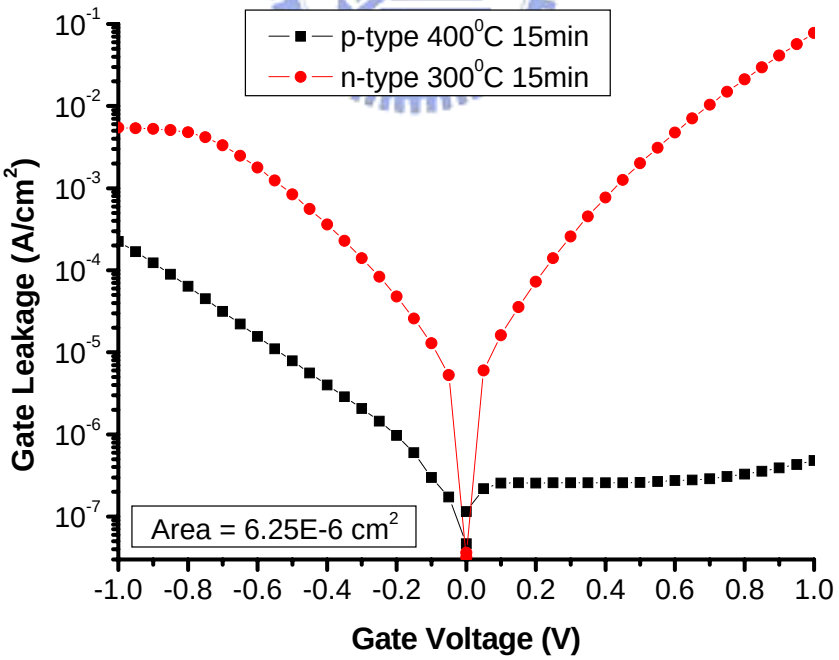
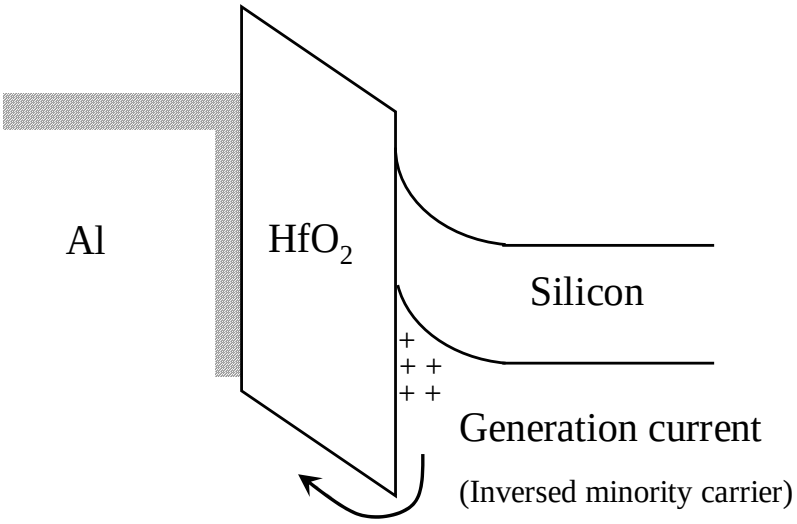
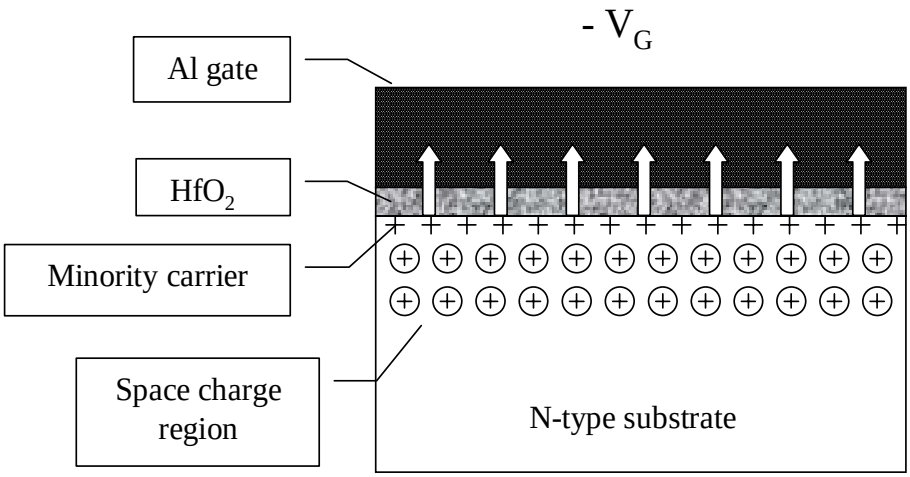


Fig. 4-12 J-V characteristics of n-type and p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area from -1 V to +1 V.



(a)



(b)

Fig. 4-13 Illumination of leakage current under negative bias. (a) energy band diagram (b) cross-section view

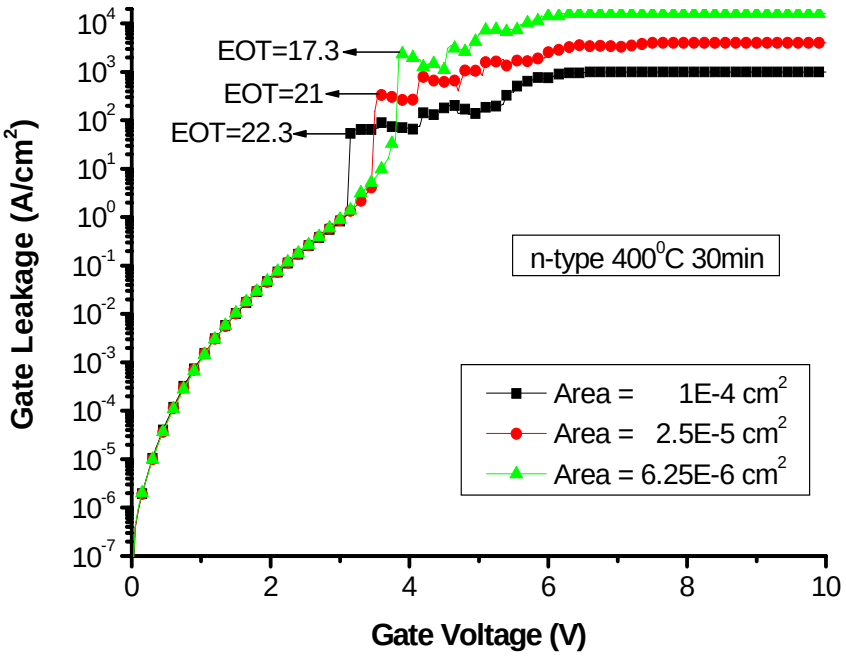


Fig. 4-14 J-V characteristics of n-type HfO_2 capacitors with different die areas under 400℃ 15 minutes oxidation condition from 0 V to +10 V.

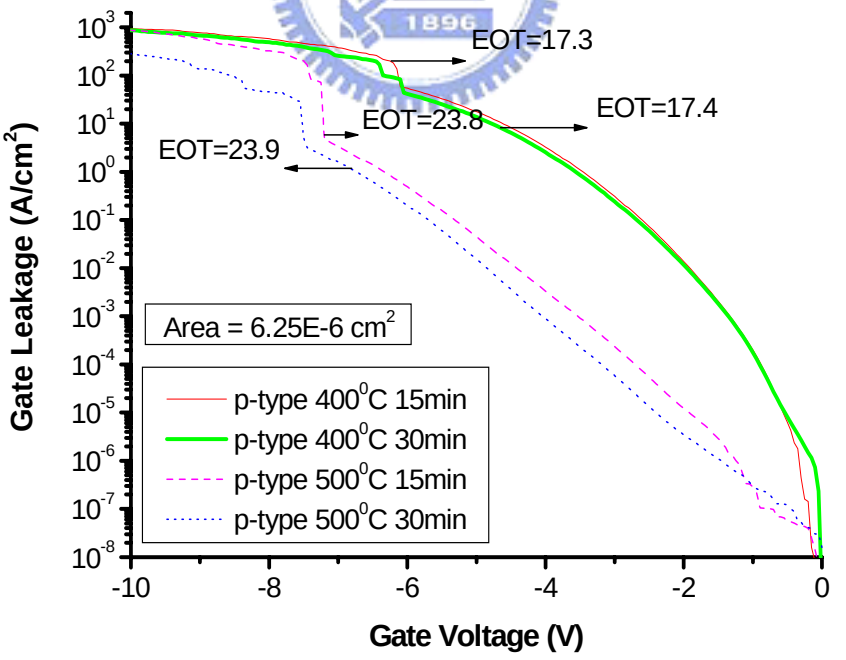


Fig. 4-15 J-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions from 0 V to -10 V.

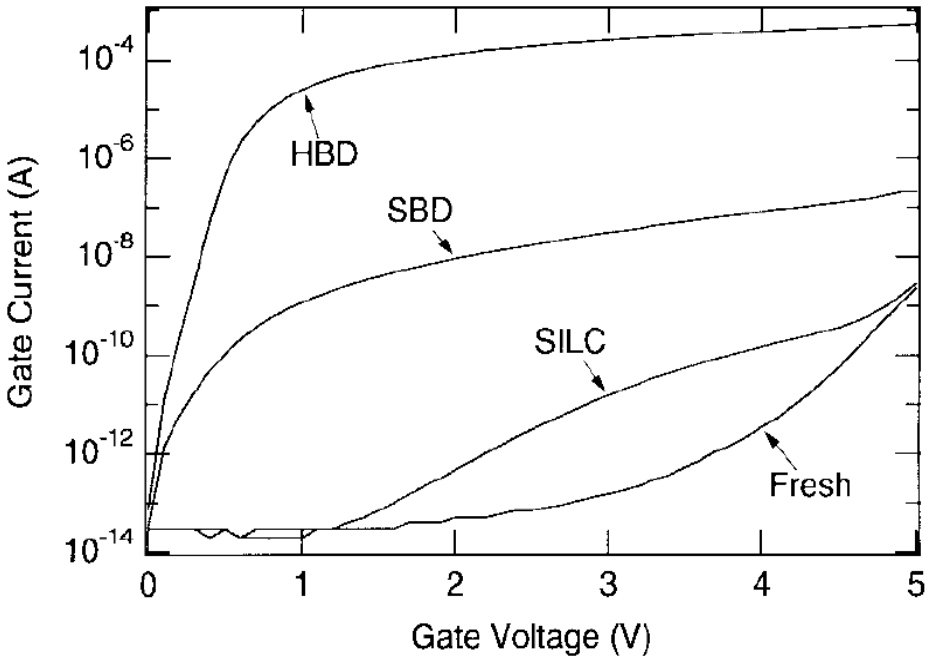


Fig. 4-16 Gate current as a function of the gate voltage for four oxide degradation stages in a 2000 μm^2 SiO_2 NMOSFET. After SBD, a large increase of the substrate current is observed in the whole voltage range. (Felice Crupi, et. al, IEEE Transactions on Electron Devices, 1998)

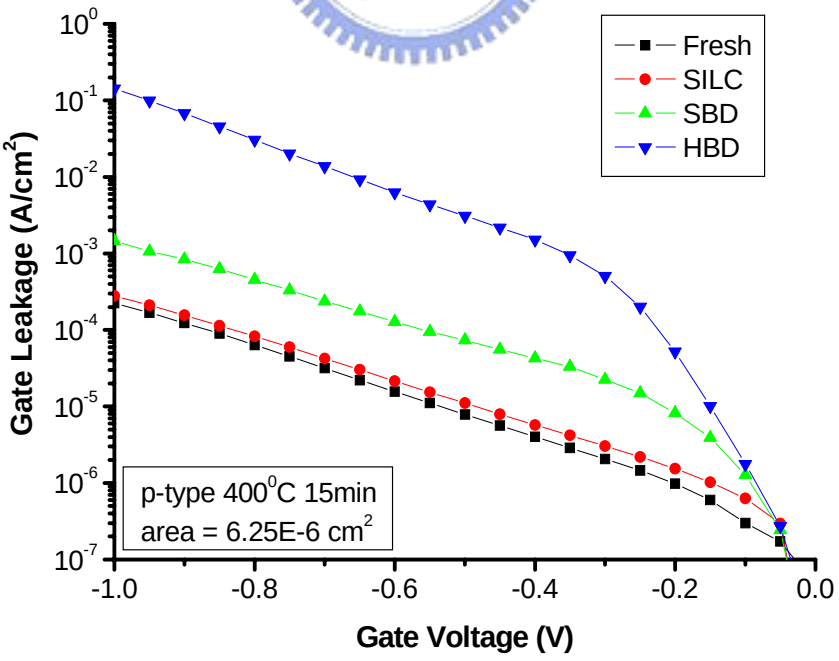


Fig. 4-17 Four oxide degradation stages of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 400℃ 15 minutes oxidation condition.

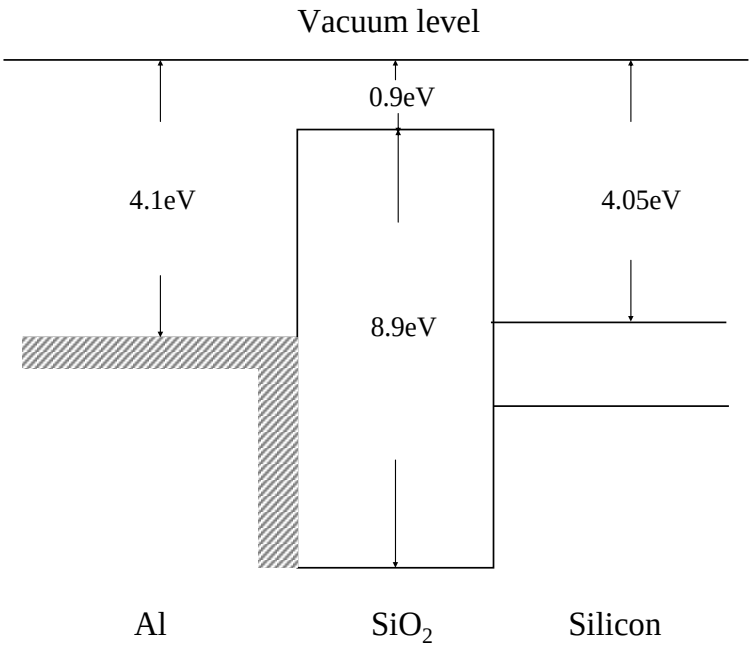


Fig. 4-18 Energy band diagram of SiO_2 capacitors with Al gate.

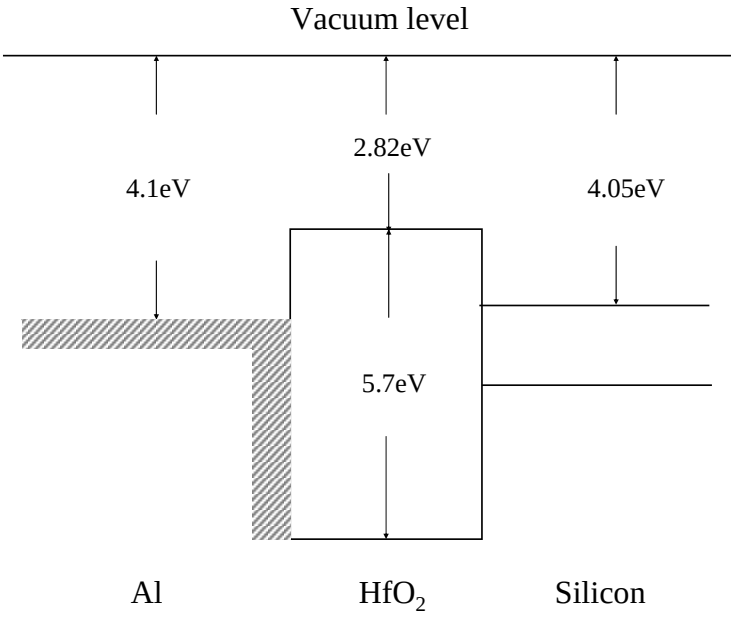


Fig. 4-19 Energy band diagram of HfO_2 capacitors with Al gate.

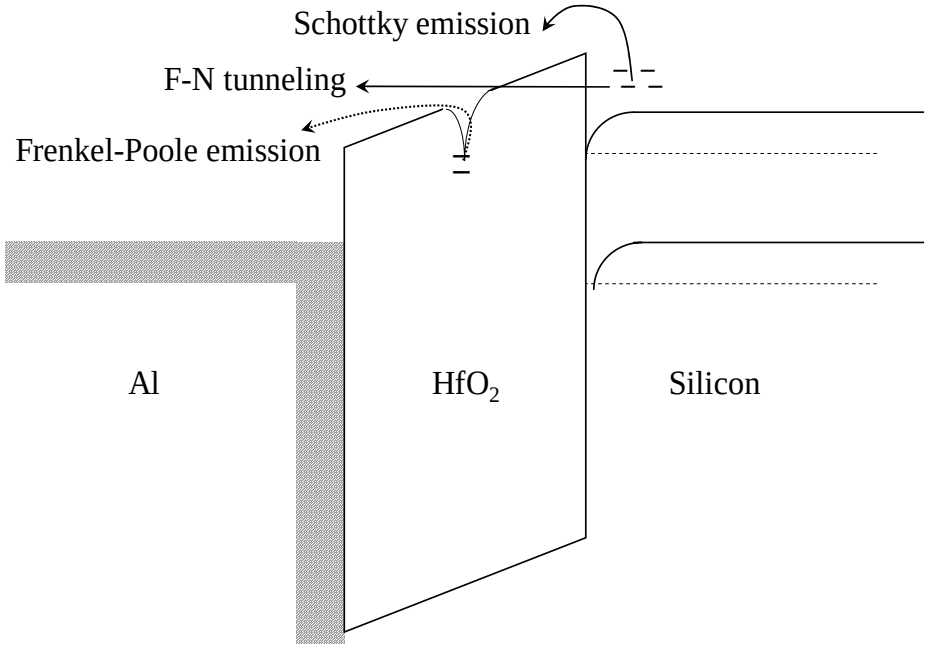


Fig. 4-20 Conduction mechanism in the oxide for MIS structure.

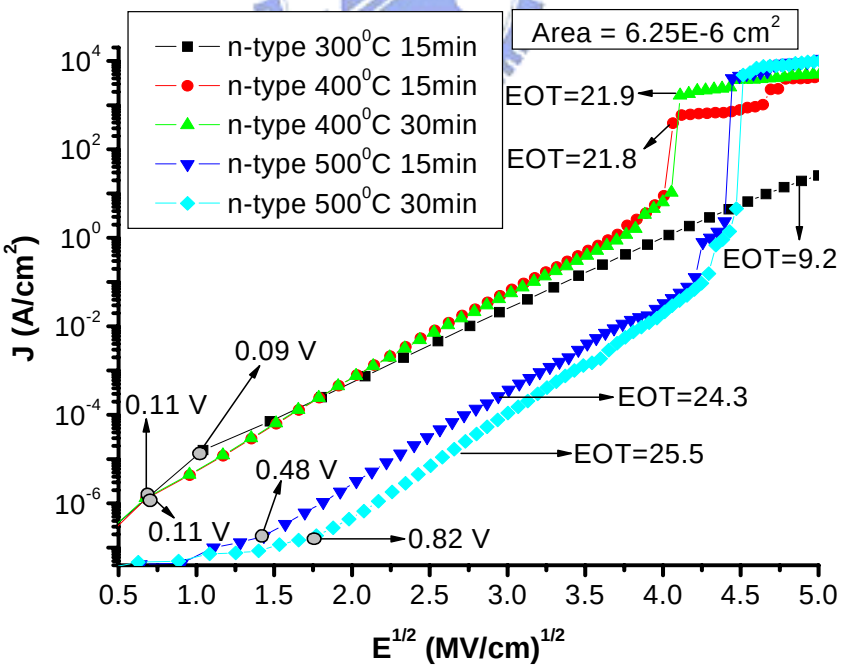


Fig. 4-21 Schottky plot of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation condition.

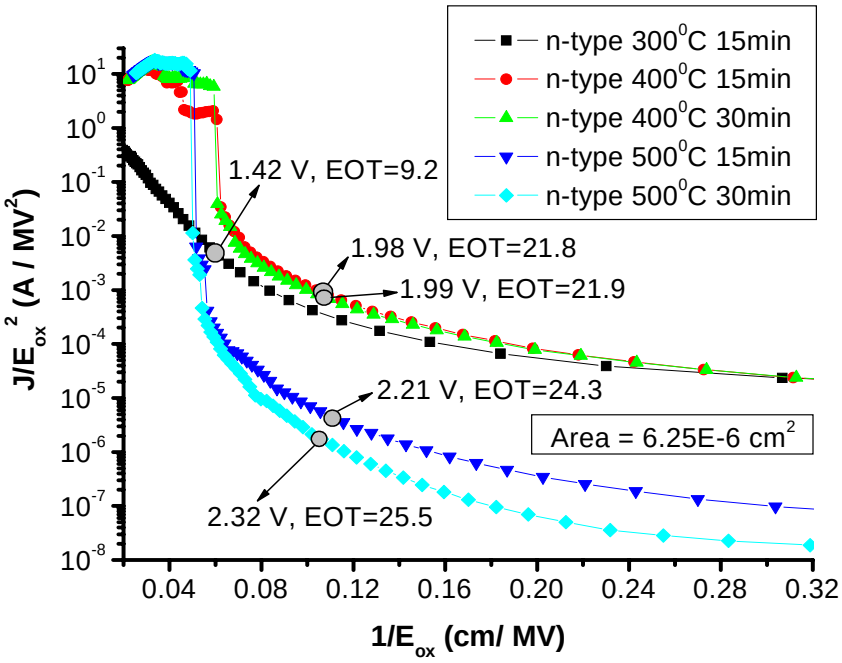


Fig. 4-22 Fowler-Nordheim plot of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation condition.

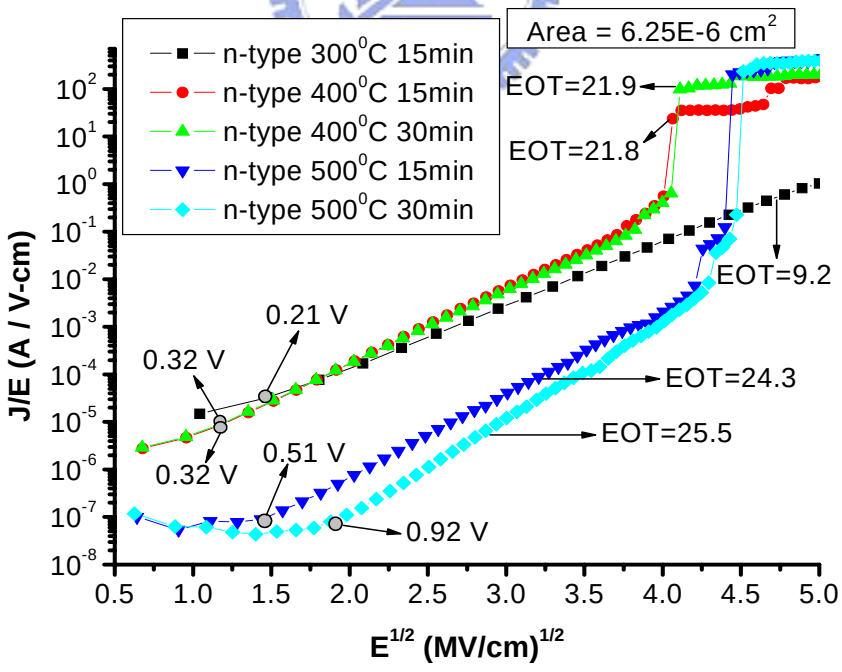


Fig. 4-23 Frenkel-Poole plot of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation condition.

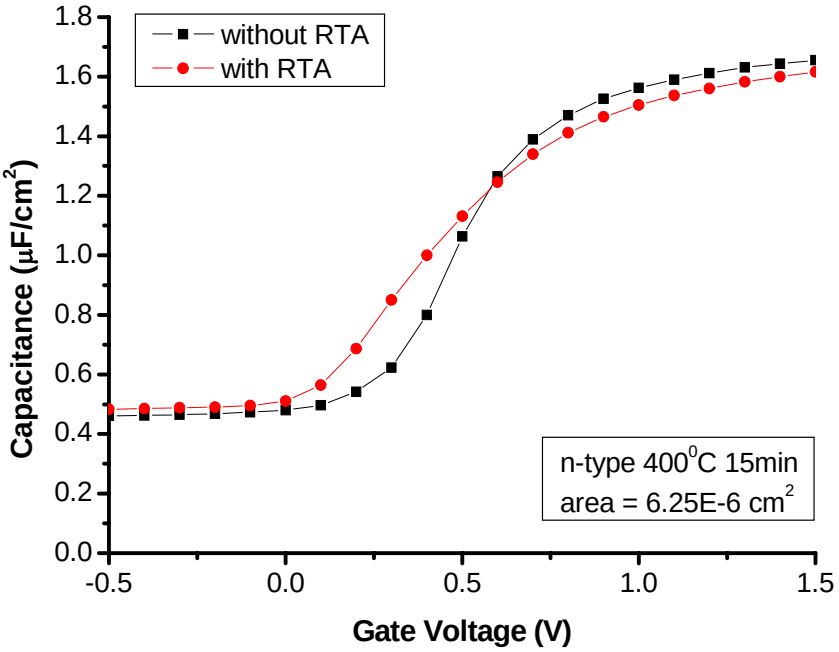


Fig. 4-24 1MHz high frequency C-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die areas under 400℃ 15 minutes oxidation condition without / with RTA.

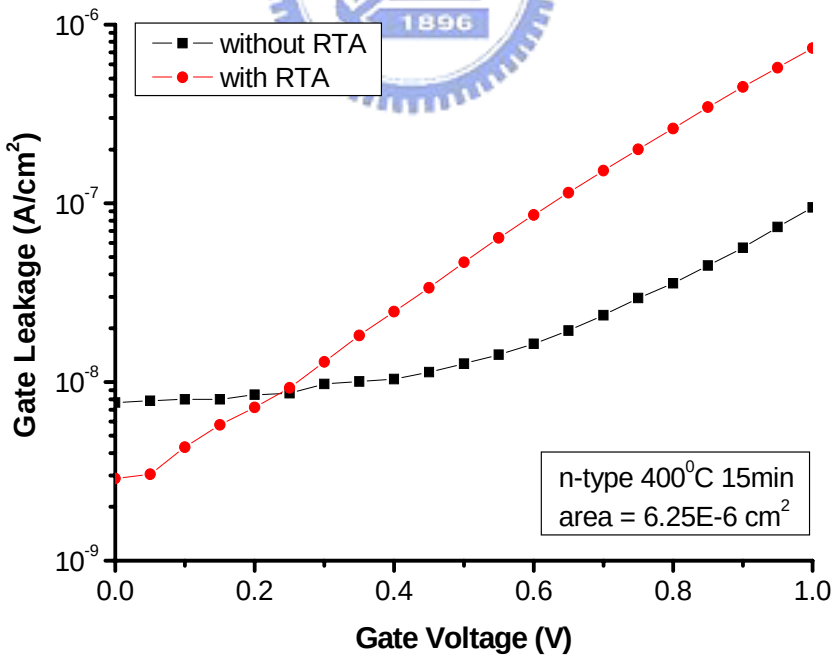


Fig. 4-25 J-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die areas under 400℃ 15 minutes oxidation condition without / with RTA.

Chapter 5

Reliability of Al/HfO_2/Si MIS Capacitors

5.1 Hysteresis

When a ferromagnetic material is magnetized in one direction, it will not relax back to zero magnetization when the applied magnetizing field is removed. It must be driven back to zero by the additional opposite direction magnetic field. If an alternating magnetic field is applied to the material, its magnetization will trace out a loop called a hysteresis loop. The lack of retrace ability of the magnetization curve is the property called hysteresis and it is related to the existence of magnetic domains in the material. Once the magnetic domains are reoriented, it takes some energy to turn them back again [1].

The hysteresis phenomenon is similar in the C-V curve of the MIS capacitor device. Fig. 5-1 shows the hysteresis of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. Hysteresis of p-type HfO_2 capacitors are about 20～30 mV. Oxidation temperature seems not influence hysteresis for p-type HfO_2 capacitors. Longer oxidation time makes hysteresis a little larger. Fig. 5-2 shows the hysteresis of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. We see that, for n-type HfO_2 capacitors, oxidation temperature influences hysteresis hardly. Atoms getting higher energy under higher oxidation temperature could reverse more easily. Thus hysteresis is smaller under higher oxidation temperature. Comparing to p-type HfO_2 capacitor, n-type HfO_2 capacitor appears much larger hysteresis. However, the limit of hysteresis for transistor in the future generation is less than 10 mV under high frequency C-V measurement. It seems we need to find some method to decrease hysteresis of HfO_2 device.

5.2 Uniformity

Fig. 5-3 and 5-4 show the distribution of p-type and n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. Measurements were made on 15 capacitors per wafer. Breakdown voltage at 50 % cumulative failure for p-type HfO_2 capacitors under 400℃-15 minutes, 400℃-30 minutes, 500℃-15 minutes and 500℃-30 minutes oxidation condition are 6.10 V, 6.20 V, 7.30 V and

7.45 V respectively. Breakdown voltage at 50 % cumulative failure for n-type HfO_2 capacitors under 400℃-15 minutes, 400℃-30 minutes, 500℃-15 minutes and 500℃-30 minutes oxidation condition are 3.55 V, 3.60 V, 4.80 V and 5.15 V respectively. We could find that devices under higher oxidation temperature and longer oxidation time have larger breakdown voltage because of thicker thickness and stronger chemical bonding. The uniformity of HfO_2 film on a p-type substrate wafer is excellent under all oxidation condition. HfO_2 film on an n-type substrate wafer shows a little worse uniformity under the same oxidation condition.

5.3 Constant Current Stress (CCS)

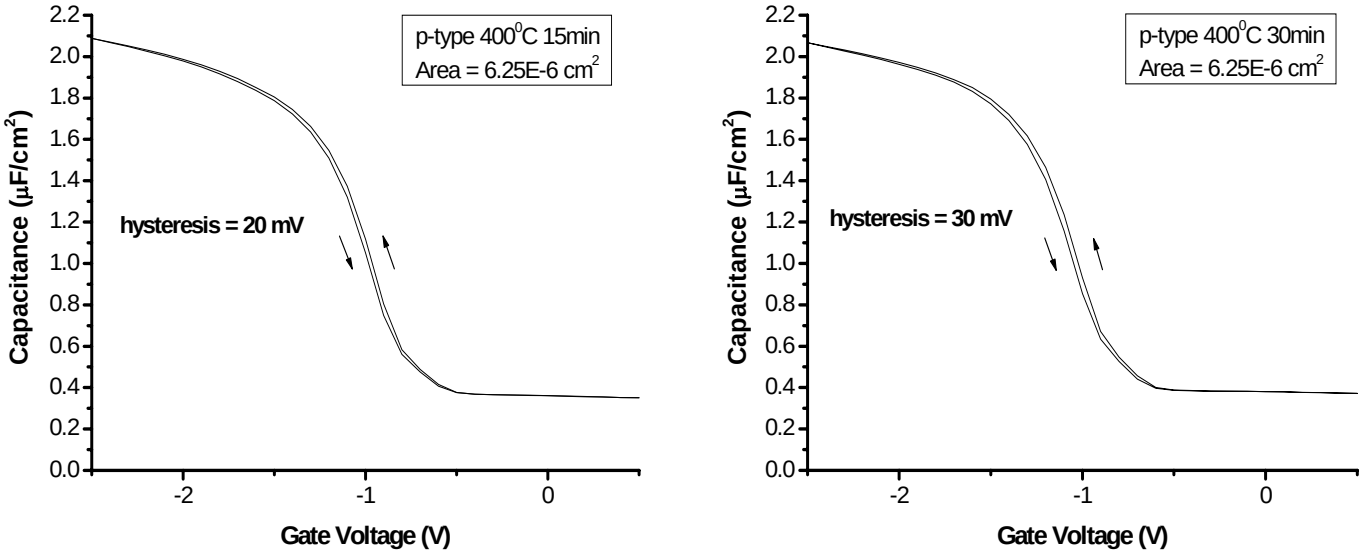
To study the reliability of HfO_2 film, stressing the film with a constant voltage or a constant current are two common methods. In our experiments, we use constant current stress (CCS) to test the reliability of HfO_2 film. Fig. 5-5 shows gate voltage shift of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions as a function of stress time during Jg = 1 A/cm^2 CCS stress. Capacitors under 400℃-15 minutes and -30 minutes oxidation condition have very similar EOT (i.e. 17.3 Å and 17.4 Å). However, we find that there is a 0.8 V drop between these two devices at the beginning gate voltage applied for. The larger initial gate voltage means device under 400℃-15 minutes oxidation condition has better capability of resisting current tunneling. In addition, gate voltage of these two devices both becomes slightly larger during the stressing period. This might result from that detrapping action fixes the defects in HfO_2 film and enhances the capability of resisting current tunneling. After stressing 30 seconds, SBD happens to p-type capacitor under 400℃-30 minutes oxidation condition, indicating that the worst capability of resisting current tunneling. P-type HfO_2 capacitor under higher oxidation temperature and longer oxidation time has larger gate voltage shift after 100 seconds CCS stress and thus has worse reliability. Fig. 5-6 shows gate voltage shift of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions as a function of stress time during Jg = 1 A/cm^2 CCS stress. Like p-type HfO_2 capacitor, n-type HfO_2 capacitor under 400℃-15 minutes oxidation condition has better capability of resisting current tunneling than under 400℃-30 minutes oxidation condition. Detrapping doesn't occur to all of n-type HfO_2 capacitors. Gate voltage shift of these four devices after 100 seconds CCS stress don't have obviously difference and are about 0.3 V. Thus the reliability is almost the same for n-type HfO_2 capacitors under different oxidation conditions.

5.4 Measured at High Temperature

As shown in figure 5-7, C-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 300℃-15 minutes oxidation condition are measured at 25℃, 75℃ and 125℃. At higher measurement temperature, HfO_2 capacitor has flatter accumulation region, steeper slope of C-V curve and smaller hysteresis. In addition, flat band voltage shifts to more negative at higher measurement. Fig. 5-8 shows J-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 300℃-15 minutes oxidation condition measured at 25℃, 75℃ and 125℃ from 0 V to 1 V. At higher measurement temperature, HfO_2 capacitor has larger gate leakage current due to the higher energy of electrons. Besides, gate leakage current at V_G = 1V has smaller increase from 75℃ to 125℃ than from 25℃ to 75℃. This hints that gate leakage current becomes to saturate at high measurement temperature. Fig. 5-9 shows J-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 400℃-15 minutes oxidation condition measured at 25℃, 75℃ and 125℃ from 0 V to -10 V. We find that HfO_2 capacitor generates breakdown more easily at higher measurement temperature. This is attributed to electrons have higher energy at higher temperature and result in harder damage in HfO_2 film.

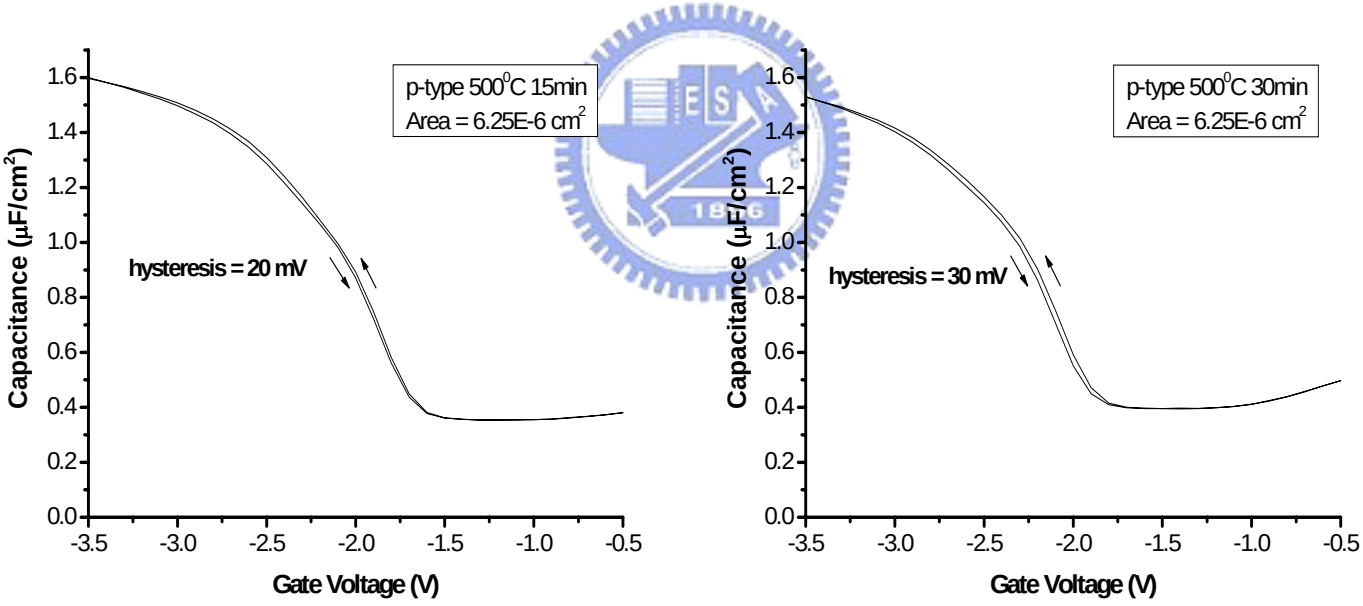
5.5 Reference

[1] HyperPhysics, C.R Nave Georgia University, 2002.



(a)

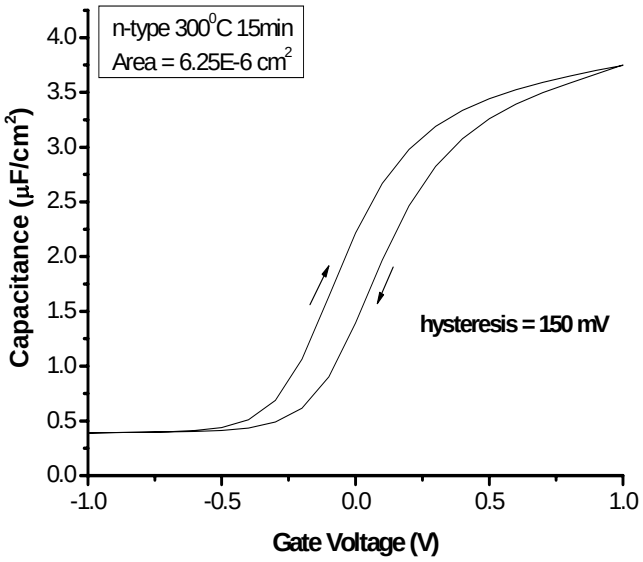
(b)



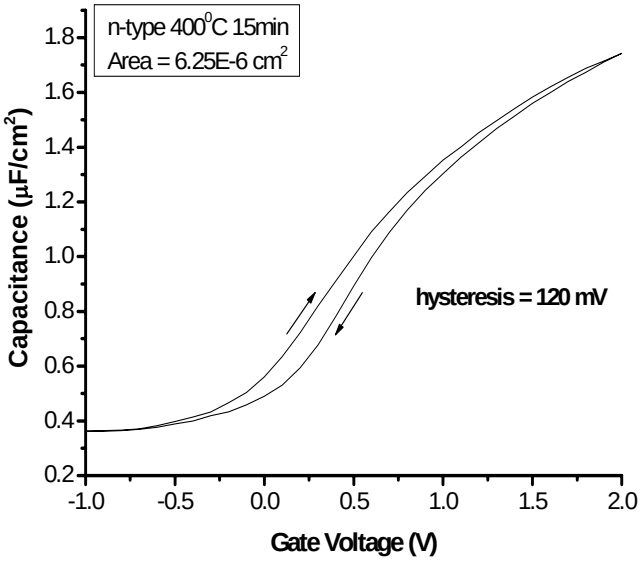
(c)

(d)

Fig. 5-1 Hysteresis of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. (a) 400℃ 15 minutes (b) 400℃ 30 minutes (c) 500℃ 15 minutes (d) 500℃ 30 minutes



(a)



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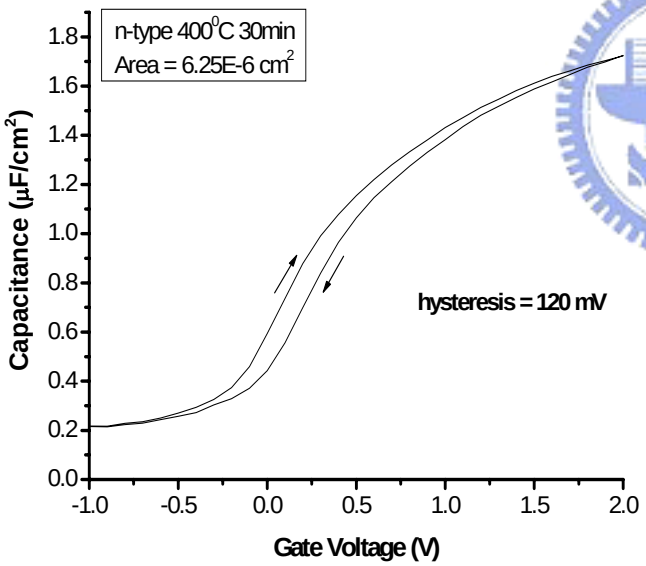
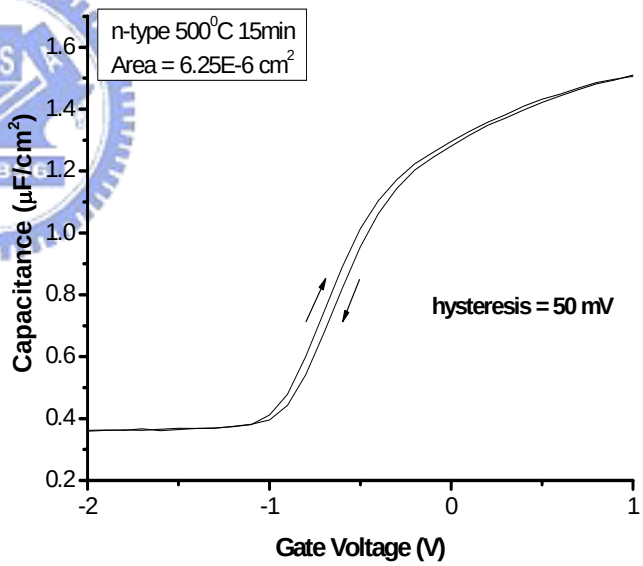


(c)



(d)

Fig. 5-2 Hysteresis of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions. (a) 300℃ 15 minutes (b) 400℃ 15 minutes (c) 400℃ 15 minutes (d) 500℃ 15 minutes

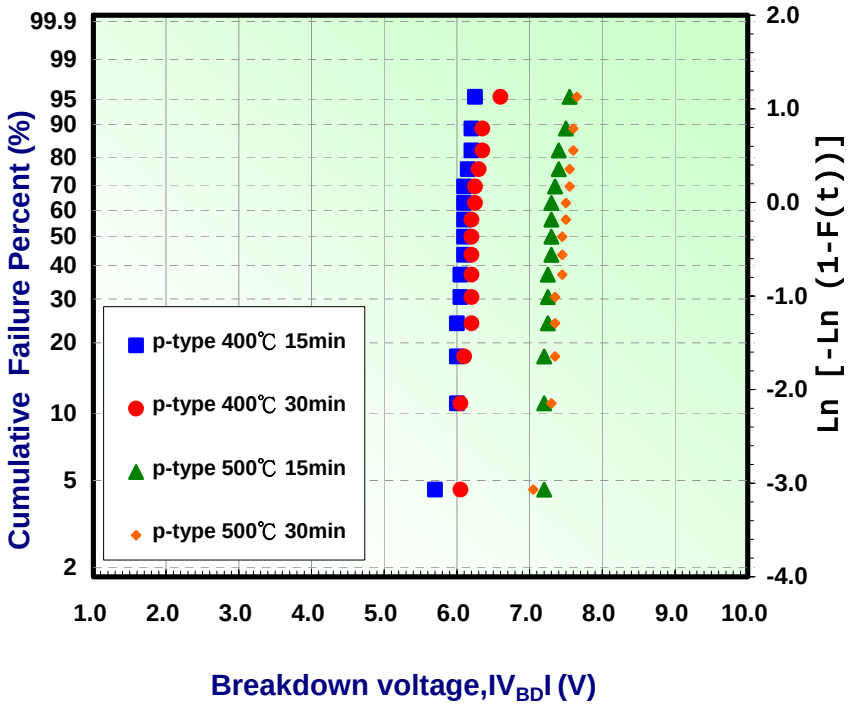


Fig. 5-3 Distribution of the breakdown voltage for p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions.

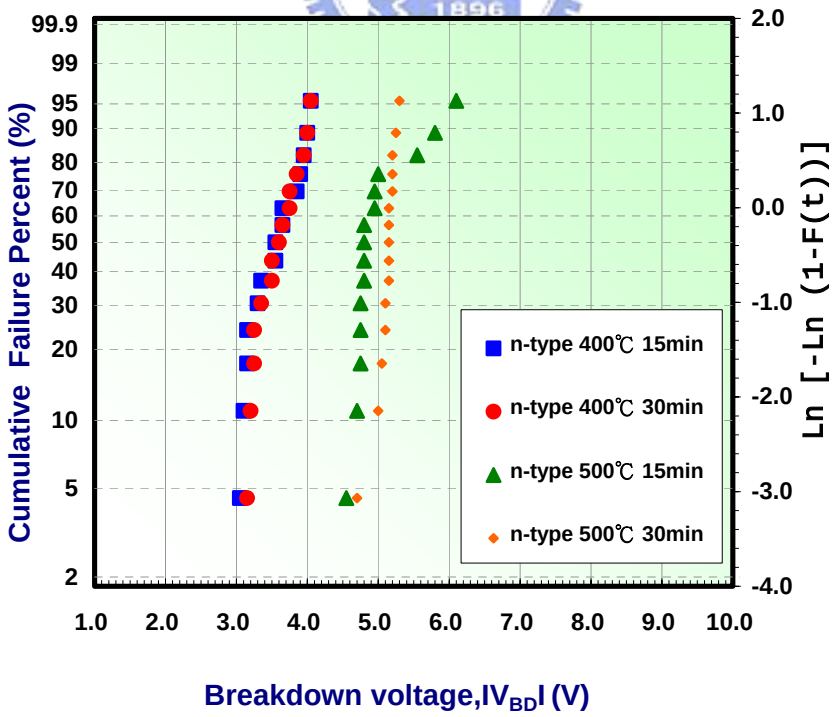


Fig. 5-4 Distribution of the breakdown voltage for n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions.

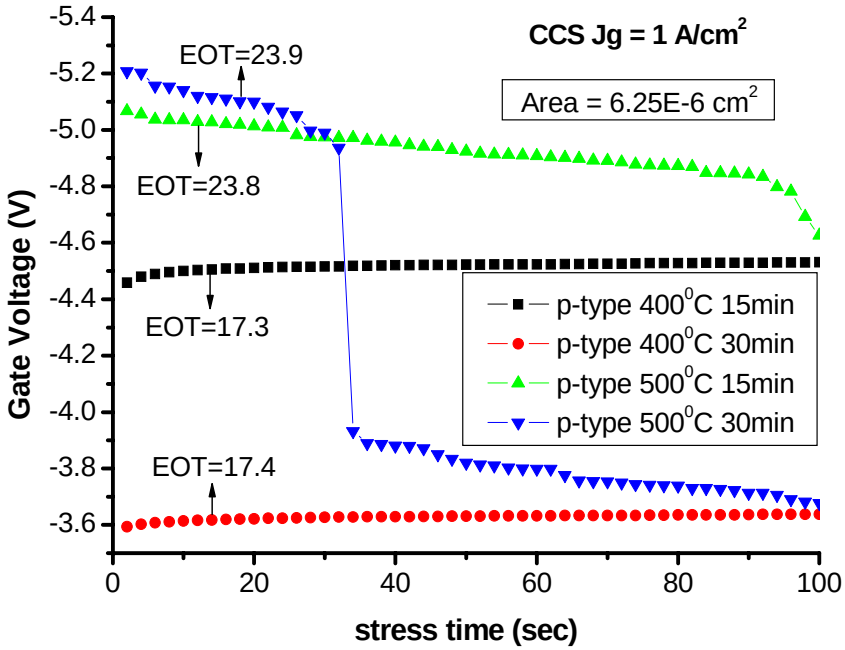


Fig. 5-5 Gate voltage shift of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions as a function of stress time during Jg = 1 A/cm^2 CCS stress.

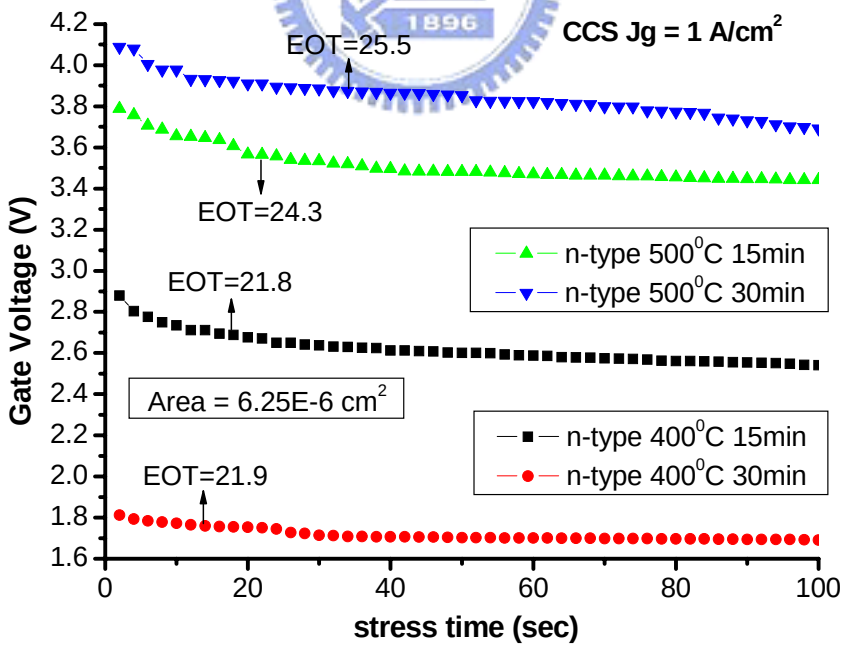


Fig. 5-6 Gate voltage shift of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under different oxidation conditions as a function of stress time during Jg = 1 A/cm^2 CCS stress.

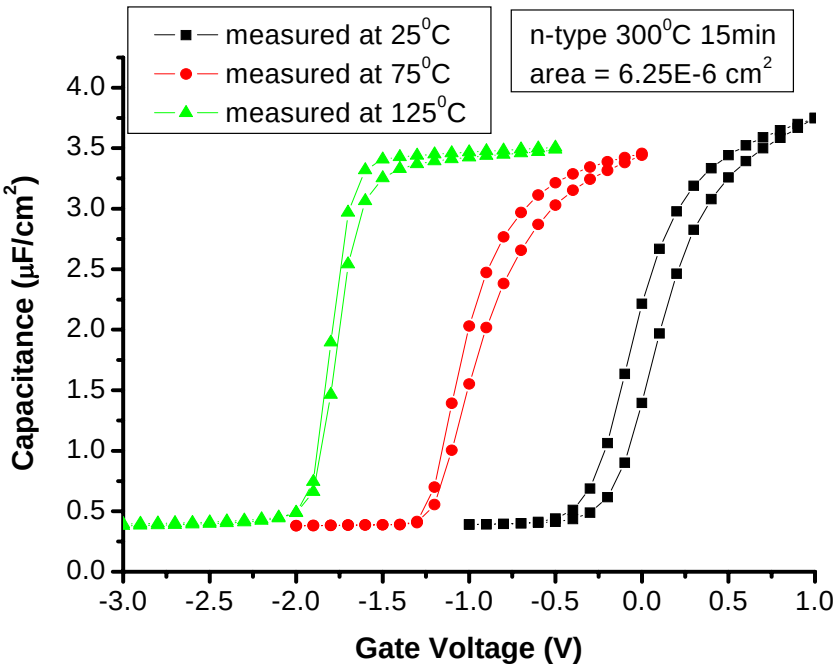


Fig. 5-7 C-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 300℃ 15 minutes oxidation condition measured at 25℃, 75℃ and 125℃.

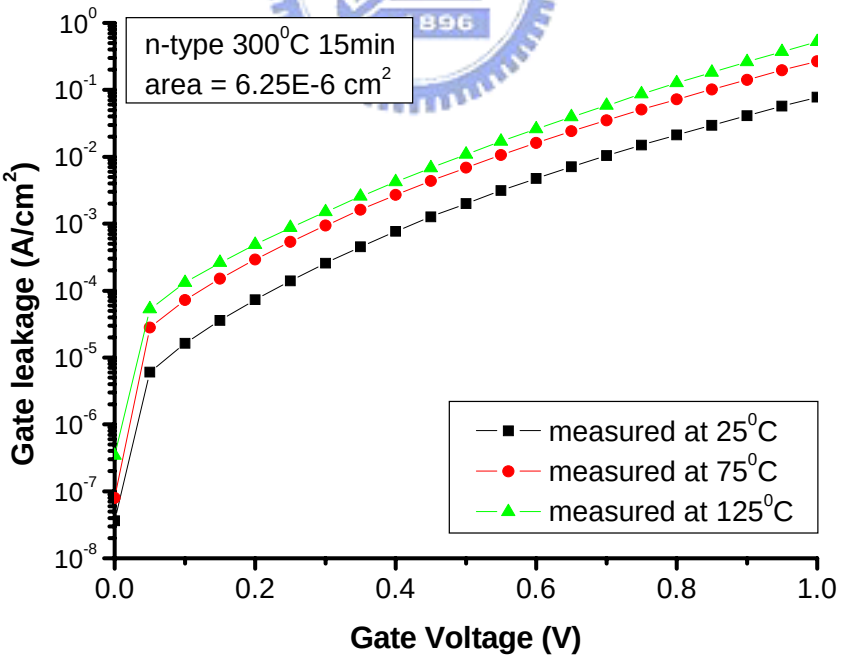


Fig. 5-8 J-V characteristics of n-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 300℃ 15 minutes oxidation condition measured at 25℃, 75℃ and 125℃ from 0 V to 1 V.

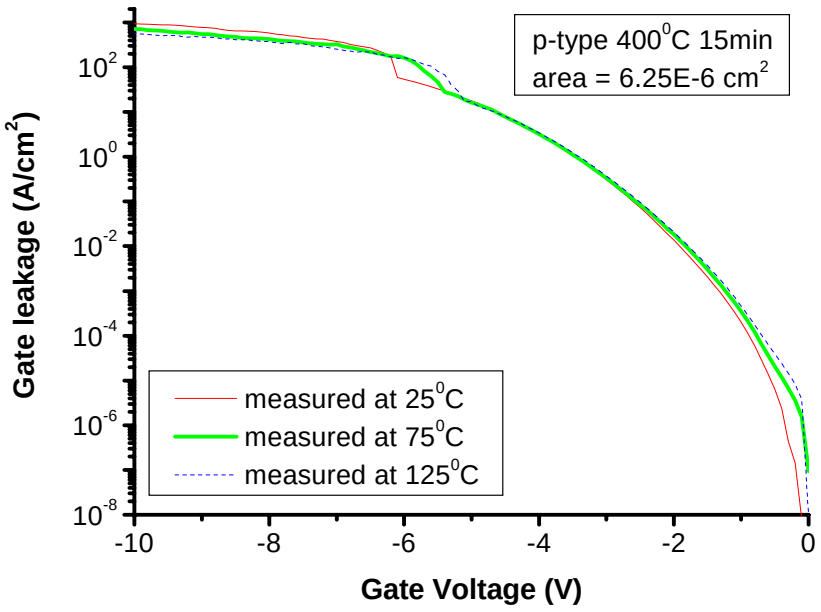


Fig. 5-9 J-V characteristics of p-type HfO_2 capacitors with 6.25×10^{-6} cm^2 die area under 400℃ 15 minutes oxidation condition measured at 25℃, 75℃ and 125℃ from 0 V to -10 V.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The Al/HfO_2/Si MIS capacitors were fabricated by DC sputter 20 Å hafnium on p-type and n-type silicon substrate and proceeds under 200℃～500℃ and 15～30 minutes oxidation conditions. Devices with different die areas under different oxidation conditions are performed and discussed.

We couldn't get effective C-V characteristics of p-type HfO_2 capacitors under 200℃ and 300℃ oxidation condition, and of n-type HfO_2 capacitors under 200℃ oxidation condition. The size of die area doesn't influence the flat band voltage. Higher oxidation temperature and longer oxidation time make the more negative flat band voltage shift. N-type HfO_2 capacitor with 6.25×10^{-6} cm^2 die area under 300℃-15 minutes oxidation condition has the smallest EOT of 9.2 Å. Device under higher oxidation temperature has thicker interfacial layer and stronger chemical bonding. Thicker physical thickness and stronger chemical bonding both contribute to the decrease of gate leakage current. Thus, higher oxidation temperature could results in larger EOT and less gate leakage current. Longer oxidation time slightly increases EOT and decreases gate leakage current. Under the same oxidation condition, p-type HfO_2 capacitor has smaller EOT and smaller gate leakage current than n-type HfO_2 capacitor. HfO_2 layer grown on p-type substrate has better quality of resisting gate leakage than on n-type substrate. EOT of devices with different die areas on the same wafer should be the same in fact. With the same EOT, using HfO_2 instead of SiO_2 for gate insulator could decrease gate leakage current more than 2~3 orders. Device with thinner thickness and weaker chemical bonding generates breakdown more easily. In addition, like SiO_2, thicker HfO_2 shows more abrupt breakdown characteristics compared to thinner HfO_2. Like SiO_2 NMOSFET, HfO_2 capacitor has four degradation stages. This hints HfO_2 might have similar breakdown mechanism with SiO_2. Schottky emission occurs at very low gate bias and F-N tunneling occurs at higher gate bias than both Schottky emission and Frenkel-Poole emission. In addition, n-type HfO_2 capacitors under 300℃-15 minutes oxidation condition always generate Schottky emission, F-N tunneling or Frenkel-Poole emission earliest because of smallest EOT. RTA treatment couldn't improve the quality of HfO_2 film, because HfO_2 is unit-combined lattice structure and thus couldn't be enhanced the value of

dielectric constant by RTA treatment. When the temperature rises to 800℃～900℃, HfO_2 would change the lattice structure from amorphous type to polycrystalline type and thus increase gate leakage current.

Hysteresis of p-type HfO_2 capacitors are about 20～30 mV. Oxidation temperature seems not influence hysteresis for p-type HfO_2 capacitors. Longer oxidation time makes hysteresis a little larger. For n-type HfO_2 capacitors, higher oxidation temperature effectively decreases hysteresis. P-type HfO_2 capacitor has much smaller hysteresis than n-type HfO_2 capacitor. Uniformity of p-type HfO_2 capacitor is excellent under all oxidation condition and a little better than of n-type HfO_2 capacitor. P-type HfO_2 capacitor under 400℃-15 minutes oxidation condition has better capability of resisting current tunneling than under 400℃-30 minutes oxidation condition. P-type HfO_2 capacitor under lower oxidation temperature and shorter oxidation time has better reliability. Reliability is almost the same for n-type HfO_2 capacitors under different oxidation conditions. At higher measurement temperature, HfO_2 capacitor has flatter accumulation region, steeper slope of C-V curve and smaller hysteresis. In addition, flat band voltage shifts to more negative at higher measurement. HfO_2 capacitor also has larger gate leakage current due to the higher energy of electrons and generates breakdown more easily at higher measurement temperature.

6.2 Future Work

The HfO_2 capacitor fabricated by our method mentioned above could provide an ultra thin dielectric layer of 9.2 Å EOT for n-type and 17.3 Å EOT for p-type. Their leakage current and film quality are acceptable for the use of devices in next generation. We think by technically and carefully controlling the oxidation condition, such as temperature and time, will effectively improve the quality of HfO_2 film.

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碩士論文：超薄二氧化鉿閘極絕緣層之特性研究

Characteristics of Ultra-Thin HfO_2 Gate Insulator