Chapter 2

NH_3 Plasma Treatment on the Electrical Characteristics of Poly-Si Thin Film Transistors

2.1 Introduction

Poly-Si TFTs are widely used in various applications, and will figure prominently in future high-resolution, but it still have several problem of poly-Si (ex. Leakage current, uniformity etc.). Many research of improved device characteristic were been proposed. It is well known that hydrogenation tends to terminate the grain-boundary dangling bonds with hydrogen atoms, remarkably improving the electrical characteristics of poly-Si TFTs, especially in leakage current (I_{off}), subthreshold awing (SS), threshold voltage (V_{th}) [2.1]. The NH_3 plasma passivation has better hot carrier endurance than H_2 plasma, due to the Si-H bond is weaker than Si-N bond so the Si-H bonds are easily broken during the hot carrier stress. In this chapter we compare plasma passivation effect on difference structure. We also discussed device characteristic improvement mechanism of poly-Si TFTs, then we development a new structure to increase the plasma treatment efficiency and further passivatred the tail state defects.

2.2 Experiment Details

2.2.1 Fabrication of bottom-gate poly-Si TFTs

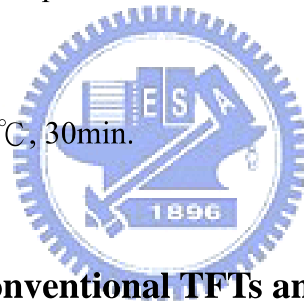
Two types of samples were fabricated called Sample A (with SiO_2 as a gate insulator) and Samples B (with Si_3N_4 as a gate insulator). The process flows is shown in Fig. 2.1. A 1.5 μm wet oxide layer was grown on the bare Si wafer as a buffer layer. Then phosphorous-doped a-Si of 100 nm was deposited at 550℃ in low pressure chemical

vapor deposition (LPCVD, vertical furnace) system. The phosphorous-doped a-Si film was annealed at 900℃ for 2hr and then patterned. An 80 nm TEOS oxide layer was deposited by plasma enhance chemical vapor deposition (PECVD) system as a gate insulator of sample A. A 100 nm silicon nitride (Si_3N_4) film was deposited by LPCVD system as a gate insulator of sample B. Ion implantation was then performed to form the regions of source and drain using pohtoresist as hard mask, afterward, furnace annealing at 600℃ for 24 hours in N_2 ambient was carried out to recrystallize the Si films. After defining the active regions, a 300nm passivation TEOS oxide was deposited by LPCVD system. Finally, the contact holes were opened followed by the Al film evaporation and metal pad definition.

The detail process flows are listed as follow:

1. Initial RCA clean
2. 1.5μm thermal Oxide: wet oxidation, 978℃.
3. An in situ doped (phosphorous) α-Si layer of 1000Å was deposited
4. Thermal annealing at 900℃ for 2 hours.
5. Mask#1: Gate electrode was defined and etched by anisotropic plasma etching.
6. P.R striped by H_2SO_4.
7. RCA cleaning.
8. Samples A: TEOS oxide (SiO_2) layer of 800Å was deposited by PECVD at 350℃ as gate insulator.
9. Samples B: Silicon nitride (Si_3N_4) layer of 1000Å was deposited by LPCVD at 700℃ as gate insulator.
10. Amorphous silicon layer of 1000Å was deposited by LPCVD at 550℃.

11. Mask #2, photo resists were defined for ion implantation.
12. Ion implantation, B, 15keV, 1E16cm^{-2}.
13. Photo resists were striped
14. Dopant activation, 600℃, 24 hrs.
15. Mask #3, active region were defined and etched by Poly RIE.
16. Photo resists were striped and RCA cleaning without final HF-dip.
17. Oxide passivation layers of 3000Å were deposited by LPCVD.
18. Mask#4, opened contact hole by BOE wet etching.
19. Photo resists were striped and dip HF.
20. A 5000 Å Al was deposited by thermal evaporation. .
21. Mask#4, defined Al pad.
22. Al etching
23. Al sintering, 400℃, 30min.



2.2.2 Fabrication of Conventional TFTs and Nitride Buffer layer TFTs

Two types of samples were fabricated called sample C (conventional TFT) and sample D (with bufferred Si_3N_4). The key process flow is shown in Fig. 2.1. A 0.5μm thermal Oxide was grown on bare Si wafer as a buffer layer. Then a non-doped α-Si of 1000Å was deposited at 550℃ in a LPCVD system as an active region, and then the sample were crystallized at 600℃ 24hr by furnace annealing. A 300Å sacrifical oxide was deposited perior to the plasma pretreatment, Next, NH_3 plasma treatment was performed for 1hr, 2hr and 4hr. followed by removing the sacrificial oxide by buffer oxide etcher (B.O.E). An 1130Å thick TEOS oxide layer was deposited by PECVD system as a gate dielectric of both sample C and sample D. A 400 nm poly-Si layers were deposited as the gate electrode. Self-align ion implantation was then performed to form the regions of

source, drain and gate. Afterward, furnace annealing at 600℃ for 24 h in N_2 ambient was carried out to dopants activate. After defining the gate regions, a 4000Å passivation SiO_2 layer was deposited by PECVD system. Finally, the contact holes were opened and the Al films were deposited and then defined.

The detail process flows are listed as follow:

1. Initial RCA clean
2. 0.5µm thermal Oxide: wet oxidation, 1100℃.
3. A 1000Å Si_3N_4 was deposited by LPCVD.
4. A 200ÅSiO_2 was deposited by PECVD.
5. A non-doped α-Si layer of 1000Å was deposited: furnace.
6. Crystallization at 600℃ for 24 h.
7. Mask#1: active region was defined and etched by anisotropic plasma etching.
8. P.R striped by H_2SO_4.
9. Pretreatment samples: plasma pretreatment sample was deposited 30nm sacrifice oxide.
10. Pretreatment samples: NH_3 plasma pretreatment for 1hr, 2hr, 4hr.
11. Pretreatment samples: remove sacrifice oxide.
12. RCA cleaning.
13. TEOS oxide (SiO_2) layer of 1130Å was deposited by PECVD.
14. Polycrystalline silicon layer of 4000Å was deposited by LPCVD.
15. Mask #2, photo resists were defined for gate electrode.
16. Photo resists were striped.
17. Self-align ion implantation, P, 60KeV, 5×10^{15} cm^{-2}.
18. Dopant activation, 600℃, 24 hrs.

19. Mask #3, contact hole were defined and etched by B.O.E.
20. Photo resists were striped and RCA cleaning without final HF-dip.
21. Oxide passivation layers of 4000Å were deposited by PECVD.
22. A5000 Å Al was deposited by thermal evaporation. .
23. Mask#4, defined Al pad.
24. All samples: Al etching
25. All samples: Al sintering, 400℃, 30min.
26. Post-treatment samples: NH_3 plasma pretreatment.

2.2.3 Fabrication of SIMS analysis sample

Two types of samples were fabricated called Sample E (SiO2) and Sample F (Si_3N_4). The key process flows as shown in Fig. 2.3. A 1.5um thermal oxide was grown on the Si wafer as a buffer layer. Then an 100nm a-Si was deposited at 550℃ in a LPCVD system. Sample E a 100nm TEOS oxide deposited by PECVD system. Sample F a 100nm Si_3N_4 layer deposited by LPCVD system. Both sample E and F the 50nm amorphous Si layer deposited by LPCVD system. Finally, a passivation TEOS SiO_2 of 300nm was deposited by LPCVD system. After NH_3 plasma treatment for 8hr, the passivation oxides of both samples were removed by B.O.E solutions.

The detail process flow is listed as flow:

1. Initial RCA clean
2. 1.5μm thermal Oxide: wet oxidation, 978℃.
3. A α-Si layer of 1000Å was deposited: vertical furnace.
4. Sample E: A TEOS oxide layer of 100nm was deposited by LPCVD.
5. Sample F: A nitride layer of 100nm was deposited by LPCVD at 600℃.
6. A α-Si layer of 50nm was deposited: vertical furnace.

7. RCA cleaning without HF dip

8. A TEOS oxide passivation layer of 300nm was deposited by LPCVD

9. All samples: NH_3 plasma treatment with 8hr.

10. All samples: A passivation layer was removed b y BOE.

2.3 Results and Discussions

2.3.1 Leakage current mechanism for Poly-Si TFTs

For poly-Si thin film transistor, the leakage current can be expressed as [2-1]

$$I_L = \frac{qW\left(T_e + T_p\right)\varepsilon_y V_{ds}}{kT}\left\{N_{st}\, e^{-\frac{(E_{F0}-2\Delta E)}{kT}}\right\} \quad (2\text{-}1)$$

where,

q	is the electron charge.
W	is the channel width.
k	is the Boltzman's constant.
T	is the temperature.
Te	is the electron tunneling probability.
Tp	is the hole tunneling probability.
ε_y	is the lateral electric field in the drain depletion region.
E_{F0}	is approximately half the band gap.
ΔE	is the drain boundary traps with respect to midgap.
Nst	is the trap density (/ (cm^3-eV))

The leakage current mechanism: as electrons form the valence band are captured by the traps via any of the three processes (i.e., thermionic emission, thermionic field emission, and tunneling), the hole generated are swept to the drain and they result in

leakage current. For the traps to remain active, it must emit the captured electrons to the conduction band. In equation (2-1), it can effectively reduce leakage current by decreasing lateral electric field and reduce effective grain boundary trap density at the channel/drain junction. The lowest activation energy is about half E_g, thermionic emission is the dominate leakage mechanism at low drain electric field (In Fig2.4 mechanism (1)). As the drain bias increase (more negative), the drain depletion field increases and activation energy decreases. As such, the dominant leakage current mechanism is thermionic field emission and it represented by mechanism (2) in Fig. 2.4. Further increase of the drain bias put activation energy below 0.1eV. Since $Ea < 0.1$ eV present almost no barrier to the carrier motion, the dominant leakage mechanism is pure tunneling.

2.3.2 Hydrogenation effect on bottom gate TFTs

Fig. 2.5 shows the transfer characteristics for comparison of bottom-gated poly-Si TFTs before and after NH_3 plasma passivation at V_{DS}=-0.1, and -5 V, respectively. After hydrogenation, the electrical characteristics of the poly-Si TFTs have been improved as listed in table 2.1. The minimum leakage current of sample A is decreases from 260 pA to 0.2 pA. Sample B is decreases from 196pA to 0.15 pA. The sample B after NH_3 plasma passivation has lower leakage current than that of sample A at high drain electric fields (V_{DS}=5V) as shown in Fig. 2.5 (b). The reduction in the leakage current is attributed to the defect reduction in the drain junction, because nitrogen and hydrogen radicals can effectively accumulate at the Si_3N_4/poly-Si interface as shown in Fig. 2.6 (a) and (b). In Fig. 2.6(a), the peak value of nitrogen concentration in nitride sample is increased from 1.61^{18} to 4.38^{21} (atom/cm^3) after NH_3 plasma treatment for 8 hours. It is obviously that the SiN concentration of nitride sample is remarkably larger than that of oxide sample near the dielectric/poly-Si interface. In Fig. 2.6 (b), we found that the hydrogen concentration of

nitride sample has larger value than that of oxide sample after NH_3 plasma treatment 8 hours. This result implies that the nitride film can effectively prevent nitrogen and hydrogen atoms from downward diffusing. In contrast, nitrogen and hydrogen atoms can diffuse into the oxide film through the channel region via hydrogenation processes. As mentioned above, the numbers of hydrogen/nitrogen atoms in the channel region with Si_3N_4 as the gate insulator is large than that with SiO_2 as the gate insulator.

In comparison of the on-state currents, sample A has large turn-on current than sample B after hydrogenation. The on-state current is dominated by donor-like tail states originated from strained bonds at the channel/dielectric interface. This is well known that the stress between the Si_3N_4 and poly-Si interface are large than that the SiO_2 and poly-Si interface, caused by larger differences in thermal expansion coefficient between Si_3N_4 and poly-Si. Although a larger number of hydrogen and nitrogen atoms are blocked at the Si_3N_4 and poly-Si interface after NH_3 plasma treatments, most of these atoms can easily passivate the deep states originating from the dangling bonds at the channel/dielectric interface. For this reason, the number of donor like tail states at Si_3N_4 and poly-Si interface after NH_3 plasma treatment is still larger than those at the SiO_2 and poly-Si interface.

2.3.3 Hydrogenation effect on Buffer Nitride layer TFTs

From the above results, we found the silicon nitride film can effectively resist the hydrogen and nitrogen atoms downward diffusion. We Si_3N_4 design the new structure (as show in Fig.2.2) for top-gate TFTs in order to improve the plasma passivation efficiency. Fig. 2.7 (a) shows the transfer curve of conventional TFT (CTFT) and buffer nitride TFT (BNTFT), where we can observed that the leakage current of the BNTFT without SiO buffer layer are large than the other sample. It is due to the large stress existing in the silicon nitride and poly-Si interface, while the stress induced defect would lead to the

formation of the back channel (as a leakage path). For this reason, a buffer oxide layer must be deposited between the silicon nitride and poly-Si layer to release stress. And we know there are same electrical characteristics for BNTFT and CTFT before plasma treatment. In Fig. 2.7 (b) is show the transfer curve of CTFT and BNTFT after plasma pretreatment 4 hr. The plasma pretreatment process not obvious the any improvement between BNTFT and CTFT, but compare to no treatment sample that pretreatment sample can improved device characteristics slightly. It is due to the greater part of Si-H bonds will be broken during high temperature process (poly-Si gate deposited (>600℃) and dopant activated). Fig. 2.8 (a) and (b) shows the transfer characteristics for comparison of BNTFTs and CTFTs before and after NH_3 plasma passivation at V_{DS} at 0.1, and 5V, respectively. After hydrogenation, the electrical characteristics of poly-Si TFTs have been improved as listed in table 2.2. We found the field effect mobility and ON-state current of BNTFT is higher than CTFT after NH_3 plasma treatment, but the threshold voltage and subthreshold swing were not improved at BNTFT. The BNTFT further improved the device characteristics of field effect mobility and ON-state current, since the NH_3 radicals in the BNTFT structure can effectively passivate the tail states. Figure 2.9 (a) and (b) show the off-state current at low drain voltage. The leakage current at low V_{DS} depends on the total density of states at mid-gap and on the density of states in the lower half of the gap [2.2] for an n-type TFT in low drain field. Figure 2.9 illustrates that the leakage of BNTFT is lower than that of CTFT. This result suggests that the buffer nitride layer effectively prevented the hydrogen atoms from downward diffusing but accumulated at the channel region. And if the hydrogen concentration increases at the channel, the tails state would further be passivated.

2.3.4 Long-time NH_3 Plasma Treatment on Threshold Voltage and Subthreshold Swing

The threshold voltage is defined as the gate voltage at a fixed drain current Id = (W/L)·10^8 at V_{DS} at 0.1 V. For the threshold voltage and subthreshold swing, after plasma treatment for 9 hr both CTFT and BNTFT have the same improvement. These two parameters are more sensitive to the deep states near the mid-gap [2.3], indicating that the deep states is easily passivated by NH_3 plasma treatment. It is because the hydrogen and nitrogen atoms are much easier to terminate the dangling bonds (deep states) than the strain bonds (tail states). In table 2.2, the CTFT and BNTFT has the same plasma passivated efficiency for threshold voltage and subthreshold swing after plasma treatment of 9hr. In Fig. 2.10, we see the passivation rate of threshold voltage. It was observed that the BNTFT have faster paasivation rate than CTFT at the first few hours, but when the passivation time higher than 400 min the threshold voltage of both structure shows not difference. We found the result for subthreshold swing characteristic was similar to the threshold voltage characteristic, because both parameters are sensitive to the deep state defects (dangling bonds). Since the number of deep state defects are roughly lower than the tail states, after long time plasma treatment the dangling bonds were terminated easily and the properties of BNTFT and CTFT reached a saturated value.

2.3.5 Long-time NH_3 Plasma Treatment on Field Effect Mobility and ON-state Current

At the turn-on condition near V_{th}, μ_{FE} is strongly influenced by the density of trap states at or above the surface Fermi-level position (the bulk Fermi level away from the interface plus the surface potential) above mid-gap [2.3]. The number of strained bonds is roughly a factor of 100 more than number of dangling bonds at grain boundary. Hydrogen

bonding in dangling bonds is far stronger than to the strain bonds (above 2eV greater binding energy than the bond-centered interstitial site) [2.4]. Hence, during passivation, as hydrogen traps and detraps at various sites, it will remain in dangling-bond sites for a significantly longer period than the tail states. Only when the hydrogen concentration enough the tail state defects will be passivated. In table 2.2, we found the mobility and ON-state current of BNTFT are higher than CTFT, indicating the buffer nitride layer can effectively accumulate the hydrogen atoms at the channel layer, then further passivating the strain bonds (tail states). Fig. 2.11 illustrates the field effect mobility of BNTFT is higher than that of CTFT, proving that the BNTFT can effectively accumulate the hydrogen and nitrogen atoms in the channel region to fix the strain bonds at channel.

We also compared the passivation rate of bottom-gate TFTs as shown in Fig. 2.12 2.13. After plasma treatment the device characteristics of silicon oxide as a gate insulator is better than that of silicon nitride, because the large stress exist in the Si_3N_4/poly-Si interface. The stress induced defect is difficult to be passivated by plasma treatment so that the device performance not observed improvement. But we found the bottom-gate structure has faster passivation rate (reach saturation point at 90 min) than top-gate structure (no saturation point being observed after 540 min treatment). During the hydrogenation process the hydrogen radical can directly passive the channel for bottom-gate structure, but for top-gate structure the radical must diffuse through the gate oxide to reach the channel region (as show in Fig 2.14 (a) and (b)). That's why the bottom-gate TFTs have a shorter passivation path and the saturation time than top-gate TFTs.

Finally, in order to justify the BNTFT can effectively improve the tail state debsity, we statistically calculated the cumulative distribution for device characteristics of BNTFT and CTFT before and after plasma treatment. Fig. 2.15 shows the cumulative distribution of field effect mobility and ON-state current, implying that the distribution of these two

parameters were similar before plasma treatment.The BNTFT will effective reduce the passivation time and gain of excellent performances. In the Fig. 2.16 the threshold voltage will more similar after plasma treatment at 9hr. In these results we prove the buffer nitride layer can accumulated hydrogen atoms at channel then further improved the tail state defects.

2.4 Summary

The traps states density are directly depend on the electrical characteristic, the ammonia plasma passivation process can effectively reduce the traps state density. The difference gate insulator (SiO_2 and Si_3N_4) will affect the passivation mechanism, that the Si_3N_4 as a gate insulator will accumulate hydrogen atoms at the channel region to further reduce the tail state defects. But there are large stress existing the Si_3N_4/poly-Si interface, then created much defect state of both deep state and tail state. For this reasonm, a buffer oxide layer must be deposited between the silicon nitride and poly-Si layer to release stress. The top-gate TFTs have slower passivation rate than bottom-gate TFTs, that the buffer nitride layer TFTs can effective increase the passivation efficiency, for long time plasma treatment BNTFT will further improved the device characteristic. The cumulate distribution justify the BNTFT can effectively improve the tail state density, and then further improve the device characteristic of field effect mobility and ON-state current.