Chapter 3

Characteristics of T-gate Poly-Si Thin film Transistors

3.1 Introduction

Poly-Si TFTs plays an important role in large-area electronics, due to it possibility of fabricating CMOS circuit. In addition to being capable of driving current [3-1], compared to the amorphous silicon TFTs, Poly-Si TFTs offer the flexibility of integrating peripheral driver circuits on glass substrates to interface with AMLCDs. Despite this achievement, the leakage current still limited the COMS performance. The large leakage current will lead to high power consumption. In most applications, the major problem is the anomalous leakage current of poly-Si TFTs, and it directly dependent on the trap state distribution and poly-Si channel quality.

The leakage current is exponentially dependent on the lateral drain electric field and directly proportional to the grain-boundary trap density at drain junction. The offset structure can effective reduced the leakage current due to it has extra high resistance region at offset channel (non-doped) [3.2], but this structure will degrade the ON-state current and the device property. On the contrary, the floating gate spacer poly-Si TFTs can effectively reduces the OFF state leakage current while maintaining a high ON current comparable to conventional TFTs [3.3].

In this chapter, we design the new structure of poly-Si TFTs. The T-gate TFTs will reduce the lateral electric field to reduce the leakage current, and maintaining the high ON-state current. We also discuss the hot carrier endurance of T-gate TFTs.

3.2 Experiment Details

3.2.1 Fabrication of Conventional TFTs and T-gate TFTs

Two types of samples were fabricated called Sample C (conventional TFT) and Sample D (T-gate TFT). The key process flows as shown in Fig. 3.1. A 0.5μm thermal Oxide was grown on bare Si wafer as the buffer layer. Then the non-doped α-Si of 1000Å was deposited at 550℃ in the low pressure chemical vapor deposition (LPCVD, furnace) system as an active region, and crystallization at 600℃ 24hr by furnace annealing. An 1130Å thick tetraethyl orthosilicate (TEOS) oxide layer was deposited by plasma enhance chemical vapor deposition (PECVD) system as the gate dielectric of both Sample C and Sample D. A 420 nm poly-Si layers were deposited as the gate electrode, and defined for gate electrode by wet etching solution. Liquid phase deposition (LPD) oxide was selective deposition on the gate dielectric and the gate electrode but not deposited on photo resisted; remove P.R by H_2SO_4 and SiO_2 etching back by B.O.E solution. Self-align ion implantation was then performed to form the regions of source, drain and gate electrode, afterward, furnace annealing at 600℃ for 24 h in N_2 ambient was carried out to dopant activation. After defining the gate regions, a 4000Å passivation SiO_2 layer was deposited by PECVD system. Finally, the contact holes were opened and the Al films were deposited and then defined.

The detail process flows are listed as follow:

1. Initial RCA clean
2. 0.5μm thermal Oxide: wet oxidation, 1100℃.
3. A non-doped α-Si layer of 1000Å was deposited: furnace, decomposed SiH_4 gases, 550℃.
4. Crystallization at 600℃ for 24 h.

5. Mask#1: active region was defined and etched by anisotropic plasma etching.
6. P.R striped by H_2SO_4.
7. RCA cleaning.
8. A TEOS oxide (SiO_2) layer of 1130Å was deposited by PECVD at 350℃ as gate insulator.
9. A polycrystalline silicon layer of 4000Å was deposited by LPCVD at 600℃.
10. Mask #2, photo resists were defined for gate electrode.
11. Sample D: Deposition LPD oxide 4000Å.
12. Sample D: SiO_2 etching back by B.O.E solution.
13. Sample D: Deposited 4000Å poly-Si by LPCVD.
14. Sample D: Poly-Si spacer formation.
15. Sample D: Remain LPD oxide remove.
16. Self-align ion implantation, P, 70KeV, 5×10^{15} cm^{-2}.
17. Dopant activation, 600℃, 24 hrs.
18. Mask #3, contact hole were defined and etched by buffer oxide etcher (B.O.E).
19. Photo resists were striped and RCA cleaning without final HF-dip.
20. Oxide passivation layers of 4000Å were deposited by PECVD at 350℃.
21. 5000 Å Al was deposited by thermal evaporation. .
22. Mask#4, defined Al pad.
23. Al etching
24. Al sintering, 400℃, 30min.
25. NH3 plasma passivation 2-hours.

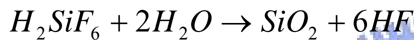
3.2.2 Selective liquid phase deposition

The chemical solution for LPD oxide deposition has been described elsewhere

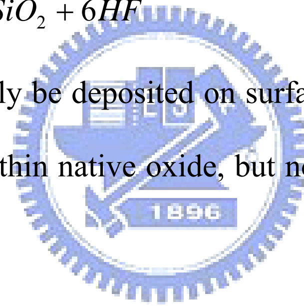
[3.4]-[3.5]. First, 75g of silica (SiO_2) powder with high purity of 99.99% was mixed into 1800 ml of hydrofiluorosilicic acid (H_2SiF_6, 4mol/L). the solution became saturated with silicic acid ($Si(OH)_4$) after being stirred at 23℃ for 48 hours. The chemical reaction in the prepared solution can be represented by the following equilibrium equation:

$$5H_2SiF_6 + SiO_2 + 6H_2O \rightarrow 4SiF_6^{2-} + 2Si(OH)_4 + 6HF + 8H^+$$

Before immersing the sample wafers, the prepared solution was filtered to remove the undissolved silica, and followed by adding deionized water into the saturated solution as it was stirred. The added deionized water enable the solution to become supersaturated with silicic acid $Si(OH)_4$. We can write the net reaction of S-LPD for $SiO_{2-x}F_x$ deposition as following:



$$H_2SiF_6 + 2H_2O \rightarrow SiO_2 + 6HF$$



The LPD oxide can only be deposited on surfaces with OH bonds, such as oxide and polycrystalline silicon with thin native oxide, but not on surfaces without OH bonds, such as Si_3N_4 and photoresist.

3.3 Results and Discussions

3.3.1 Electrical characteristics of T-gate poly-Si thin film transistors

We known anomalous leakage current of conventional TFTs increases exponentially with difference between gate and drain voltage. In this chapter we design a new structure (T-shape gate) of poly-Si thin film transistor in order to decrease the leakage current. Because the new structure can effective reduce the drain electric field by T-gate structure. The simulated results we known the T-gate structure can effectively reduce the horizontal and the vertical electric field [3.6]-[3.7], and modulate the oxide thickness of gate offset region to control device property [3.8].

We compare the poly-Si thin film transistors with T-shape gate to conventional

poly-Si TFTs. Fig. 3.2 (a) illustrates the transfer curve of conventional TFT (CTFT) and T-gate TFT (TGTFT) with difference thickness of offset region ranging from 100 nm to 200 nm. It can be observed that the sample of TGTFT have lower leakage current with offset oxide thickness increase, indicated T-gate structure can reduce the drain side electric field then reduce the leakage current [3.8]. The T-gate structure can effectively reduce leakage current but the ON-state current still decreases cause by the offset region will increase the source drain series resistance. In Fig. 3.2 (b) show the transfer curve with linear scale, the ON-state current of convention TFT has two times than TGTFT, and with the offset oxide thickness increase the ON current will further decreases.

3.3.2 Threshold Voltage and Subthreshold Swing Characteristics of T-gate poly-Si TFTs

The subthreshold characteristic can be expressed as [3.9]:

$$SS \approx \frac{kT}{q} \ln 10 \times (1 + C_D / C_i) \quad (3.1)$$

where, q is the electron charge.

k is the Boltzman's constant.

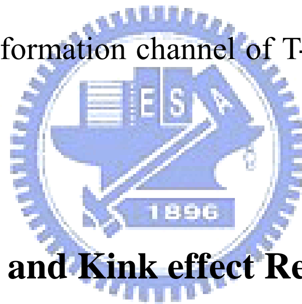
T is the temperature.

C_D is the depletion-layer capacitance per unit area.

C_i is the gate insulator capacitance per unit area.

The device electrical characteristics were listed in table 3.1.We found that the substhreshold property of conventional TFTs is better than TGTFT, and the substhreshold slope increase with offset oxide thickness increases (as shown in Fig. 3.2). Assume the channel doping of CTFT and TGTFT are similar concentration, and gate insulator deposited for both CTFT and TGTFT at same process, the depletion

capacitance of TGTFT should the same as CTFT. In this reason, there are two reason of dominated substhreshold characteristic of TGTFT. One is the insulator capacitance C_i (equation 3.1) because the T-gate structure will reduce the gate insulator capacitance (per unit area) by increase the offset oxide thickness. Then offset oxide thickness increases the gate insulator capacitance will decreases (oxide thickness influence on insulator capacitance) and increase the subthreshold slope. Another reason is that TFT operation at subthreshold regime the current is due to carrier diffusion, so it limited by source junction potential barrier [3.9]. Then T-gate structure will increase the potential barrier at drain/source junction lead to the subthreshold slope increase. We also found the threshold voltage of CTFT is lower than TGTFT. Because the offset region of T-gate structure has thicker gate insulator than conventional device, then when applied voltage to accumulated carrier to formation channel of T-gate structure need larger voltage than conventional.



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3.3.3 Off-state Current and Kink effect Reduction

The T-gate structure is also reducing the off state leakage, due to the higher channel resistance and lower drain electric field. In Fig. 3.3 the drain current measured at Vg=-4 V (the device operated at off-regime) is shown for CTFT and TGTFT: the off-characteristics present, as a common feature, at high V_{DS} the off-current starts to rise again with steeper slope if compared to the low-V_{DS} regime. The clearly confirming how the presence of an offset region at the drain can significantly reduce the off-current. In Fig. 3.4 the output characteristics, measure at Vg=20V, are shown. As can be noted the output characteristics show the kink effect for T-gate poly-Si TFTs been suppressed, because the T-gate structure also reduce the impact ionization at drain junction. The kink point of the CTFT was clearly shown at V_{DS}=15V, but the kink point of the TGTFT was not observed at V_{DS} below 30V.

3.3.4 Hot Carrier Endurance

As described in above section, that the T-gate structure would increase the channel resistance and reduce the lateral electric field. Therefore, the hot carrier endurance of TGTFT can be greatly improved by the elevated offset oxide thickness with T-gate structure. Figures 3.5(a) and 3.5(b) depict the variations of typical *Id-Vg* curve (V_{DS}=0.1V) after hot carrier stress for CTFT and TGTFT (d=100nm), respectively. The stress condition was chosen from the output characteristic when device operated at saturation region (Vg=18V; V_{DS}=42V). The on current degradation for CTFT has serious than TGTFT. In this figure we found the much degradation for the CTFT but the TGTFT not degradation observed. Fig. 3.6(a) and 3.6(b) show the degradation rate of threshold voltage and subthreshold swing after hot carrier stress for CTFT and TGTFT, respectively. The shift of of Vth and S.S after hot carrier stress for CTFT is higher than TGTFT. It is due to the fact that under the same stress condition, the stress current of CTFT is about two times lager than TGTFT from their output characteristics [3.10]. Another result is the intra-grain bulk states are generated in poly-Si film. Because the poly-Si film was formed by solid-phase crystallization method, intra-grain bulk state density is much higher.

3.3.5 NH_3 Plasma Passivation effect

In Fig. 3.2, we found the device transfer characteristic was poor for both CTFT and TGTFT, it cause by there are many defect state exist in the gate dielectric and the poly-Si channel layer. Then we used NH_3 plasma passivation for both CTFTs and TGTFTs, since the hydrogenation process tends to terminate the grain-boundary dangling bonds with hydrogen atoms then improving the electrical characteristic of poly-Si TFTs. In Fig. 3.7 show the transfer curve of CTFT and TGTFT after NH_3 plasma treatment 2 hours. We found the CTFT have better performance than TGTFT after NH_3 plasma treatment. In the

plasma passivation mechanism we know that the hydrogen atoms to passivated the channel defects must along the gate insulator edge, due to the hydrogen atoms are difficult diffuse through the gate electrode then passivated the channel layer. The TGTFT have extra offset region will increase the hydrogen passivated path (as show in Fig. 3.8), so that the TGTFT electrical property is poorer than CTFT after plasma treatment. In order to justify this mechanism then we determined the traps state density N_{it} by the theory established by Levinson *et. al.* [3.11], however, for CTFT the effective traps density decreased from 2.10E13 to 1.23E13 after 120min NH3 plasma treatment, and for TGTFT (d=100 nm) the effective traps density decreased from 2.06E13 to 1.46E13 (as show in Fig. 3.9), so that plasma passivation effect for CTFT was improved 41% but TGTFT only 29% improvement. In these results we know that T-gate structure have slower passivation rate than conventional structure, due to the offset structure increased the passivation path. Fig. 3.10 illustrates the transfer curve with drain current at linear scale. We found the ON-state current after NH3 plasma treatment were increases three times of both CTFT and TGTFT (the ON-state current of CTFT still remain 2 times than TGTFT).

3.4 Summary

In this chapter, we thoroughly examined the electrical characteristics of the proposed TGTFT structure. Increasing the offset oxide thickness was beneficial for suppressing the OFF-state leakage current of TFTs, but the ON current degradation slightly. In this experiment we not addition extra mask and success to reduce the drain electric field. After ammonia plasma treatment the T-gate structure increase the extra passivation path, lead to device passivation rate slower than conventional device. The new structure can effectively reduce the kink effect and off-state leakage current, and the hot carrier endurance can be improved.