Chapter 4

Conclusions

4.1 Conclusions

In this thesis, we used the SiO_2 and Si_3N_4 as the gate insulator of bottom-gate TFTs to investigate the device characteristics by NH_3 plasma treatment. And improve the plasma passivation efficient by the nitride buffer poly-Si TFT. Furthermore, we also compare the passivation effect of the bottom-gate and top-gate structure.

For poly-Si TFT the leakage current strongly depends on the deep state defects, then after NH_3 plasma treatment the leakage of the Si_3N_4 as the gate insulator is lower than SiO_2 as the gate insulator for bottom-gate structure. In the SIMS analysis we found the silicon nitride film can effectively prevent the hydrogen atoms downward diffused then accumulated at the channel. Then we design the new structure (buffer nitride layer thin film transistors), this structure can effectively accumulate hydrogen atoms at the channel then further passivated the tail state defects. However, the defect reduction of poly-Si thin film transistor can effectively reduce the leakage current and improve the device characteristics. Using silicon nitride to accumulate hydrogen atoms at the channel during plasma treatment will increase the passivation efficiency.

In this paper we use the selective liquid phase deposition to formation the T-gate poly-Si TFT. And the T-gate structure will reduce the lateral electric field in the drain junction and the ON-state current degradation slightly. But the T-gate structure increase extra passivation path then reducing the passivation efficiency. The offset oxide increase the leakage current decrease but the ON-state current reduce. Optimize the offset oxide thickness become more important. The T-gate TFT have high hot carrier endurance because the T-gate structure reduce the drain electric field and also reduce the hot carrier

stress.

4.2 Future works

In above section, we known the Si_3N_4 film as the diffusion barrier then that the hydrogen atoms accumulated at channel layer. However, the channel thickness will affect the plasma treatment efficiency. Because the carrier motion only at the surface of the channel that the trap state defects of the thinner active layer will further reduce by plasma treatment. Otherwise using the excimer laser annealing (ELA) to crystallization active region that the effectively reduce trap state density lower than SPC method. The T-gate TFT with ELA process will non-sensitive to plasma treatment

The T-gate poly-Si thin film transistor can reduce the electric field at the drain junction, but the threshold voltage will slight increase due to the offset region was difficult to form channel. We can combine the buffer nitride layer poly-Si TFTs and T-gate structure to improve the poly-Si TFTs characteristics (as shown in Fig.4.1). Use the lightly doped drain (LDD) process to increasing the channel doped concentration that the threshold voltage decreases (as shown in Fig. 4.2), and modulate the spacer width to optimize the device property.

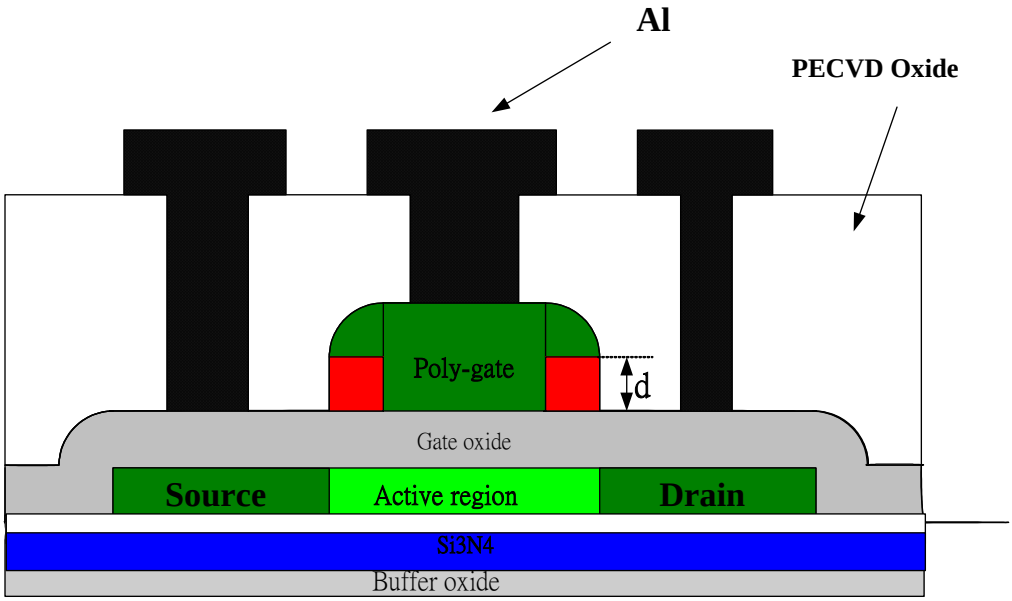

Figure 4.1 A new structure of combine the buffer nitride layer and the T-gate structure poly-Si TFTs

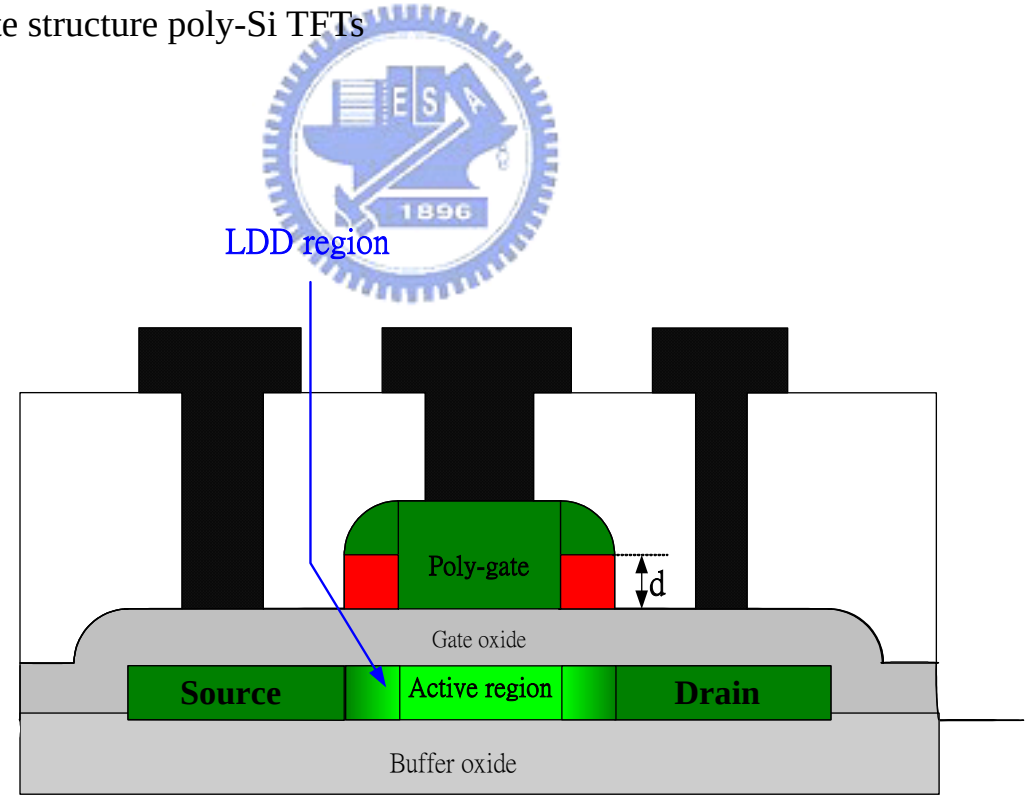

Figure 4.2 A new structure of T-gate poly-Si TFTs with lightly doped drain.