

## Reference

- [1.1] K. Chung, M. P. Hong, C. W. Kim, and I. Kang, "Needs and solutions of future flat panel display for information technology industry," in *IEDM Tech. Dig.*, 2002
- [1.2] J. Ohwada, M. Takabatake, Y. A. Ono, A. Mimura, K. Ono and N. Konish, "Peripheral circuit integrated poly-Si TFT LCD with gray scale representation", *IEEE Trans. Electron Devices*, vol, 36,no. 9, p.1923, 1989.
- [1.3] I. W. Wu, W. B. Jackson, T. Y. Huang, A. G. Lewis and Ciang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation", *IEEE Electron Device Lett.*, vol.12, p. 181, 1991.
- [1.4] Y. Morimoto, Y. Jinno, K. Hirai, H. Ogata, T. Yamada and K. Yoneda, "Influence of the Grain Boundaries and Intragrain Defects on the Performance of Poly-Si Thin Film Transistors", *J. Electrochem. Soc.*, vol. 144, 2495, 1997.
- [1.5] K. Shimizu, O. Sugiura, and M. Matsumura, "On-chip bottom-gate polysilicon and amorphous silicon thin-film transistors using excimer laser annealing," *Jpn. J. Appl. Phys.*, vol. 29, pp. L1775-1777, 1990.
- [1.6] \_\_\_\_\_ "On-chip bottom-gate polysilicon and amorphous silicon thin-film transistors using excimer laser annealing," *Jpn. J. Appl. Phys.*, vol. 29, pp. L1775-1777, 1990.
- [1.7] I.-W. Wu, "Polycrystalline silicon thin film transistors for liquid crystal displays," *Solid State Phenomena*, vol. 37-38, pp. 553-564, 1994.
- [1.8] G. K. Giust, T. W. Sigmon, J. B. Boyce, and J. Ho, "High-performance Laser-Processed Polysilicon Thin-Film Transistors" *IEEE Electron Device Lett.*, vol. 20, NO. 2, 1999
- [1.9] R. B. Iverson and R. Reif, "Stochastic model for grain size versus dose in implanted and annealed polycrystalline silicon films on SiO<sub>2</sub>," *J. Appl. Phys.*, vol. 57, p. 5165, 1985.
- [1.10] T. Noguchi, H. Hayashi and T. Ohshima, "Advanced superthin polysilicon film obtained by Si<sup>+</sup> implantation and subsequent annealing, " *J. Electrochem. Soc.*, vol. 134, p. 1771, 1987.
- [1.11] M. K. Hatalis and D. W. Greve, "Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited

- amorphous silicon films," *J. Appl. Phys.*, vol. 63, p. 2260, 1988.
- [1.12] A. Chiang, T. Y. Huang, I-W. Wu and M. H. Zarzycki, "Effects of silicon implantation and processing temperature on performance of poly-crystalline silicon thin-film transistors fabricated from low temperature CVD amorphous silicon," in *Mat. Res. Soc. Symp. Proc.*, vol.106, p. 305, 1998.
- [1.13] R. C. Cammarata, C. V. Thompson, C. Hayzelden, and K. N. Tu, *J. Mater. Res.*, 5, 2133, 1990.
- [1.14] C. Hayzelden and J. L. Batstone, "Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films," *J. Appl. Phys.*, vol. 73, p.8297, 1993.
- [1.15] S. W. Lee, T. H. Ihn and S. K. Joo, "Low-temperature dopant activation and its application to polycrystalline silicon thin film transistors," *Appl. Phys. Lett.*, vol. 69, p.380, 1996.
- [1.16] M. Miyasaka, K. Makihira, T. Asano, E. Polychroniadis and J. Stoemenos, "In situ observation of nickel metal-induced lateral crystallization of amorphous silicon thin films," *Appl. Phys. Lett.*, vol. 80, p.944, 2002.
- [1.17] C. Hayzelden, J. L. Batstone, "Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films." *J. Appl. Phys.* 73 (12), 15 June 1993.
- [1.18] T. F. Chen, C. F. Yeh and J. C. Lou, "Investigation of grain boundary control in the drain junction on laser-crystalized poly-Si thin film transistors", *IEEE Electron Device Lett.*, vol.24, p. 457, 2003.
- [1.19] C. L. Fan and M. C. Chen, "Performance improvement of excimer laser annealed poly-Si TFTs using fluorine ion implantation," *Electrochem. And Solid State Lett.*, vol. 5, G75, 2002.
- [1.20] K. C. Moon, J. H. Lee and M. K. Han, "improvement of polycrystalline silicon thin film transistors using oxygen plasma pretreatment before laser crystallization" *IEEE Trans. Electron Devices*, vol. 49, p. 1319, 2002.
- [1.21] C. M. Yu, H. C. Lin, T. Y. Huang and T. F. Lei, "H<sub>2</sub> and NH<sub>3</sub> plasma passivation on poly-Si TFTs with bottom-sub-gate induced electrical junction," *J. Electrochem. Soc.*, vol. 150, G843, 2003.
- [1.22] K. Y. Lee, Y. K. Fang, C. W. Chen, K. C. Huang, M. S. Liang and S. G. Wu, "The anomalous behavior of hydrogenated/unhydrogenated polysilicon thin-film transistors under electric stress," *IEEE Electron Device Lett.*, vol.

18, p. 382, 1997.

- [1.23] Y. J. Tung, J. Boyce, J. Ho, X. Huang and T. J. King, "A comparison of hydrogen and deuterium plasma treatment effects on polysilicon TFT performance and DC reliability," *IEEE Electron Device Lett.*, vol. 20, p. 387, 1999.
- [1.24] Keiji Tanaka, Hitoshi Arai, Shigeto Kohda, "Characteristics of Offset-Structure polycrystalline-silicon thin-film transistors" *IEEE Electron Device Lett.*, vol. 9, NO. 1, 1988.
- [1.25] A. Bonfiglietti, M. Cuscuna, A. Valletta, L. Mariucci, A. Pecora, G. Fortunato, S. D. Brotherton, and J. R. Ayres, "Analysis of electrical characteristics of gate overlapped lightly doped drain (GOLDD) polysilicon thin-film transistors with different LDD doping concentration." *IEEE transactions on electron devices*, vol. 50, no. 12, 2003.
- [2.1] B. A. Khan and R. Pandya, "Activation energy of source-drain current in hydrogenated and unhydrogenated polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 1727-1734, 1990.
- [2.2] O. K. B. Lui, M. J. Quinn, S. W-B. Tam, T. M. Brown, P. Migliorato, and H. Ohshima, "Investigation of the low field leakage current mechanism in polysilicon TFT's," *IEEE Trans. Electron Devices*, vol. 45, pp. 213, 1998.
- [2.3] Tsu-jae King, Michael G. Hack, I-Wei Wu "Effective density-of-states distributions for accurate modeling of polycrystalline-silicon thin-film transistors," *J. Appl Phys.* 75 (2), 15 1994
- [2.4] I-Wei Wu, Tiao-Yuan Huang, W. B. Jackson, A. G. Lewis, and Anne Chiang, "Passivation kinetic of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Devices Lett.*, vol. 12, p. 181, 1991.
- [3.1] A. G. Lewis *et al.*, "Degradation of polysilicon TFT's during dynamic stress," *IEDM Tech. Dig.*, p. 575, 1991.
- [3.2] Keiji Tanaka, Hitoshi Arai, Shigeto Kohda, "Characteristics of Offset-Structure polycrystalline-silicon thin-film transistors" *IEEE Electron Device Lett.*, vol. 9, NO. 1, 1988.
- [3.3] Tiemin Zhao, Min Cao, James D. Plummer, Krishna C. Saraswat, "A novel floating gate spacer polysilicon TFT," *IEDM 93. 1993*

- [3.4] C. F. Yeh, C. L. Chen, and G. H. Lin, "The physicochemical properties and growth mechanism of oxide ( $\text{SiO}_{2-x}\text{F}_x$ ) by liquid phase deposition with  $\text{H}_2\text{O}$  addition only," *J. Electrochem.Soc.*, vol. 141, no. 11, p. 3177, 1994
- [3.5] Po-Sheng Shih, Chun-Yen Chang, Ting-Chang Chang, Tiao-Yuan Huang, Du-Zen Peng, Ching-Fa Yeh, "A novel lightly doped drain polysilicon thinfilm transistor with oxide sidewall spacer formed by one-atep selective liquid phase deposition" *IEEE Electron Device Letts*, vol. 20, NO. 8, 1999
- [3.6] K. Kurimoto, S. Odanaka, "A T-gate overlapped LDD device with high circuit performance and high reliability," *IEDM 1991*
- [3.7] Min-Cheol Lee, Sang-Hoon Jung, In-Hyuk Song, Min-Koo Han, "A new poly-Si TFT structure with air cavities at the gate-oxide edges," *IEEE Electron Device Letts*, vol. 22, no. 11, 2001
- [3.8] Han-Wook Hwang, C J Kang, Yong-Sang Kim, "A novel structured polysilicon thin-film transistor that increases the on/off current ratio," *Institute of Physics Publishing Semiconductor Science and Technology 2003*
- [3.9] S. M. Sze "physics of semiconductor devices" John Wiley & Sons central book company.
- [3.10] Du-Zen Peng, Ting-Chang Chang, Chun-Yen Chang, Ming-Liang Tsai, Chun-Hao Tu, Po-Tsun Liu "Characteristics and stress-induced degradation of laser-activated low temoerature polycrystalline silicon thin-film transistors." *Journal of Applied Physics Vol. 93, 2003*
- [3.11] J. Levinson, G. Este, M. Rider, P. J. Scanlon, F. R. Shepherd, and W. D. Westwood, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, no. 2, p. 1193, 1982.