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Application of secondary electron potential contrast on junction leakage isolation

Po-Tsun Liu,[1,a] Jeng-Han Lee,[2] Y. S. Huan,[3] and David Su[3]
[1]*Department of Photonics and Display Institute, National Chiao Tung University, 1001 Ta-Hsueh Rd., HsinChu 300, Taiwan*
[2]*Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., HsinChu 30010, Taiwan*
[3]*Q&R, Taiwan Semiconductor Manufacturing Company, No. 8, Li-Hsin Rd 6, Hsinchu Science Park, Hsinchu 300-77, Taiwan*

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Secondary electron potential contrast (SEPC) technology with an *in situ* dynamic trigger was studied to inspect P^+/N-well junction leakage arising from *P*-well misalignment in a static random access memory cell. Combining SEPC with scanning electron microscopy observations allows direct identification of the junction shift. Furthermore, an *in situ* negative bias applied to the *P*-well can create a wider depletion region and eliminate the leakage path in P^+/N-well contacts, allowing the P^+/N well to operate normally. This proposed *in situ* dynamic trigger method is a promising and effective approach to investigating device physics under a dynamic scope. © *2009 American Institute of Physics*. [doi:10.1063/1.3233963]

Developments in microelectronic integrated circuit technology shrink transistor dimensions to increase device performance. The scaling down of semiconductor devices was initially achieved by simply reducing the physical width of the wells. The first issue related to downscaling the physical well width is controlling photomask alignment and dimension uniformity.[1,2] Poor control can create unwanted leakage paths. Numerous reports have described how to inspect the distribution of implanted dopant profiles in junctions, for instance, chemical delineation uses nitric and fluride acids to selectively etch the heavily doped areas.[3] However, this method has difficulty revealing the precise well profile due to low dosage of the dopants. In addition, wet etching methods are destructive, meaning that the doping area will be etched out permanently. Other methods such as secondary ion mass spectrometry and scanning capacitance microscopropy could work for dopant profile inspection, but they provide insufficient spatial resolution for small areas.[4,5] Recently, secondary electron potential contrast (SEPC) using scanning electron microscopy (SEM) has demonstrated a strong applicability to dopant profile imaging.[6,7] The SEPC signals arise from differences in the built-in potential between different doping areas. Since this inspection method uses the built-in potential of a diode, it affords a nondestructive approach to doping inspection. Numerous publications have conducted studies on materials with wide energy bandgaps, such as SiC;[8] however, SEPC signal inspection is more difficult with silicon having a small band gap energy of 1.1 eV. This study illustrates SEPC inspection of silicon P^+/N-well junctions and also develops a dynamic trigger for isolating P^+/N-well junction leakage.

In this experiment, a static random access memory (SRAM) cell was manufactured for junction study. A *p*-type (100) silicon wafer with a resistivity of 8–12 ohm-cm served as the substrate. After shallow trench isolation (STI), phosphorous dopants were implanted with a dosage of 2.6×10^{13} ions cm^{-2} and an ion energy of 150 keV into the silicon wafer to form the *N* well, while boron implantation was carried out to form a *P*-well region with a dosage of 3.0×10^{13} ions cm^{-2} and an ion energy of 160 keV. After the well formation process, P^+-type source and drain regions were formed by boron implantation with a dosage of 1.5×10^{15} ions cm^{-2} and ion energy of 5 keV. Thermal activation at 1000 °C for 5 s and metallization were carried out sequentially as formal procedures. The sample was plane polished to the contact layer for conductive atomic force microscopy (C-AFM) measurements. The sample was manually polished to the cross section site of interest for cross sectional SEPC inspection. A Hitachi S4700, equipped with a through-the-lens $E \times B$ detector, was the major tool for SEPC inspection. The $E \times B$ detector can remove the high energy tail of the backscattered electron and act as a low pass filter to enhance the SEPC effect on the silicon. An optimum SEM operation conditions were set to view the image of the diode. The secondary electron comes from an inelastic collision between the primary electron and the inner shell electron. The energy of the secondary electron is typically smaller than 50 eV. It is well known that the built-in potential of a diode can be expressed as a function of dopant concentrations:

$$V_{\mathrm{bi}} = \frac{kT}{q} \times \ln\left(\frac{N_a N_d}{N_i^2}\right),$$

where k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and N_a and N_d are the concentration of the acceptors and donors, respectively. N_i is the intrinsic carrier concentration of silicon. For silicon, the maximum built-in potential is equal to its band gap energy of 1.1 eV.

This work studies an SRAM with a high standby current issue. Figure 1(a) depicts the electrical characteristics of tip current versus substrate voltage for leaky and nonleaky P^+/N-well contact regions by C-AFM. The leaky contact suffered early breakdown in its reverse bias region. Figure

[a]Author to whom correspondence should be addressed. Tel.: 886-3-5712121 ext. 52994. FAX: 886-3-5735601. Electronic mail: ptliu@mail.nctu.edu.tw.

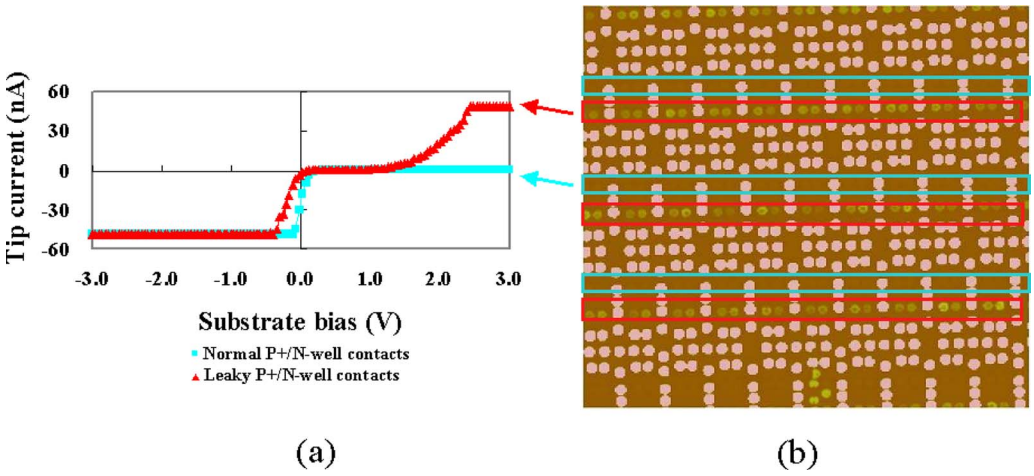

FIG. 1. (Color online) (a) Characteristics of tip current versus substrate voltage for the leaky and nonleaky P^+/N-well contacts. (b) A current map of a SRAM chip under conductive atomic force microscope.

1(b) shows a current map of the SRAM chip under C-AFM. The map indicates that the contacts standing on the P^+/N well exhibited abnormal leakage. The leaky contacts appeared in alternative rows. A misalignment during the manufacture of well region contacts was suspected to be the cause of the leakage.

Figure 2 shows a cross sectional SEPC inspection of the P^+/N-well region, and shows a clear and sharp interface between the P and N wells. The P-well image is bright, and the N-well image is dark. In this case, the P well was shifted a little to the right. In a properly aligned P^+/N-well region, the brighter image of the P^+ contact area would be situated on the darker N-well area. However, a P^+ contact region with a leaky contact on the left side is invisible because the leaky P^+/N well has the same contrast as the N well. No obvious interface was observed between the P^+ and N well in the leaky area. In this study, the SEPC technology directly revealed evidence of P^+/N-well junction leakage originating from a short to the P^+ contact area, due to misalignment of the P well. Applying a negative bias to the P-well region can extend the width of the depletion region between the N and P well—eliminating the leakage path from P^+ to the adjacent P well and returning the electrical operation of the P^+/N-well junction to normal. Figure 3 shows the potential contrast when applying a bias of −1.8 V to the substrate. The image of the leaky P^+ junction reappeared, which means that the P^+/N well will work normally—the negative bias eliminated the leakage path.

The formation of leaky paths due to the P-well misalignment, as well as the effect of negative bias trigger can be illustrated as follows. A misalignment of the P-well region to the right caused the P-type dopant to be implanted in the sidewall of the STI structure, producing a leakage path that passed through the P^+ region to the STI sidewall. As shown in Fig. 4(a), the leakage path passed through the P^+ contact region to the adjacent P-well. SEPC inspection conducted with a floating P-well substrate showed that the depletion width was small. Applying a negative bias of −1.8 V to the P-well increased the depletion area width and pinched off the leakage path from the P^+ region to P-well, as shown in Fig. 4(b). Since this cut off the leakage path, the image of the leaky P^+ region reappeared in the SEPC inspection. Therefore, the proposed *in situ* dynamic trigger effectively isolated the P^+/N-well junction leakage, allowing the junction to operate normally.

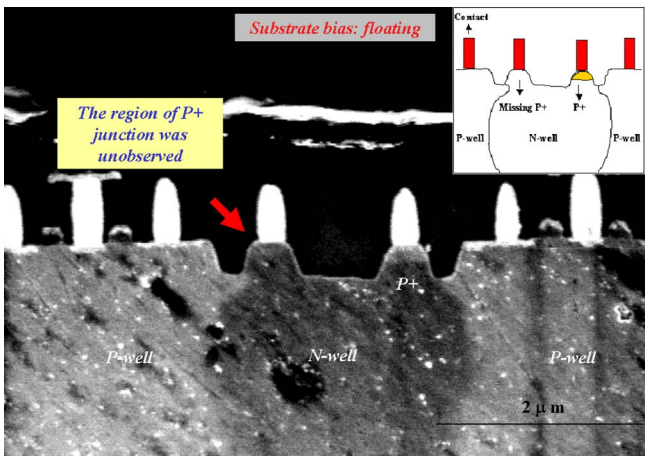

FIG. 2. (Color online) An SEPC image of the P^+/N-well diode with a floating substrate. The inset shown in the upper right corner is a schematic cross section. The P well is shifted a little to the right. A P^+ region with a leaky contact on the left side is not observed, while the image of a nonleaky P^+ contact region on the right is observed clearly.

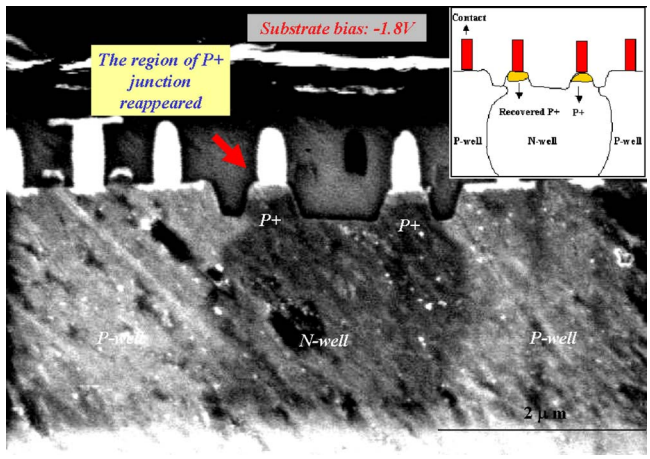

FIG. 3. (Color online) SEPC image of the P^+/N-well diode with a substrate bias of −1.8 V. The inset is a schematic cross section. The previous missing image of P^+ region with leaky contact is clearly seen.

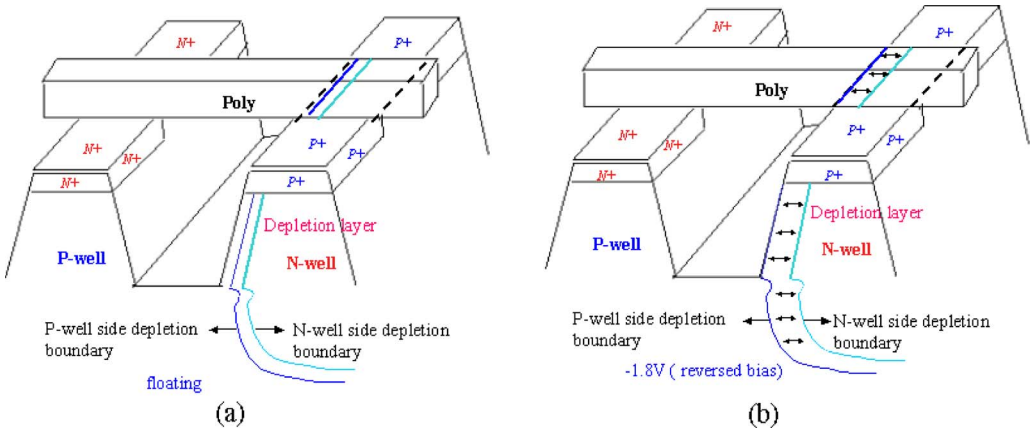

FIG. 4. (Color online) (a) Schematic to demonstrate leakage behavior of the P^+/N-well diode with a floating substrate. (b) Schematic of a P^+/N-well diode with a substrate bias of -1.8 V to demonstrate an extended depletion region for eliminating the leakage path from P^+ to the adjacent P well.

In summary, SEPC proves to be an excellent method for profiling two-dimensional junctions of silicon devices—it can characterize the leakage mechanism in a P^+/N-well junction. A misalignment of P wells was identified as the cause of junction leakage and, in this case, negative substrate biasing created an extended depletion width that eliminated the leakage path. The potential contrast of the leaky P^+/N-well reappeared and normal operation returned. This offers a promising and effective approach to investigating device physics under a dynamic scope.

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