國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

利用複數導數相消之低功率、高線性度混波器

Low-Power and High-Linearity Mixer Adopting Derivative Cancellation by Complex Transconductance Equivalent Circuit

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中 華 民 國 九十四 年 七 月

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摘要

本篇論文提出一個複數轉導的等效電路，藉此應用於多閘極架構之線性度分析，相較於之前所提出的分析，此複數轉導能得到更精確之元件參數，以利於電路設計之用。根據此種分析方法，折疊式混頻器與前端電路分別經由晶片製作來驗證。

第一顆晶片在於設計與分析應用於無線區域網路之低功率、高線性度之混頻器。量測結果顯示此一混頻器在只消耗 1.8 mW 之功率損耗下，有著 4.7 dB 之轉換增益，9 dB 之輸入反迴損耗以及 10.3 dBm 之輸入第三階交會點。

在第二顆晶片中，適用於無線區域網路接收端之低功率前端電路被設計與分析，此電路包含了一個低雜訊放大器，一個相位分離器以及一個直接降頻混頻器。量測結果顯示此前端電路有 9.5 dB 的轉換增益，21.5 dB 之輸入反迴損耗以及-2.6 dBm 之輸入第三階交會點，此外此電路消耗之功率爲 10.1mW.

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ABSTRACT

A compact equivalent circuit using a complex transconductance is proposed for linearity design in the multiple gated transistors configuration. This complex transconductance gives better design parameters as compared to previous published analysis. Following the complex transconductance analysis, a folded mixer and a front-end circuit were verified through two individual.

In the first chip, a low-power and high-linearity mixer is analyzed and designed for wireless local area network. Measured data shows that the designed mixer has conversion gain of 4.7 dB, input return loss of 9 dB, and input third-order intercept point (IIP3) of 10.3 dBm with only 1.8 mW power dissipation.

In the second chip, a low-power front-end circuit, intended for use in the receiver path of the wireless local area network systems, is analyzed and designed. This front-end circuit is composed of a low noise amplifier, a phase splitter, and a direct down-conversion mixer. Measured data shows that the front-end circuit has conversion gain of 9.5 dB, input return loss of 21.5 dB, input third-order intercept point (IIP3) of -2.6 dBm, while consuming only 10.1mW.

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九四年七月

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CHAPTER 1

Introduction

1.1 Motivation

In recent years commercial wireless communication systems have been developed extensively and applied to various applications. The advance of integrated circuit technology helps miniaturize the size and reduce the consumption power of wireless transceivers. Therefore CMOS technology, which is attractive due to its advantages of low cost, high-level integration, and enhancing performance by scaling, becomes popular in system implementation. Until now, research on low-power RF systems is still an emergent topic in order to prolong battery lifetime.

The direct down-conversion receiver becomes more attractive since it has the advantages of low complexity, low power, and less extra components. And it lets system-on-chip become possible. Typical, the first stage of the receiver is a low noise amplifier (LNA), which provides high gain and low noise to suppress the overall system's noise performance. On the other hand, the mixer transforms the radio-frequency (RF) signal into base-band directly and needs high linearity to avoid the distortion of the signal. How to improve the linearity of the mixer without extra power consumption is the main object of this thesis.

In the first one for wireless LAN application, some low-power topology is used to reduce supply voltage. Multiple gated transistors (MGTR) technology is adopted and a compact equivalent circuit using a complex transconductance is proposed for linearity design in this configuration.

In the second one for wireless LAN application, a low-power front-end circuit which includes a LNA, a phase splitter, and the MGTR mixer is designed. The LNA uses L-degeneration to achieve noise and power matching simultaneously. The single-ended signal is transformed into a differential form by the phase splitter. And the mixer provides higher linearity by using MGTR technology.

1.2 Thesis Organization

In the chapter 2 of the thesis, some basic concepts of RF design are introduced. These basic concepts which include the introduction of receiver architecture, WLAN standards, noise and linearity provide the guidance for RF circuit design.

In the chapter 3 of the thesis, the design consideration of some circuit blocks which include LNA, phase splitter and mixer is introduced. Based on these circuits, a mixer and a front-end circuit are designed and verified in later chapter.

In the chapter 4 of the thesis, the nonlinear sources of the device are analyzed. The multiple gated transistors configuration is introduced and a compact equivalent circuit using a complex transconductance is proposed for linearity design in this configuration. Following the above analysis, a low-power and high-linearity direct down-conversion mixer is designed. Finally, measurement result of the mixer chip fabricated by TSMC 0.18um CMOS technology is discussed.

In the chapter 5 of the thesis, a low-power front-end circuit is designed. The first stage is the LNA using inductive source degeneration topology for input matching. The second stage is the phase splitter which transforms single-ended signal into differential form. The last stage is the mixer which is the same as that in chapter 4. Overall front-end circuit is implemented.

In the last chapter, the work is summarized and concluded.

CHAPTER 2

Basic Concepts in RF Design

2.1 Receiver Architecture

2.1.1 Heterodyne Receiver

In heterodyne architectures, the signal band is translated into much lower frequencies by down-conversion mixer, and the filters are used to select the band and channel of the interested signals. In general, the low noise amplifier is placed in front of the down-conversion mixer, since the noise of the down-conversion mixer is high. A simple heterodyne architecture is shown in Fig. 2.1. This architecture is the most reliable reception technique today. But if the cost, complexity, integration and power dissipation are the primary criteria, the heterodyne receiver will become unsuitable due to its complexity and the need for a large number of external components.

Frequency planning is an important thing in heterodyne receiver. For high-side injection, an undesired signal (image) at a frequency of $\omega_{IM} = \omega_{LO} + (\omega_{LO} - \omega_{RF})$ is translated into the same frequency, intermediate frequency (IF), as the desired signal. Similarly, for low-side injection, the image

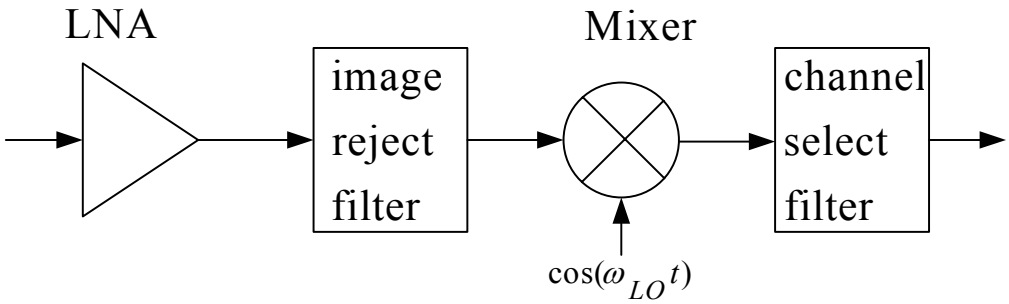


Figure 2.1 Simple heterodyne architecture

frequency is at $\omega_{IM} = \omega_{LO} - (\omega_{RF} - \omega_{LO})$. Therefore the image would cause the distortion of the signal at the intermediate frequency. As shown in Fig. 2.2, some techniques are necessary to suppress the image, such as image reject filter. How to choose the intermediate frequency? If $2\omega_{IF}$ is sufficiently large, the image reject filter will have a relatively small loss in the signal band and a large attenuation in the image band. But a lower $2\omega_{IF}$ will release the quality factor of the channel select filter to get great suppression of nearby interferers. Therefore we must take a trade-off between image rejection and channel selection.

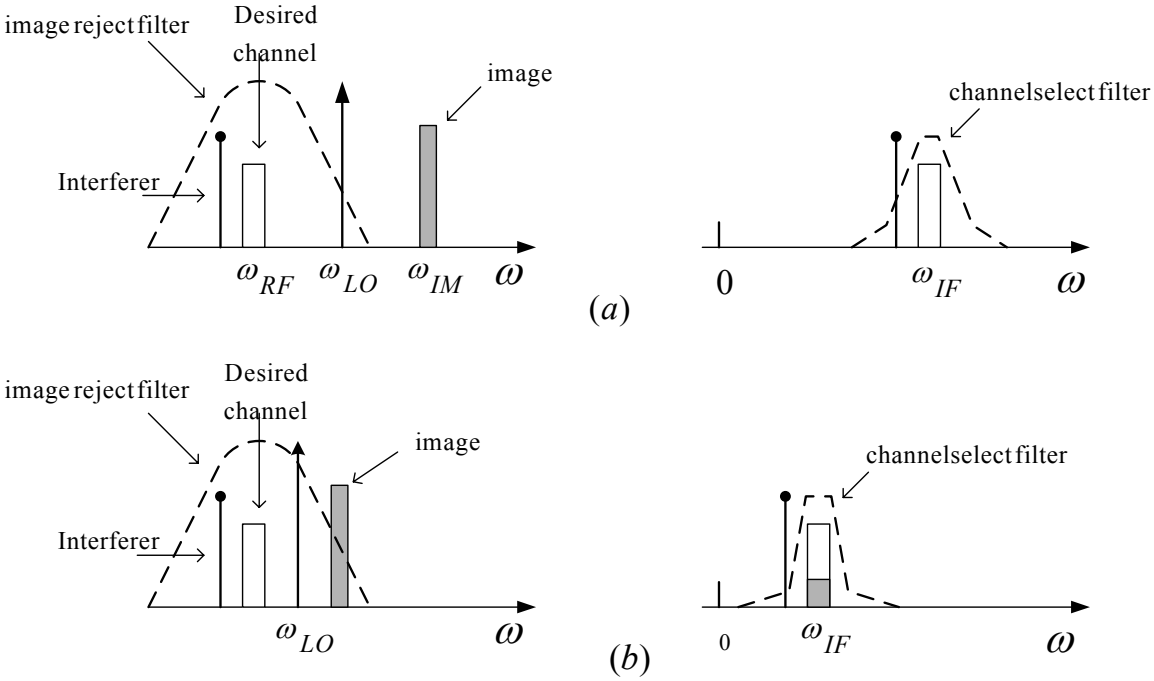


Figure 2.2 Rejection of image versus suppression of interferers for (a) large ω_{IF} (b) small ω_{IF}

2.1.2 Homodyne Receiver

The homodyne receiver is also called “direct-conversion” or “zero-IF” architecture, since the RF signal is directly down-converted to the baseband in the first downconversion. In the homodyne receiver, the LO frequency is equal to the input carrier frequency, and channel selection requires only a low-pass filter with

relatively sharp cutoff characteristics. The simple homodyne architecture is shown in Fig. 2.3. But quadrature outputs are needed for frequency and phase-modulated signals, since the two sides of FM or QPSK spectra carry different information.

In recent years, this architecture becomes the topic of active research gradually due to the following reasons:

(1) The problem of image is removed due to $\omega_{IF} = 0$. Therefore no image filter is required, and the LNA need not drive a 50-Ω load.

(2) It is attractive for monolithic integration because this architecture needs less external components.

For the above reasons, this architecture is suitable for low-power and single-chip design. But some extra issues that do not exist or are not as serious in a heterodyne receiver must be entailed, such as channel selection, DC offset, I/Q mismatch, even-order distortion, and flicker noise.

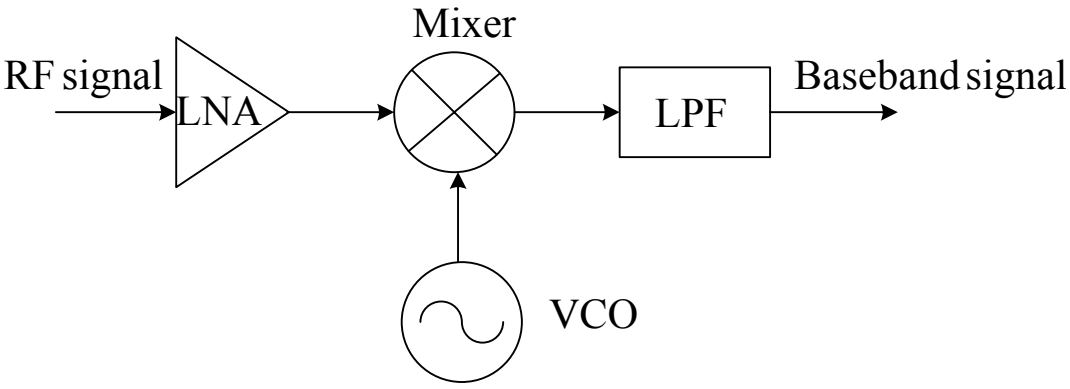


Figure 2.3 Simple homodyne receiver architecture

2.2 Wireless Local Area Network

In recent years, wireless local area networks (WLANs) become an important role in our life gradually. Some standards were established to regulate the development of the

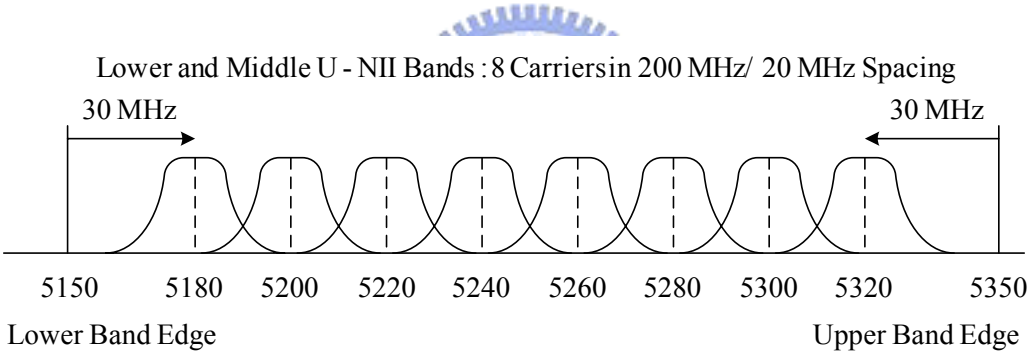
WLNAs. A brief introduction of our application is listed below:

IEEE 802.11a

The IEEE 802.11a standard was defined by the Institute of Electrical and Electronics Engineers in 1999. The channelization scheme for this standard is shown in Table 2.1 and Fig. 2.4, and its physical layer is based on a 52 sub-carriers orthogonal frequency division multiplexing (OFDM) modulation scheme.

Table 2.1 - The set of the channelization

Regulatory domain	Band	Channel center frequencies
United States	U-NII lower band 5.15-5.25 (GHz)	5180 MHz, 5200 MHz 5220 MHz, 5240 MHz
United States	U-NII middle band 5.25-5.35 (GHz)	5260 MHz, 5280 MHz 5300 MHz, 5320 MHz
United States	U-NII upper band 5.725-5.825 (GHz)	5745 MHz, 5765 MHz 5785 MHz, 5805 MHz



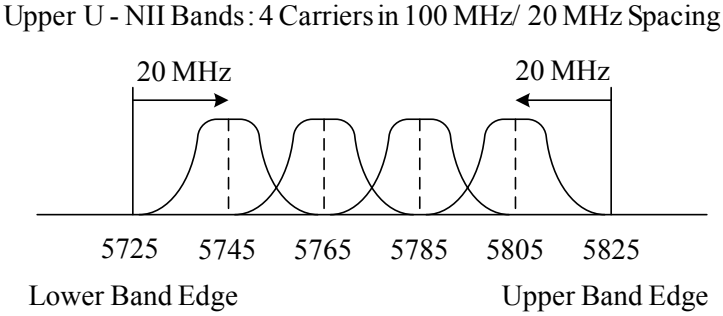


Figure 2.4 802.11a channel distribution

This OFDM system provides a wireless LAN with data payload communication capabilities of 6, 9, 12, 18, 24, 36, 48, 54 Mbits/s, and its rate-dependent modulation parameters is shown in Table 2.2.

Table 2.2 - Rate-dependent parameters

Data rate (Mbits/s)	Modulation	Coding rate	Coded bits per subcarrier	Coded bits per OFDM symbol	Data bits per OFDM symbol
6	BPSK	1/2	1	48	24
9	BPSK	3/4	1	48	36
12	QPSK	1/2	2	96	48
18	QPSK	3/4	2	96	72
24	16-QAM	1/2	4	192	96
36	16-QAM	3/4	4	192	144
48	64-QAM	2/3	6	288	192
54	64-QAM	3/4	6	288	216

For a NF of 10 dB and 5 dB implementation margins, the minimum input levels are shown in Table 2.3, and the maximum input power level is -30 dBm.

Table 2.3 – Receiver performance requirements

Data rate (Mbits/s)	Minimum sensitivity (dBm)	Adjacent channel rejection (dB)	Alternate adjacent channel rejection (dB)
6	-82	16	32
9	-81	15	31
12	-79	13	29
18	-77	11	27
24	-74	8	24
36	-70	4	20
48	-66	0	16
54	-65	-1	15

2.3 Noise Basic

Noise can be loosely defined as any random interference unrelated to the signal of interest, and noise is characterized by a PDF and a PSD. In analog circuits, the signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. But in RF design, most of the front-end receiver blocks are characterized in terms of their noise figure, which is a measure of SNR degradation due to the added noise from the circuit/system, rather than the input-referred noise. Noise factor can be expressed as

$$\text{noise factor} = \frac{\text{total output noise power}}{\text{output noise power due to input source}} \tag{2-1}$$

the noise figure (NF) is simply the noise factor expressed in decibels. If a system has no noise, then noise figure is 0 dB regardless of the gain. In reality, the finite noise of a system degrades the SNR, yielding noise figure > 0 dB. For those whose noise factor is quite close to unity, noise temperature, T_N, is an alternative way of expressing the effect of noise contribution due to its higher-resolution description of noise performance, and is defined as the increase in temperature required of the source resistance for it to account for all of the output noise at the reference temperature T_{ref} (which is 290 K). It is related to the noise factor as follows:

$$\text{noise factor} = 1 + \frac{T_N}{T_{ref}} \Rightarrow T_N = T_{ref} \cdot (\text{noise factor} - 1) \tag{2-2}$$

2.3.1 Noise Source

Thermal noise:

Thermally agitated charge carriers in a conductor constitute a randomly varying current that gives rise to a random voltage due to their Brownian motion. Thermal noise is often called Johnson noise or Nyquist noise. The noise voltage has a zero average value, but a nonzero mean-square value.

In a resistor R, thermal noise can be represented by a series noise voltage source $\overline{v_n^2} = 4kTR\Delta f$ or by a shunt noise current source $\overline{i_n^2} = \frac{4kT\Delta f}{R}$, where k is Boltzmann's constant (about 1.38×10^{-23} J/K), T is the absolute temperature in Kelvins, and Δf is the noise bandwidth. However, purely reactive elements generate no thermal noise.

Shot Noise:

Shot noise occurs in PN junctions, and two conditions for shot noise to occur:

(1) There must be direct current flow.

(2) There must be energy barrier over which a charge carrier hops.

Charge comes in discrete bundles. The randomness of the arrival time gives rise to the whiteness of shot noise. Therefore the shot noise can be modeled by a shunt noise current source $\overline{i_n^2} = 2qI_{DC}\Delta f$, where q is the electronic charge, I_{DC} is the DC current in amperes, and Δf is the noise bandwidth in hertz.

Flicker Noise:

Flicker noise appears as 1/f character and is found in all active devices, as well as in some discrete passive element such as carbon resistors. In diodes, flicker noise is caused by traps associated with contamination and crystal defects in the depletion regions. The traps capture and release carriers in a random fashion and the time constants associated with the process give rise to the 1/f nature of the noise power density. The flicker noise in diode can be represented as $\overline{i_j^2} = \frac{K}{f} \cdot \frac{I}{A_j} \cdot \Delta f$, where K is the process-dependent constant, A_j is the junction area, and I is the bias current. In MOSFET, charge trapping phenomena are invoked in surface, and his type of noise is much greater than that of the bipolar transistor. The flicker noise in MOSFET can be given by

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \approx \frac{K}{f} \cdot \omega_T^2 \cdot A \cdot \Delta f \qquad (2\text{-}3)$$

where K is the process-dependent constant and A is the area of the gate.

2.3.2 Noise Model of MOSFET

The dominant noise source in CMOS devices is channel noise, which basically is thermal noise originated from the voltage-controlled resistor mechanism of a MOSFET. This source of noise can be modeled as a shunt current source in the output

circuit of the device. The channel noise of MOSFET is given by

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \tag{2-4}$$

where γ is bias-dependent factor, and g_{d0} is the zero-bias drain conductance of the device. Another source of drain noise is flicker noise and is given by (2-3). Hence, the total drain noise source is given by

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f + \frac{K}{f}\cdot\frac{g_m^2}{WLC_{ox}^2}\cdot\Delta f \tag{2-5}$$

At RF frequencies, the thermal agitation of channel charge leads to a noisy gate current because the fluctuations in the channel charge induce a physical current in the gate terminal due to capacitive coupling. This source of noise can be modeled as a shunt current source between gate and source terminal with a shunt conductance g_g, and may be expressed as

$$\overline{i_{ng}^2} = 4kT\delta g_g\Delta f \tag{2-6}$$

where the parameter g_g is shown as

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{2-7}$$

and δ is the gate noise coefficient. This gate noise is partially correlated with the channel thermal noise because both noise currents stem from thermal fluctuations in the channel, and the magnitude of the correlation can be expressed as

$$c \equiv \frac{\overline{i_g\cdot i_d^*}}{\sqrt{\overline{i_g^2}\cdot\overline{i_d^2}}} \approx -0.395j \tag{2-8}$$

where the value of -0.395j is exact for long channel devices. Hence, the gate noise can be re-expressed as

$$\overline{i_{ng}^2} = \overline{(i_{ngc}+i_{ngu})^2} = 4kT\delta g_g\Delta f\,|c|^2 + 4kT\delta g_g\Delta f(1-|c|^2) \tag{2-9}$$

where the first term is correlated and the second term is uncorrelated to channel noise. From previous introduction of MOSFET noise source, a standard MOSFET noise model can be presented in Fig. 2.5, where $\overline{i_{nd}^2}$ is the drain noise source, $\overline{i_{ng}^2}$ is the gate noise source, and $\overline{v_{rg}^2}$ is thermal noise source of gate parasitic resistor r_g.

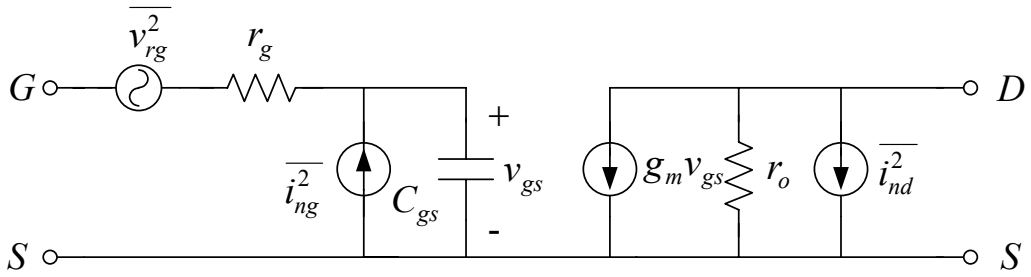


Figure 2.5 Standard noise model of MOSFET

2.3.3 Noise Figure of Cascaded Stages

For a cascade of m stages, the overall noise figure can be characterized by Friis formula

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \ldots + \frac{NF_m - 1}{A_{p(m-1)}} \quad (2\text{-}10)$$

where NF_n is the noise factor of stage n, and A_{pn} denotes the power gain of stage n. This equation indicates that the noise contributed by each stage decreases as the gain preceding the stage increases. Hence, the first few stages in a cascade are the most critical for noise figure. But if a stage exhibits attenuation, then the noise figure of the following circuit is amplified when referred to the input of that stage.

2.4 Linearity Basic

The nonlinearity of the system often leads to interesting and important phenomena,

such as harmonics, gain compression, desensitization, blocking, cross modulation, intermodulation, etc. These distortions will degrade the performance of the system. Volterra series will be used for distortion computations. It can provide designers some information to derive which circuit parameters or circuit elements they have to modify in order to obtain the required specifications. Therefore, we introduce Volterra series in the section.

2.4.1 Fundamental of the Volterra Series

In fact a Volterra series describes a nonlinear system in a way which is equivalent to the way Taylor series approximate an analytic function. A nonlinear system which is excited by a signal with small amplitude can be described by a Volterra series which can be broken down after the first few terms. The higher the input amplitude, the more terms of that series need to be taken into account in order to describe the system behavior properly. For very high amplitudes, the series diverges, just as Taylor series. Hence, Volterra series are only suitable for the analysis of weakly nonlinear circuits.

The Volterra series approach has been proven to very attractive for hand calculations of small transistor networks. Since Volterra kernels retain phase information, they are especially useful for high-frequency analysis.

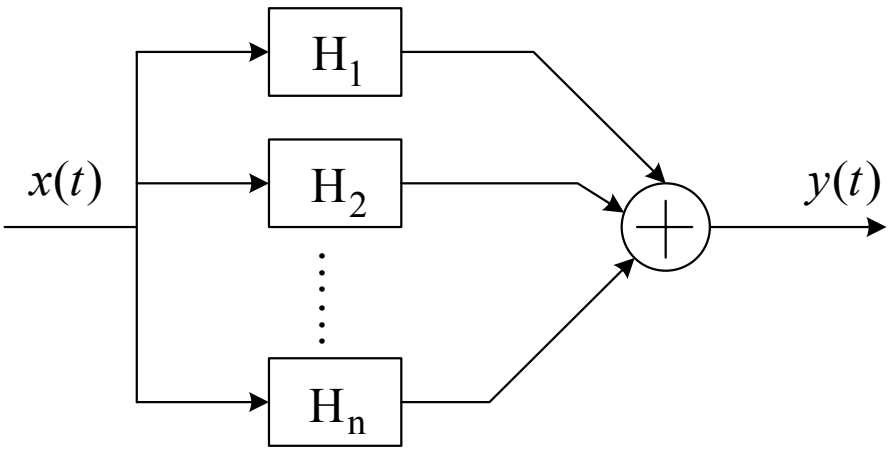


Figure 2.6 Schematic representation of a system characterized by a Volterra series

The theory of Volterra series can be viewed as an extension of the theory of linear, first-order systems to weakly nonlinear systems. And a system is considered as the combination of different operators of different order in the Volterra series description, as shown in Fig. 2.6. Every block H_1, H_2, and H_n represents an operator of order 1, 2, and n, respectively. How much operators must be used is dependent on the input amplitude. In general, the weakly nonlinear effects can be described accurately by taking into account third-order effects only.

In the time domain, the transformation on an input signal, x(t), performed by a nth-order Volterra operator is given by

$$H_n[x(t)] = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \tau_2, \cdots, \tau_n) x(t-\tau_1) x(t-\tau_2) \cdots x(t-\tau_n) d\tau_1 d\tau_2 \cdots d\tau_n \quad (2\text{-}11)$$

the n-dimension integral is seen to be an nth-order convolution integral. The function $h_n(\tau_1, \tau_2, \cdots, \tau_n)$ is an nth-order Volterra kernel. The output of a nonlinear system can be represented as the sum of the output of a first-order Volterra operator with the output of a second-order one, a third-order one, and so on, as shown in Fig. 2.6. The Volterra series representation of the nonlinear system can be expressed as

$$y(t) = H_1[x(t)] + H_2[x(t)] + H_3[x(t)] + \cdots + H_n[x(t)] \quad (2\text{-}12)$$

In the frequency domain, the nth-order Volterra kernel can be given by

$$H_n(s_1, \cdots, s_n) = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \cdots, \tau_n) e^{-(s_1\tau_1 + \cdots + s_n\tau_n)} d\tau_1 d\tau_2 \cdots d\tau_n \quad (2\text{-}13)$$

and is called the nth-order nonlinear transfer function or the nth-order kernel transform.

2.4.2 Nonlinear Performance Parameters in Terms of Volterra Kernels

When a system that can be described by a Volterra series up to order three, is excited by the sum of two sinusoidal excitations $A_1 \cos \omega_1 t$ and $A_2 \cos \omega_2 t$, then the output is given by the sum of the responses listed in Table 2.4. From Table 2.4, the

Table. 2.4 Different responses at the output of a nonlinear system described by Volterra kernels.

Order	Frequency of response	Amplitude of response	Type of response
1 1	ω_1 ω_2	$A_1\lvert H_1(j\omega_1)\rvert$ $A_2\lvert H_1(j\omega_2)\rvert$	Linear
2 2	$\omega_1+\omega_2$ $\lvert\omega_1-\omega_2\rvert$	$A_1A_2\lvert H_2(j\omega_1,j\omega_2)\rvert$ $A_1A_2\lvert H_2(j\omega_1,-j\omega_2)\rvert$	2nd-order intermodulation products
2 2	$2\omega_1$ $2\omega_2$	$\frac{1}{2}A_1^2\lvert H_2(j\omega_1,j\omega_1)\rvert$ $\frac{1}{2}A_2^2\lvert H_2(j\omega_2,j\omega_2)\rvert$	2nd harmonics
2 2	0 0	$\frac{1}{2}A_1^2\lvert H_2(j\omega_1,-j\omega_1)\rvert$ $\frac{1}{2}A_2^2\lvert H_2(j\omega_2,-j\omega_2)\rvert$	DC shift
3 3 3 3	$2\omega_1+\omega_2$ $\lvert 2\omega_1-\omega_2\rvert$ $\omega_1+2\omega_2$ $\lvert\omega_1-2\omega_2\rvert$	$\frac{3}{4}A_1^2A_2\lvert H_3(j\omega_1,j\omega_1,j\omega_2)\rvert$ $\frac{3}{4}A_1^2A_2\lvert H_3(j\omega_1,j\omega_1,-j\omega_2)\rvert$ $\frac{3}{4}A_1A_2^2\lvert H_3(j\omega_1,j\omega_2,j\omega_2)\rvert$ $\frac{3}{4}A_1A_2^2\lvert H_3(j\omega_1,-j\omega_2,-j\omega_2)\rvert$	Third-order intermodulation products
3 3	$\omega_1+\omega_2-\omega_2=\omega_1$ $\omega_1-\omega_1+\omega_2=\omega_2$	$\frac{3}{4}A_1A_2^2\lvert H_3(j\omega_1,j\omega_2,-j\omega_2)\rvert$ $\frac{3}{4}A_1^2A_2\lvert H_3(j\omega_1,-j\omega_1,j\omega_2)\rvert$	Third-order desensitization
3 3	$2\omega_1-\omega_1=\omega_1$ $2\omega_2-\omega_2=\omega_2$	$\frac{3}{4}A_1^3\lvert H_3(j\omega_1,j\omega_1,-j\omega_1)\rvert$ $\frac{3}{4}A_2^3\lvert H_3(j\omega_2,j\omega_2,-j\omega_2)\rvert$	Third-order compression or expansion
3 3	$3\omega_1$ $3\omega_2$	$\frac{1}{4}A_1^3\lvert H_3(j\omega_1,j\omega_1,j\omega_1)\rvert$ $\frac{1}{4}A_2^3\lvert H_3(j\omega_2,j\omega_2,j\omega_2)\rvert$	Third harmonics

expressions for the second and third harmonic distortion in terms of general Volterra are given by

$$HD_2 = \frac{A_1}{2}\left|\frac{H_2(j\omega_1, j\omega_1)}{H_1(j\omega_1)}\right| \tag{2-14}$$

$$HD_3 = \frac{A_1^2}{4}\left|\frac{H_3(j\omega_1, j\omega_1, j\omega_1)}{H_1(j\omega_1)}\right| \tag{2-15}$$

Furthermore, among the intermodulation products, the third-order intermodulation products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ is important. Since if the difference between ω_1 and ω_2 is small, the distortions at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will appear in the vicinity of ω_1 and ω_2. Using Table 2.4 the third-order intermodulation distortion in terms of Volterra kernel transforms

$$IM_3 = \frac{3}{4}A_2^2\left|\frac{H_3(-j\omega_1, j\omega_2, j\omega_2)}{H_1(j\omega_1)}\right| \tag{2-16}$$

This effect causes some distortion at our desired frequency and damages desired signals. Therefore third intercept point (IP3) is used to characterize this behavior. This parameter is measured by supplying a two-tone signal to the system. This input signal must be chosen to be sufficiently small in order to remove higher-order nonlinear terms. In a typical test, A_1=A_2=A, hence the magnitude of third-order intermodulation products grows at three times the rate at which the fundamental signal on a logarithmic scale when input signal increases. The third-order intercept point is defined to be the point at which third-order intermodulation product equals to the fundamental signal, and the corresponding input signal is called input IP3 (IIP3) and the corresponding output signal is called output IP3 (OIP3). The A_{IP3}, therefore, can be obtained by setting $IM_3 = 1$ and expressing as

$$A_{IP3}^2 = \frac{4}{3}\left|\frac{H_1(j\omega_1)}{H_3(-j\omega_1, j\omega_2, j\omega_2)}\right| \tag{2-17}$$

Besides, a quick method of measuring IIP3 is as follows. As shown in Fig. 2.7, If the power of the two-tone signal, P_{in}, is small enough to ignore higher order nonlinear terms, then IIP3 can be expressed as

$$IIP_3\ |_{dBm} = \frac{\Delta P\ |_{dB}}{2} + P_{in}\ |_{dBm} \tag{2-18}$$

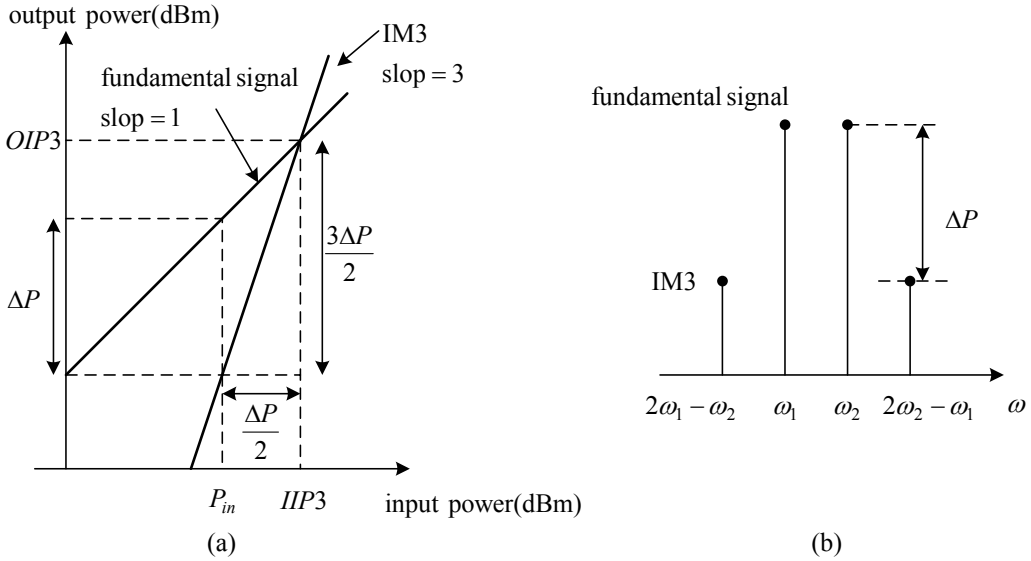


Figure 2.7 (a) Growth of output components in an intermodulation test
(b) Intermodulation distortion

CHAPTER 3

Design Consideration in Front-End Circuit Design

3.1 Low Noise Amplifier Basic

Low noise amplifier is the first gain stage in the receive path so its noise figure directly adds to that of the system. There, therefore, are several common goals in the design of LNA. These include minimizing noise figure of the amplifier, providing enough gain with sufficient linearity and providing a stable 50 Ω input impedance to terminate an unknown length of transmission line which delivers signal from antenna to the amplifier [5]. Among LNA architectures, inductive source degeneration is the most popular method since it can achieve noise and power matching simultaneously, as shown in Fig. 3.1. The following analysis is based on this architecture.

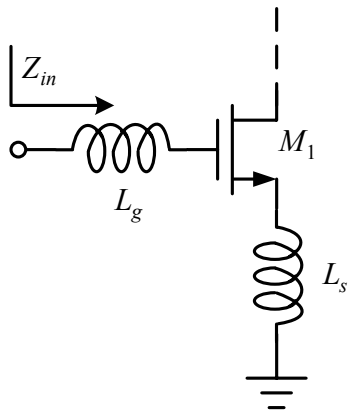


Figure 3.1 Common-source input stage with inductive source degeneration

3.1.1 Low Noise Amplifier Architecture Analysis

In Fig. 3.1, the input impedance can be expressed as

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s$$
$$= \left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s \quad at \quad \omega = \omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{3-1}$$

As shown in (3-1), the input impedance is equal to the multiplication of cutoff frequency of the device and source inductor at resonant frequency. Therefore it can be set to 50 Ω for input matching while resonant frequency is designed to be equal to the operating frequency.

According to prior introduction, the equivalent noise model of common-source LNA with inductive source degeneration can be expressed as Fig. 3.2, where R_l is the parasitic resistance of the inductor, R_g is the gate resistance of the device. Note that the overlap capacitance C_{gd} has also been neglected in the interest of simplicity. Then the noise figure can be obtained by computing the total output noise power and output noise power due to input source. To find the output noise, we first evaluate the transconductance of the input stage. With the output current proportional to the voltage on C_{gs} and noting that the input circuit takes the form of series-resonant network, the transconductance at the resonant frequency can be expressed as

$$G_m = g_m Q_{in} = \frac{g_m}{\omega_o C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega_o R_s} \tag{3-2}$$

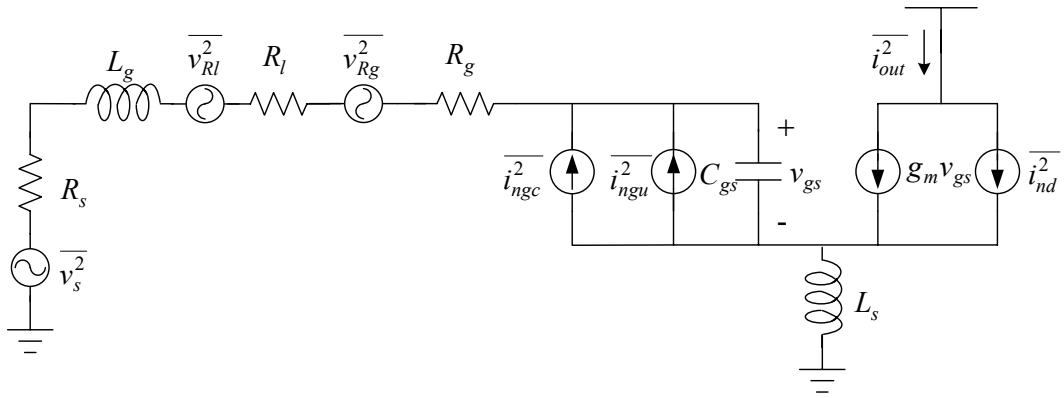


Figure 3.2 Equivalent noise model of Figure 3.1

where Q_{in} is the effective Q of the amplifier input circuit. So the output noise power density due to the source can be expressed as

$$S_{a,Rs}(\omega_o) = S_{Rs} G_{m.eff}^2 = \frac{4kT\omega_T^2}{\omega_o^2 R_s (1+\frac{\omega_T L_s}{R_s})^2} \tag{3-3}$$

In the similar way, the output noise power density due to R_g and R_l is

$$S_{a,R_g,R_l}(\omega_o) = \frac{4kT(R_g + R_l)\omega_T^2}{\omega_o^2 R_s^2 (1+\frac{\omega_T L_s}{R_s})^2} \tag{3-4}$$

Furthermore, channel current noise of the device is the dominant noise contributor, and its noise power density associated with the correlated portion of the gate noise can be expressed as

$$S_{a,i_{nd},i_{ngc}}(\omega_o) = \frac{4kT\gamma\kappa g_{do}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{3-5}$$

where γ is the coefficient of channel thermal noise, $\alpha = g_m / g_{d0}$ and

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1 + |c| Q_L \sqrt{\frac{\delta\alpha 2}{5\gamma}}\right]^2 \tag{3-6}$$

$$Q_L = \frac{1}{\omega_o R_s C_{gs}} \tag{3-7}$$

The last noise term is the contribution of the uncorrelated portion of the gate noise, and its output noise power density can be expressed as

$$S_{a,i_{ngu}}(\omega_o) = \frac{4kT\gamma\xi g_{do}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{3-8}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q_L^2) \tag{3-9}$$

According to (3-3), (3-4), (3-5) and (3-8), the noise figure at the resonant frequency can be expressed as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma\chi}{\alpha Q_L}\left(\frac{\omega_o}{\omega_T}\right) \tag{3-10}$$

where

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1+Q_L^2) \tag{3-11}$$

From (3-11), we observe that χ includes the terms which are constant, proportional to Q_L, and proportional to Q_L^2. It follows that (3-11) will contain terms which are proportional to Q_L as well as inversely proportional to Q_L. A minimum noise figure, therefore, exits for a particular Q_L.

3.1.2 Optimizations of Low Noise Amplifier Design Flow

The analysis of the previous section can now be drawn upon in designing the LNA. In order to pick the appropriate device size and bias point to optimize noise performance given specific objectives for gain and power dissipation, a simple second-order model of the MOSFET transconductance can be employed which accounts for high-field effects in short channel devices. Assuming that the drain current, I_d, has the form

$$I_{DS} = WC_{ox}v_{sat}\frac{(V_{gs}-V_T)}{1+\frac{LE_{sat}}{V_{gs}-V_T}} = WC_{ox}v_{sat}LE_{sat}\frac{\rho^2}{1+\rho} \tag{3-12}$$

where $\rho \equiv \frac{V_{gs}-V_T}{LE_{sat}}$. And the (3-7) can be replace as

$$Q_L = \frac{3}{2\omega_o WLC_{ox}R_s} \Rightarrow C_{ox} = \frac{3}{2R_sQ_L\omega_o WL} \tag{3-13}$$

The power consumption of the LNA, therefore, can be expressed as

$$P_D = V_{DD} I_{DS} = \frac{3}{2} V_{DD} \frac{1}{Q_L R_s \omega_o} v_{sat} E_{sat} \frac{\rho^2}{1+\rho} \tag{3-14}$$

The noise figure can be expressed in terms of P_D and V_{gs}. Two parameters linked to power dissipation need to be accounted for.

$$\omega_T \approx \frac{g_m}{C_{gs}} = f_1(V_{gs}) \tag{3-15}$$

$$Q_L = \frac{3V_{DD} v_{sat} E_{sat}}{2P_D \omega_o R_s} \frac{\rho^2}{1+\rho} = \frac{P_o}{P_D} \frac{\rho^2}{1+\rho} = f_2(V_{gs}, P_D) \tag{3-16}$$

where $P_o = \frac{3V_{DD} v_{sat} E_{sat}}{2\omega_o R_s}$.

The noise figure of the LNA, therefore, can be expressed as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha Q_L} \left(\frac{\omega_o}{\omega_T} \right) \left(1 + 2|c| Q_L \sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma} (1 + Q_L^2) \right) = f(V_{gs}, P_D) \tag{3-17}$$

In general, there are two approaches to optimize noise figure. The first approach assumes a fixed transconductance, G_m. The second approach assumes fixed power consumption.

(1) Fixed G_m optimization: To fix the value of the transconductance, G_m, we need only assign a constant value to ρ. Once ρ is determined, the optimization of the noise figure can be obtained by (3-17):

$$\left. \frac{\partial f(V_{gs}, P_D)}{\partial P_D} \right|_{fixed\,Vgs} = 0 \Rightarrow P_{D.opt} \Rightarrow Q_{L.opt} \Rightarrow F = f(V_{gs}, P_{D.opt}) \tag{3-18}$$

From (3-13), we can obtain the optimal width to get the minimal noise figure for a given G_m under the assumption of matched input impedance. In this approach, the designer can achieve high gain and low noise performance by selecting the desired transconductance, but its disadvantage is that we must sacrifice the power consumption to achieve minimum noise figure.

(2) Fixed P_D optimization: An alternative method of optimization fixes the power dissipation and adjusts device size and bias point to minimize the noise figure. Once P_D is determined, the optimization of the noise figure can be obtained by (3-19):

$$\left.\frac{\partial f(V_{gs}, P_D)}{\partial V_{gs}}\right|_{fixed\ P_D} = 0 \Rightarrow V_{gs.opt} \Rightarrow Q_{L.opt} \Rightarrow F = f(V_{gs.opt}, P_D) \quad (3\text{-}19)$$

Then the optimum device size can be obtained to get the best noise performance for fixed power dissipation. In this approach, the designer can specify the power dissipation and find the optimal noise performance, but its disadvantage is that the transconductance is held up by the optimal noise condition.

3.2 Phase Splitter Basic

Differential phase splitters are basic cells required in microwave components such as balanced mixers, multipliers, and phase shifters. An ideal differential phase splitter will generate a 180 degree phase difference at its two outputs and the same magnitude of the power at each output from a single input [16].

In RFIC, there are passive and active differential phase splitters. The passive differential phase splitters can be achieved by using the LC networks or microstriplines. But the spiral inductors, MIM capacitors, and microstriplines are too expensive due to their larger physical size at lower microwave frequencies. Besides, the passive differential phase splitters may cause some signal loss. There are three categories of active differential phase splitters normally employed in lower microwave frequencies for wireless communications: single FET circuits, common-gate common-source circuits, and differential amplifier circuits. The differential amplifier circuit is the most popular architecture in recent years, and

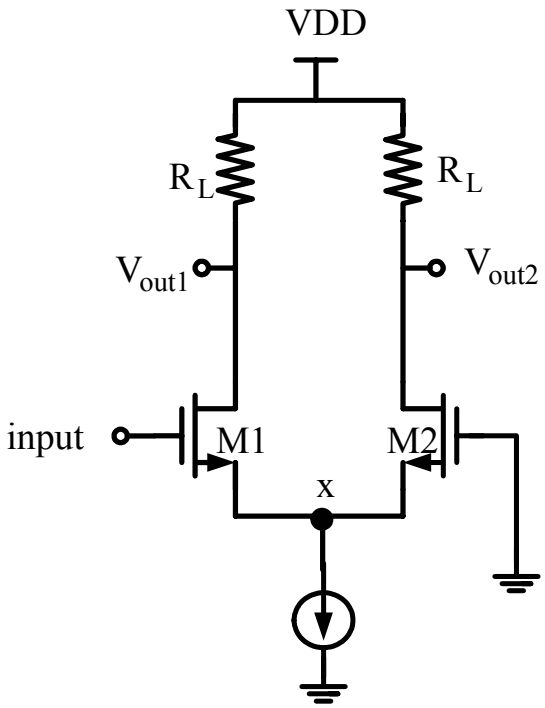


Figure 3.3 Differential pair amplifier

therefore the following introduction is based on this architecture.

The differential amplifier circuit is shown in Fig. 3.3. Ideally, this circuit will provide equal amplitude and 180 degree phase difference. However, the finite impedance at node x caused by strong parasitic at high frequency will affect the phase difference and gain balance of the circuit.

Now, we assume that the common source input impedance of M1 and M2 equals Z. The input ac signal v_{in} can be expressed as

$$v_{in} = v_{gs1} - v_{gs2} \tag{3-20}$$

and the v_{gs1} and v_{gs2} have the following relation as

$$-\frac{v_{gs2}}{v_{gs1}} = \frac{R_{source} // Z}{Z} = \frac{R_{source}}{R_{source} + Z} \tag{3-21}$$

where R_{source} is the input impedance of the current source.

In practice, the value of the R_{source} is finite. This will cause that $|v_{gs1}| > |v_{gs2}|$ and their phase difference is not 180 degree. The output signal, therefore, will not balance,

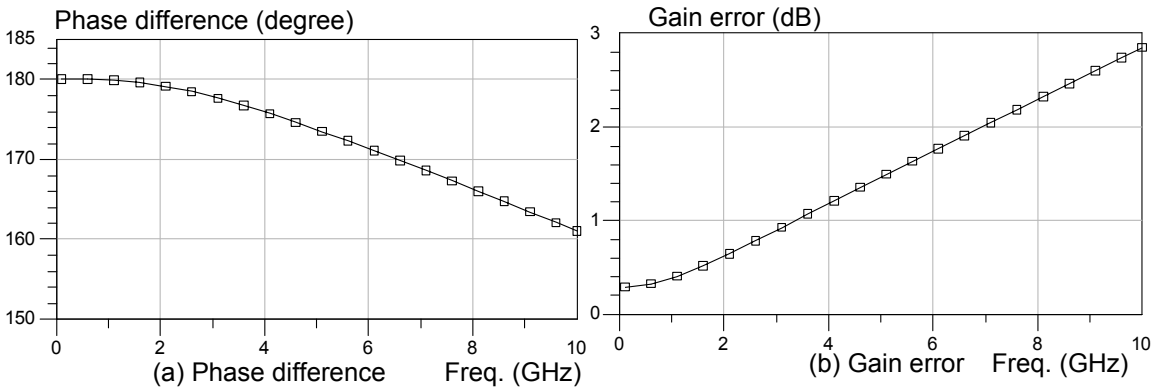


Figure 3.4 Simulated results of Fig. 3.3 (a) phase difference (b) gain error

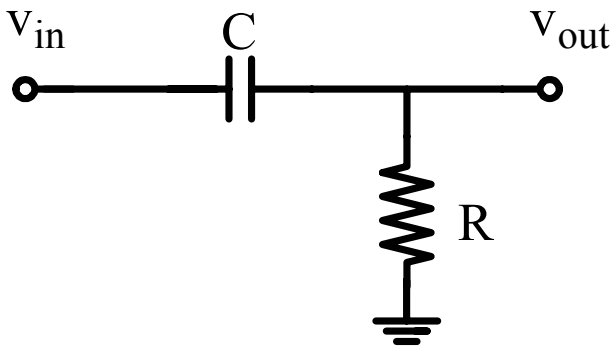


Figure 3.5 Phase compensation circuit

as shown in Fig. 3.4. To overcome this problem, some compensation method must be used.

To let the magnitude of the v_{gs1} and v_{gs2} be equal and the phase difference of the v_{gs1} and v_{gs2} equals 180 degree, a RC feedback circuit shown in Fig. 3.5 can be used to compensate phase error [15]. The phase difference between input port and output port can be expressed as

$$PhaseShift = 90 - \tan^{-1}(RC\omega) \qquad (3\text{-}22)$$

So we can obtain a desirable phase shift at the desired frequency by choosing proper value of R and C.

Fig. 3.6 shows the schematic of the phase splitter with RC compensation. The current source is realized by an active device. R_1 and R_2 are used to bias the transistors, M1 and M2, and their parallel resistance will be the resistance of the Fig.

3.5. The resistor, R_f, is used to compensate the gain error. The relation between the v_{d1} and v_{g2} can be expressed as

$$v_{g2} = v_{d1} \frac{R_{eq} // Z_1}{(R_{eq} // Z_1) + 1/\omega C_f + R_f} \tag{3-23}$$

where $R_{eq} = R_1 // R_2$ and Z_1 is the input impedance of M2 . The v_{g2}, therefore, can be adjusted by changing the value of R_{eq}, C_f, R_f, and Z_1. The phase error can be compensated by proper selection of R_{eq} and C_f, and the gain balance is achieved by adjusting the value of R_{eq}, C_f, R_f, and Z_1.

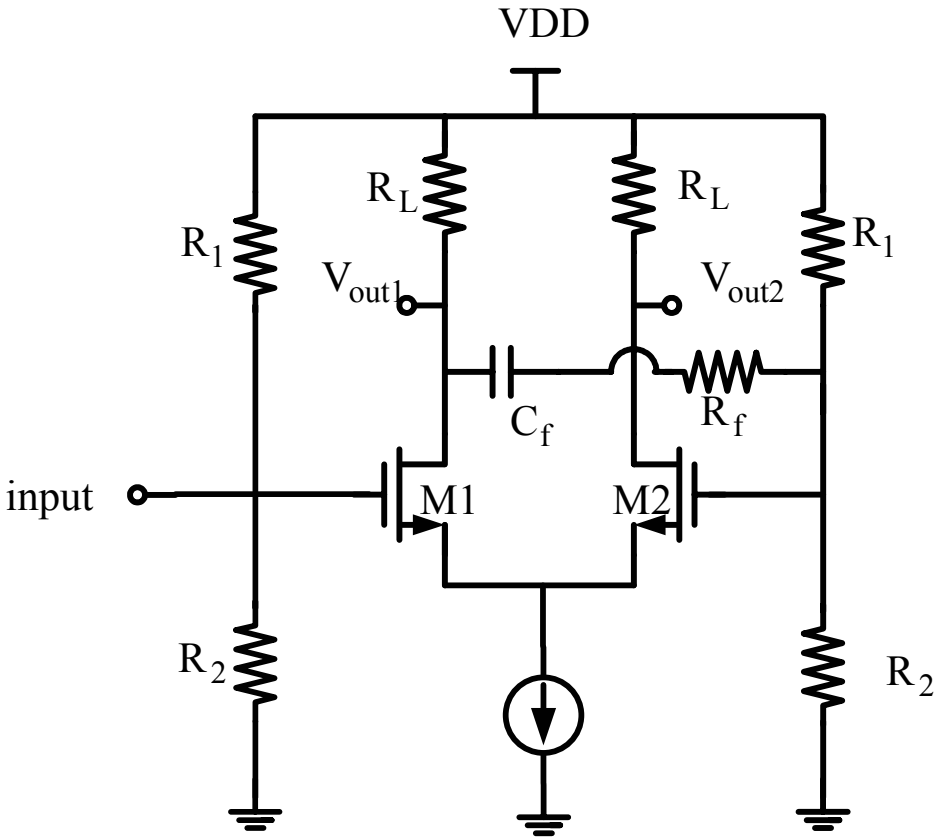


Figure 3.6 Phase splitter with RC compensation

3.3 Down-Conversion Mixer Basic

The purpose of the mixer is to convert a signal from one frequency to another. In a receiver, this conversion is from radio frequency to intermediate frequency or zero-IF. Mixing requires a circuit with a nonlinear transfer function, since nonlinearity is

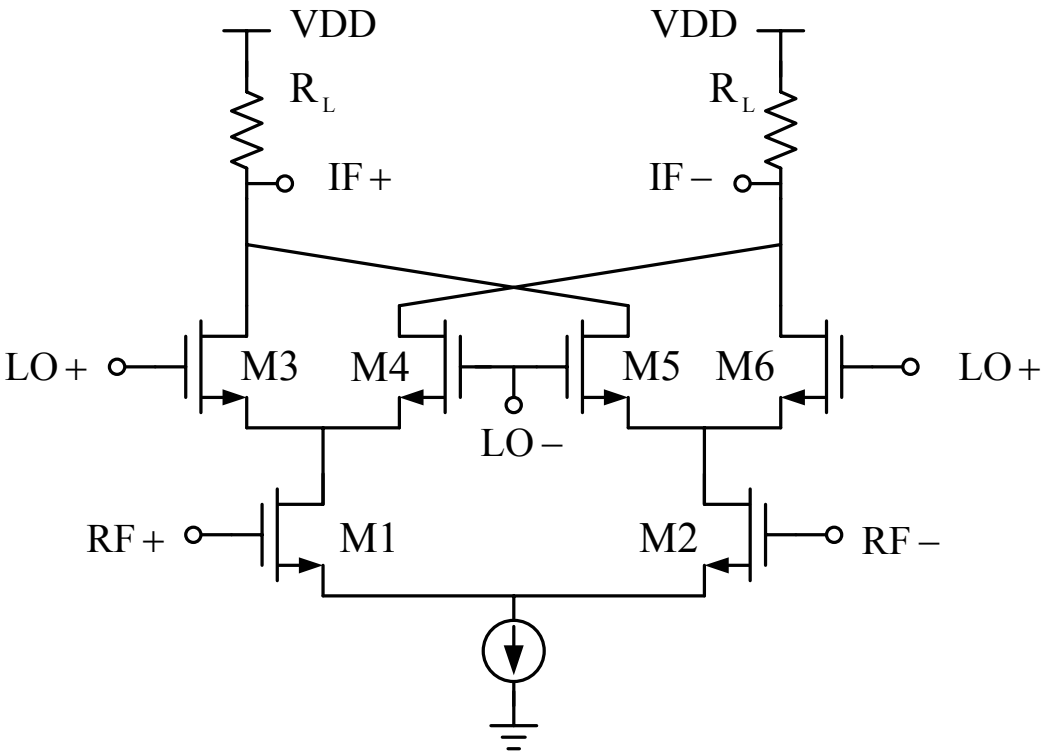


Fig. 3.7 Simplified CMOS Gilbert Cell mixer

fundamentally necessary to generate new frequencies. Fig. 3.7 shows a simplified CMOS Gilbert Cell mixer, which is composed of transconductance stage and switching stage.

The RF input must be linear, or adjacent channels could intermodulate and interfere with the desired channel. And the third-order intermodulation term from the two other signals will be directly on top of the desired signal. The LO input need not be linear, since the LO is clean and of known amplitude. In fact, the LO input is usually designed to switch the upper quad so that for half the cycle M3 and M6 are on and taking all current to output loading. For the other half of the LO cycle, M3 and M6 are off and M4 and M5 are on. This stage will be, therefore, like switch to mixing RF signal to IF signal.

3.3.1 Conversion Gain

The gain of mixers must be carefully defined to avoid confusion. The voltage

conversion gain of a mixer is defined as the ratio of the rms voltage of the IF signal and rms voltage of the RF signal. Note that the frequencies of these two signals are different. The power conversion gain of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source. If the impedances are both matched to 50 Ω, then the voltage conversion gain and power conversion gain of the mixer are equal when they are expressed in decibels.

Now, we assume that M3-M6 work like an ideal switch, and the conversion transconductance of the mixer can be expressed as

$$G_c = \frac{2}{\pi} g_m \tag{3-24}$$

where gm is the transcondcutanc of M1 and M2, and 2/π is produced by switching stage.

3.3.2 Switching Stage

For small LO amplitude, the amplitude of the output depends on the amplitude of the LO signal. Thus, gain is larger for larger LO amplitude. For Large LO signals, the upper quad switches and no further increase occur. Thus, at this point, there is no longer any sensitivity to LO amplitude. Besides, if upper quad transistors are alternately switched between completely off and fully on, the noise will be minimized. Since upper transistor contributes no noise when it is fully off, and when fully on, the upper transistor behaves like a cascode transistor which does not contribute significantly to noise.

The large LO signal is required to let upper quad transistors achieve complete switching. But if the LO voltage is made too large, a lot of current has to be moved into and out of the transistors during transitions. This can lead to spikes in the signals and can actually reduce the switching speed and cause an increase in LO feed-through.

Thus, too large a signal can be just as bad as too small a signal.

3.3.3 Mixer Noise

Noise figure for a mixer is defined as

$$\text{noise factor} = \frac{\text{total output noise power at the IF}}{\text{output noise power at IF due to input source}} \tag{3-25}$$

In general, the noise figure of the mixer is divided to two categories, single-sideband (SSB) noise figure and double-sideband (DSB) noise figure. The difference between the two definitions is the value of the denominator in (3-25). In the case of SSB noise figure, only the noise at the output frequency due to the source that originated at the RF frequency is considered, and it is usually used in heterodyne systems. In the case of DSB noise figure, all the noise at the output frequency due to the source is considered (noise of the source at the input and image frequencies), and it is usually used in homodyne systems.

Because of the added complexity and the presence of noise that is frequency translated, mixers tend to be much noisier than LNAs. In generally, mixers have three frequency bands where noise is important:

(1) Noise already presents at the IF: The transistors and resistors in the circuit will generate noise at the IF. Some of this noise will make it to the output and corrupt the signal.

(2) Noise at the RF and image frequency: The noise presents at the RF and image frequency will be mixed down to the IF.

(3) Noise at multiples of the LO frequencies: Any noise that is near a multiple of the LO frequency can also be mixed down to the IF, just like the noise at the RF.

Besides, the flicker noise will become more important in the homodyne receiver. In the design of the direct down-conversion mixer, how to reduce the flicker noise of

upper quad transistors is the important thing. According to (2-3), this noise can be reduced by increasing the device size for a given g_m.

3.3.4 Port-to-Port Isolation

The isolation between each two ports of a mixer is critical. The LO-RF feed-through results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO feed-through allows strong interferers in the RF path to interact with the local oscillator driving the mixer. The LO-IF feed-through is important because if substantial LO signal exists at the IF output even after low-pass filtering, then the following stage may be desensitized. Fortunately, this feed-through can be reduced largely by used the double-balanced architecture. Finally, the RF-IF isolation determines what fraction of the signal in the RF path directly appears in the IF, a critical issue with respect to the even-order distortion problem in homodyne receivers.

The required isolation levels greatly depend on the environment in which the mixer is employed. If the isolation provided by the mixer is inadequate, the preceding or following circuits may be modified to remedy the problem.

3.3.5 Linearity

As far as cascaded stages are concerned, linearity is a very important performance in mixer stage. In general, it will dominate the distortion of the entire receiver. The detail analysis will be introduced in Chapter 4.

CHAPTER 4

5.5 GHz Low-Power and High-Linearity Mixer

The mixer is based on the conventional doubly balanced CMOS Gilbert Cell mixer, as shown in Fig. 3.7 and it is composed of transconductance stage, mixing stage, load impedance and current source. The doubly balanced configuration exhibits following advantages:

(a) It generates less even-order distortion resulted from transconductance stage.

(b) It has less LO-IF feed-through. Because the differential pairs M3-M4 and M5-M6 add the amplified LO signal with opposite phases, thereby providing a first-order cancellation.

4.1 Low-Power Design Consideration

Since each of conducting MOSFETs are ideally in saturation, the expected drain to source voltage is $V_T + 200mV$, neglecting body effect. Consequently, this architecture needs at least $3V_T + 600mV$. This high voltage is not suitable for low-power design therefore we adopt following techniques to reduce supply voltage.

4.1.1 Low Voltage Topology

In order to reduce supply voltage, we adopt a typical low-voltage topology shown in Fig. 4.1(a). This topology uses two RF traps and one coupling capacitor. The function of the RF traps is provide a low impedance across its terminals at dc and high impedance at RF, and the function is usually realized by using on-chip LC tanks. The function of the coupling capacitor is used to couple the RF energy between the two

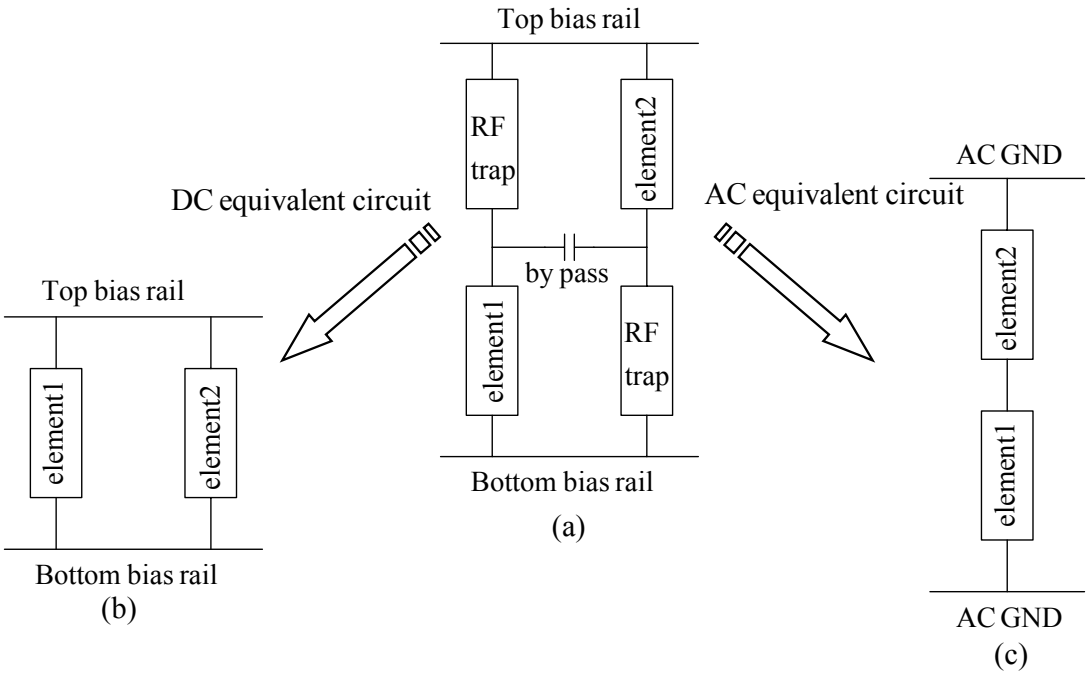


Figure 4.1 Low-voltage topology

elements. Therefore the dc equivalent circuit becomes two independent biasing paths, as shown in Fig. 4.1(b), and the function of the ac equivalent circuit is the same as that of the cascode topology [3]. So this topology can achieve following advantages:

(a) Lower supply voltage.

(b) The property of the cascode topology is retained.

(c) The two paths can be biased at different bias condition based on the different consideration.

4.1.2 Narrowband Source-Coupled Pair

As shown in Fig. 4.2 (a), the first stage of the Gilbert cell mixer is the source-coupled pair transconductance stage. The high impedance of the current source forces the output currents to be balanced when input signal is unbalanced. On the other hand, if the input signal is perfectly differential, the output current is also balanced. The architecture is unsuitable for low-power design since the current source needs at least $V_T + 200mV$. In some cases, the current source is removed to reduce

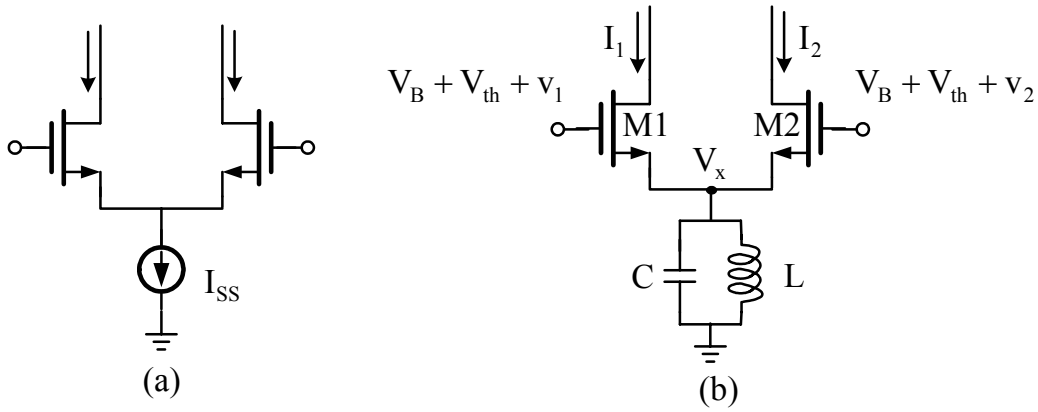


Figure 4.2 Source-coupled pair (a) conventional approach (b) narrowband approach

supply voltage, but the drawback of the omission is that the mixer will not reject unbalance in the RF differential inputs. Therefore we adopt a LC tank to replace the conventional current source, as shown in Fig. 4.2 (b). In dc biasing condition, the inductor provides a low resistance path for the dc bias current of M1 and M2 to ground, hence it almost needs no dc voltage drop across the source-coupled pair. At the operating frequency, the high impedance of the tank exhibits the ac function of the current source when the resonance frequency of the tank is tuned at ω_0 (i.e., $1/LC = \omega_0^2$).

The detail analysis is as follows. In Fig. 4.2 (b), the current of the M1 and M2 can be expressed as

$$I_1 = \frac{K_n}{2}(V_B + v_1 - V_x)^2 \tag{4-1}$$

$$I_2 = \frac{K_n}{2}(V_B + v_2 - V_x)^2 \tag{4-2}$$

where K_n is the large signal transconductance parameter. The voltage V_x of the common-source node can be expressed as (4-3) by using Kirchoff's current law

$$I_1 + I_2 = C\frac{dV_x}{dt} + \frac{1}{L}\int Vxdt \tag{4-3}$$

Thus, from (4-1), (4-2) and (4-3), we can obtain (4-4)

$$\frac{d^2}{dt^2}Vx + 2\frac{g_m}{C}\frac{d}{dt}Vx + \frac{1}{LC}Vx = \frac{K_n}{C}\frac{d}{dt}\left[(V_B - Vx)(v_1 + v2) + V_x^2 + \frac{v_1^2 + v_2^2}{2}\right] \quad (4\text{-}4)$$

then the solution of the voltage V_x depends on the input signals, v_1 and v_2.

In the case of a single-ended input signal ($v_1 = A\sin\omega_0 t, v_2 = 0$), the voltage V_x can be expressed as

$$Vx = \frac{A}{2}\sin\omega_0 t + \psi \quad (4\text{-}5)$$

where ψ represents the solution of the nonlinear differential equation, (4-6),

$$\frac{d^2}{dt^2}\psi + 2\frac{g_m}{C}\left(1 - \frac{\psi}{V_B}\right)\frac{d}{dt}\psi + \omega_0^2\psi = \omega_0\frac{K_n}{C}\frac{A^2}{4}\sin 2\omega_0 t \quad (4\text{-}6)$$

In equation (4-6), the ψ contain the harmonics of $2\omega_0$ and maybe higher, but none at ω_0.

In the case of a differential input signal ($v_1 = -v_2 = (A/2)\sin\omega_o t$), the voltage V_x can be expressed as

$$Vx = \psi \quad (4\text{-}7)$$

and the solution can be verified in Fig. 4.3.

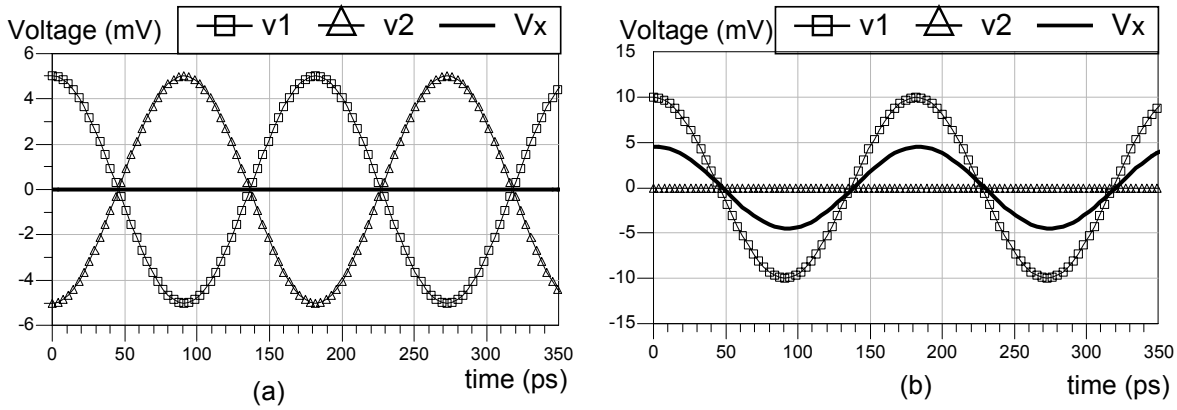


Figure 4.3 (a) Differential input signal (b) Single-ended input signal

As shown in Fig. 4.3, if the input signal is single-ended, the common-source terminals will have a voltage wave of 1/2 the input amplitude. On the other hand, the common-source terminals will exhibit no power at ω_0 when input signal is differential pair. Therefore the transconductance stage responds to difference between v_1 and v_2. In other words, the common-mode gain is reduced by the LC tank.

Besides, the differential output current can be expressed as

$$I_0 = I_1 - I_2 = g_m A\sin(\omega_0 t) - K_n \psi A\sin(\omega_0 t) \quad (4\text{-}8)$$

In (4-8), the first term is the linear transform, and the second term is the distortion signals. Of particular interest is the third-order distortion term which is generated by multiplying the second-harmonics ($2\omega_0$) of the ψ and the $\sin(\omega_0 t)$. Thus the low impedance at $2\omega_0$ will cause lower second-harmonics and get better linearity than that of the conventional current source.

4.2 Analysis of Linearity

In low-power RF transceiver design, linearity requirement becomes more and more challenging. Circuit nonlinearity results in various system distortions associated with the even- and odd-order nonlinearities. Of these distortions, the third-order intermodulation is one of the most critical terms responsible for linearity degradation in general RF systems. Due to the fact, how to improve the linearity of RF circuits without extra power consumption becomes an important topic to be studied.

As far as cascaded stages are concerned, system design calls for high linearity in the mixer stage to alleviate the distortion issues. A mixer is generally composed of a transconductance amplifier and a switching stage. Linearity is most limited by the transconductance amplifier, and therefore we will discuss the nonlinear effect of the

common-source amplifier in section 4.2.1.

In recent years, several techniques have been proposed to improve the linearity of MS/RF circuits by linearization of the nonlinear transconductance, such as degeneration feedback [5] and a bisymmetric Class-AB stage [6]. Another scheme is the superposition of auxiliary transistors operated in different bias conditions to null the derivative of device transconductance [7, 8]. Combined with the technique of out-of-band impedance termination, circuit linearity can be further enhanced, as indicated by the Volterra series analysis [9, 10]. The scheme, named as derivative superposition or multiple gated transistors (MGTR), offers a good opportunity to extend linearity without increasing power consumption, and is introduced in section 4.2.2.

Reference [10] gives designs showing that the device size of the auxiliary transistor (AT) is larger than that of the main transistor (MT), which does not precisely match to the derivative cancellation analysis derived through DC transconductance analysis. It is proposed that a complex transconductance shall be employed to search for the optimal design parameters. Therefore we propose a compact box-type equivalent circuit for the design of the multiple gated transistors technique in section 4.2.3.

4.2.1 Nonlinear Effects of Common-Source Amplifier

For the common-source amplifier, the nonlinear effect is dominated by the transconductance and the output conductance of the device. The nonlinear effects of the capacitances and substrate can be neglected, and they can be considered as linear elements [11]. Therefore we only consider the transconductance and the output conductance as the nonlinear source for the following analysis.

Fig. 4.4 shows a common-source amplifier, where Z1 is the input impedance, and Z2 is the output impedance. From the above-mentioned introduction and assuming that the common-source amplifier works in the weakly nonlinear region, the

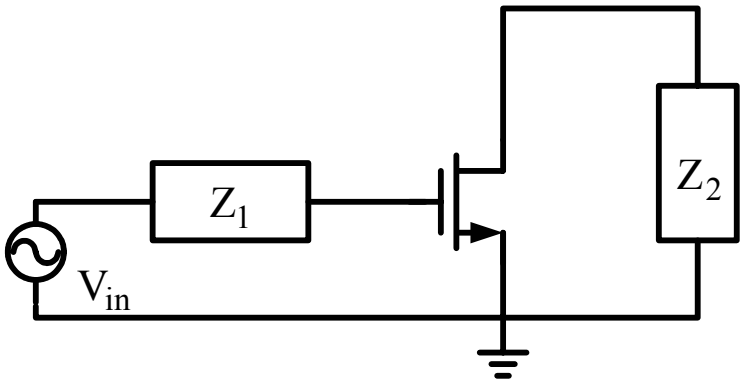


Figure 4.4 Common-source amplifier

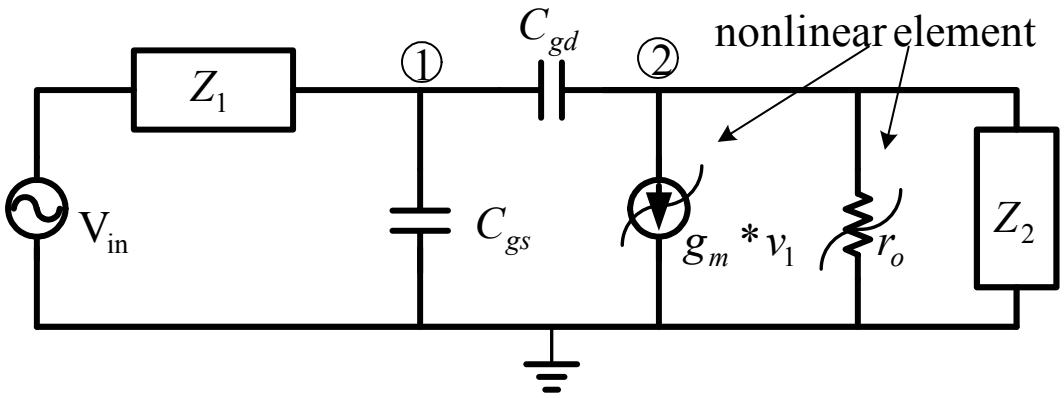


Figure 4.5 Equivalent circuit of the common-source amplifier

equivalent circuit of the common-source amplifier can be shown as Fig. 4.5, where the transconductance (g_m) and the output conductance (r_0) are the nonlinear elements. Therefore the I-V curve of the device can be expressed as

$$\begin{aligned} i_{DS} &= I_{dc} + g_m.v_{gs} + \frac{g_m^{'}}{2!}.v_{gs}^2 + \frac{g_m^{''}}{3!}.v_{gs}^3 + ... \\ &+ g_o.v_{ds} + \frac{g_o^{'}}{2!}.v_{ds}^2 + \frac{g_o^{''}}{3!}.v_{ds}^3 + ... \end{aligned} \tag{4-9}$$

where $g_m^{(n)}$ and $g_o^{(n)}$ represents the n[th]-order derivatives of the transconductance and output conductance, and $g_o = 1/r_o$.

The nonlinear distortion can be obtained by calculating the Volterra kernels of order one, two and three of voltages [12].

First-order kernels

In order to obtain the first-order Volterra kernels, the nonlinear elements must be replaced with its linearized equivalent, as shown in Fig. 4.6. Applying Kirchoff's current law at node 1 and 2 in Fig. 4.6 yields:

$$\begin{bmatrix} (\frac{1}{Z_1(s)} + sC_{gs} + sC_{gd}) & -sC_{gd} \\ (g_m - sC_{gd}) & sC_{gd} + \frac{1}{Z_2(s) // r_o} \end{bmatrix} \cdot \begin{bmatrix} H_{11}(s) \\ H_{12}(s) \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_1(s)} \\ 0 \end{bmatrix} \tag{4-10}$$

where $H_{11}(s)$ and $H_{12}(s)$ are the Volterra kernels. The first subscript in these two transfer functions indicates the order of the transfer function, whereas the second subscript corresponds to the numbering of the node voltages. Then the first-order kernels $H_{11}(s)$ and $H_{12}(s)$ can be expressed as

$$H_{11}(s) = \frac{1 + sC_{gd}.Z_3(s)}{(g_m + g(s)).Z_x(s)} \tag{4-11}$$

$$H_{12}(s) = \frac{sC_{gd}.Z_3(s) - g_m.Z_3(s)}{(g_m + g(s)).Z_x(s)} \tag{4-12}$$

where

$$Z_3(s) = Z_2(s) // r_o \tag{4-13}$$

$$Z_x(s) = sC_{gd}.Z_1(s).Z_3(s) \tag{4-14}$$

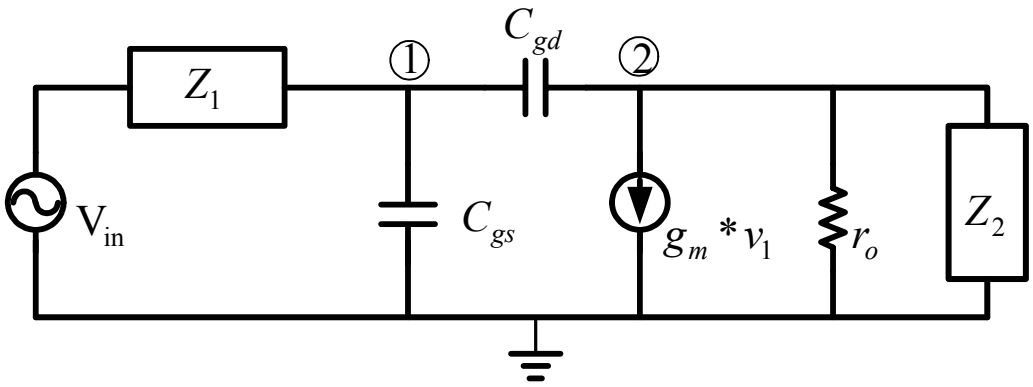


Figure 4.6 Linearized equivalent of the circuit of the Fig. 4.5

$$g(s)=\frac{1+sC_{gd}.(Z_1(s)+Z_3(s))+sC_{gs}.(Z_1(s)+Z_x(s))}{Z_x(s)} \tag{4-15}$$

Second-order kernels

For computing second-order kernels, the input signal v_{in} is replaced by a short circuit, and the second-order nonlinear current sources are applied to the linearized circuit, as shown in Fig 4.7. Applying Kirchoff's current law at node 1 and 2 in Fig. 4.7 yields:

$$\begin{bmatrix} (\frac{1}{Z_1(s')}+s'C_{gs}+s'C_{gd}) & -s'C_{gd} \\ (g_m-s'C_{gd}) & s'C_{gd}+\frac{1}{Z_3(s')} \end{bmatrix}\cdot\begin{bmatrix} H_{21}(s_1,s_2) \\ H_{22}(s_1,s_2) \end{bmatrix}=\begin{bmatrix} 0 \\ -(i_{NL2gm}+i_{NL2go}) \end{bmatrix} \tag{4-16}$$

where $H_{21}(s_1,s_2)$ and $H_{22}(s_1,s_2)$ are the second-order kernels, and

$$s'=s_1+s_2 \tag{4-17}$$

$$i_{NL2gm}(s_1,s_2)=\frac{g_m^{'}}{2!}H_{11}(s_1).H_{11}(s_2) \tag{4-18}$$

$$i_{NL2go}(s_1,s_2)=\frac{g_o^{'}}{2!}H_{12}(s_1).H_{12}(s_2) \tag{4-19}$$

Then the second-order kernels $H_{21}(s_1,s_2)$ and $H_{22}(s_1,s_2)$ can be expressed as

$$H_{21}(s_1,s_2)=\frac{-Z_1(s').Z_3(s').s'C_{gd}.(i_{NL2gm}+i_{NL2go})}{(g_m+g(s')).Z_x(s')} \tag{4-20}$$

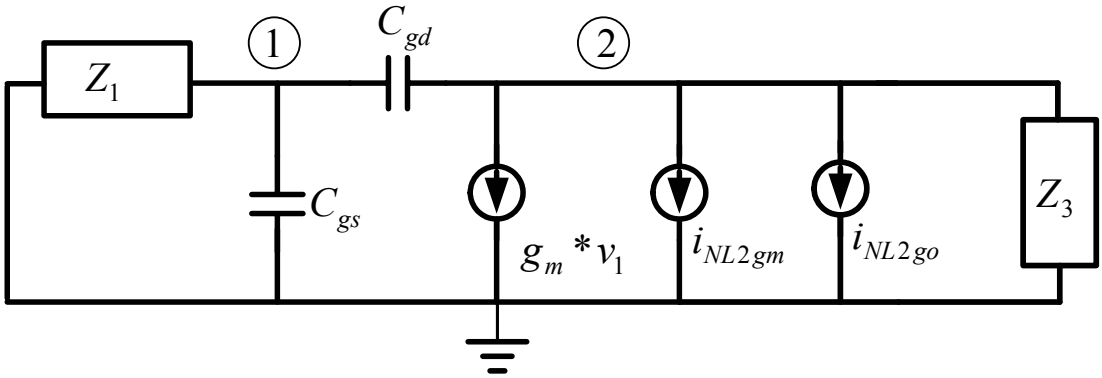


Figure 4.7 Equivalent circuit for the computation of the second-order kernels in Fig. 4.5

$$H_{22}(s_1,s_2)=\frac{-Z_1(s').Z_3(s').(\frac{1}{Z_1(s')}+s'C_{gs}+s'C_{gd}).(i_{NL2gm}+i_{NL2go})}{(g_m+g(s')).Z_x(s')} \tag{4-21}$$

Third-order kernels

Just as second-order kernels, the third-order ones are computed as the response to the third-order nonlinear current sources, as shown in Fig. 4.8. Applying Kirchoff's current law at node 1 and 2 in Fig. 4.8 yields:

$$\begin{bmatrix} (\frac{1}{Z_1(s'')}+s''C_{gs}+s''C_{gd}) & -s''C_{gd} \\ (g_m-s''C_{gd}) & s''C_{gd}+\frac{1}{Z_3(s'')} \end{bmatrix}\cdot\begin{bmatrix} H_{31}(s_1,s_2,s_3) \\ H_{32}(s_1,s_2,s_3) \end{bmatrix}=\begin{bmatrix} 0 \\ -(i_{NL3gm}+i_{NL3go}) \end{bmatrix} \tag{4-22}$$

where $H_{31}(s_1,s_2,s_3)$ and $H_{32}(s_1,s_2,s_3)$ are the third-order kernels, and

$$s''=s_1+s_2+s_3 \tag{4-23}$$

$$\begin{aligned} i_{NL3gm}(s_1,s_2,s_3)=&\frac{g_m''}{3!}.H_{11}(s_1).H_{11}(s_2).H_{11}(s_3)+\frac{g_m'}{3}[H_{11}(s_1).H_{21}(s_2,s_3) \\ &+H_{11}(s_2).H_{21}(s_1,s_3)+H_{11}(s_3).H_{21}(s_1,s_2)] \end{aligned} \tag{4-24}$$

$$\begin{aligned} i_{NL3go}(s_1,s_2,s_3)=&\frac{g_o''}{3!}.H_{12}(s_1).H_{12}(s_2).H_{12}(s_3)+\frac{g_o'}{3}[H_{12}(s_1).H_{22}(s_2,s_3) \\ &+H_{12}(s_2).H_{22}(s_1,s_3)+H_{12}(s_3).H_{22}(s_1,s_2)] \end{aligned} \tag{4-25}$$

Then the third-order kernels $H_{31}(s_1,s_2,s_3)$ and $H_{32}(s_1,s_2,s_3)$ can be expressed as

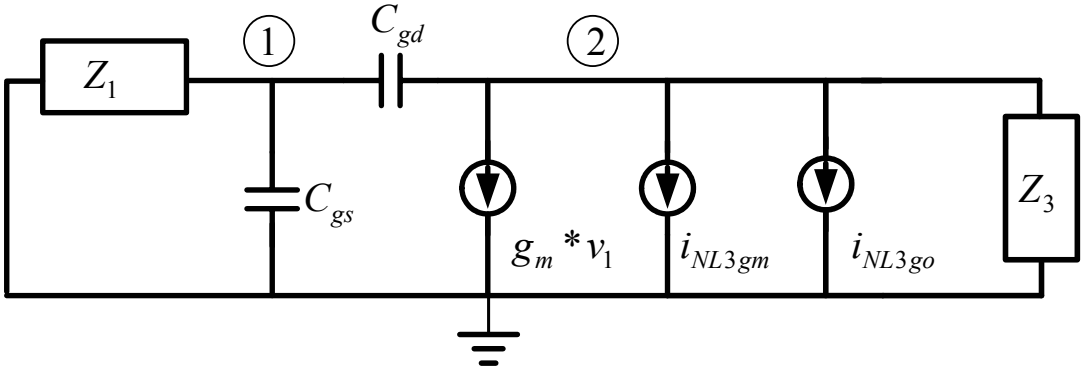


Figure 4.8 Equivalent circuit for the computation of the third-order kernels in Fig. 4.5

$$H_{31}(s_1,s_2,s_3)=\frac{-Z_1(s'').Z_3(s'').s''C_{gd}.(i_{NL3gm}+i_{NL3go})}{(g_m+g(s'')).Z_x(s'')} \tag{4-26}$$

$$H_{32}(s_1,s_2,s_3)=\frac{-Z_1(s'').Z_3(s'').(\frac{1}{Z_1(s'')}+s''C_{gs}+s''C_{gd}).(i_{NL3gm}+i_{NL3go})}{(g_m+g(s'')).Z_x(s'')} \tag{4-27}$$

Of the nonlinear distortions, the third-order intermodulation is one of the most critical terms responsible for linearity degradation in general RF systems. In order to obtain the third-order intermodulation distortion, input signal is replaced by a two-tone test signal ($V_1=A\sin(\omega_1 t)$ $V_2=A\sin(\omega_2 t)$), and the fundamental signal at ω_1 and the distortion at $2\omega_1-\omega_2$ must be computed by (4-12) and (4-27). By assuming $s_1=s_2=j\omega_1=s$, $s_3=-j\omega_2\approx -s$, and $j\omega_1-j\omega_2=\Delta s$, then the third-order intermodulation distortion (IM_3) can be expressed as

$$\begin{aligned} IM_3 &= \frac{3}{4}.A^2.\left|\frac{H_{32}(j\omega_1,j\omega_1,-j\omega_2)}{H_{12}(j\omega_1)}\right| = \frac{3}{4}.A^2.\left|\frac{H_{32}(s,s,-s)}{H_{12}(s)}\right| \\ &= \frac{3}{4}.A^2.\frac{|1+sC_{gd}.Z_1(s)+sC_{gs}.Z_1(s)|}{|sC_{gd}-g_m|}.|i_{NL3gm}(s,s,-s)+i_{NL3go}(s,s,-s)| \end{aligned} \tag{4-28}$$

In addition, the A_{IP3} can be obtained by assuming $IM_3=1$ and expressed as

$$A_{IP3}^2=\frac{4}{3}.\frac{|sC_{gd}-g_m|}{|1+sC_{gd}.Z_1(s)+sC_{gs}.Z_1(s)|}.\frac{1}{|i_{NL3gm}(s,s,-s)+i_{NL3go}(s,s,-s)|} \tag{4-29}$$

If we assume that $\omega_1=5.5GHz$, $\omega 2=5.505GHz$, A=1mV, and $Z_1=Z_2=50$, the IM_3 can be shown in Fig. 4.9, where * denotes the simulated result of TSMC 0.18um RFCMOS device by ADS simulator and o denotes the calculated result of (4-28). The calculated result has good agreement with harmonic-balance simulation except $v_{gs}\approx 0.58V$, where the g_m'' is around zero so the neglected extrinsic elements and nonlinear effects of other elements becomes relatively important and cause this deviation.

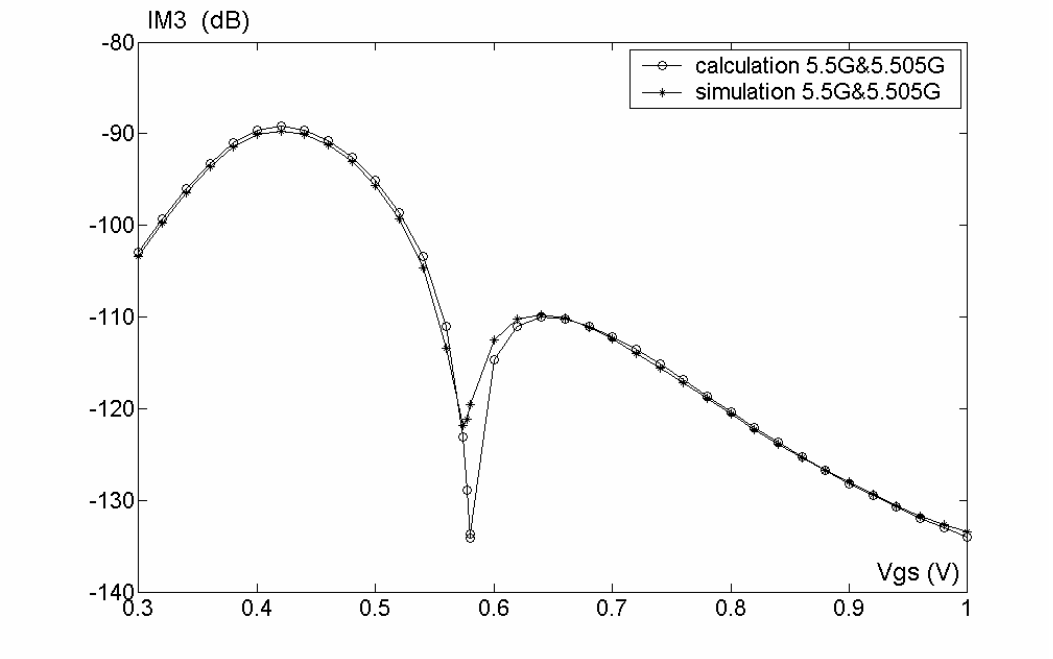


Figure 4.9 The third-order intermodulation distortion (IM_3). The device size is nr=16, width=2.5um, and length=0.18um.

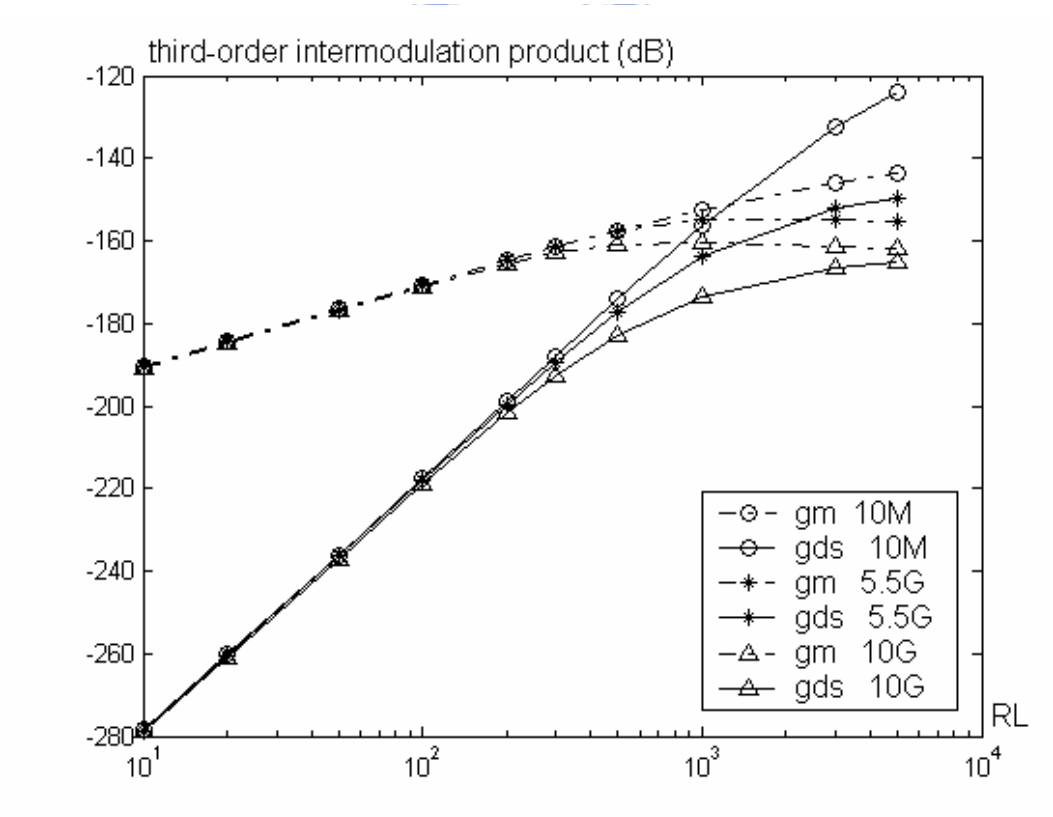


Figure 4.10 Nonlinear effects of the transconductance and the output conductance

The nonlinear distortions result from the nonlinear effects of the transconductance and the output conductance and vary with different load impedance. Fig. 4.10 shows the influence of the two nonlinear elements. Solid line denotes the nonlinear effects of the output conductance, and dash line denotes the nonlinear effects of the transconductance. As shown in Fig. 4.10, the linearity is dominated by the device transconductance in the case of low load impedance.

4.2.2 Multiple Gated Transistors Method

According to above discussion, the I-V curve of the device can be rewritten as

$$i_{DS} = I_{dc} + g_m.v_{gs} + \frac{g_m^{'}}{2!}.v_{gs}^2 + \frac{g_m^{''}}{3!}.v_{gs}^3 + ... \tag{4-30}$$

and (4-28) can be simplified as

$$IM_3 = \frac{3}{4}.A^2.|H(s)|.|A(s)|^3.|\varepsilon(\Delta s, 2s)| \tag{4-31}$$

where $H(s)$ is the related to equivalent IMD_3 voltage to the IMD_3 response of the drain current nonlinear term, $A(s)$ is the linear transfer function for the input voltage of v_{gs}, and can be expressed as

$$H(s) = \frac{|1 + sC_{gd}.Z_1(s) + sC_{gs}.Z_1(s)|}{|sC_{gd} - g_m|} \tag{4-32}$$

$$A(s) = \frac{|1 + sC_{gd}.Z_3(s)|}{|(g_m + g(s)).Z_x(s)|} \tag{4-33}$$

$$\varepsilon(\Delta s, 2s) = \frac{g_m^{''}}{3!} - \frac{g_m^{'}}{3}.\left(\frac{2}{g_m + g(\Delta s)} + \frac{1}{g_m + g(2s)}\right) \tag{4-34}$$

The $H(s)$ and $A(s)$ are linear transform function, hence high IIP3 requires minimizing the factor $\varepsilon(\Delta s, 2s)$. Actually it is found that its first term, $g_m^{''}$, is generally much larger than its second term in the general case. The major effort,

therefore, is to reduce the g_m''.

Fig. 4.11(a) is a common-source architecture, and its small-signal parameter, $g_m \& g_m' \& g_m''$, is shown in Fig. 4.12. The g_m'' arrives its positive peak value in the subthreshold region, and it arrives a negative peak value in the gate drive voltage range of 0.1~0.4V, which is the usual bias voltage for high-gain, low-noise, and low-power applications. This negative value will cause serious linearity degradation.

Ref. [10] introduces multiple gated transistors (MGTR) technique, as shown in Fig. 4.11(b). The main transistor (MT) provides the gain of the circuit. The auxiliary transistor is used to cancel the g_m'' of the MT by selecting appropriate size and biasing voltage. Fig. 4.13 shows the results. In this plot the device sizes of MT and AT are chosen as finger numbers of 16 and 12 (N_F=16, 12), respectively, and the shift voltage, V_{shift}, is 0.18V. As can be seen, g_m'' appears close to zero in the superposed configuration. The best gate bias voltage, V_{gs}, is revealed to be as 0.65V. The shift voltage actually drives AT in the subthreshold region consuming insignificant power.

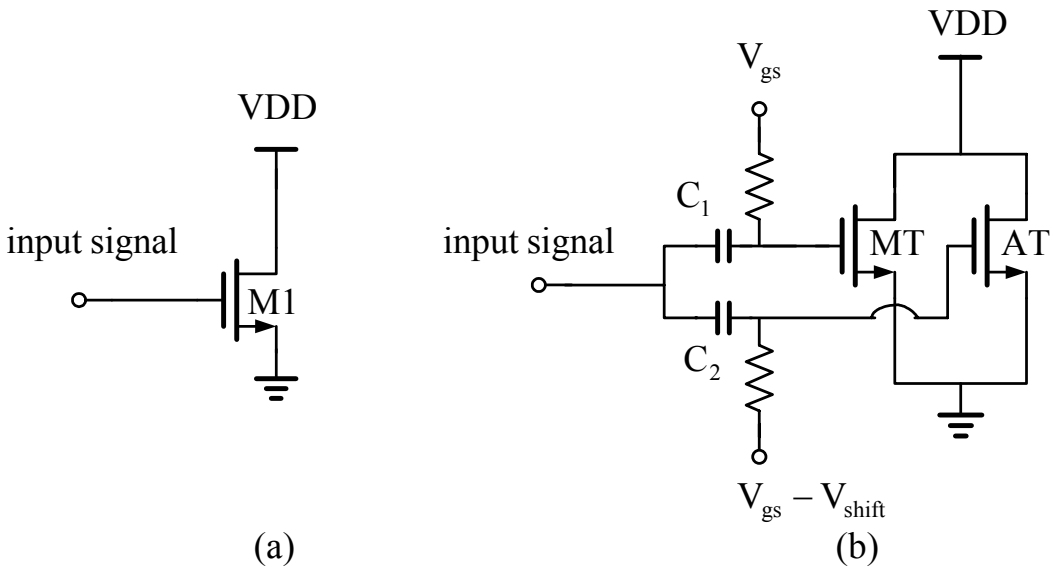


Figure 4.11 (a) Common-source architecture (b) MGTR architecture

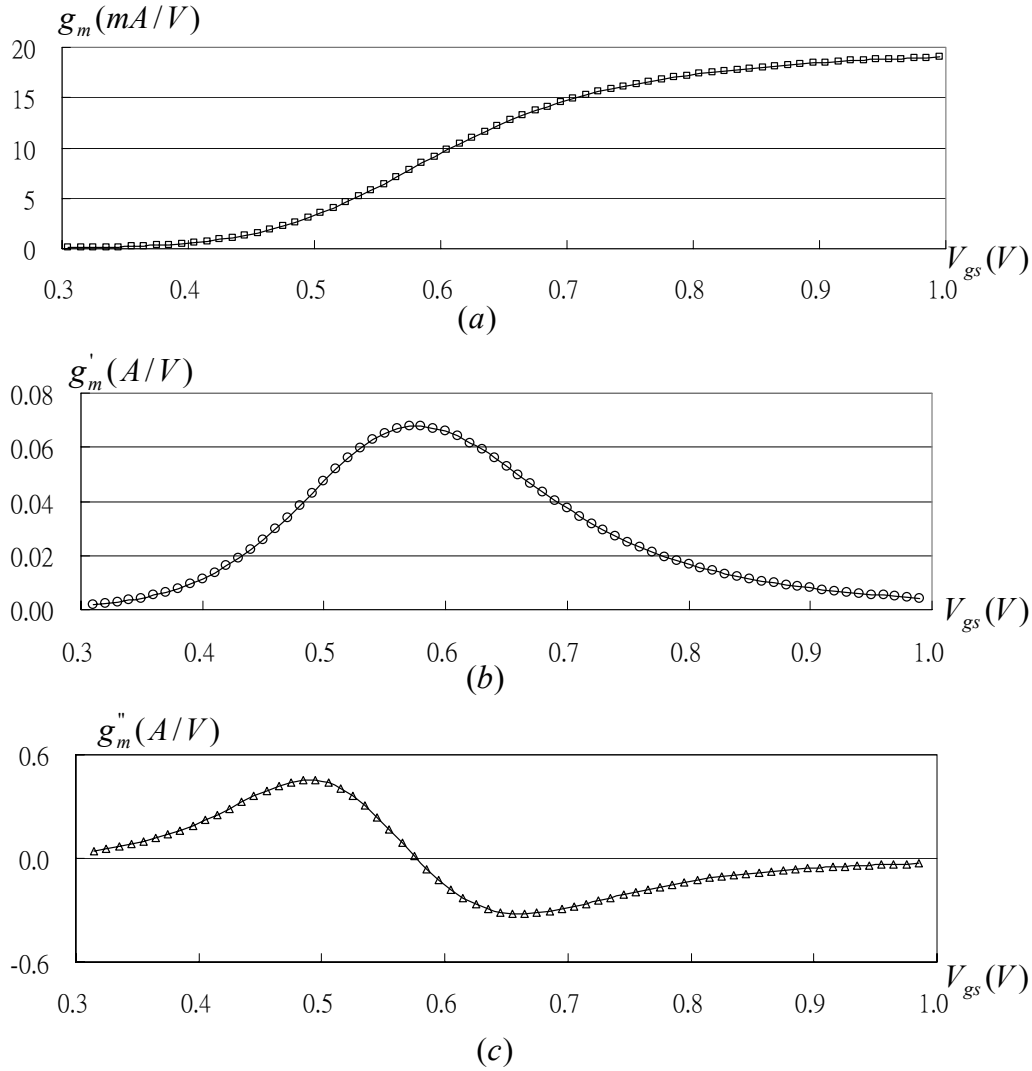


Figure 4.12 Small-signal parameter of NMOS (a) g_m (b) $g_m^{'}$ (c) $g_m^{''}$

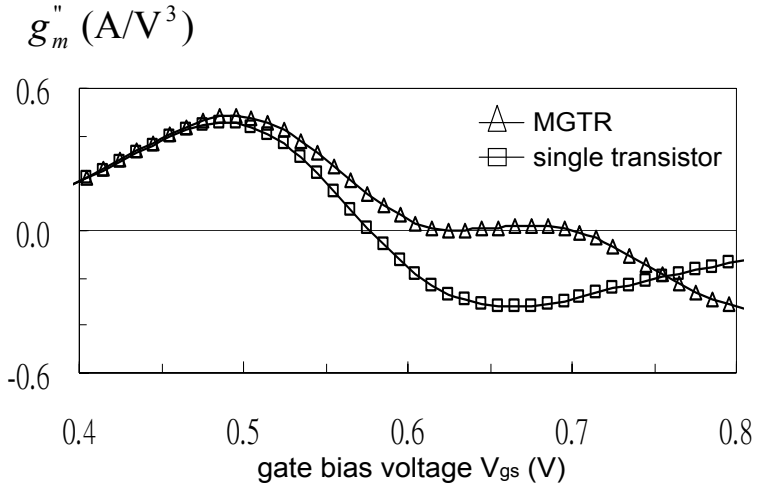


Figure 4.13. Cancellation of DC $g_m^{''}$ in MGTR configuration. The device sizes of MT and AT are N_F=16 and 12, respectively. V_{shift}=0.18V.

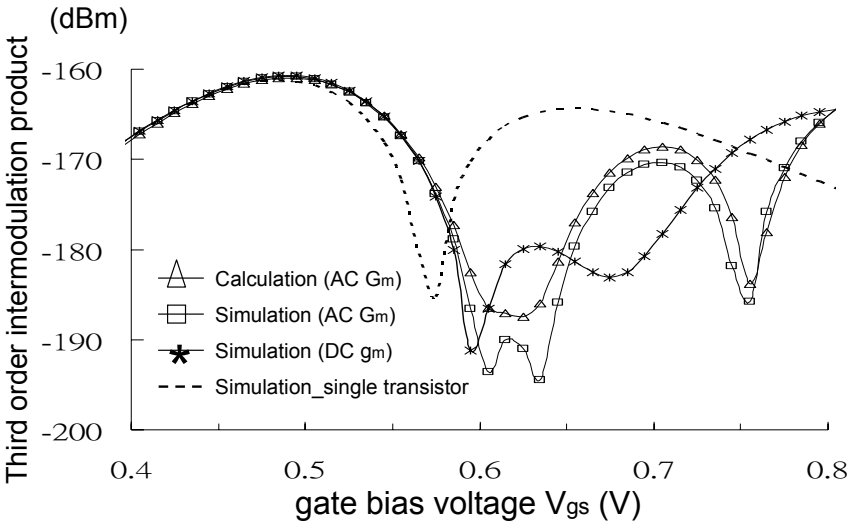


Figure 4.14 The third-order intermodulation distortions at 5.5GHz by harmonic-balance simulations and equation calculations.

Harmonic-balance simulation of the amplifier circuit at 5.5GHz does indicate linearity improvement, as shown in Fig. 4.14. Nevertheless better linearity improvement can be still found in the case that the size of AT is N_F=20, and V_{shift}, is 0.21V. Obviously this size does not match to previous analysis.

Essentially nonlinear distortion is frequency-dependent. By using DC transconductance the conventional analysis lacks of accuracy to predict the high-frequency operating condition and to obtain the truly optimized linearity. This error results from the lacks of the extrinsic elements in deep sub-micro CMOS technologies. If the analysis method of the DC gm includes all intrinsic and extrinsic elements, this will cause that DC gm method is too complicated to get optimized transistor size and gate bias shifting of the auxiliary transistor for circuit. A new method using complex AC transconductance is therefore introduced in this study to achieve optimized transistor size tuning and gate bias shifting for the auxiliary transistor.

4.2.3 Complex Transconductance Analysis

Fig. 4.15 show a transconductance amplifier using MGTR technique, including the source impedance, Z_g, the load impedance, Z_L, and the source-degeneration circuit

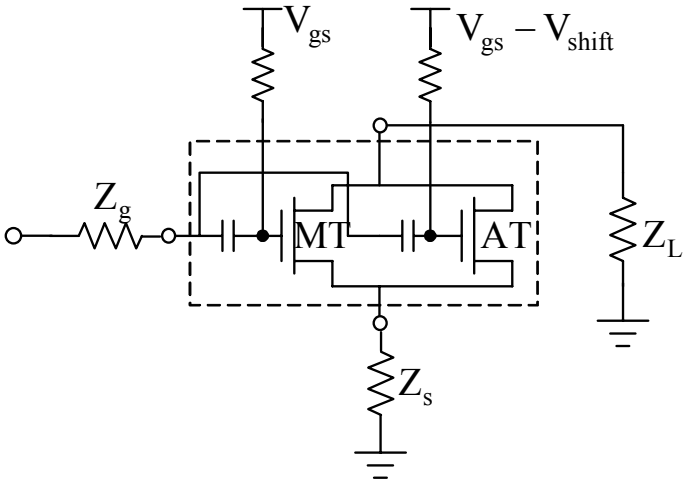


Figure 4.15 MGTR architecture

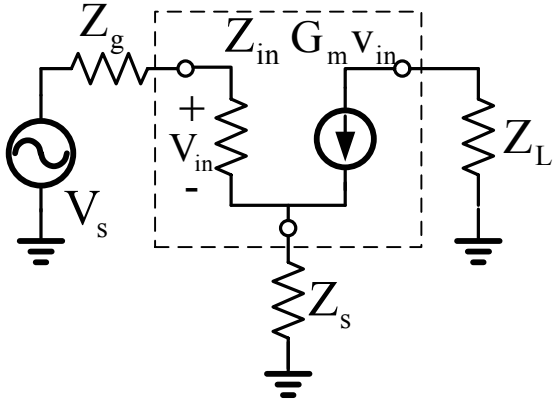


Figure 4.16 Equivalent circuit of the Fig. 4.15

impedance Z_s. Without loss of generality in this nonlinear analysis, the superposed configuration in MGTR can be simply represented by the input impedance $Z_{in}(\omega)$ and the transconductance element $G_m(\omega)$. The transconductance G_m is defined in the same way as the ratio of the output current to the input voltage, including all the intrinsic and extrinsic frequency-dependency of MOSFET devices. It could be a complex value at high frequencies. Its nonlinearity shall be related to the load impedance and the operation frequency. Consequently the equivalent circuit model of a transconductance amplifier is shown in Fig. 4.16.

Similar to (4-30), the I-V curve of the device can be expressed as

$$i_{DS} = I_{dc} + G_m.v_{gs} + \frac{G_m^{'}}{2!}.v_{gs}^2 + \frac{G_m^{''}}{3!}.v_{gs}^3 + ... \tag{4-35}$$

, and the third-order intermodulation product IMD_3 in a two-tone test is derived by Volterra series analysis and expressed as

$$IMD_3 = \frac{3}{4}.A^3.\frac{|Z_s(\omega)+Z_{in}(\omega)+Z_g(\omega)|.|Z_L(\omega)|.|i_{NL3Gm}|}{|Z_s(\omega)+Z_s(\omega)Z_{in}(\omega)G_m(\omega)+Z_{in}(\omega)+Z_g(\omega)|} \tag{4-36}$$

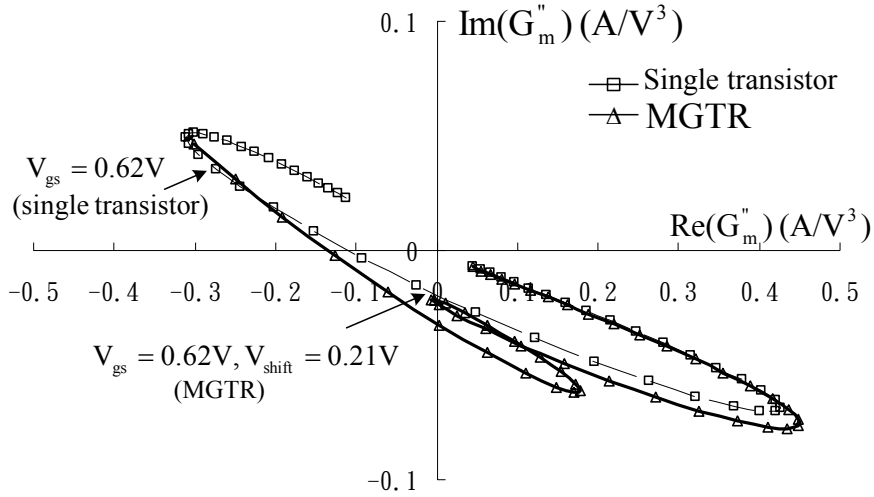
where

$$|i_{NL3Gm}| = |H(\omega)|^3.|\varepsilon(\omega,\Delta\omega,2\omega)| \tag{4-37}$$

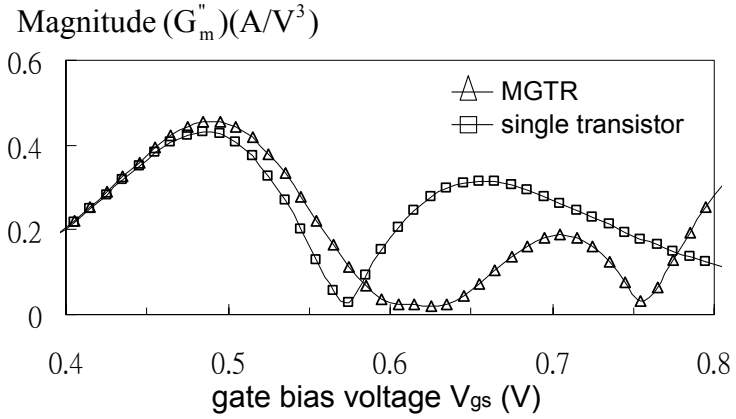
$$\begin{aligned}\varepsilon(\omega,\Delta\omega,2\omega) = \frac{G_m^{''}(\omega)}{3!} - \frac{2}{3}\frac{G_m^{'}(\omega)}{2!}[2Z_s(\Delta\omega)H(\Delta\omega)\frac{G_m^{'}(\Delta\omega)}{2!} \\ + Z_s(2\omega)H(2\omega)\frac{G_m^{'}(2\omega)}{2!}]\end{aligned} \tag{4-38}$$

$$H(\omega) = \frac{Z_{in}(\omega)}{Z_s(\omega)+Z_s(\omega)Z_{in}(\omega)G_m(\omega)+Z_{in}(\omega)+Z_g(\omega)} \tag{4-39}$$

$H(\omega)$ is the linear transfer function from v_s to v_{in}. Lower IMD_3 can be obtained by reducing ε in (4-37). Similarly the major effort is cancellation of $G_m^{''}(\omega)$, which is conducted in the complex domain as shown in Fig. 4.17. This complex transconductance analysis actually suggests that the device sizes of MT and AT are chosen as N_F=16 and 20, respectively, and V_{shift} as 0.21V. In addition, calculation by (4-36) has good agreement with harmonic-balance simulation, as shown in Fig. 4.14. Although there is some error, which results from the neglected feedback effect of the device, its result has good agreement with simulation in general. This validates the usefulness of the compact box-type equivalent circuit model



(a)



(b)

Figure 4.17 Cancellation of AC G_m" in MGTR configuration. The device sizes of MT and AT are N_F=16 and 20, respectively. V_{shift}=0.21V.

4.3 Chip Implementation and Measured Result

4.3.1 Circuit Implementations

Following the low-power technique and complex transconductance analysis, a low-power and high-linearity direct down-conversion mixer is designed. The mixer is a fully differential folded Gilbert mixer, consisting of the MGTR transconductance and the switching stage. The schematic is shown in Fig. 4.18.

According to the discussion in the section 4.1, the folded topology is beneficial to lower power design since the traditional cascoded Gilbert cell mixer requires a supply

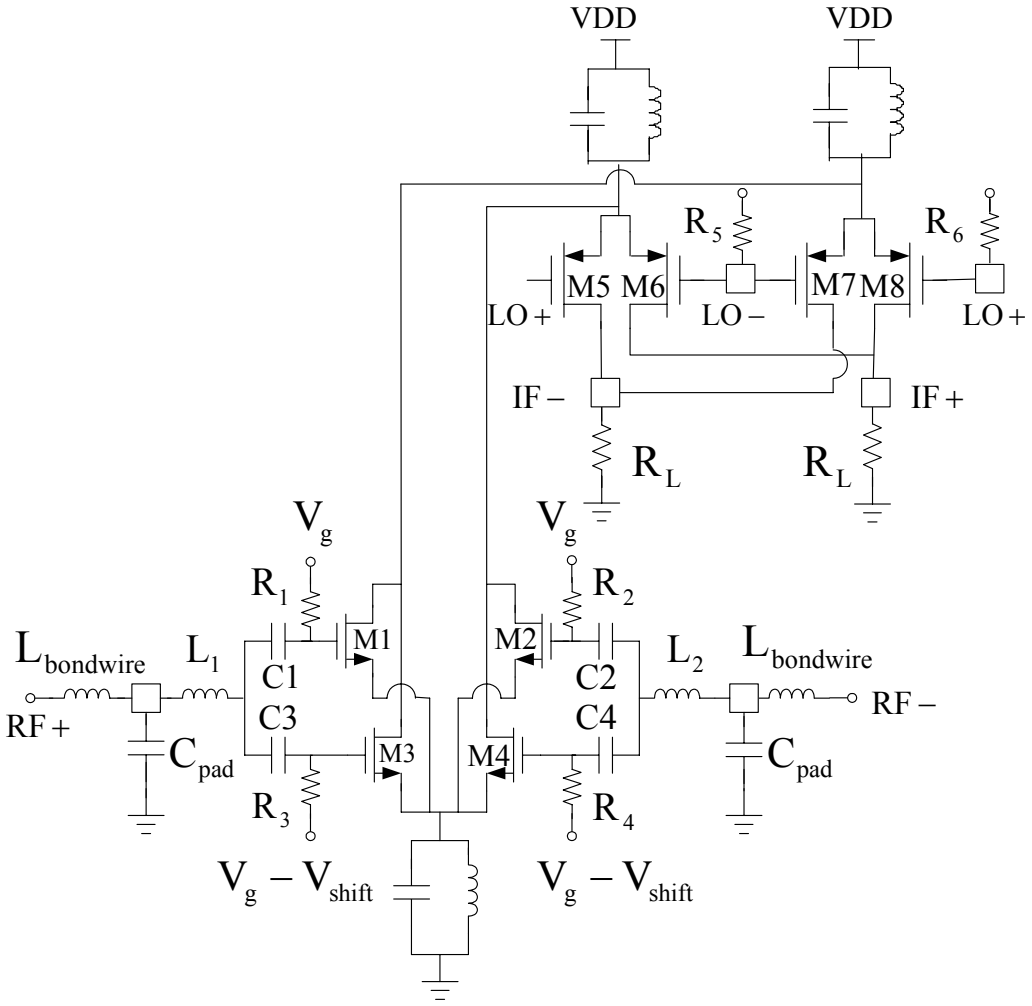


Figure 4.18 Schematic of the folded MGTR direct conversion mixer.

voltage of at least triple threshold voltage. In addition, the transconductance and the switching stages can be biased differently at a high current level and a low level, respectively, to achieve high gain and noise suppression. LC tanks are further applied to supply current driving without voltage drop and provide high impedance at the desired frequency.

The MGTR consists of M1 – M4. M1 and M2 are MT providing major gain of the mixer, and M3 and M4 are AT compensating for the third-order nonlinear distortion. The device sizes are as N_F=16 and 20 for MT and AT, respectively, and the bias conditions are V_{gs}=0.62V and V_{shift}=0.21V. The input matching network includes an on-chip inductor, the bond pad, and the bond wire. The switching stage is implemented

by four PMOS transistors, M5 – M8, since this stage does not need high ω_T. The flicker noise is a concern for direct down-conversion mixer because its corner is around 1MHz, and it can be expressed as (2-3). Therefore increasing the transistor length and decreasing the bias current of transistor is a solution to decrease flicker noise.

4.3.2 Experimental Results

The MGTR mixer is fabricated using 0.18um RF CMOS technology. The full chip of circuit is shown by microphotograph in Fig. 4.19. The total die area including bonding pads is 1.09 mm by 1.08 mm. Measurement is conducted by mounting the mixer die on FR4 board, as shown in Fig. 4.20. Input testing signal is transformed into a differential form at RF and LO ports by hybrid couplers which gain error and phase error are smaller than 0.8dB and 8° respectively from 4GHz to 8GHz. Fig. 4.21 shows the measurement diagram. A unit gain output buffer is used to transform the differential

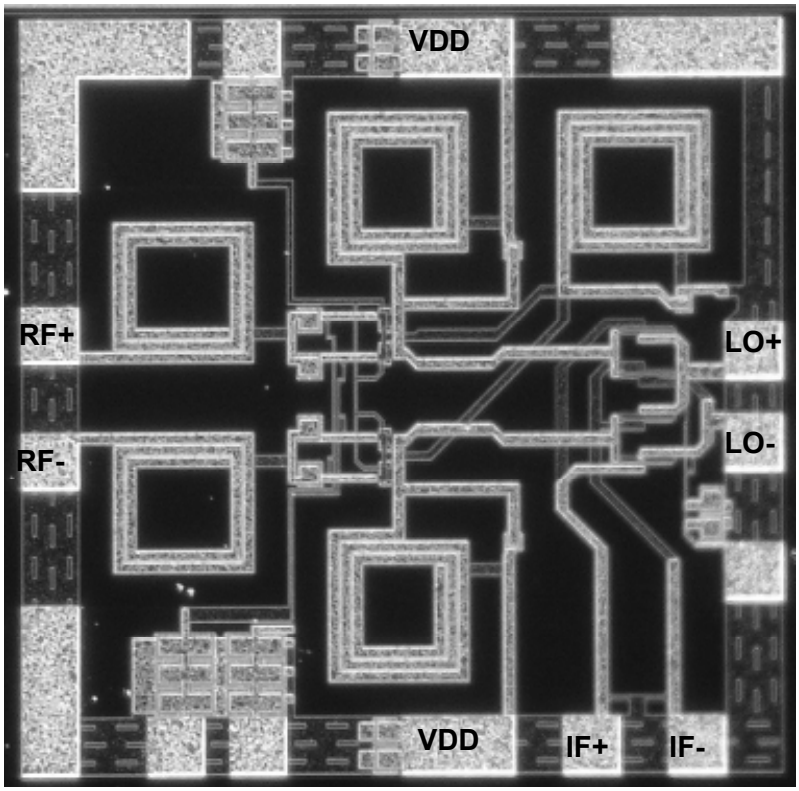


Figure 4.19 Microphotograph of MGTR mixer

signal into the single-ended form, and provides high input impedance to reduce loading effect.

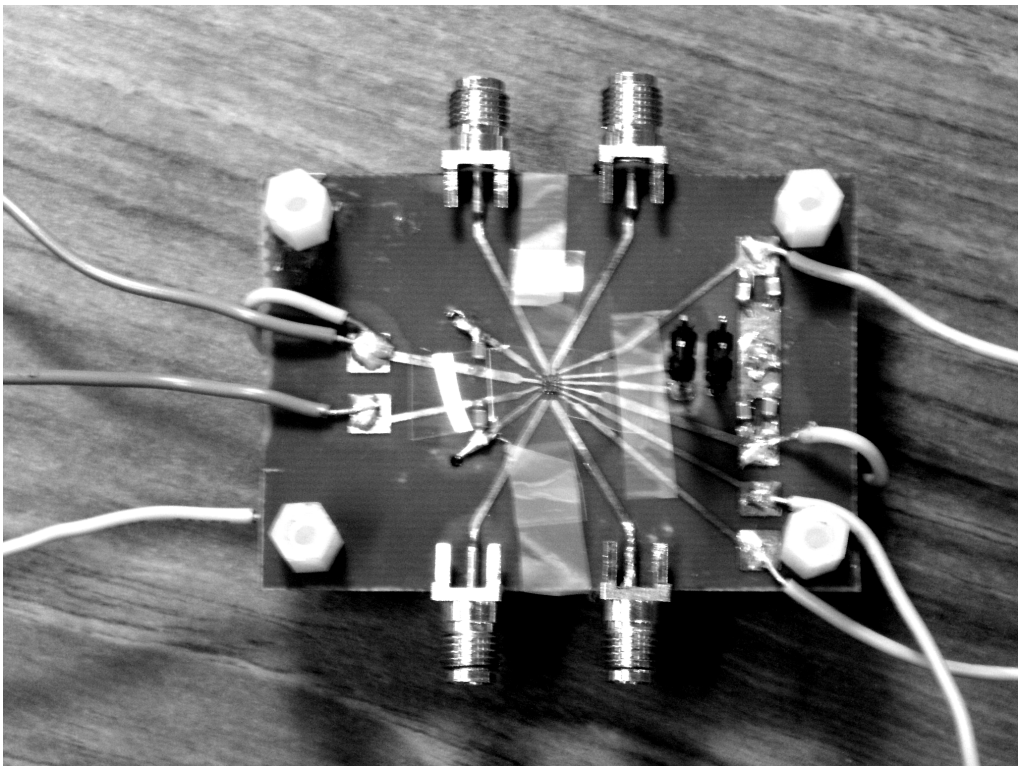


Figure 4.20 PCB layout of the MGTR mixer

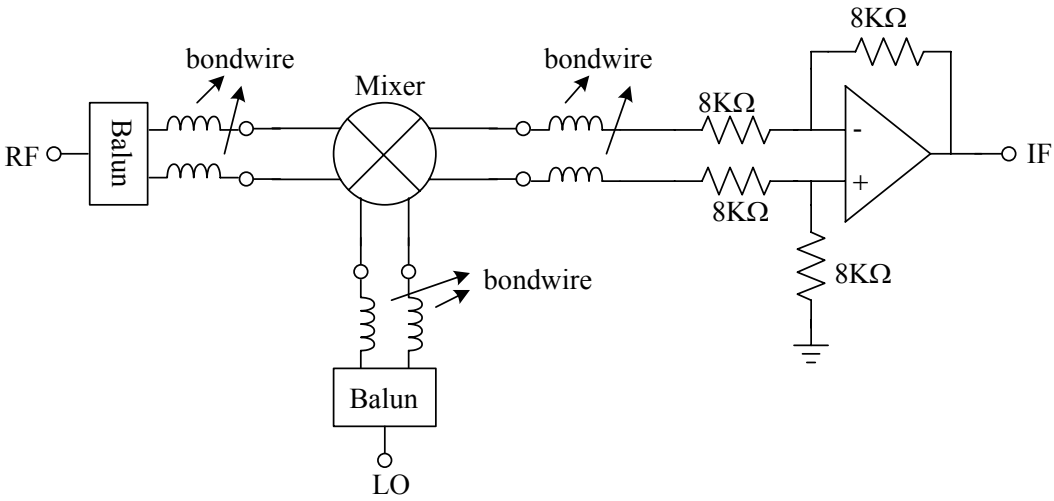


Figure 4.21 Measurement diagram including unit gain output buffer

Fig. 4.22 shows the single-end input return loss. The measured result exhibits a higher input-matching frequency. The discrepancy between measured data and simulation result on the input return loss may be due to the variation of the parasitic bond-wire inductance, pad capacitance, and input-matching inductor. We adjust the value of the bond-wire inductance to 1.5nH and the parasitic capacitance of the pad to 30fF. The value of input-matching inductor is added by 0.2nH, and then the simulation result has better agreement with the measured data. And the deeper phenomenon may result from the parasitic effect of the SMA connectors and the FR4 board. The measured conversion gain is 4.7 dB. Fig. 4.23 shows the measured input P_{-1dB} of 0.2 dBm. Fig. 4.24 shows the measured IIP3 of the MGTR folded mixer at two conditions. One is the MGTR operation condition, and the other is single transistor condition that the AT gate bias voltage is ground. As can be seen, linearity improvement achieves more than 7 dB without extra power consumption. And Fig. 4.25 shows the IIP3 variation at different bias voltage of the AT. Complete measured results are

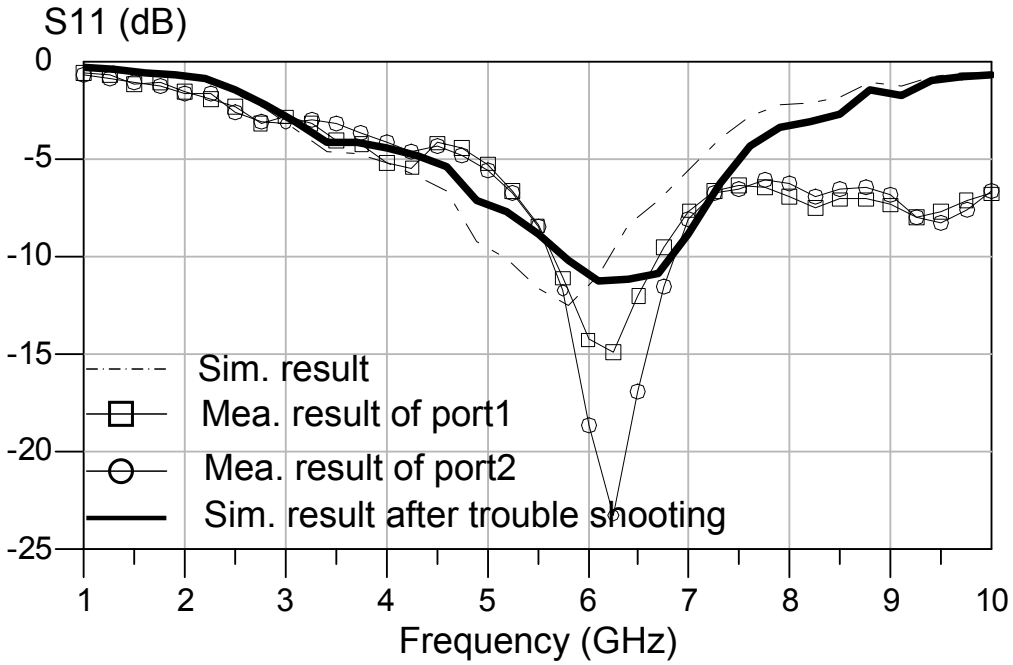


Figure 4.22 Single-end input return loss of the MGTR mixer

summarized in Table 4.1 together with simulation results for comparison. In Table 4.2 listed is comparison of circuit performance with previous work.

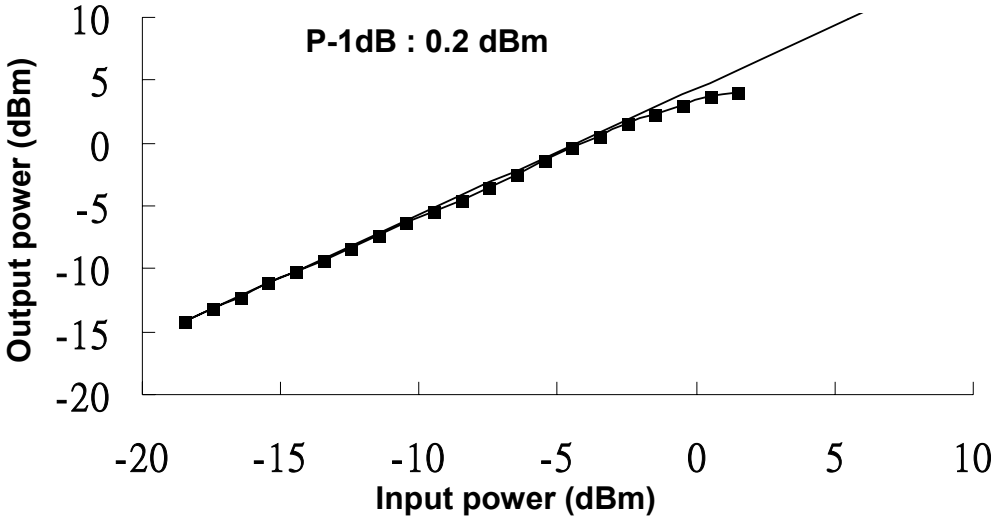


Figure 4.23 P_{-1dB} measurement of MGTR mixer.

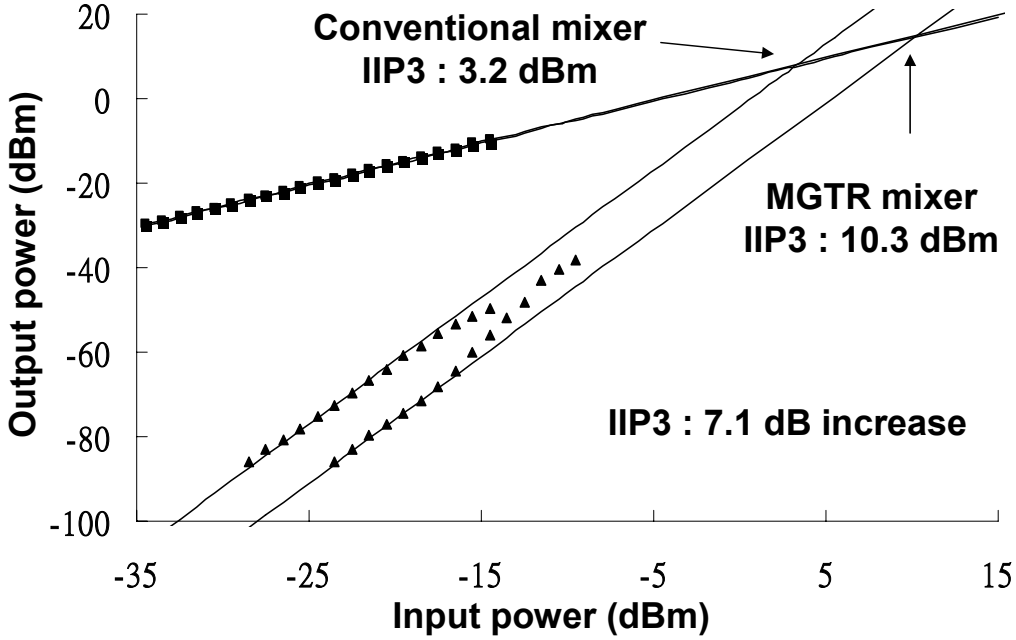


Figure 4.24 IIP3 measurement of conventional mixer and MGTR mixer.

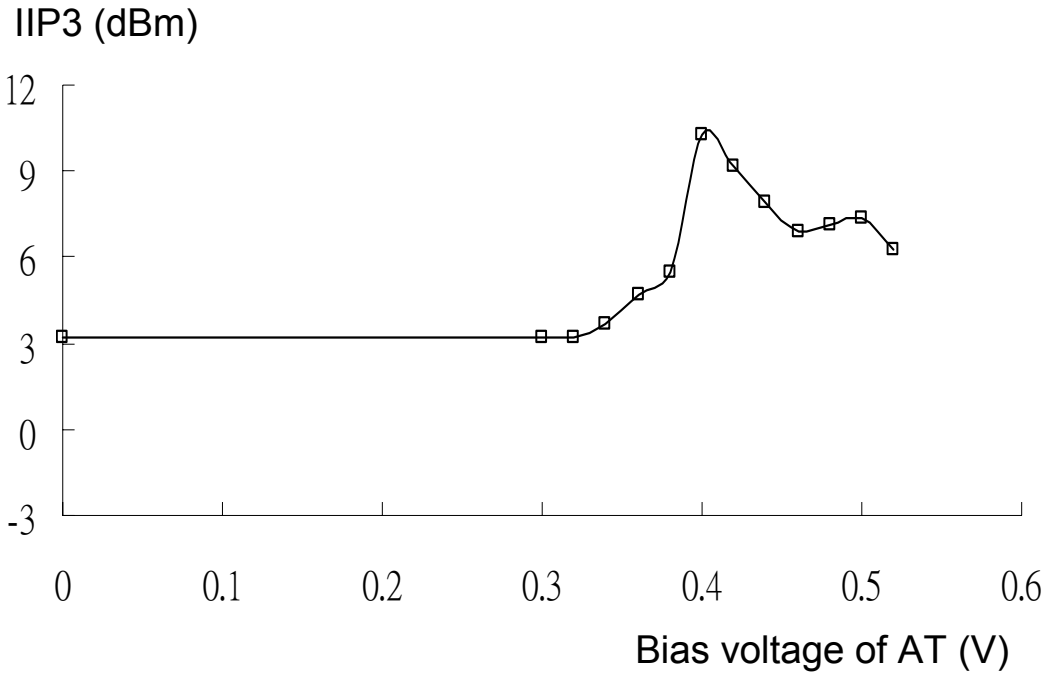


Figure 4.25 IIP3 measurement versus AT gate bias voltage

Table 4.1. Summary of simulation and measured results of MGTR mixer.

	Simulation	Measurement
Process	TSMC 0.18um RFCMOS	
Frequency	5.5 GHz	5.5 GHz
Supply voltage	1.0 V	1.0 V
Conversion gain	8.3 dB	4.7 dB
S_{11}	-13.4 dB	- 9 dB
P_{-1dB}	-3.5 dBm	0.2 dBm
LO power	-1 dBm	5.3 dBm
IIP3	3.8 dBm	10.3 dBm
Noise Figure (DSB)	13.9 dB @ 1MHz	20.9 dB@ 10MHz
LO-RF isolation	-60.9 dB	-47.5 dB
Power consumption	2.2 mW	1.8 mW

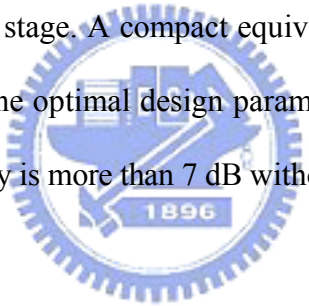
Table 4.2. Performance comparison of CMOS mixers.

	RF frequency (GHz)	IIP3/DC (dBm/mW)
This work	5.5	10.3/1.8
Ref. [10]	2.4	9/5.4
Ref. [13]	8	3.5/6.9
Ref. [14]*	2.5	-1/2.8

* simulation results

4.3.3 Discussions

A low-power and high-linearity folded direct conversion mixer, intended for use in the receiver path of a wireless local area network, is designed in standard 0.18um CMOS technology. The MGTR technique is adopted to improve the linearity of the mixer in the transconductance stage. A compact equivalent circuit using AC complex transconductance truly gives the optimal design parameters. Measured data show that the improvement of the linearity is more than 7 dB without extra power consumption.



CHAPTER 5

Low-Power Front-End Circuit

5.1 Introduction

In recent years research on low-power systems is still an emergent topic in order to prolong battery lifetime. Operating at high frequencies, RF integrated circuits are critical circuit blocks to consume a high power level. The front-end circuits, including the low noise amplifier and the mixer, must be on at all times even at the standby mode. Saving power in these circuits shall significantly increase the allowed standby time.

This chapter is aimed at the low-power RF front-end circuit in wireless receivers. For the concern of low power consumption, Direct Conversion Receiver is chosen as the system architecture. It offers great possibility of better form factor, lower cost, less power consumption, and the single-chip solution. In this work, a low-voltage, low-power direct down-conversion front-end circuit is implemented. The front-end circuit includes a low noise amplifier, a phase splitter, and a direct down-conversion mixer, as shown in Fig. 5.1.

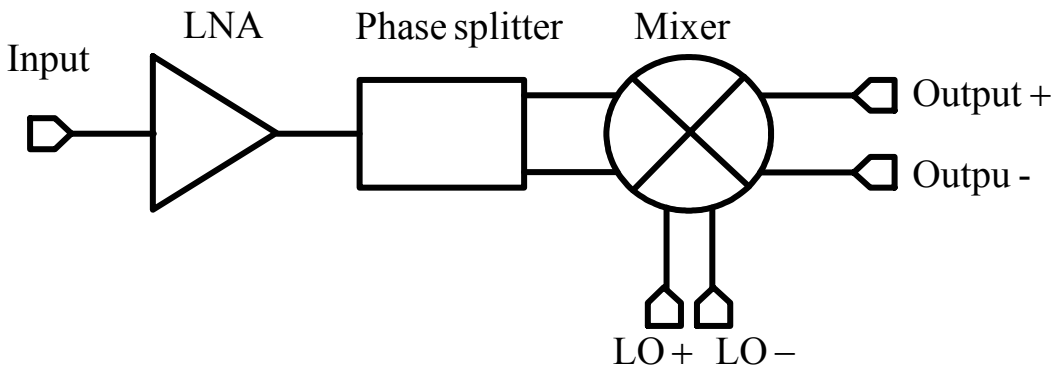


Figure 5.1 The block diagram of the front-end circuit

5.2 Principle of the Circuit Design

In this section, the design principle of the low-power front-end circuit is introduced. Fig. 5.2 shows the schematic of the low-power front-end circuit. The principle emphasizes on the features of each block, which include low noise amplifier, phase splitter, and direct down-conversion mixer.

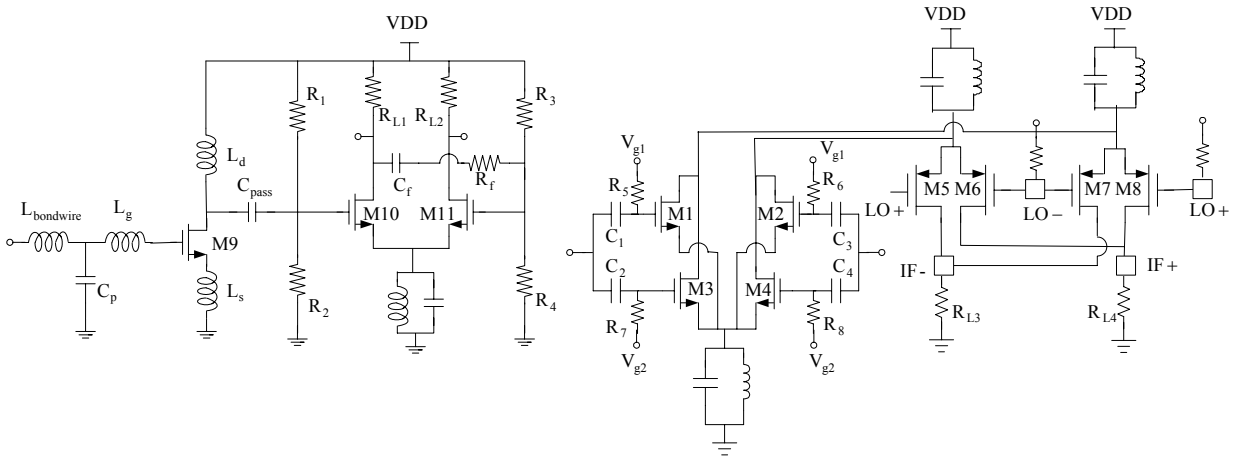


Figure 5.2 The schematic of the front-end circuit

5.2.1 Low Noise Amplifier

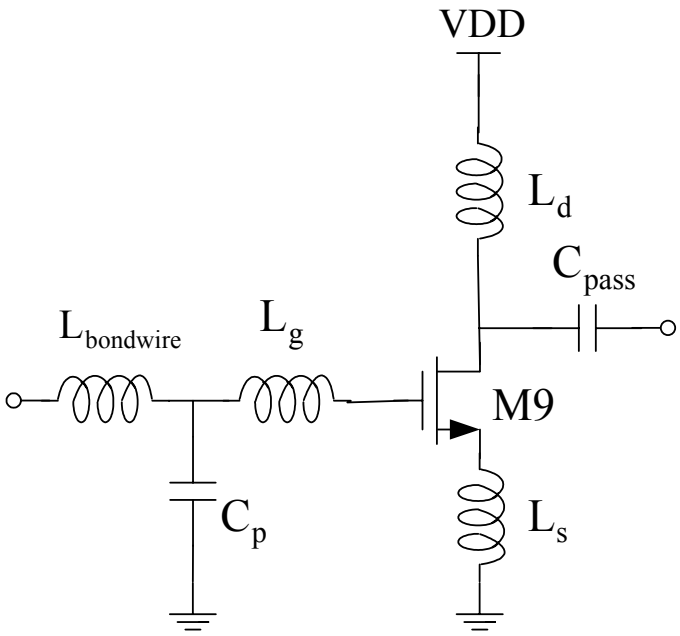


Figure 5.3 The schematic of low noise amplifier

The low noise amplifier is the first stage of the front-end circuit. This stage must provide high gain and low noise to suppress the overall system's noise performance. The inductive source degeneration topology, therefore, is used to achieve noise and power matching simultaneously [5]. Fig. 5.3 shows the schematic of the low noise amplifier, where $L_{bondwire}$ is the parasitic inductance of the bond-wire, C_p is the parasitic capacitance of the pad. In order to simplify analysis, we ignore the effect of the C_{gd} and the C_p. The input impedance, therefore, can be simply expressed as

$$Z_{in} = s(L_{bondwire} + L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \tag{5-1}$$

The imaginary part of the impedance can be set to zero by choosing $L_{bondwire}$ and L_g appropriately at the resonant frequency, and the real part can be made equal to 50Ω by choosing appropriate value of the L_s for input matching.

At the condition of the input matching, the equivalent transconductance of this architecture can be expressed as

$$G_m = \frac{\omega_T}{2\omega_o R_s} \tag{5-2}$$

where ω_T is equal to g_m/C_{gs} approximately.

Besides, the noise performance is the most critical parameter in the design of LNA. From noise analysis of the LNA in section 3.1, we can get the optimal noise performance. Fig. 5.4 shows the simulation result of noise figure of LNA under the assumption of matched input impedance, where we ignore the parasitic resistance of the inductor. For fixed power dissipation, we can adjust device size and bias point to minimize the noise figure. When the optimum device size is selected, the equivalent transconductance , G_m, is decided by $V_{gs.opt.}$

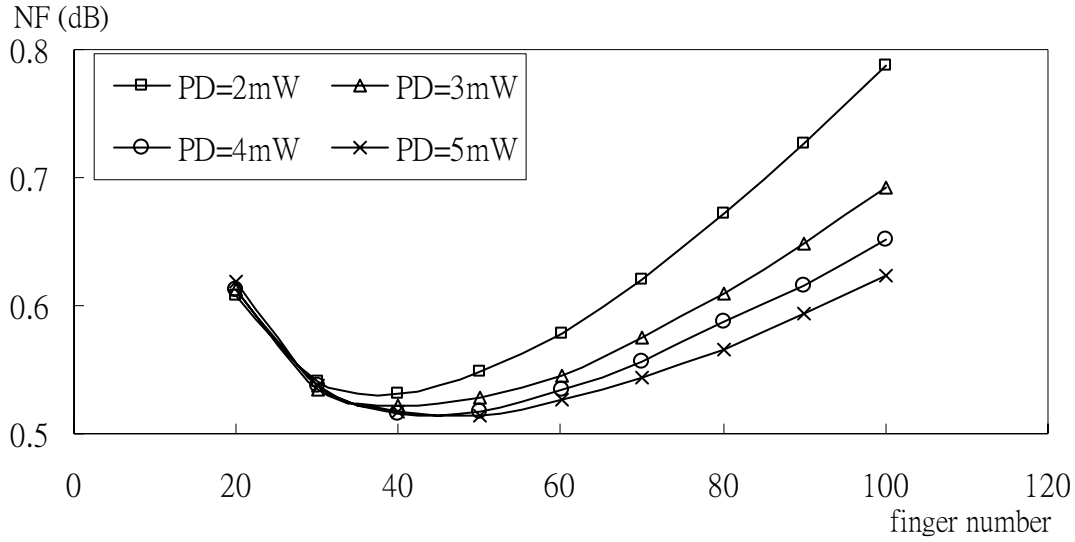


Figure 5.4 Simulation result of noise figure for several power dissipations at different device size, where ignoring the parasitic resistance, R_l.

5.2.2 Phase Splitter

In section 3.2, we have introduced the basic principle of phase splitter and a phase splitter with RC compensation, as shown in Fig. 3.6. An active device is used as the current source. However, the voltage drop across the drain and source make it difficult to realize in low power supply circuit.

Fig. 5.5 shows the schematic of the improved phase splitter. The current source is replaced by a LC tank which resonates at the desired frequency. This LC tank needs no dc voltage drop and provides high impedance at the resonant frequency. The phase error can be compensated by proper selection of R_{eq} ($R_{eq} = R_1 // R_2$) and C_f, and the gain balance is achieved by adjusting the value of R_{eq}, C_f, R_f, and Z_1. However, the outputs are slightly unbalanced even though the gates of M1 and M2 are perfectly balanced. This error results from the parasitic effects of the device and the diversion of some portion of the energy from the drain of M1 to the gate of M2 at the high frequency. So we must slightly adjust the value of R_{eq}, C_f, R_f, and Z_1 to compensate the effect.

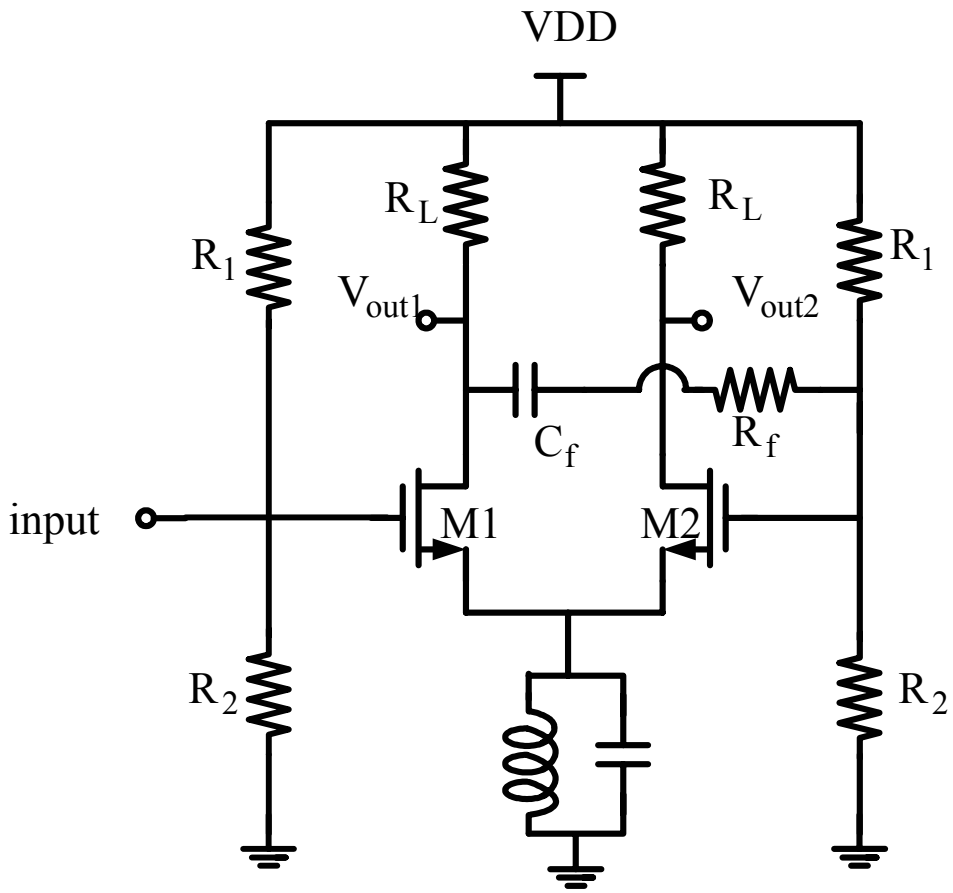


Figure 5.5 Improved phase splitter

Fig. 5.6 shows the phase difference of the improved phase splitter. The phase difference at the desired frequency (5.5GHz) is around 180 degree. And the magnitude of the gain is almost the same, as shown in Fig. 5.7.

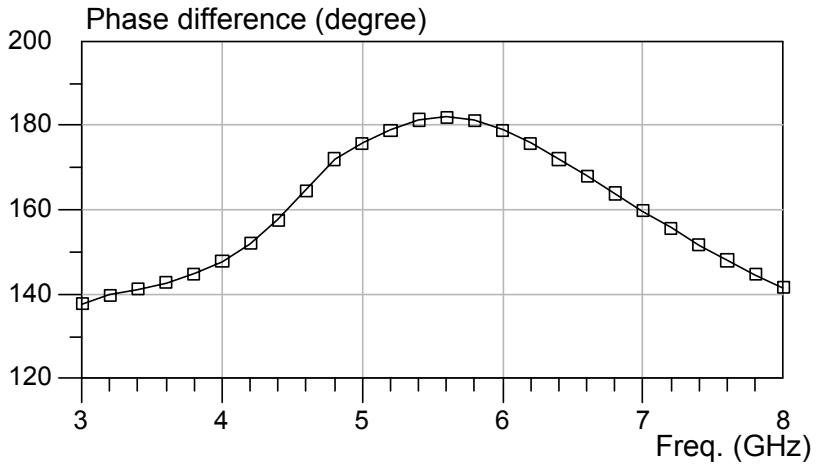


Figure 5.6 Simulation result of phase difference of the Fig. 5.5

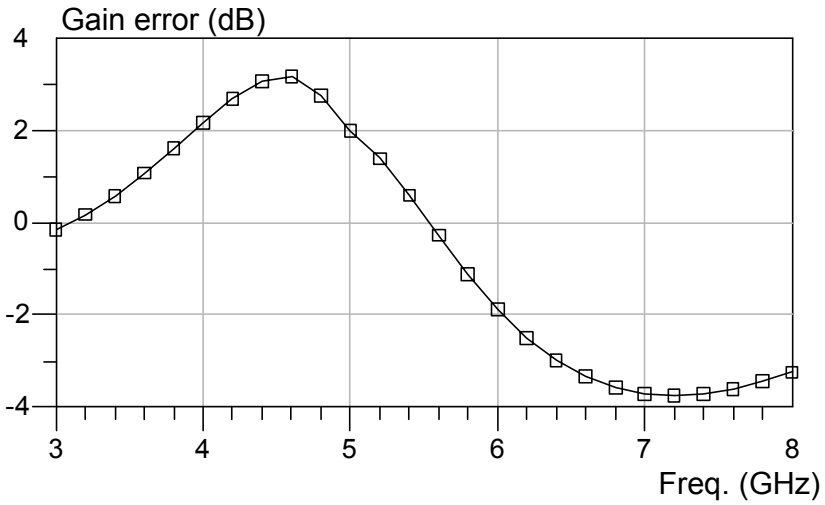


Figure 5.7 Simulation result of gain error of the Fig. 5.5

5.2.3 Direct Down-Conversion Mixer

The direct down-conversion mixer transforms the radio-frequency (RF) signal into base-band directly and needs high linearity to avoid the distortion of the signal. Following the discussion in the section 4.1 and 4.2.3, a low-power and high-linearity direct down-conversion mixer is design, as shown in Fig. 5.8.

The folded topology is beneficial to lower power design since the traditional cascoded Gilbert cell mixer requires a supply voltage of at least triple threshold voltage. In addition, the transconductance and the switching stages can be biased differently at a high current level and a low level, respectively, to achieve high gain and noise suppression. LC tanks are further applied to supply current driving without voltage drop and provide high impedance at the desired frequency

The MGTR consists of M1 – M4. M1 and M2 are MT providing major gain of the mixer, and M3 and M4 are AT compensating for the third-order nonlinear distortion. The switching stage includes four PMOS transistors, M5 – M8, for the concern of Flicker noise.

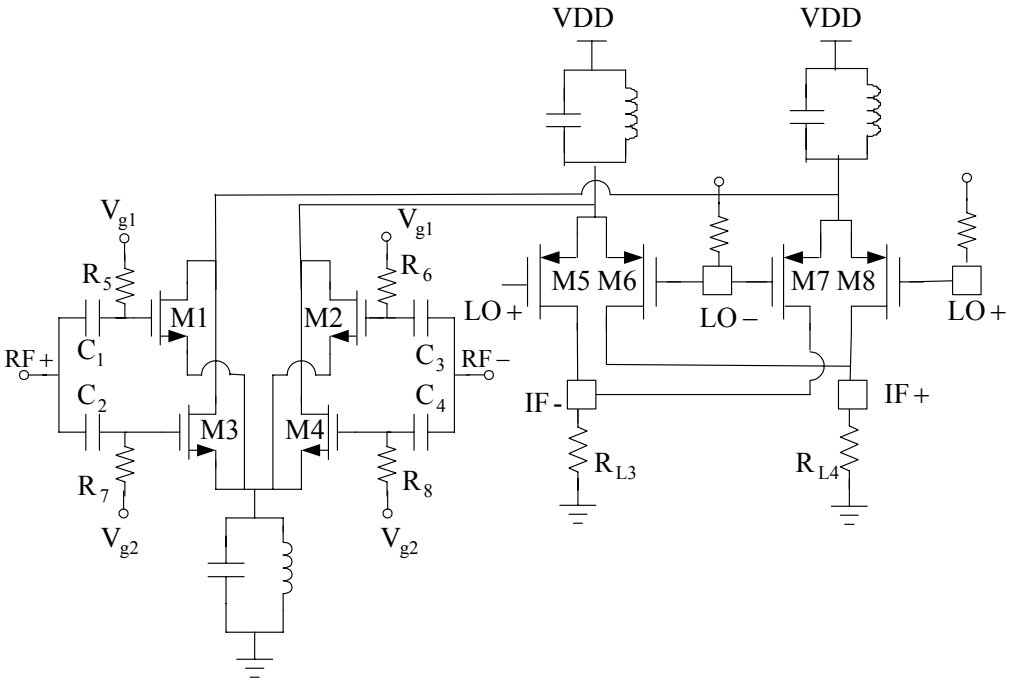


Figure 5.8 The schematic of the folded MGTR direct conversion mixer.

5.3 Chip Implementation and Measured Result

5.3.1 Circuit Implementations

Following the above-mentioned analysis, a front-end circuit is designed, as shown in Fig. 5.2. The front-end circuit is fabricated using 0.18um RF CMOS technology. The full chip of circuit is shown by microphotograph in Fig. 5.9. The total die area including bonding pads is 1.14 mm by 1.4 mm.

The RF input is placed on the left side, the LO input is placed on the right side, and the IF input is placed on the down side of the chip. The placement of pads is considered for the on-board measurement. In order to minimize the effect of the substrate noise on the system, a solid ground plane, constructed using a low resistive metal-1 material, is placed between the signal pads and the substrate. Besides, there are many ground pads to minimize the effect of the bond-wire.

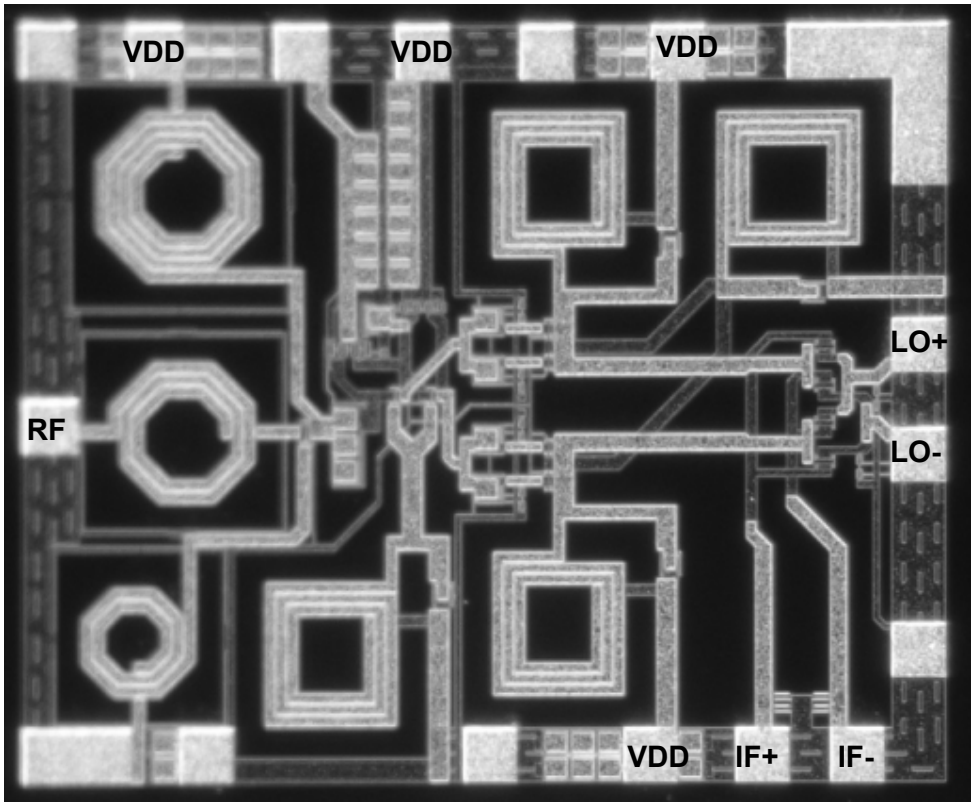


Figure 5.9 Microphotograph of front-end circuit

5.3.2 Experimental Results

Measurement is conducted by mounting the mixer die on FR4 board, as shown in Fig. 5.10. Input testing signal is transformed into a differential form at LO ports by hybrid couplers which gain error and phase error are smaller than 0.8dB and 8° respectively from 4GHz to 8GHz. Fig. 5.11 shows the measurement diagram. A unit gain output buffer is used to transform the differential signal into the single-ended form, and provides high input impedance to reduce loading effect.

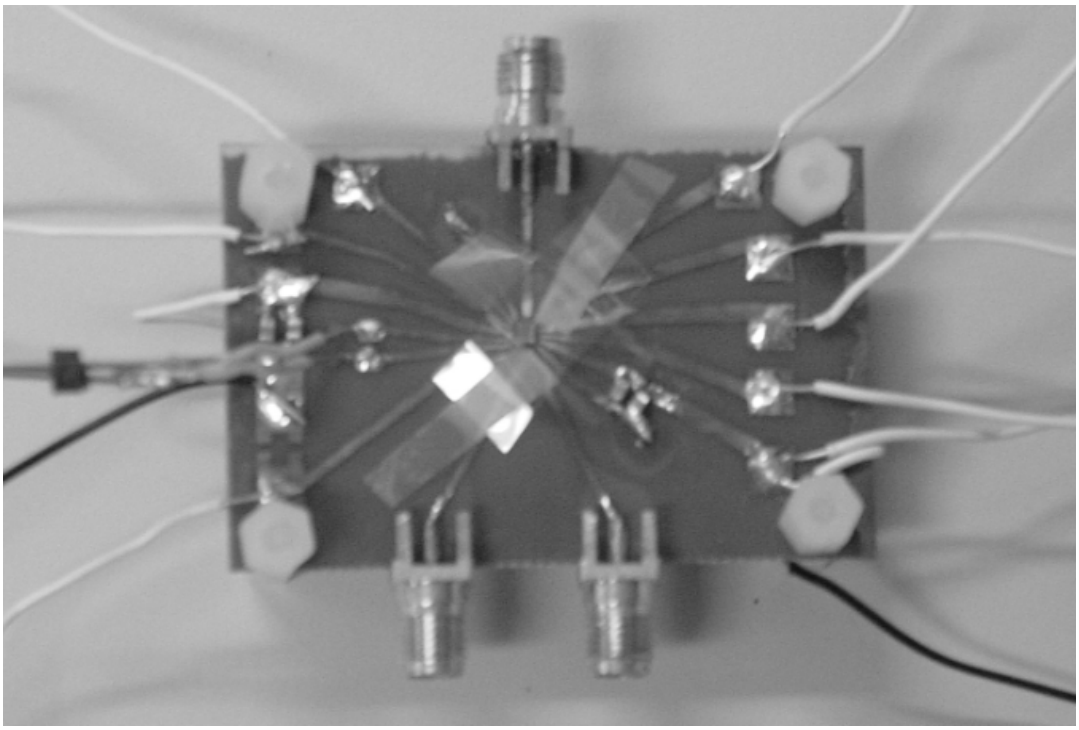


Figure 5.10 PCB layout of front-end circuit

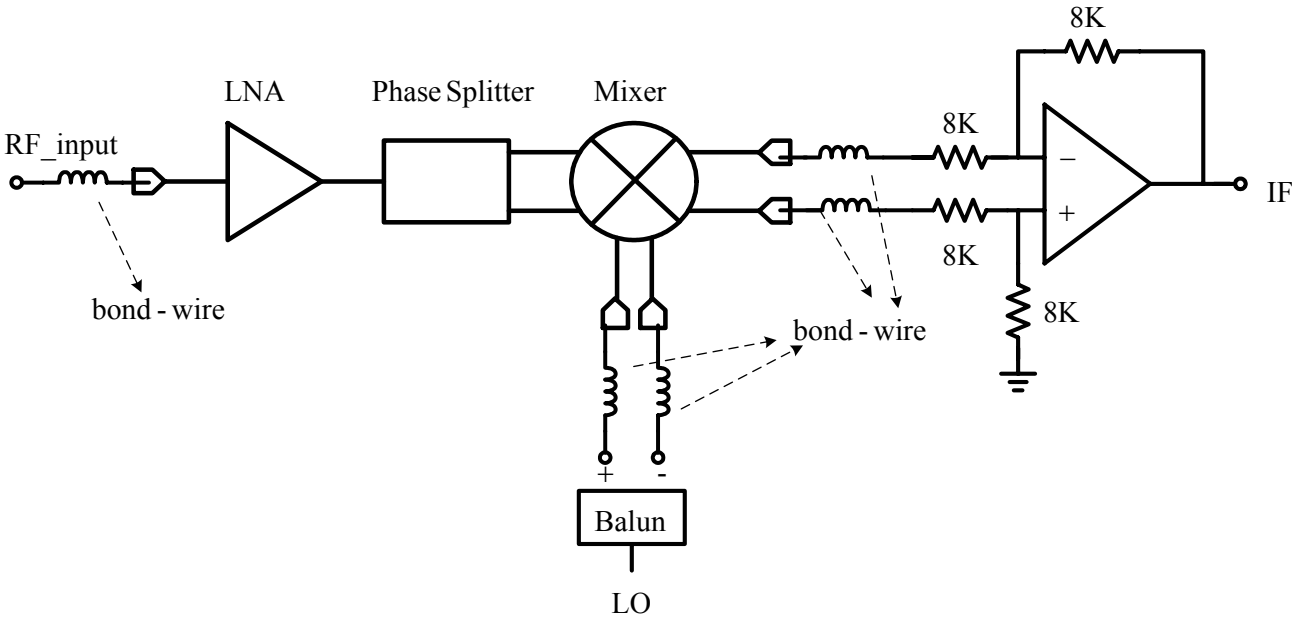


Figure 5.11 Measurement diagram including unit gain output buffer

The measured input return loss is plotted in Fig. 5.12 together with simulation result for comparison. The measured result has good agreement with the simulation data. The deeper phenomenon of measured input return loss may result from the parasitic effect of the SMA connectors and the FR4 board. The simulation result of DSB noise figure versus intermediate frequency (IF) is shown in Fig. 5.13 and its value is 6.9dB at IF of 1MHz.

The measured conversion gain of front-end circuit is 9.5 dB. Linearity analysis is conducted by the two-tone test. The measured result of the third-order intermodulation distortion is plotted in Fig. 5.14. Fig. 5.15 shows the measured input P_{-1dB} of -16 dBm, and Fig. 5.16 shows the measured input second intercept point (IIP2) of 19 dBm. Complete measured results are summarized in Table 5.1 together with simulation results for comparison. The deviation of IIP2 may result from the mismatch of the devices. The equivalent input noise voltage of the output buffer is approximately equal to the noise voltage of the circuit, and this condition caused some inaccuracy.

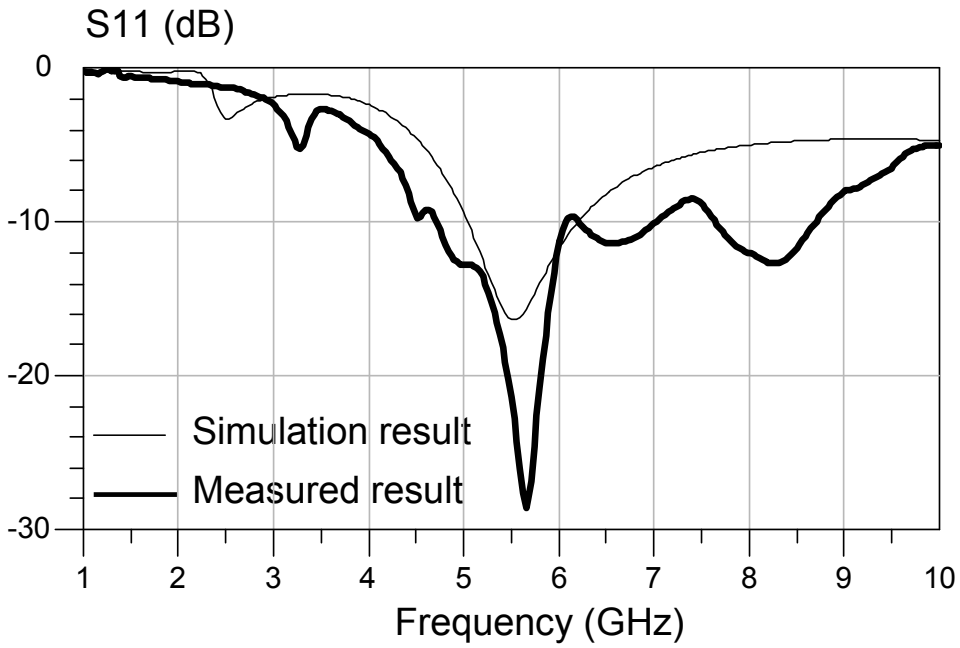


Figure 5.12 Input return loss of front-end circuit

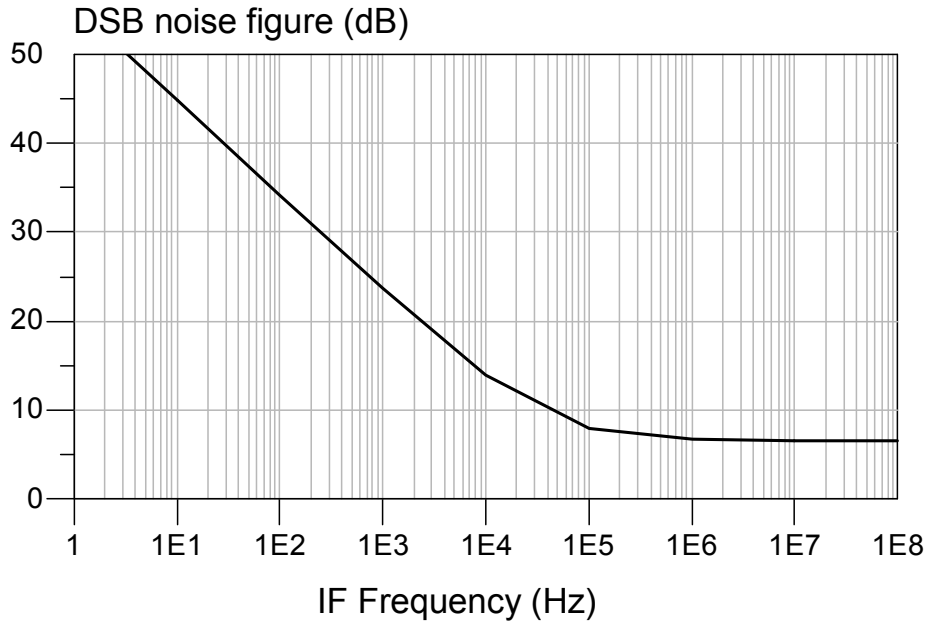


Figure 5.13 Simulation result of DSB noise figure

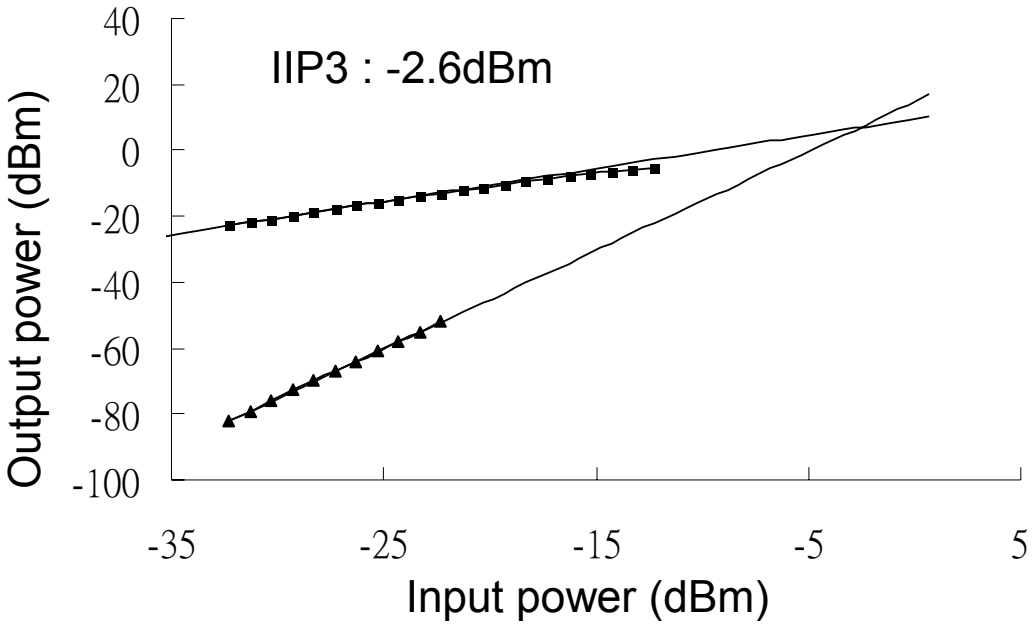


Figure 5.14 IIP3 measurement of front-end circuit

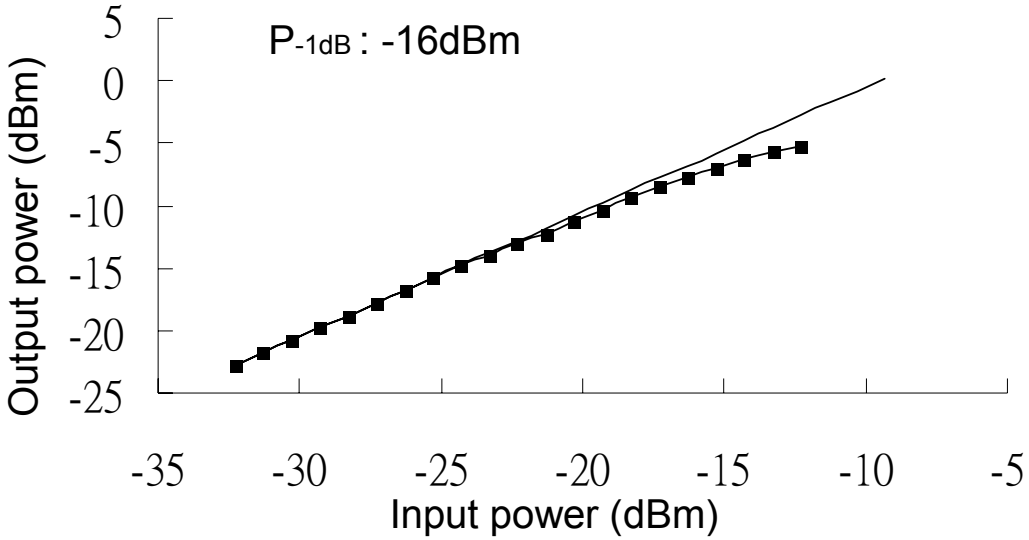


Figure 5.15 P_{-1dB} measurement of front-end circuit

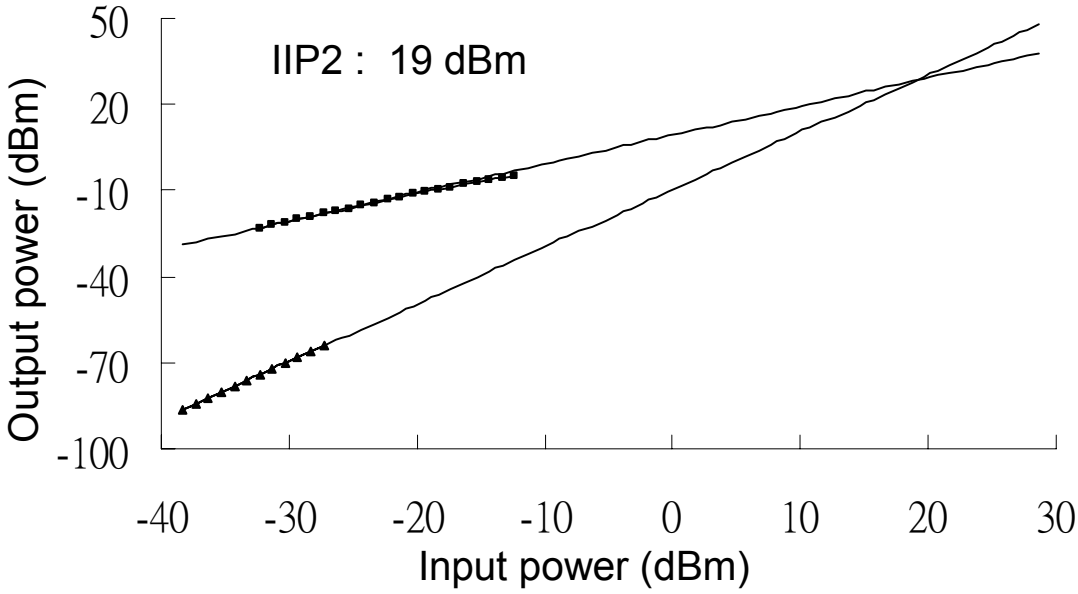


Figure 5.16 IIP2 measurement of front-end circuit

Table 5.1 Summary of simulation and measured results of front-end circuit

	Simulation	Measurement
Process	TSMC CMOS 0.18um	
Frequency	5.5 GHz	5.5 GHz
Supply Voltage	1.0 V	1.0 V
LO power	2 dBm	2.6 dBm
Conversion gain	18 dB	9.5 dB
S11	-16.3 dB	-21.5 dB
Noise Figure(DSB)	6.9 dB @ 1MHz	22.5 dB@ 10MHz
P_{-1dB}	-17 dBm	-16 dBm
IIP3	-8.4 dBm	-2.6 dBm
IIP2	30.3 dBm	19 dBm
Power Dissipation	8.6 mW	10.1 mW

5.3.3 Discussions

A low-power front-end circuit, intended for use in the receiver path of a wireless local area network, is designed in standard 0.18um CMOS technology. It is composed of a low noise amplifier, a phase splitter, and a direct down-conversion mixer. The improvement of the linearity of this circuit is not obvious comparing with the folded mixer in Chapter 4, and the change of in-band and out-of-band impedance may be the major reason. Measured data shows that the front-end circuit achieves conversion gain of 9.5 dB, input return loss of 21.5 dB, input third-order intercept point (IIP3) of -2.6 dBm, and input second-order intercept point (IIP2) of 19 dBm, while consuming only 10.1mW.

CHAPTER 6

Summary and Future Work

6.1 Summary

In Chapter 2, some architectures of the receiver, the IEEE 802.11a standard of wireless LAN, noise sources, and the theoretical MOSFET noise model are introduced. Besides, Volterra series is presented for the analysis of the linearity.

In Chapter 3, the design consideration of LNA, phase splitter and mixer is introduced. By analyzing and improving these circuits, a low-power and high-linearity and a low-power front-end circuit are designed and verified.

In Chapter 4, a folded MGTR direct down-conversion mixer is analyzed and verified in standard 0.18um CMOS technology. The MGTR technique is adopted to improve the linearity of the mixer in the transconductance stage. A compact equivalent circuit using AC complex transconductance truly gives the optimal design parameters. Measured data show that the improvement of the linearity is more than 7 dB without extra power consumption.

In Chapter 5, a low-power front-end circuit, intended for use in the receiver path of a wireless local area network, is designed in standard 0.18um CMOS technology. It is composed of a low noise amplifier, a phase splitter, and a direct down-conversion mixer. The LNA uses L-degeneration to achieve noise and power matching simultaneously. The single-ended signal is transformed into a differential form by the phase splitter. And the mixer provides higher linearity by using MGTR technology. Measured data shows that the front-end circuit achieves conversion gain of 9.5 dB,

input return loss of 21.5 dB, input third-order intercept point (IIP3) of -2.6 dBm, and input second-order intercept point (IIP2) of 19 dBm, while consuming only 10.1mW.

6.2 Future Work

The linearity can be improved by minimized the second term of (4-37), $\varepsilon(\omega,\Delta\omega,2\omega)$. The MGTR technique is an effective way to cancel the $G_m''(\omega)$ of the device. But the second term of (4-38) may become important while out-of-band impedances of source and load are altered, this condition is especially obvious when the $G_m''(\omega)$ is small. Therefore, we can keep the original performance, such as gain, noise figure, etc. and improve the linearity by fixing the in-band impedance and appropriately change out-of-band impedance. If this method is realized together with MGTR technique or used to cancel the $G_m''(\omega)$, the improvement of the linearity will be obvious.

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